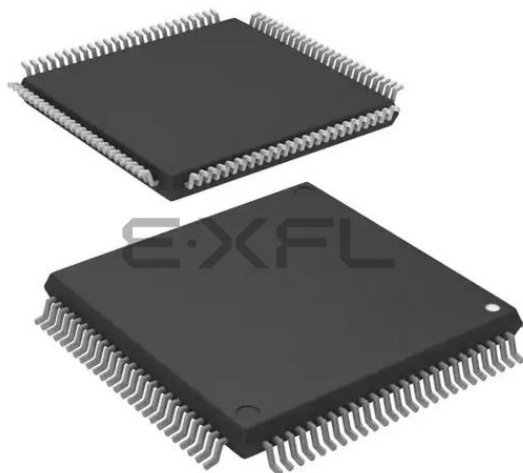




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Details

Product Status	Discontinued at Digi-Key
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I ² C, LINbus, SCI, SPI, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	78
Program Memory Size	1.5MB (1.5M x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b, 14x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f5631jddfp-v0

Table 1.4 Pin Functions (6/6)

Classifications	Pin Name	I/O	Description
Analog power supply	AVCC0	Input	Analog voltage supply pin for the 12-bit A/D converter. Connect this pin to VCC if the 12-bit A/D converter is not to be used.
	AVSS0	Input	Analog ground pin for the 12-bit A/D converter. Connect this pin to VSS if the 12-bit A/D converter is not to be used.
	VREFH0	Input	Analog reference voltage supply pin for the 12-bit A/D converter. Connect this pin to VCC if the 12-bit A/D converter is not to be used.
	VREFL0	Input	Analog reference ground pin for the 12-bit A/D converter. Connect this pin to VSS if the 12-bit A/D converter is not to be used.
	VREFH	Input	Reference voltage input pin for the 10-bit A/D converter and D/A converter. This is used as the analog power supply for the respective modules. Connect this pin to VCC if neither the 10-bit A/D converter nor the D/A converter is in use.
	VREFL	Input	Reference ground pin for the 10-bit A/D converter and D/A converter. This is used as the analog ground for the respective modules. Set this pin to the same potential as the VSS pin.
I/O ports	P00 to P03, P05, P07	I/O	6-bit input/output pins.
	P10 to P17	I/O	8-bit input/output pins.
	P20 to P27	I/O	8-bit input/output pins.
	P30 to P37	I/O	8-bit input/output pins. (P35 is an input pin)
	P40 to P47	I/O	8-bit input/output pins.
	P50 to P57	I/O	8-bit input/output pins.
	P60 to P67	I/O	8-bit input/output pins.
	P70 to P77	I/O	8-bit input/output pins.
	P80 to P87	I/O	8-bit input/output pins.
	P90 to P97	I/O	8-bit input/output pins.
	PA0 to PA7	I/O	8-bit input/output pins.
	PB0 to PB7	I/O	8-bit input/output pins.
	PC0 to PC7	I/O	8-bit input/output pins.
	PD0 to PD7	I/O	8-bit input/output pins.
	PE0 to PE7	I/O	8-bit input/output pins.
	PF0 to PF5	I/O	6-bit input/output pins.
	PG0 to PG7	I/O	8-bit input/output pins.
	PJ3, PJ5	I/O	2-bit input/output pins.

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	
15	PE2	PE3	P70	P65	P67	VSS	VCC	PG7	PA6	PB0	P72	PB4	VSS	VCC	PC1	15
14	PE1	PE0	VSS	PE7	PG3	PA0	PA1	PA2	PA7	VCC	PB1	PB5	P73	P75	P74	14
13	P63	P64	PE4	VCC	PG2	PG4	PG6	PA3	VSS	P71	PB3	PB7	PC0	PC2	P76	13
12	P60	VSS	P62	PE5	PE6	P66	PG5	PA4	PA5	PB2	PB6	P77	PC3	PC4	P80	12
11	PD6	PG1	VCC	P61	RX63N Group RX631 Group PTBG0176GA-A (176-pin LFBGA) (Top perspective view)							P81	P82	PC6	VCC	11
10	P97	PD4	PG0	PD7								PC5	PC7	P83	VSS	10
9	VCC	P96	PD3	PD5								P50	P51	P52	P84	9
8	P94	PD1	PD2	VSS								P53	VCC_USB	USB1_DP	USB1_DM	8
7	VSS	P92	PD0	P95								P54	P55	VSS_USB	USB0_DP	7
6	VCC	P91	P90	P93								P56	P57	VCC_USB	USB0_DM	6
5	P46	P47	P45	P44								P13	P12	P10	P11	5
4	P42	P41	P43	P00	VSS	BSCANP	PF4	P35	PF3	PF1	P25	P86	P15	P14	P85	4
3	VREFL0	P40	VREFH0	P03	PF5	PJ3	MD/FINED	RES#	P34	PF2	PF0	P24	P22	P87	P16	3
2	AVCC0	P07	VREFH	P02	EMLE	VCL	XCOUT	VSS	VCC	P32	P30	P26	P23	P17	P20	2
1	AVSS0	P05	VREFL	P01	PJ5	VBATT	XCIN	XTAL	EXTAL	P33	P31	P27	VCC	VSS	P21	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	

Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.5, List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA).

Figure 1.4 Pin Assignment (176-Pin LFBGA)

Table 1.7 List of Pins and Pin Functions (145-Pin TFLGA) (5/5)

Pin No. 145-pin TFLGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timers (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SC1c, SC1d, RSPI, RIIC, CAN, IEB, USB, and PDC)	Interrupt	S12AD AD DA
N7	TRDATA3	P55	WAIT#/ EDREQ0	MTIOC4D/TMO3	CRX1/ET_EXOUT	IRQ10	
N8	VSS						
N9		PC7	A23/CS0#	MTIOC3A/MTCLKB/ TIOCB6/TMO2/PO31	TXD8/SMOSI8/SSDA8/ MISOA/ET_COL	IRQ14	
N10	TRSYNC	P82	EDREQ1	MTIOC4A/PO28	TXD10/SMOSI10/SSDA10/ ET_ETXD1/RMII_TXD1		
N11		PC3	A19	MTIOC4D/TCLKB/PO24	TXD5/SMOSI5/SSDA5/ IETXD/ET_TX_ER		
N12		P75	CS5#	PO20	SCK11/ET_ERXD0/ RMII_RXD0		
N13		P74	CS4#	PO19	CTS11#/RTS11#/SS11#/ ET_ERXD1/RMII_RXD1		

Note 1. The BCLK function is multiplexed with the I/O port function for pin P53, so the port function is not available if the external bus is enabled.

Note 2. Enabled only for the ROM capacity: 2 Mbytes/1.5 Mbytes

Table 1.10 List of Pins and Pin Functions (100-Pin LQFP) (2/4)

Pin No. 100-pin LQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC	Timers (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SCIC, SCID, RSPI, RIIC, CAN, IEB, USB)	Interrupt	S12AD AD DA
31		P15		MTIOC0B/MTCLKB/ TIOCB2/TCLKB/TMC12/ PO13	RXD1/SCK3/SMISO1/ SSCL1/CRX1-DS	IRQ5	
32		P14		MTIOC3A/MTCLKA/ TIOCB5/TCLKA/TMR12/ PO15	CTS1#/RTS1#/SS1#/ CTX1/USB0_DPUPE/ USB0_OVRCURA	IRQ4	
33		P13		MTIOC0B/TIOCA5/ TMO3/PO13	TXD2/SMOSI2/SSDA2/ SDA0[FM+]	IRQ3	ADTRG#
34		P12		TMC11	RXD2/SMISO2/SSCL2/ SCL0[FM+]	IRQ2	
35	VCC_USB						
36					USB0_DM		
37					USB0_DP		
38	VSS_USB						
39		P55	WAIT#/ EDREQ0	MTIOC4D/TMO3	CRX1/ET_EXOUT	IRQ10	
40		P54	ALE/EDACK0	MTIOC4B/TMC11	CTS2#/RTS2#/SS2#/ CTX1/ET_LINKSTA		
41		P53*2	BCLK				
42		P52	RD#		RXD2/SMISO2/SSCL2/ SSLB3		
43		P51	WR1#/BC1#/ WAIT#		SCK2/SSLB2		
44		P50	WR0#/WR#		TXD2/SMOSI2/SSDA2/ SSLB1		
45		PC7	A23/CS0#	MTIOC3A/MTCLKB/ TMO2/PO31	TXD8/SMOSI8/SSDA8/ MISOA/ET_COL	IRQ14	
46		PC6	A22/CS1#	MTIOC3C/MTCLKA/ TMC12/PO30	RXD8/SMISO8/SSCL8/ MOSIA/ET_ETXD3	IRQ13	
47		PC5	A21/CS2#/ WAIT#	MTIOC3B/MTCLKD/ TMR12/PO29	SCK8/RSPCKA/ ET_ETXD2		
48		PC4	A20/CS3#	MTIOC3D/MTCLKC/ TMC11/PO25/POE0#	SCK5/CTS8#/RTS8#/ SS8#/SSLA0/ ET_TX_CLK		
49		PC3	A19	MTIOC4D/TCLKB/ PO24	TXD5/SMOSI5/SSDA5/ IETXD/ET_TX_ER		
50		PC2	A18	MTIOC4B/TCLKA/PO21	RXD5/SMISO5/SSCL5/ SSLA3/IERXD/ ET_RX_DV		
51		PC1	A17	MTIOC3A/TCLKD/ PO18	SCK5/SSLA2/ ET_ERXD2	IRQ12	
52		PC0	A16	MTIOC3C/TCLKC/ PO17	CTS5#/RTS5#/SS5#/ SSLA1/ET_ERXD3	IRQ14	
53		PB7	A15	MTIOC3B/TIOCB5/ PO31	TXD9/SMOSI9/SSDA9/ ET_CRS/ RMII_CRS_DV		
54		PB6	A14	MTIOC3D/TIOCA5/ PO30	RXD9/SMISO9/SSCL9/ ET_ETXD1/RMII_TXD1		
55		PB5	A13	MTIOC2A/MTIOC1B/ TIOCB4/TMR11/PO29/ POE1#	SCK9/ET_ETXD0/ RMII_TXD0		
56		PB4	A12	TIOCA4/PO28	CTS9#/RTS9#/SS9#/ ET_TX_EN/ RMII_TXD_EN		
57		PB3	A11	MTIOC0A/MTIOC4A/ TIOC3D/TCLKD/TMO0/ PO27/POE3#	SCK6/ET_RX_ER/ RMII_RX_ER		
58		PB2	A10	TIOCC3/TCLKC/PO26	CTS6#/RTS6#/SS6#/ ET_RX_CLK/REF50CK		

Table 1.12 List of Pins and Pin Functions (64-Pin LQFP) (2/3)

Pin Number 64-Pin LQFP	Power Supply Clock System Control	I/O Port	Timer (MTU2a, TPUa, TMR, PPG, RTCa, POE2a)	Timer Communications (SC1c, SC1d, RSPI, RIIC, CAN, IEB, USB)	Interrupt	S12ADa, DAa
32		PC2	MTIOC4B/TCLKA/ PO21	RXD5/SMISO5/SSCL5/ SSLA3/IERXD		
33		PB7/ PC1	MTIOC3B/TIOCB5/ PO31	TXD9/SMOSI9/SSDA9		
34		PB6/ PC0	MTIOC3D/TIOCA5/ PO30	RXD9/SMISO9/SSCL9		
35		PB5	MTIOC2A/MTIOC1B/ TIOCB4/TMRI1/PO29/ POE1#	SCK9		
36		PB3	MTIOC0A/MTIOC4A/ TIOCD3/TCLKD/TMO0/ PO27/POE3#	SCK6		
37		PB1	MTIOC0C/MTIOC4C/ TIOCB3/TMCI0/PO25	TXD6/SMOSI6/SSDA6	IRQ4-DS	
38	VCC					
39		PB0	MTIC5W/TIOCA3/PO24	RXD6/SMISO6/SSCL6/ RSPCKA	IRQ12	
40	VSS					
41		PA6	MTIC5V/MTCLKB/ TIOCA2/TMCI3/PO22/ POE2#	CTS5#/RTS5#/SS5#/ MOSIA		
42		PA4	MTIC5U/MTCLKA/ TIOCA1/TMRI0/PO20	TXD5/SMOSI5/SSDA5/ SSLA0	IRQ5-DS	
43		PA3	MTIOC0D/MTCLKD/ TIOCD0/TCLKB/PO19	RXD5/SMISO5/SSCL5	IRQ6-DS	
44		PA1	MTIOC0B/MTCLKC/ TIOCB0/PO17	SCK5/SSLA2/SCL2	IRQ11	
45		PA0	MTIOC4A/TIOCA0/ PO16	SSLA1		
46		PE5	MTIOC4C/MTIOC2B	RSPCKB	IRQ5	AN013
47		PE4	MTIOC4D/MTIOC1A/ PO28	SSLB0		AN012
48		PE3	MTIOC4B/PO26/POE8#	CTS12#/RTS12#/ SS12#/MISOB		AN011
49		PE2	MTIOC4A/PO23	RXD12/SMISO12/ SSCL12/RXDX12/ SSLB3/MOSIB	IRQ7-DS	AN010
50		PE1	MTIOC4C/PO18	TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/SSLB2/ RSPCKB		AN009
51		PE0		SCK12/SSLB1		AN008
52	VREFL					
53		P46			IRQ14-DS	AN006
54	VREFH					
55		P44			IRQ12-DS	AN004
56		P43			IRQ11-DS	AN003
57		P42			IRQ10-DS	AN002
58		P41			IRQ9-DS	AN001
59	VREFL0					
60		P40			IRQ8-DS	AN000

Table 4.1 List of I/O Registers (Address Order) (13/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 7394h	ICU	Interrupt source priority register 148	IPR148	8	8	2	ICLK	ICUb
0008 7396h	ICU	Interrupt source priority register 150	IPR150	8	8	2	ICLK	
0008 7398h	ICU	Interrupt source priority register 152	IPR152	8	8	2	ICLK	
0008 739Ch	ICU	Interrupt source priority register 156	IPR156	8	8	2	ICLK	
0008 73A0h	ICU	Interrupt source priority register 160	IPR160	8	8	2	ICLK	
0008 73A1h	ICU	Interrupt source priority register 161	IPR161	8	8	2	ICLK	
0008 73A4h	ICU	Interrupt source priority register 164	IPR164	8	8	2	ICLK	
0008 73A6h	ICU	Interrupt source priority register 166	IPR166	8	8	2	ICLK	
0008 73AAh	ICU	Interrupt source priority register 170	IPR170	8	8	2	ICLK	
0008 73ADh	ICU	Interrupt source priority register 173	IPR173	8	8	2	ICLK	
0008 73B0h	ICU	Interrupt source priority register 176	IPR176	8	8	2	ICLK	
0008 73B3h	ICU	Interrupt source priority register 179	IPR179	8	8	2	ICLK	
0008 73B6h	ICU	Interrupt source priority register 182	IPR182	8	8	2	ICLK	
0008 73B7h	ICU	Interrupt source priority register 183	IPR183	8	8	2	ICLK	
0008 73B8h	ICU	Interrupt source priority register 184	IPR184	8	8	2	ICLK	
0008 73B9h	ICU	Interrupt source priority register 185	IPR185	8	8	2	ICLK	
0008 73BAh	ICU	Interrupt source priority register 186	IPR186	8	8	2	ICLK	
0008 73BBh	ICU	Interrupt source priority register 187	IPR187	8	8	2	ICLK	
0008 73BCh	ICU	Interrupt source priority register 188	IPR188	8	8	2	ICLK	
0008 73BDh	ICU	Interrupt source priority register 189	IPR189	8	8	2	ICLK	
0008 73BEh	ICU	Interrupt source priority register 190	IPR190	8	8	2	ICLK	
0008 73BFh	ICU	Interrupt source priority register 191	IPR191	8	8	2	ICLK	
0008 73C0h	ICU	Interrupt source priority register 192	IPR192	8	8	2	ICLK	
0008 73C1h	ICU	Interrupt source priority register 193	IPR193	8	8	2	ICLK	
0008 73C2h	ICU	Interrupt source priority register 194	IPR194	8	8	2	ICLK	
0008 73C3h	ICU	Interrupt source priority register 195	IPR195	8	8	2	ICLK	
0008 73C4h	ICU	Interrupt source priority register 196	IPR196	8	8	2	ICLK	
0008 73C5h	ICU	Interrupt source priority register 197	IPR197	8	8	2	ICLK	
0008 73C6h	ICU	Interrupt source priority register 198	IPR198	8	8	2	ICLK	
0008 73C7h	ICU	Interrupt source priority register 199	IPR199	8	8	2	ICLK	
0008 73C8h	ICU	Interrupt source priority register 200	IPR200	8	8	2	ICLK	
0008 73C9h	ICU	Interrupt source priority register 201	IPR201	8	8	2	ICLK	
0008 73CAh	ICU	Interrupt source priority register 202	IPR202	8	8	2	ICLK	
0008 73CBh	ICU	Interrupt source priority register 203	IPR203	8	8	2	ICLK	
0008 73CEh	ICU	Interrupt source priority register 206	IPR206	8	8	2	ICLK	
0008 73CFh	ICU	Interrupt source priority register 207	IPR207	8	8	2	ICLK	
0008 73D0h	ICU	Interrupt source priority register 208	IPR208	8	8	2	ICLK	
0008 73D6h	ICU	Interrupt source priority register 214	IPR214	8	8	2	ICLK	
0008 73D9h	ICU	Interrupt source priority register 217	IPR217	8	8	2	ICLK	
0008 73DCh	ICU	Interrupt source priority register 220	IPR220	8	8	2	ICLK	
0008 73DFh	ICU	Interrupt source priority register 223	IPR223	8	8	2	ICLK	
0008 73E2h	ICU	Interrupt source priority register 226	IPR226	8	8	2	ICLK	
0008 73E5h	ICU	Interrupt source priority register 229	IPR229	8	8	2	ICLK	
0008 73E8h	ICU	Interrupt source priority register 232	IPR232	8	8	2	ICLK	
0008 73EBh	ICU	Interrupt source priority register 235	IPR235	8	8	2	ICLK	
0008 73EEh	ICU	Interrupt source priority register 238	IPR238	8	8	2	ICLK	
0008 73F1h	ICU	Interrupt source priority register 241	IPR241	8	8	2	ICLK	
0008 73F4h	ICU	Interrupt source priority register 244	IPR244	8	8	2	ICLK	
0008 73F7h	ICU	Interrupt source priority register 247	IPR247	8	8	2	ICLK	
0008 73FAh	ICU	Interrupt source priority register 250	IPR250	8	8	2	ICLK	
0008 73FDh	ICU	Interrupt source priority register 253	IPR253	8	8	2	ICLK	

Table 4.1 List of I/O Registers (Address Order) (22/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 862Ah	MTU4	Timer general register D	TGRD	16	16	2, 3 PCLKB	2 ICLK	MTU2a
0008 862Ch	MTU3	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK	
0008 862Dh	MTU4	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK	
0008 8630h	MTU	Timer interrupt skipping set register	TITCR	8	8	2, 3 PCLKB	2 ICLK	
0008 8631h	MTU	Timer interrupt skipping counter	TITCNT	8	8	2, 3 PCLKB	2 ICLK	
0008 8632h	MTU	Timer buffer transfer set register	TBTER	8	8	2, 3 PCLKB	2 ICLK	
0008 8634h	MTU	Timer dead time enable register	TDER	8	8	2, 3 PCLKB	2 ICLK	
0008 8636h	MTU	Timer output level buffer register	TOLBR	8	8	2, 3 PCLKB	2 ICLK	
0008 8638h	MTU3	Timer buffer operation transfer mode register	TBTM	8	8	2, 3 PCLKB	2 ICLK	
0008 8639h	MTU4	Timer buffer operation transfer mode register	TBTM	8	8	2, 3 PCLKB	2 ICLK	
0008 8640h	MTU4	Timer A/D converter start request control register	TADCR	16	16	2, 3 PCLKB	2 ICLK	
0008 8644h	MTU4	Timer A/D converter start request cycle set register A	TADCORA	16	16	2, 3 PCLKB	2 ICLK	
0008 8646h	MTU4	Timer A/D converter start request cycle set register B	TADCORB	16	16	2, 3 PCLKB	2 ICLK	
0008 8648h	MTU4	Timer A/D converter start request cycle set buffer register A	TADCOBRA	16	16	2, 3 PCLKB	2 ICLK	
0008 864Ah	MTU4	Timer A/D converter start request cycle set buffer register B	TADCOBRB	16	16	2, 3 PCLKB	2 ICLK	
0008 8660h	MTU	Timer waveform control register	TWCR	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 8680h	MTU	Timer start register	TSTR	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 8681h	MTU	Timer synchronous register	TSYR	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 8684h	MTU	Timer read/write enable register	TRWER	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 8690h	MTU0	Noise filter control register	NFCR	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 8691h	MTU1	Noise filter control register	NFCR	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 8692h	MTU2	Noise filter control register	NFCR	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 8693h	MTU3	Noise filter control register	NFCR	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 8694h	MTU4	Noise filter control register	NFCR	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 8695h	MTU5	Noise filter control register	NFCR	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 8700h	MTU0	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK	
0008 8701h	MTU0	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK	
0008 8702h	MTU0	Timer I/O control register H	TIORH	8	8	2, 3 PCLKB	2 ICLK	
0008 8703h	MTU0	Timer I/O control register L	TIORL	8	8	2, 3 PCLKB	2 ICLK	
0008 8704h	MTU0	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK	
0008 8705h	MTU0	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK	
0008 8706h	MTU0	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	
0008 8708h	MTU0	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	
0008 870Ah	MTU0	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	
0008 870Ch	MTU0	Timer general register C	TGRC	16	16	2, 3 PCLKB	2 ICLK	
0008 870Eh	MTU0	Timer general register D	TGRD	16	16	2, 3 PCLKB	2 ICLK	
0008 8720h	MTU0	Timer general register E	TGRE	16	16	2, 3 PCLKB	2 ICLK	
0008 8722h	MTU0	Timer general register F	TGRF	16	16	2, 3 PCLKB	2 ICLK	
0008 8724h	MTU0	Timer interrupt enable register2	TIER2	8	8	2, 3 PCLKB	2 ICLK	
0008 8726h	MTU0	Timer buffer operation transfer mode register	TBTM	8	8	2, 3 PCLKB	2 ICLK	
0008 8780h	MTU1	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK	
0008 8781h	MTU1	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK	
0008 8782h	MTU1	Timer I/O control register	TIOR	8	8	2, 3 PCLKB	2 ICLK	
0008 8784h	MTU1	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK	
0008 8785h	MTU1	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK	
0008 8786h	MTU1	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	
0008 8788h	MTU1	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	
0008 878Ah	MTU1	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	
0008 8790h	MTU1	Timer input capture control register	TICCR	8	8	2, 3 PCLKB	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (38/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
000A 0000h	USB0	System configuration control register	SYSCFG	16	16	3 to 4 PCLKB	2, 3 ICLK	USBa
000A 0004h	USB0	System configuration status register 0	SYSSTS0	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 0008h	USB0	Device state control register 0	DVSTCTR0	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 0014h	USB0	CFIFO port register	CFIFO	16	8, 16	3 to 4 PCLKB	2, 3 ICLK	
000A 0018h	USB0	D0FIFO port register	D0FIFO	16	8, 16	3 to 4 PCLKB	2, 3 ICLK	
000A 001Ch	USB0	D1FIFO port register	D1FIFO	16	8, 16	3 to 4 PCLKB	2, 3 ICLK	
000A 0020h	USB0	CFIFO port select register	CFIFOSEL	16	16	3 to 4 PCLKB	2, 3 ICLK	
000A 0022h	USB0	CFIFO port control register	CFIFOCTR	16	16	3 to 4 PCLKB	2, 3 ICLK	
000A 0028h	USB0	D0FIFO port select register	D0FIFOSEL	16	16	3 to 4 PCLKB	2, 3 ICLK	
000A 002Ah	USB0	D0FIFO port control register	D0FIFOCTR	16	16	3 to 4 PCLKB	2, 3 ICLK	
000A 002Ch	USB0	D1FIFO port select register	D1FIFOSEL	16	16	3 to 4 PCLKB	2, 3 ICLK	
000A 002Eh	USB0	D1FIFO port control register	D1FIFOCTR	16	16	3 to 4 PCLKB	2, 3 ICLK	
000A 0030h	USB0	Interrupt enable register 0	INTENB0	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 0032h	USB0	Interrupt enable register 1	INTENB1	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 0036h	USB0	BRDY interrupt enable register	BRDYENB	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 0038h	USB0	NRDY interrupt enable register	NRDYENB	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	

Table 5.4 DC Characteristics (3) (for D and G Versions (-40 ≤ Ta ≤ +85°C))

Conditions: VCC = AVCC0 = VREFH = VCC_USB = V_{BATT} = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0,
VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V, T_a = T_{opr}

Item				Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
Supply current*1	High-speed operating mode	Max.*2		I _{CC} *3	—	—	100	mA	ICLK = 100 MHz PCLKA = 100MHz PCLKB = 50 MHz FCLK = 50 MHz BCLK = 100MHz	
		Normal*4	Peripheral function: clock signal supplied*4		—	52	—			
			Peripheral function: clock signal stopped*4		—	40	—			
		Sleep mode			—	25	65			
		All-module-clock-stop mode (reference value)			—	20	38			
		Increased by BGO operation*5			—	15	—			
	Low-speed operating mode 1*6				—	4	—			ICLK = 1 MHz
	Low-speed operating mode 2				—	1	—			
	Software standby mode				—	0.2	6			
	Deep software standby mode	Power supplied to RAM and USB resume detecting unit			—	22	200			μA
		Power not supplied to RAM and USB resume detecting unit	Power-on reset circuit and low-power consumption function disabled	—	21	60				
			Power-on reset circuit and low-power		—	6.2	28			
		Increase when the RTC is operating		When a crystal oscillator for low clock loads is in use	—	1.0	—			
	When a crystal oscillator for standard clock loads is in use			—	3.0	—				
	RTC operating while VCC is off (with the battery backup function, only the RTC and sub-clock oscillator operate)		When a crystal oscillator for low clock loads is in use	—	0.9	—	V _{BATT} = 2.0 V, VCC = 0V			
				—	1.6	—	V _{BATT} = 3.3 V, VCC = 0V			
			When a crystal oscillator for standard clock loads is in use	—	1.7	—	V _{BATT} = 2.0 V(for products with 100 pins or more), V _{BATT} = 2.3 V (for the 64-pin product), VCC = 0V			
				—	3.3	—	V _{BATT} = 3.3 V, VCC = 0V			
	Analog power supply current*7	During 12-bit A/D conversion (including temperature sensor)			I _{AVCC0}	—	2.3	3.2	mA	
		During 10-bit A/D conversion			I _{VREFH} *9	—	1.0	1.65		mA
During D/A conversion (per unit)			—	0.7		1.0	mA			
Waiting for A/D, D/A conversion (all units)*10			—	—	25	35		μA		
A/D, D/A converter in standby mode (all units)*10				—	0.1	4.0	μA			
Reference power supply current	During 12-bit A/D conversion			I _{VREFH0}	—	0.6		0.7	mA	
	Waiting for 12-bit A/D conversion (per unit)				—	0.5	0.6	mA		
	12-bit A/D converter in standby mode (per unit)				—	0.1	2.0			μA

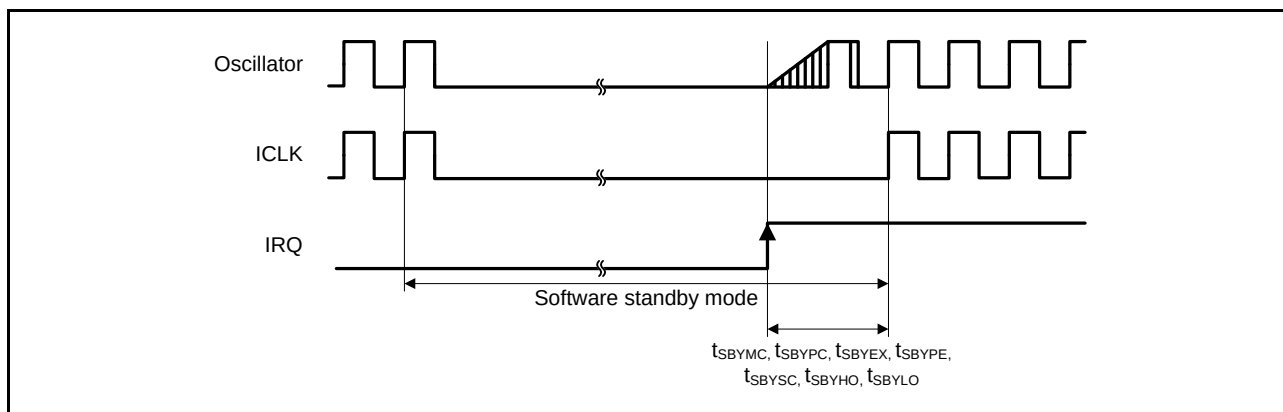


Figure 5.13 Software Standby Mode Cancellation Timing

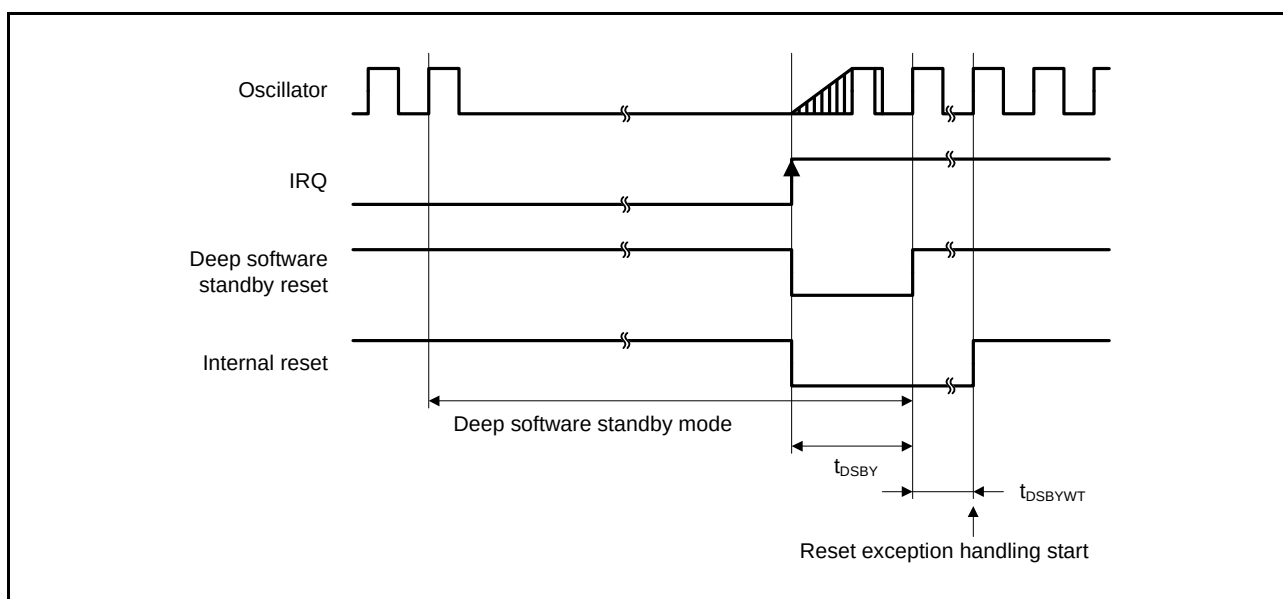


Figure 5.14 Deep Software Standby Mode Cancellation Timing

5.3.4 Control Signal Timing

Table 5.15 Control Signal Timing

Conditions: $V_{CC} = AVCC0 = VREFH = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, $VREFH0 = 2.7$ V to $AVCC0$,
 $VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0$ V, $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
NMI pulse width	t_{NMIW}	200	—	—	ns	$t_c (PCLK) \times 2 \leq 200$ ns Figure 5.15
		$t_c (PCLK) \times 2$				$t_c (PCLK) \times 2 > 200$ ns Figure 5.15
IRQ pulse width	t_{IRQW}	200	—	—	ns	$t_c (PCLK) \times 2 \leq 200$ ns Figure 5.16
		$t_c (PCLK) \times 2$				$t_c (PCLK) \times 2 > 200$ ns Figure 5.16

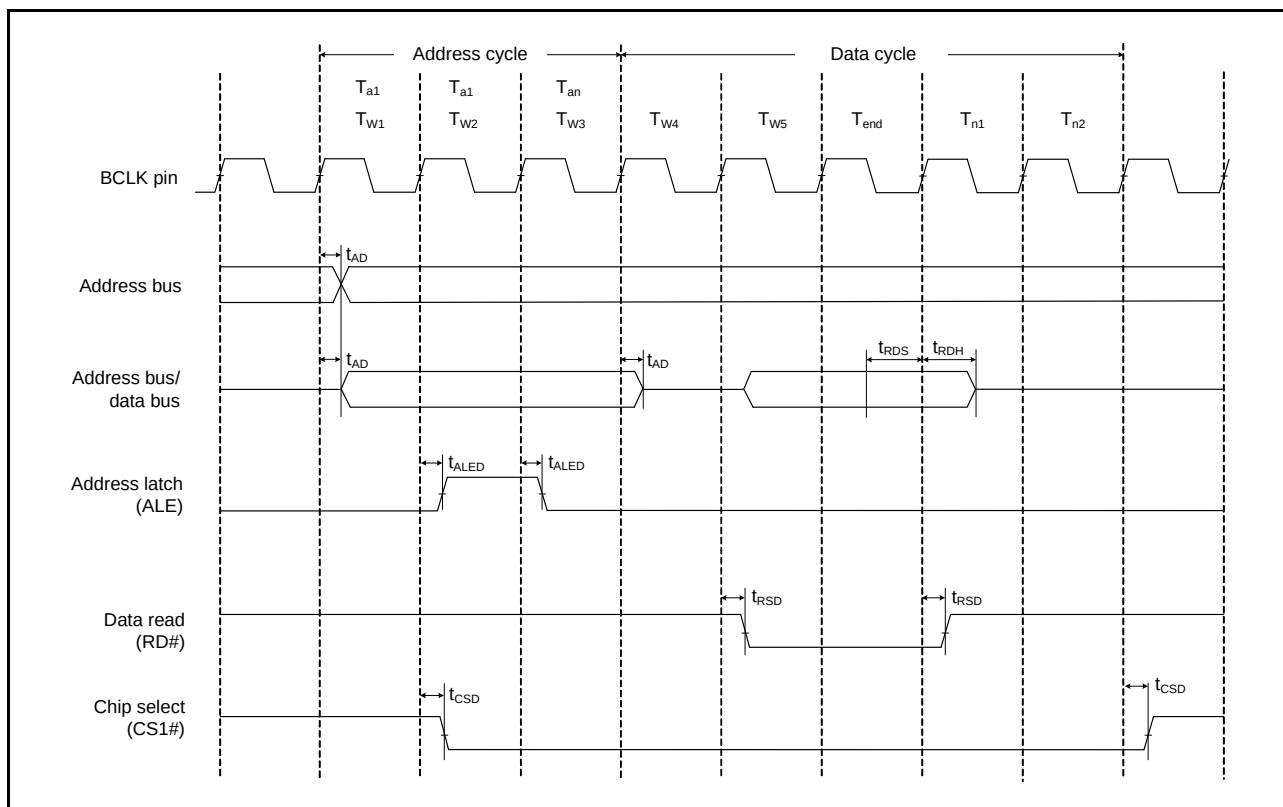


Figure 5.17 Address/Data Multiplexed Bus Read Access Timing

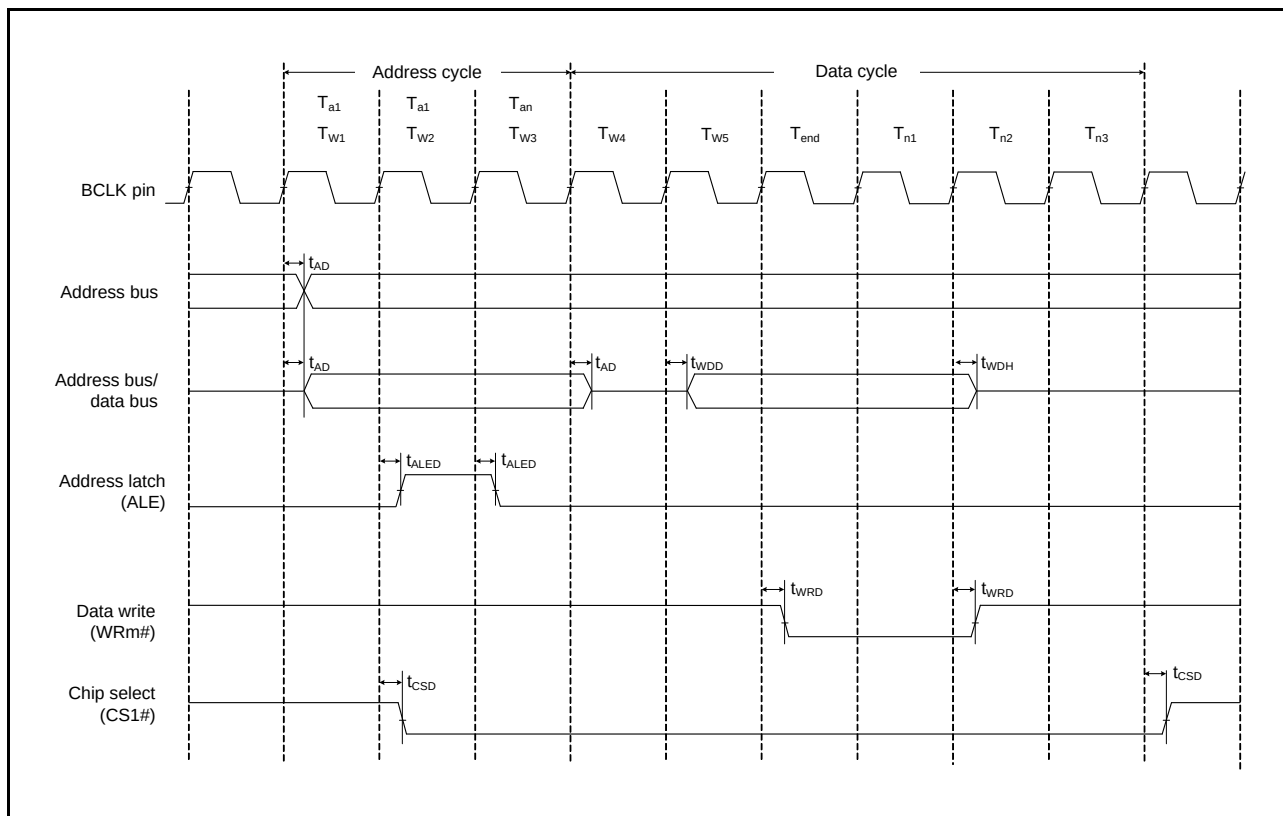


Figure 5.18 Address/Data Multiplexed Bus Write Access Timing

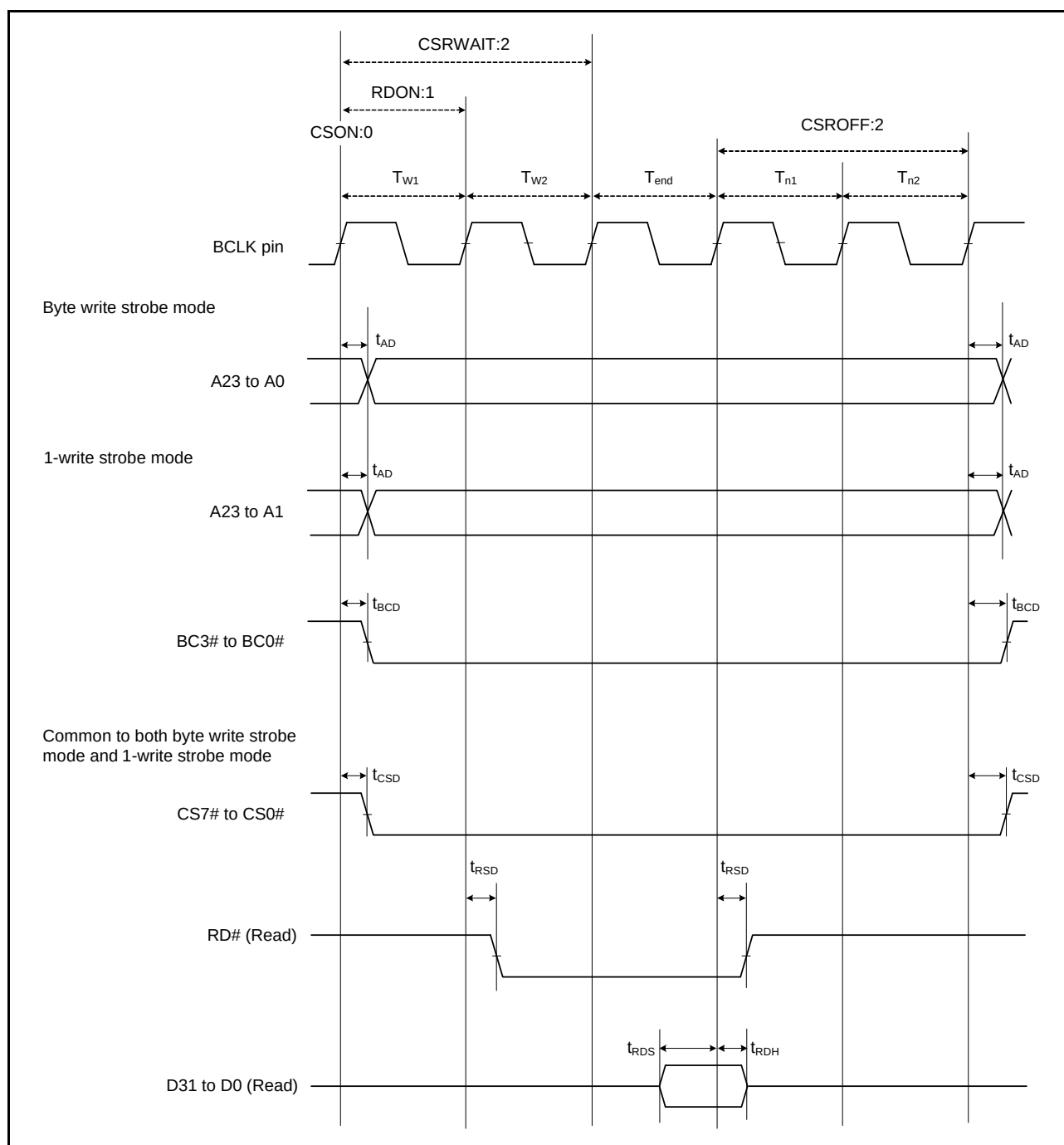


Figure 5.19 External Bus Timing/Normal Read Cycle (Bus Clock Synchronized)

5.3.7 Timing of On-Chip Peripheral Modules

Table 5.19 Timing of On-Chip Peripheral Modules (1)

Conditions: VCC = AVCC0 = VREFH = VCC_USB = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0,
VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V
PCLK = 8 to 50 MHz
T_a = T_{opr}
High drive output is selected by the drive capacity control register.

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
I/O ports	Input data pulse width		t _{PRW}	1.5	—	t _{Pcyc}	Figure 5.34
MTU/TPU	Input capture input pulse width	Single-edge setting	t _{TICW}	1.5	—	t _{Pcyc}	Figure 5.35
		Both-edge setting		2.5	—		
	Timer clock pulse width	Single-edge setting	t _{TCKWH} , t _{TCKWL}	1.5	—	t _{Pcyc}	Figure 5.36
		Both-edge setting		2.5	—		
		Phase counting mode		2.5	—		
POE	POE# input pulse width		t _{POEW}	1.5	—	t _{Pcyc}	Figure 5.37
8-bit timer	Timer clock pulse width	Single-edge setting	t _{TMCWH} , t _{TMCWL}	1.5	—	t _{Pcyc}	Figure 5.38
		Both-edge setting		2.5	—		
SCI	Input clock cycle	Asynchronous	t _{Scyc}	4	—	t _{Pcyc}	Figure 5.39
		Clock synchronous		6	—		
	Input clock pulse width		t _{SCKW}	0.4	0.6	t _{Scyc}	Figure 5.40
	Input clock rise time		t _{SCKr}	—	20	ns	
	Input clock fall time		t _{SCKf}	—	20	ns	
	Output clock cycle	Asynchronous	t _{Scyc}	16	—	t _{Pcyc}	
		Clock synchronous		4	—		
	Output clock pulse width		t _{SCKW}	0.4	0.6	t _{Scyc}	
	Output clock rise time		t _{SCKr}	—	20	ns	
	Output clock fall time		t _{SCKf}	—	20	ns	
	Transmit data delay time	Clock synchronous	t _{TXD}	—	40	ns	
	Receive data setup time	Clock synchronous	t _{RXS}	40	—	ns	
	Receive data hold time	Clock synchronous	t _{RXH}	40	—	ns	
A/D converter	10-bit A/D converter trigger input pulse width		t _{TRGW}	1.5	—	t _{Pcyc}	Figure 5.41
	12-bit A/D converter trigger input pulse width			1.5	—		

Note 1. t_{Pcyc}: PCLK cycle

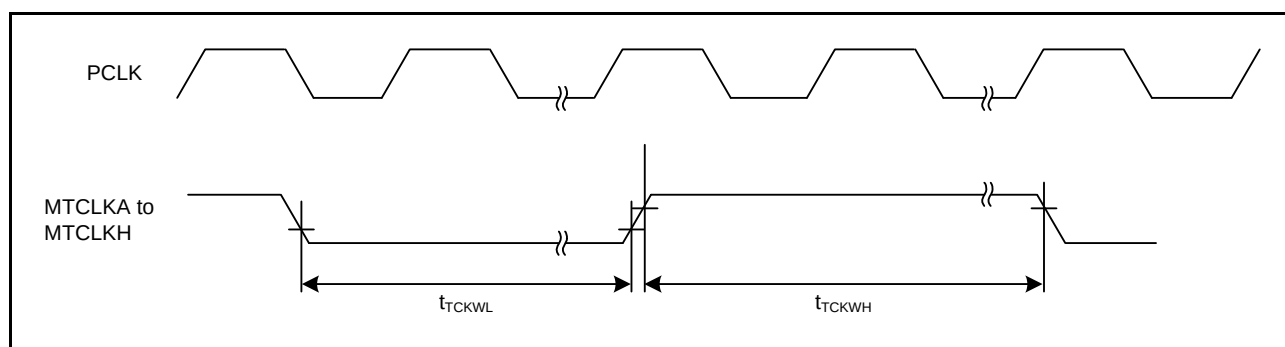


Figure 5.36 MTU Clock Input Timing

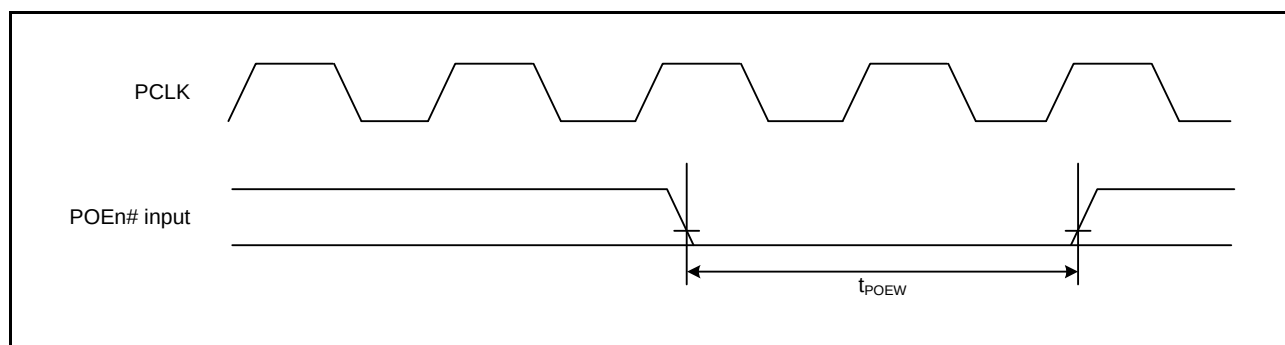


Figure 5.37 POE# Input Timing

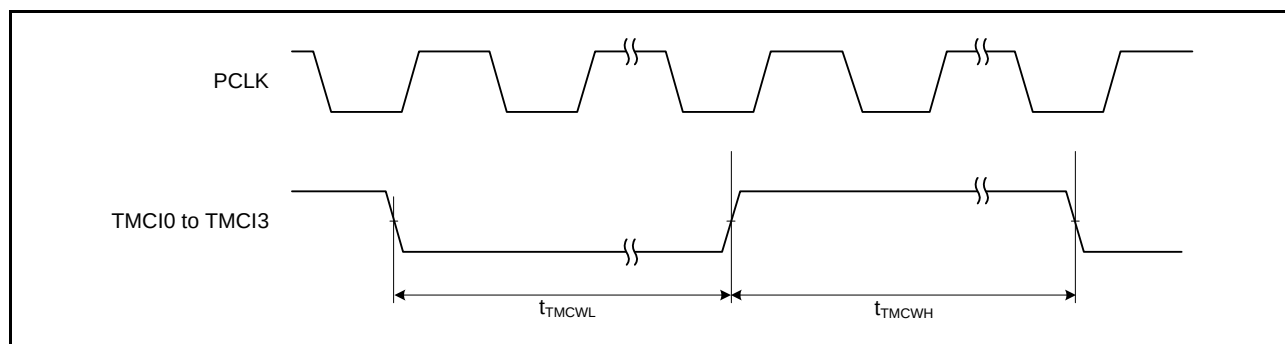


Figure 5.38 8-Bit Timer Clock Input Timing

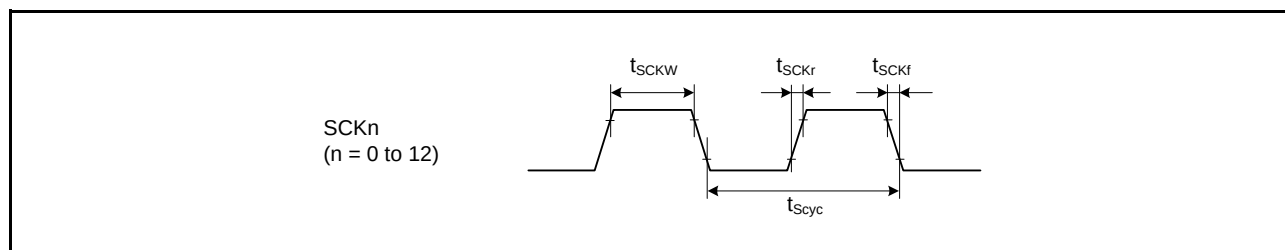


Figure 5.39 SCK Clock Input Timing

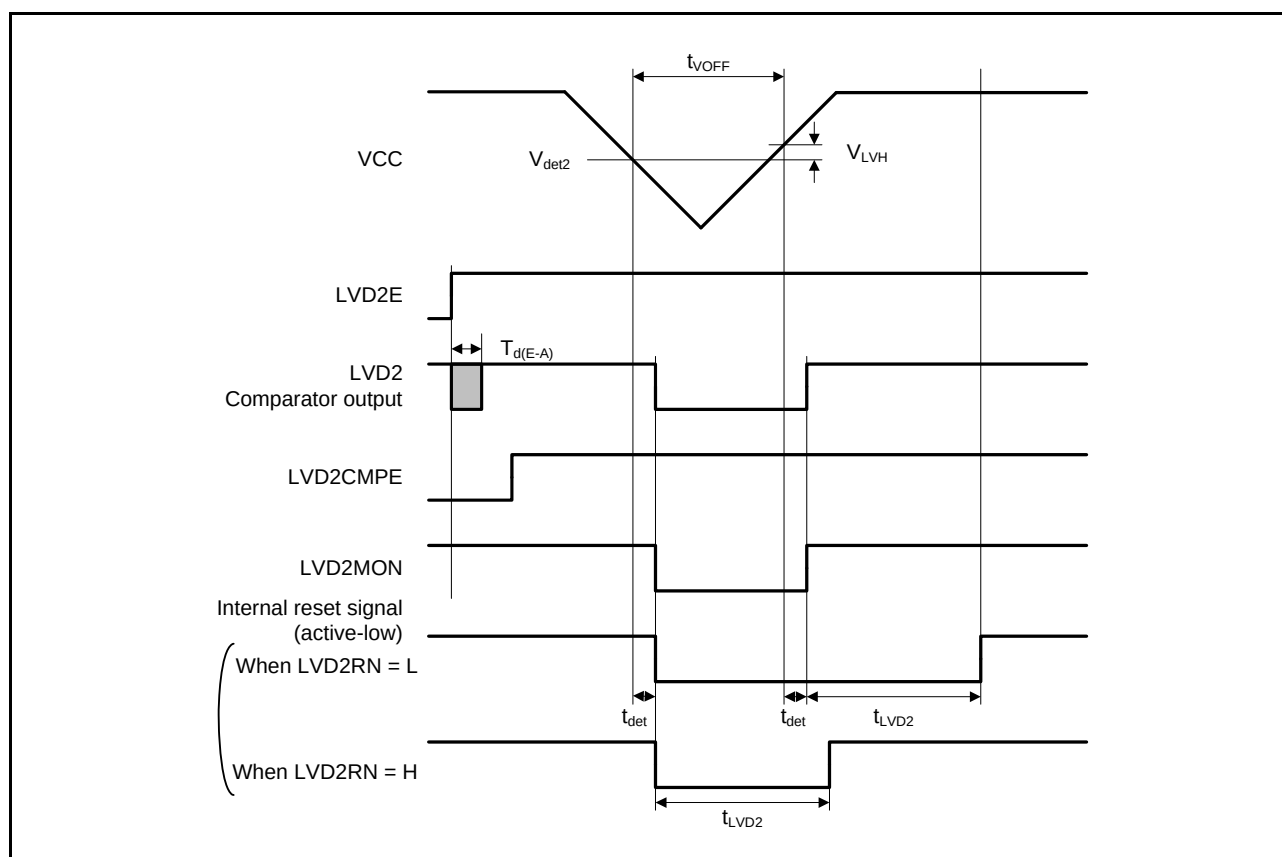


Figure 5.66 Voltage Detection Circuit Timing (V_{det2})

5.12 E² Flash Characteristics**Table 5.38 E² Flash Characteristics (1)**

Conditions: VCC = AVCC0 = VREFH = VCC_USB = 2.7 to 3.6V, VREFH0 = 2.7V to AVCC0
 VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0V
 Temperature range for the programming/erasure operation: T_a = T_{opr}

Item	Symbol	min	typ	max	Unit	Condition
Reprogram/erasure cycle*1	N _{DPEC}	100000	—	—	Times	
Data hold time	t _{DDRP}	30*2	—	—	Year	T _a = +85°C

Note 1. Definition of reprogram/erase cycle:

The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 100000), erasing can be performed n times for each block. For instance, when 128-byte programming is performed 16 times for different addresses in 2-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).

Note 2. The result obtained from the reliability test.

Table 5.39 E² Flash Characteristics (2)

Conditions: VCC = AVCC0 = VREFH = VCC_USB = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0
 VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V
 Temperature range for the programming/erasure operation: T_a = T_{opr}

Item		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 50 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time N _{PEC} ≤ 100 times	2 bytes	t _{DP2}	—	0.7	6	—	0.25	2	ms
Programming time N _{PEC} > 100 times	2 bytes	t _{DP2}	—	0.7	6	—	0.25	2	ms
Erasure time N _{PEC} ≤ 100 times	32 bytes	t _{DE32}	—	4	40	—	2	20	ms
Erasure time N _{PEC} > 100 times	32 bytes	t _{DE32}	—	7	40	—	4	20	ms
Blank check time	2 bytes	t _{DBC2}	—	—	100	—	—	30	μs
Suspend delay time during programming		t _{DSPD}	—	—	250	—	—	120	μs
First suspend delay time during erasure (in suspend priority mode)		t _{DSESD1}	—	—	250	—	—	120	μs
Second suspend delay time during erasure (in suspend priority mode)		t _{DSESD2}	—	—	500	—	—	300	μs
Suspend delay time during erasure (in erasure priority mode)		t _{DSEED}	—	—	500	—	—	300	μs

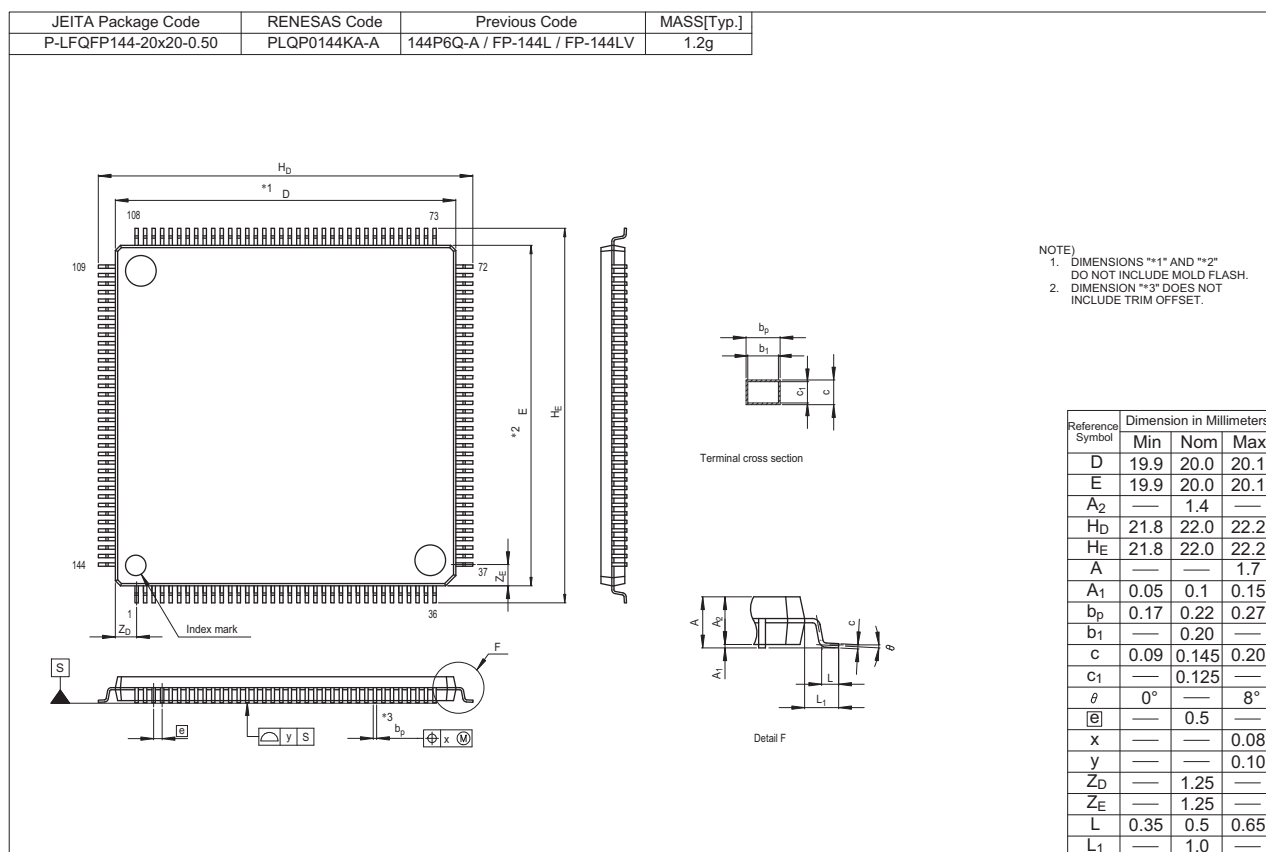


Figure E 144-pin LQFP (PLQP0144KA-A)

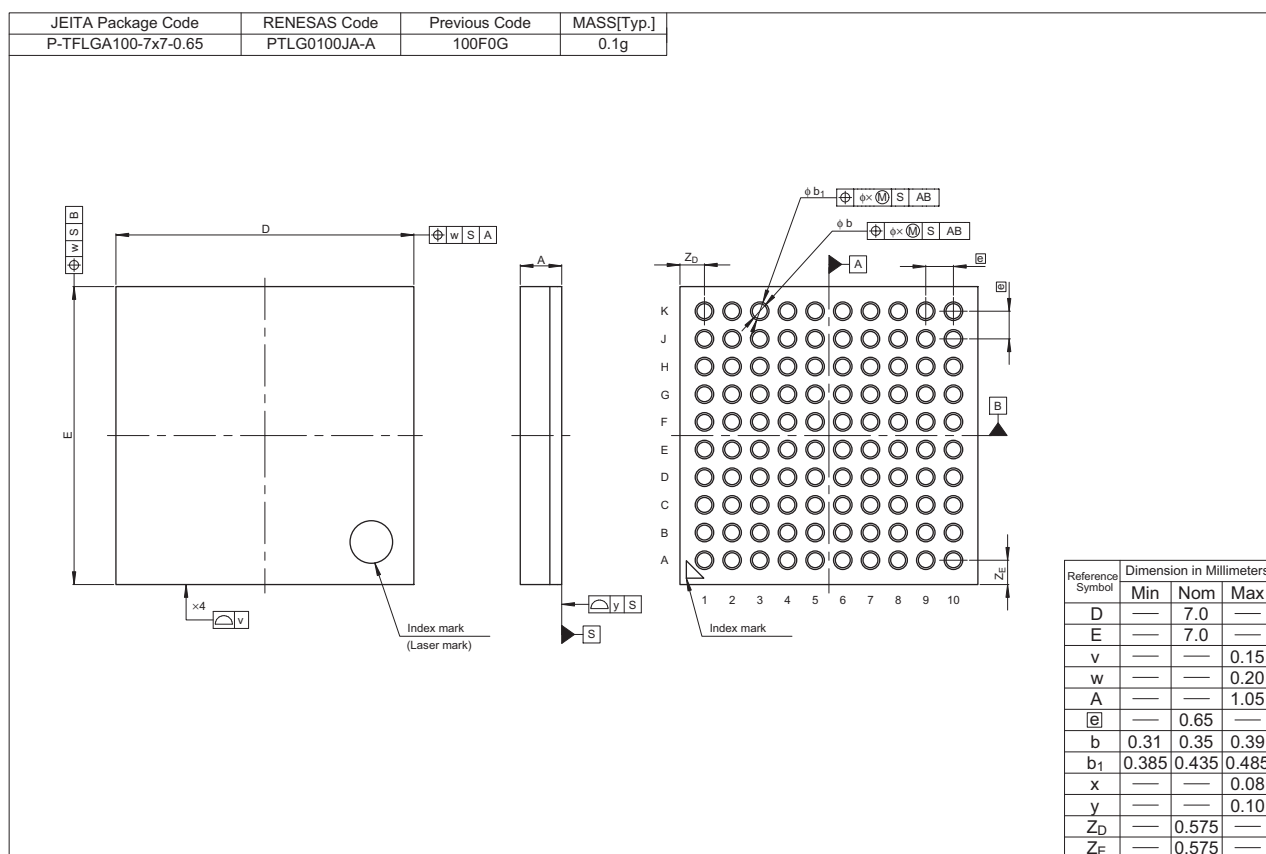


Figure F 100-pin TFLGA (PTLG0100JA-A)

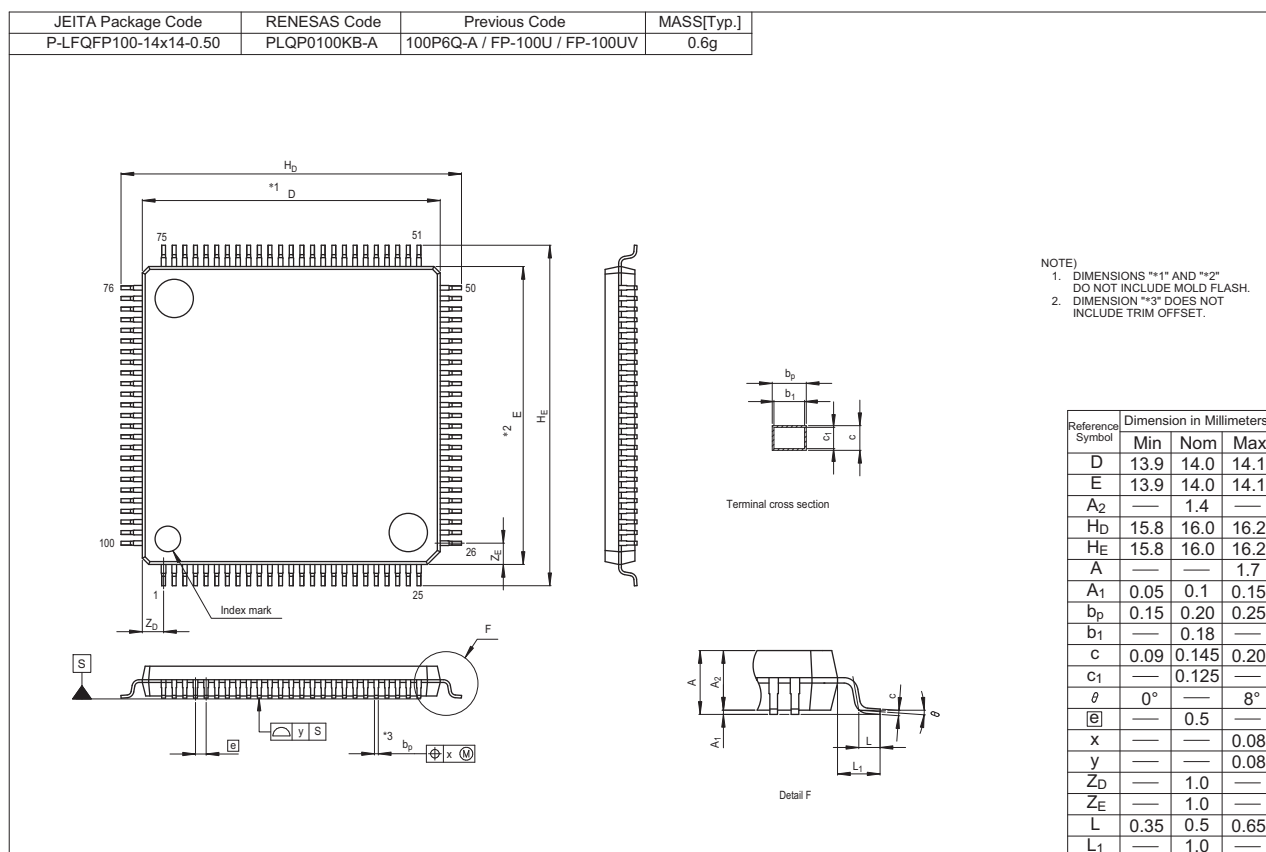


Figure G 100-pin LQFP (PLQP0100KB-A)

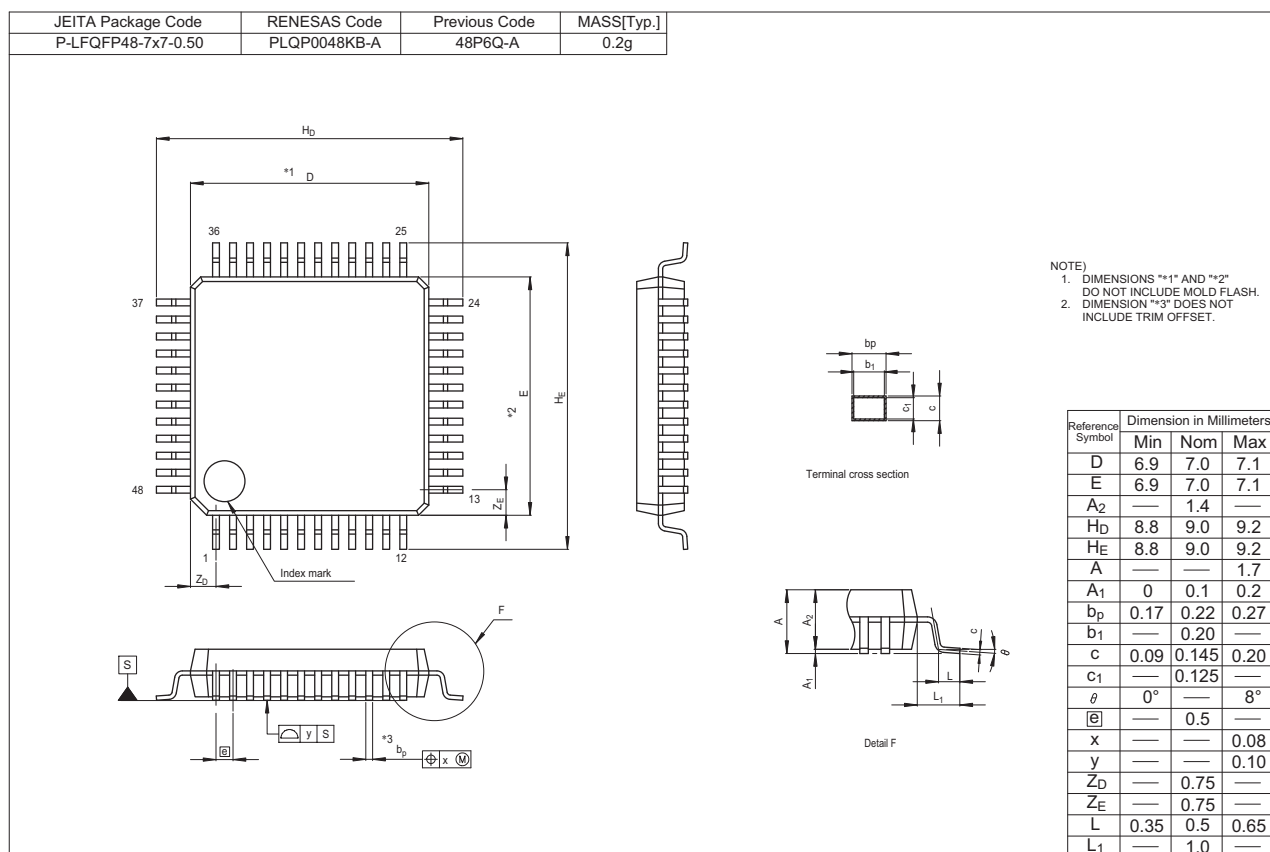


Figure J 48-pin LQFP (PLQP0048KB-A)