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Details

Product Status	Discontinued at Digi-Key
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I ² C, LINbus, SCI, SPI, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	111
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b, 21x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LFQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f5631kddfb-v0

Table 1.3 List of Products (2/8)

Group	Part No.	Package	ROM Capacity	RAM Capacity	E2 Data Flash	Operating Frequency (Max.)	Operating Temp. Range
RX63N (D version)	R5F563NDDDLK	PTLG0145KA-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NBCDLK	PTLG0145KA-A	1 Mbyte	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NBDDLK	PTLG0145KA-A	1 Mbyte	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NACDLK	PTLG0145KA-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NADDLK	PTLG0145KA-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NFHDFB	PLQP0144KA-A	2 Mbytes	256 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NFDDFB	PLQP0144KA-A	2 Mbytes	256 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NKHDFB	PLQP0144KA-A*1	2 Mbytes	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NKDDFB	PLQP0144KA-A	2 Mbytes	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NECDFB	PLQP0144KA-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NEDDFB	PLQP0144KA-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NJHDFB	PLQP0144KA-A*1	1.5 Mbytes	256 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NJDDFB	PLQP0144KA-A*1	1.5 Mbytes	256 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NGHDFB	PLQP0144KA-A*1	1.5 Mbytes	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NGDDFB	PLQP0144KA-A*1	1.5 Mbytes	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NDCDFB	PLQP0144KA-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NDDDFB	PLQP0144KA-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NYHDFB	PLQP0144KA-A	1 Mbyte	256 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NYDDFB	PLQP0144KA-A	1 Mbyte	256 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NWHDFB	PLQP0144KA-A	1 Mbyte	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NWDDFB	PLQP0144KA-A	1 Mbyte	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NBCDFB	PLQP0144KA-A	1 Mbyte	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NBDDFB	PLQP0144KA-A	1 Mbyte	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NACDFB	PLQP0144KA-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NADDFB	PLQP0144KA-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NECDLJ	PTLG0100JA-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NEDDLJ	PTLG0100JA-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NDCDLJ	PTLG0100JA-A*1	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NDDDLJ	PTLG0100JA-A*1	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NBCDLJ	PTLG0100JA-A	1 Mbyte	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NBDDLJ	PTLG0100JA-A	1 Mbyte	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NACDLJ	PTLG0100JA-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NADDLJ	PTLG0100JA-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NFHDFP	PLQP0100KB-A	2 Mbytes	256 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NFDDFP	PLQP0100KB-A	2 Mbytes	256 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NKHDFP	PLQP0100KB-A*1	2 Mbytes	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NKDDFP	PLQP0100KB-A	2 Mbytes	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NECDFP	PLQP0100KB-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NEDDFP	PLQP0100KB-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NJHDFP	PLQP0100KB-A*1	1.5 Mbytes	256 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NJDDFP	PLQP0100KB-A*1	1.5 Mbytes	256 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NGHDFP	PLQP0100KB-A*1	1.5 Mbytes	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NGDDFP	PLQP0100KB-A*1	1.5 Mbytes	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NDCDFP	PLQP0100KB-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NDDDFP	PLQP0100KB-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C

Table 1.3 List of Products (8/8)

Group	Part No.	Package	ROM Capacity	RAM Capacity	E2 Data Flash	Operating Frequency (Max.)	Operating Temp. Range
RX631 (G version) *2	R5F5631GDGFB	PLQP0144KA-A	1.5 Mbytes	192 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631DDGFB	PLQP0144KA-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631YDGFB	PLQP0144KA-A	1 Mbyte	256 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631WDGFB	PLQP0144KA-A	1 Mbyte	192 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631BDGFB	PLQP0144KA-A	1 Mbyte	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631ADGFB	PLQP0144KA-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F56318SGFB	PLQP0144KA-A	512 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F56318DGFB	PLQP0144KA-A	512 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F56317SGFB	PLQP0144KA-A	384 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F56317DGFB	PLQP0144KA-A	384 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F56316SGFB	PLQP0144KA-A	256 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F56316DGFB	PLQP0144KA-A	256 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631FDGFP	PLQP0100KB-A	2 Mbytes	256 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631KDGFP	PLQP0100KB-A	2 Mbytes	192 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631EDGFP	PLQP0100KB-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631JDGFP	PLQP0100KB-A	1.5 Mbytes	256 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631GDGFP	PLQP0100KB-A	1.5 Mbytes	192 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631DDGFP	PLQP0100KB-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631YDGFP	PLQP0100KB-A	1 Mbyte	256 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631WDGFP	PLQP0100KB-A	1 Mbyte	192 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631BDGFP	PLQP0100KB-A	1 Mbyte	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631ADGFP	PLQP0100KB-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F56318DGFP	PLQP0100KB-A	512 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F56317DGFP	PLQP0100KB-A	384 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F56316DGFP	PLQP0100KB-A	256 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631PDGFM	PLQP0064KB-A	512 Kbytes	64 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631NDGFM	PLQP0064KB-A	384 Kbytes	64 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631MDGFM	PLQP0064KB-A	256 Kbytes	64 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631PDGFL	PLQP0048KB-A	512 Kbytes	64 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631NDGFL	PLQP0048KB-A	384 Kbytes	64 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631MDGFL	PLQP0048KB-A	256 Kbytes	64 Kbytes	32 Kbytes	100 MHz	-40 to +105°C

Note 1. In the planning stage

Note 2. The specifications of the temperature sensor calibration and unique ID for G-version products differ from those for other products. For details, see section 45.2.2, Temperature Sensor Calibration Data Registers (TSCDRH, TSCDRL), section 45.3, Using the Temperature Sensor, and section 47.2.22, Unique ID Registers n (UIDRn) (n = 0 to 15) in the User's manual: Hardware.

	A	B	C	D	E	F	G	H	J	K	L	M	N	
13	PE3	PE4	VSS	PE6	P67	PA2	PA4	PA7	PB1	PB5	VSS	VCC	P74	13
12	PE1	PE2	P70	PE5	P65	PA1	VCC	PB0	PB2	PB6	P73	PC1	P75	12
11	P62	P61	PE0	VCC	P66	VSS	PA6	P71	PB4	PB7	PC2	PC0	PC3	11
10	VSS	VCC	P63	PE7	PA0	PA3	PA5	P72	PB3	P76	PC4	P77	P82	10
9	PD6	PD4	PD7	P64	RX63N Group RX631 Group PTLG0145KA-A (145-pin TFLGA) (Top perspective view)					P80	PC5	P81	PC7	9
8	PD2	PD0	PD3	P60						VCC	P83	PC6	VSS	8
7	P92	P91	PD1	PD5						P51	P52	P50	P55	7
6	P90	P47	VSS	P93						P53	P56	VSS_ USB	USB0_ DP	6
5	P45	P43	P46	VCC	P44					P54	P13	VCC_ USB	USB0_ DM	5
4	P42	VREFL0	P41	P01	EMLE	VBATT	BSCANP	P35	P30	P15	P24	P12	P14	4
3	P40	P05	VREFH0	P03	PJ5	PJ3	MD/ FINED	VSS	P32	P31	P16	P86	P87	3
2	P07	AVCC0	P02	PF5	VCL	XCOUT	RES#	VCC	P33	P26	P23	P17	P20	2
1	AVSS0	VREFH	VREFL	P00	VSS	XCIN	XTAL	EXTAL	P34	P27	P25	P22	P21	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	

Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.7, List of Pins and Pin Functions (145-Pin TFLGA).

Figure 1.6 Pin Assignment (145-Pin TFLGA)

Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (5/5)

Pin Number 177-Pin TFLGA 176-Pin LFBGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SCIC, SCID, RSPI, RIIC, CAN, IEB, USB, and PDC)	Interrupt	S12AD, AD, DA
P1	VSS						
P2		P17		MTIOC3A/MTIOC3B/ TIOCB0/TCLKD/TMO1/ PO15/POE8#	SCK1/TXD3/SMOSI3/ SSDA3/MISOA/SDA2-DS/ IETXD/USB1_VBUS/ PIXD3	IRQ7	ADTRG#
P3		P87		TIOCA2	PIXD2		
P4		P14		MTIOC3A/MTCLKA/ TIOCB5/TCLKA/TMRI2/ PO15	CTS1#/RTS1#/SS1#/ CTX1/USB0_DPUPE/ USB0_OVRCURA	IRQ4	
P5		P10		MTIC5W/TMRI3		IRQ0	
P6	VCC_USB						
P7	VSS_USB						
P8					USB1_DP		
P9		P52	RD#		RXD2/SMISO2/SSCL2/ SSLB3		
P10		P83	EDACK1	MTIOC4C	ET_CRS/RMII_CRS_DV/ CTS10#/RTS10#/SS10#		
P11		PC6	A22/CS1#	MTIOC3C/MTCLKA/ TIOCA6/TMC12/PO30	ET_ETXD3/RXD8/ SMISO8/SSCL8/MOSIA	IRQ13	
P12		PC4	A20/CS3#	MTIOC3D/MTCLKC/ TIOCC6/TCLKE/TMC11/ PO25/POE0#	ET_TX_CLK/SCK5/ CTS8#/RTS8#/SS8#/ SSLA0		
P13		PC2	A18	MTIOC4B/TCLKA/PO21	ET_RX_DV/RXD5/ SMISO5/SSCL5/SSLA3/ IERXD		
P14		P75	CS5#	PO20	ET_ERXD0/RMII_RXD0/ SCK11		
P15	VCC						
R1		P21		MTIOC1B/TIOCA3/ TMC10/PO1	RXD0/SMISO0/SSCL0/ SCL1/USB0_EXICEN/ PIXD5	IRQ9	
R2		P20		MTIOC1A/TIOCB3/ TMRI0/PO0	TXD0/SMOSI0/SSDA0/ SDA1/USB0_ID/PIXD4	IRQ8	
R3		P16		MTIOC3C/MTIOC3D/ TIOCB1/TCLKC/TMO2/ PO14/RTCOU	TXD1/RXD3/SMOSI1/ SMISO3/SSDA1/SSCL3/ MOSIA/SCL2-DS/IERXD/ USB0_VBUS/ USB0_VBUSEN/ USB0_OVRCURB	IRQ6	ADTRG0#
R4		P85					
R5		P11		MTIC5V/TMC13	SCK2	IRQ1	
R6					USB0_DM		
R7					USB0_DP		
R8					USB1_DM		
R9		P84					
R10	VSS						
R11	VCC						
R12		P80	EDREQ0	MTIOC3B/PO26	ET_TX_EN/ RMII_TXD_EN/SCK10		
R13		P76	CS6#	PO22	ET_RX_CLK/REF50CK/ RXD11/SMISO11/SSCL11		
R14		P74	CS4#	PO19	ET_ERXD1/RMII_RXD1/ CTS11#/RTS11#/SS11#		
R15		PC1	A17	MTIOC3A/TCLKD/PO18	ET_ERXD2/SCK5/SSLA2/ SDA3	IRQ12	

Note 1. 176-pin LFBGA does not have E5 pin

Note 2. The BCLK function is multiplexed with the I/O port function for pin P53, so the port function is not available if the external bus is enabled.

Table 1.6 List of Pin and Pin Functions (176-Pin LQFP) (3/5)

Pin Number	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SCIC, SCID, RSPI, RIIC, CAN, IEB, USB, and PDC)	Interrupt	S12AD, AD, DA
72		P50	WR0#/WR#		TXD2/SMOSI2/SSDA2/ SSLB1		
73	VSS						
74		P83	EDACK1	MTIOC4C	ET_CRS/RMII_CRS_DV/ CTS10#/RTS10#/SS10#		
75	VCC						
76		PC7	A23/CS0#	MTIOC3A/MTCLKB/ TIOCB6/TMO2/PO31	ET_COL/TXD8/SMOSI8/ SSDA8/MISOA	IRQ14	
77		PC6	A22/CS1#	MTIOC3C/MTCLKA/ TIOCA6/TMCI2/PO30	ET_ETXD3/RXD8/ SMISO8/SSCL8/MOSIA	IRQ13	
78		PC5	A21/CS2#/ WAIT#	MTIOC3B/MTCLKD/ TIOCD6/TCLKF/TMRI2/ PO29	ET_ETXD2/SCK8/ RSPCKA		
79		P82	EDREQ1	MTIOC4A/PO28	ET_ETXD1/RMII_TXD1/ TXD10/SMOSI10/SSDA10		
80		P81	EDACK0	MTIOC3D/PO27	ET_ETXD0/RMII_TXD0/ RXD10/SMISO10/SSCL10		
81		P80	EDREQ0	MTIOC3B/PO26	ET_TX_EN/ RMII_TXD_EN/SCK10		
82		PC4	A20/CS3#	MTIOC3D/MTCLKC/ TIOCC6/TCLKE/TMCI1/ PO25/POE0#	ET_TX_CLK/SCK5/ CTS8#/RTS8#/SS8#/ SSLA0		
83		PC3	A19	MTIOC4D/TCLKB/PO24	ET_TX_ER/TXD5/ SMOSI5/SSDA5/IETXD		
84		P77	CS7#	PO23	ET_RX_ER/RMII_RX_ER/ TXD11/SMOSI11/SSDA11		
85		P76	CS6#	PO22	ET_RX_CLK/REF50CK/ RXD11/SMISO11/SSCL11		
86		PC2	A18	MTIOC4B/TCLKA/PO21	ET_RX_DV/RXD5/ SMISO5/SSCL5/SSLA3/ IERXD		
87		P75	CS5#	PO20	ET_ERXD0/RMII_RXD0/ SCK11		
88		P74	CS4#	PO19	ET_ERXD1/RMII_RXD1/ CTS11#/RTS11#/SS11#		
89		PC1	A17	MTIOC3A/TCLKD/PO18	ET_ERXD2/SCK5/SSLA2/ SDA3	IRQ12	
90	VCC						
91		PC0	A16	MTIOC3C/TCLKC/PO17	ET_ERXD3/CTS5#/ RTS5#/SS5#/SSLA1/ SCL3	IRQ14	
92	VSS						
93		P73	CS3#	PO16	ET_WOL		
94		PB7	A15	MTIOC3B/TIOCB5/PO31	ET_CRS/RMII_CRS_DV/ TXD9/SMOSI9/SSDA9		
95		PB6	A14	MTIOC3D/TIOCA5/PO30	ET_ETXD1/RMII_TXD1/ RXD9/SMISO9/SSCL9		
96		PB5	A13	MTIOC2A/MTIOC1B/ TIOCB4/TMRI1/PO29/ POE1#	ET_ETXD0/RMII_TXD0/ SCK9		
97		PB4	A12	TIOCA4/PO28	ET_TX_EN/ RMII_TXD_EN/CTS9#/ RTS9#/SS9#		
98		PB3	A11	MTIOC0A/MTIOC4A/ TIOCD3/TCLKD/TMO0/ PO27/POE3#	ET_RX_ER/RMII_RX_ER/ SCK4/SCK6		
99		PB2	A10	TIOCC3/TCLKC/PO26	ET_RX_CLK/REF50CK/ CTS4#/RTS4#/CTS6#/ RTS6#/SS4#/SS6#		

3. Address Space

3.1 Address Space

This LSI has a 4-Gbyte address space, consisting of the range of addresses from 0000 0000h to FFFF FFFFh. That is, linear access to an address space of up to 4 Gbytes is possible, and this contains both program and data areas.

Figure 3.1 shows the memory maps in the respective operating modes. Accessible areas will differ according to the operating mode and states of control bits.

Table 4.1 List of I/O Registers (Address Order) (2/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 201Ch	DMAC0	DMA transfer enable register	DMCNT	8	8	2	ICLK	DMACA
0008 201Dh	DMAC0	DMA software start register	DMREQ	8	8	2	ICLK	
0008 201Eh	DMAC0	DMA status register	DMSTS	8	8	2	ICLK	
0008 201Fh	DMAC0	DMA activation source flag control register	DMCSL	8	8	2	ICLK	
0008 2040h	DMAC1	DMA source address register	DMSAR	32	32	2	ICLK	
0008 2044h	DMAC1	DMA destination address register	DMDAR	32	32	2	ICLK	
0008 2048h	DMAC1	DMA transfer count register	DMCRA	32	32	2	ICLK	
0008 204Ch	DMAC1	DMA block transfer count register	DMCRB	16	16	2	ICLK	
0008 2050h	DMAC1	DMA transfer mode register	DMTMD	16	16	2	ICLK	
0008 2053h	DMAC1	DMA interrupt setting register	DMINT	8	8	2	ICLK	
0008 2054h	DMAC1	DMA address mode register	DMAMD	16	16	2	ICLK	
0008 205Ch	DMAC1	DMA transfer enable register	DMCNT	8	8	2	ICLK	
0008 205Dh	DMAC1	DMA software start register	DMREQ	8	8	2	ICLK	
0008 205Eh	DMAC1	DMA status register	DMSTS	8	8	2	ICLK	
0008 205Fh	DMAC1	DMA activation source flag control register	DMCSL	8	8	2	ICLK	
0008 2080h	DMAC2	DMA source address register	DMSAR	32	32	2	ICLK	
0008 2084h	DMAC2	DMA destination address register	DMDAR	32	32	2	ICLK	
0008 2088h	DMAC2	DMA transfer count register	DMCRA	32	32	2	ICLK	
0008 208Ch	DMAC2	DMA block transfer count register	DMCRB	16	16	2	ICLK	
0008 2090h	DMAC2	DMA transfer mode register	DMTMD	16	16	2	ICLK	
0008 2093h	DMAC2	DMA interrupt setting register	DMINT	8	8	2	ICLK	
0008 2094h	DMAC2	DMA address mode register	DMAMD	16	16	2	ICLK	
0008 209Ch	DMAC2	DMA transfer enable register	DMCNT	8	8	2	ICLK	
0008 209Dh	DMAC2	DMA software start register	DMREQ	8	8	2	ICLK	
0008 209Eh	DMAC2	DMA status register	DMSTS	8	8	2	ICLK	
0008 209Fh	DMAC2	DMA activation source flag control register	DMCSL	8	8	2	ICLK	
0008 20C0h	DMAC3	DMA source address register	DMSAR	32	32	2	ICLK	EXDMACa
0008 20C4h	DMAC3	DMA destination address register	DMDAR	32	32	2	ICLK	
0008 20C8h	DMAC3	DMA transfer count register	DMCRA	32	32	2	ICLK	
0008 20CCh	DMAC3	DMA block transfer count register	DMCRB	16	16	2	ICLK	
0008 20D0h	DMAC3	DMA transfer mode register	DMTMD	16	16	2	ICLK	
0008 20D3h	DMAC3	DMA interrupt setting register	DMINT	8	8	2	ICLK	
0008 20D4h	DMAC3	DMA address mode register	DMAMD	16	16	2	ICLK	
0008 20DCh	DMAC3	DMA transfer enable register	DMCNT	8	8	2	ICLK	
0008 20DDh	DMAC3	DMA software start register	DMREQ	8	8	2	ICLK	
0008 20DEh	DMAC3	DMA status register	DMSTS	8	8	2	ICLK	
0008 20DFh	DMAC3	DMA activation source flag control register	DMCSL	8	8	2	ICLK	
0008 2200h	DMAC	DMACA module activation register	DMAST	8	8	2	ICLK	
0008 2400h	DTC	DTC control register	DTCCR	8	8	2	ICLK	DTCa
0008 2404h	DTC	DTC vector base register	DTCVBR	32	32	2	ICLK	
0008 2408h	DTC	DTC address mode register	DTCADMOD	8	8	2	ICLK	
0008 240Ch	DTC	DTC module start register	DTCST	8	8	2	ICLK	
0008 240Eh	DTC	DTC status register	DTCSTS	16	16	2	ICLK	
0008 2800h	EXDMAC0	EXDMA source address register	EDMSAR	32	32	1, 2	BCLK	EXDMACa
0008 2804h	EXDMAC0	EXDMA destination address register	EDMDAR	32	32	1, 2	BCLK	
0008 2808h	EXDMAC0	EXDMA transfer count register	EDMCRA	32	32	1, 2	BCLK	
0008 280Ch	EXDMAC0	EXDMA block transfer count register	EDMCRB	16	16	1, 2	BCLK	
0008 2810h	EXDMAC0	EXDMA transfer mode register	EDMTMD	16	16	1, 2	BCLK	
0008 2812h	EXDMAC0	EXDMA output setting register	EDMOMD	8	8	1, 2	BCLK	
0008 2813h	EXDMAC0	EXDMA interrupt setting register	EDMINT	8	8	1, 2	BCLK	
0008 2814h	EXDMAC0	EXDMA address mode register	EDMAMD	32	32	1, 2	BCLK	

Table 4.1 List of I/O Registers (Address Order) (9/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 7128h	ICU	DTC activation enable register 040	DTCER040	8	8	2	ICLK	ICUb
0008 712Ah	ICU	DTC activation enable register 042	DTCER042	8	8	2	ICLK	
0008 712Bh	ICU	DTC activation enable register 043	DTCER043	8	8	2	ICLK	
0008 712Dh	ICU	DTC activation enable register 045	DTCER045	8	8	2	ICLK	
0008 712Eh	ICU	DTC activation enable register 046	DTCER046	8	8	2	ICLK	
0008 7140h	ICU	DTC activation enable register 064	DTCER064	8	8	2	ICLK	
0008 7141h	ICU	DTC activation enable register 065	DTCER065	8	8	2	ICLK	
0008 7142h	ICU	DTC activation enable register 066	DTCER066	8	8	2	ICLK	
0008 7143h	ICU	DTC activation enable register 067	DTCER067	8	8	2	ICLK	
0008 7144h	ICU	DTC activation enable register 068	DTCER068	8	8	2	ICLK	
0008 7145h	ICU	DTC activation enable register 069	DTCER069	8	8	2	ICLK	
0008 7146h	ICU	DTC activation enable register 070	DTCER070	8	8	2	ICLK	
0008 7147h	ICU	DTC activation enable register 071	DTCER071	8	8	2	ICLK	
0008 7148h	ICU	DTC activation enable register 072	DTCER072	8	8	2	ICLK	
0008 7149h	ICU	DTC activation enable register 073	DTCER073	8	8	2	ICLK	
0008 714Ah	ICU	DTC activation enable register 074	DTCER074	8	8	2	ICLK	
0008 714Bh	ICU	DTC activation enable register 075	DTCER075	8	8	2	ICLK	
0008 714Ch	ICU	DTC activation enable register 076	DTCER076	8	8	2	ICLK	
0008 714Dh	ICU	DTC activation enable register 077	DTCER077	8	8	2	ICLK	
0008 714Eh	ICU	DTC activation enable register 078	DTCER078	8	8	2	ICLK	
0008 714Fh	ICU	DTC activation enable register 079	DTCER079	8	8	2	ICLK	
0008 7162h	ICU	DTC activation enable register 098	DTCER098	8	8	2	ICLK	
0008 7166h	ICU	DTC activation enable register 102	DTCER102	8	8	2	ICLK	
0008 717Eh	ICU	DTC activation enable register 126	DTCER126	8	8	2	ICLK	
0008 717Fh	ICU	DTC activation enable register 127	DTCER127	8	8	2	ICLK	
0008 7180h	ICU	DTC activation enable register 128	DTCER128	8	8	2	ICLK	
0008 7181h	ICU	DTC activation enable register 129	DTCER129	8	8	2	ICLK	
0008 7182h	ICU	DTC activation enable register 130	DTCER130	8	8	2	ICLK	
0008 7183h	ICU	DTC activation enable register 131	DTCER131	8	8	2	ICLK	
0008 7184h	ICU	DTC activation enable register 132	DTCER132	8	8	2	ICLK	
0008 7185h	ICU	DTC activation enable register 133	DTCER133	8	8	2	ICLK	
0008 7186h	ICU	DTC activation enable register 134	DTCER134	8	8	2	ICLK	
0008 7187h	ICU	DTC activation enable register 135	DTCER135	8	8	2	ICLK	
0008 7188h	ICU	DTC activation enable register 136	DTCER136	8	8	2	ICLK	
0008 7189h	ICU	DTC activation enable register 137	DTCER137	8	8	2	ICLK	
0008 718Ah	ICU	DTC activation enable register 138	DTCER138	8	8	2	ICLK	
0008 718Bh	ICU	DTC activation enable register 139	DTCER139	8	8	2	ICLK	
0008 718Ch	ICU	DTC activation enable register 140	DTCER140	8	8	2	ICLK	
0008 718Dh	ICU	DTC activation enable register 141	DTCER141	8	8	2	ICLK	
0008 718Eh	ICU	DTC activation enable register 142	DTCER142	8	8	2	ICLK	
0008 718Fh	ICU	DTC activation enable register 143	DTCER143	8	8	2	ICLK	
0008 7190h	ICU	DTC activation enable register 144	DTCER144	8	8	2	ICLK	
0008 7191h	ICU	DTC activation enable register 145	DTCER145	8	8	2	ICLK	
0008 7194h	ICU	DTC activation enable register 148	DTCER148	8	8	2	ICLK	
0008 7195h	ICU	DTC activation enable register 149	DTCER149	8	8	2	ICLK	
0008 7196h	ICU	DTC activation enable register 150	DTCER150	8	8	2	ICLK	
0008 7197h	ICU	DTC activation enable register 151	DTCER151	8	8	2	ICLK	
0008 7198h	ICU	DTC activation enable register 152	DTCER152	8	8	2	ICLK	
0008 7199h	ICU	DTC activation enable register 153	DTCER153	8	8	2	ICLK	
0008 719Ah	ICU	DTC activation enable register 154	DTCER154	8	8	2	ICLK	
0008 719Bh	ICU	DTC activation enable register 155	DTCER155	8	8	2	ICLK	

Table 4.1 List of I/O Registers (Address Order) (20/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 8368h	RIIC3	I ² C bus status register 1	ICSR1	8	8	2, 3 PCLKB	2 ICLK	RSPI
0008 8369h	RIIC3	I ² C bus status register 2	ICSR2	8	8	2, 3 PCLKB	2 ICLK	
0008 836Ah	RIIC3	Slave address register L0	SARL0	8	8	2, 3 PCLKB	2 ICLK	
0008 836Bh	RIIC3	Slave address register U0	SARU0	8	8	2, 3 PCLKB	2 ICLK	
0008 836Ch	RIIC3	Slave address register L1	SARL1	8	8	2, 3 PCLKB	2 ICLK	
0008 836Dh	RIIC3	Slave address register U1	SARU1	8	8	2, 3 PCLKB	2 ICLK	
0008 836Eh	RIIC3	Slave address register L2	SARL2	8	8	2, 3 PCLKB	2 ICLK	
0008 836Fh	RIIC3	Slave address register U2	SARU2	8	8	2, 3 PCLKB	2 ICLK	
0008 8370h	RIIC3	I ² C bus bit rate low-level register	ICBRL	8	8	2, 3 PCLKB	2 ICLK	
0008 8371h	RIIC3	I ² C bus bit rate high-level register	ICBRH	8	8	2, 3 PCLKB	2 ICLK	
0008 8372h	RIIC3	I ² C bus transmit data register	ICDRT	8	8	2, 3 PCLKB	2 ICLK	
0008 8373h	RIIC3	I ² C bus receive data register	ICDRR	8	8	2, 3 PCLKB	2 ICLK	
0008 8380h	RSPI0	RSPI control register	SPCR	8	8	2, 3 PCLKB	2 ICLK	
0008 8381h	RSPI0	RSPI slave select polarity register	SSLP	8	8	2, 3 PCLKB	2 ICLK	
0008 8382h	RSPI0	RSPI pin control register	SPPCR	8	8	2, 3 PCLKB	2 ICLK	
0008 8383h	RSPI0	RSPI status register	SPSR	8	8	2, 3 PCLKB	2 ICLK	
0008 8384h	RSPI0	RSPI data register	SPDR	32	16, 32	2, 3 PCLKB	2 ICLK	
0008 8388h	RSPI0	RSPI sequence control register	SPSCR	8	8	2, 3 PCLKB	2 ICLK	
0008 8389h	RSPI0	RSPI sequence status register	SPSSR	8	8	2, 3 PCLKB	2 ICLK	
0008 838Ah	RSPI0	RSPI bit rate register	SPBR	8	8	2, 3 PCLKB	2 ICLK	
0008 838Bh	RSPI0	RSPI data control register	SPDCR	8	8	2, 3 PCLKB	2 ICLK	
0008 838Ch	RSPI0	RSPI clock delay register	SPCKD	8	8	2, 3 PCLKB	2 ICLK	
0008 838Dh	RSPI0	RSPI slave select negation delay register	SSLND	8	8	2, 3 PCLKB	2 ICLK	
0008 838Eh	RSPI0	RSPI next-access delay register	SPND	8	8	2, 3 PCLKB	2 ICLK	
0008 838Fh	RSPI0	RSPI control register 2	SPCR2	8	8	2, 3 PCLKB	2 ICLK	
0008 8390h	RSPI0	RSPI command register 0	SPCMD0	16	16	2, 3 PCLKB	2 ICLK	
0008 8392h	RSPI0	RSPI command register 1	SPCMD1	16	16	2, 3 PCLKB	2 ICLK	
0008 8394h	RSPI0	RSPI command register 2	SPCMD2	16	16	2, 3 PCLKB	2 ICLK	
0008 8396h	RSPI0	RSPI command register 3	SPCMD3	16	16	2, 3 PCLKB	2 ICLK	
0008 8398h	RSPI0	RSPI command register 4	SPCMD4	16	16	2, 3 PCLKB	2 ICLK	
0008 839Ah	RSPI0	RSPI command register 5	SPCMD5	16	16	2, 3 PCLKB	2 ICLK	RSPI
0008 839Ch	RSPI0	RSPI command register 6	SPCMD6	16	16	2, 3 PCLKB	2 ICLK	
0008 839Eh	RSPI0	RSPI command register 7	SPCMD7	16	16	2, 3 PCLKB	2 ICLK	
0008 83A0h	RSPI1	RSPI control register	SPCR	8	8	2, 3 PCLKB	2 ICLK	
0008 83A1h	RSPI1	RSPI slave select polarity register	SSLP	8	8	2, 3 PCLKB	2 ICLK	
0008 83A2h	RSPI1	RSPI pin control register	SPPCR	8	8	2, 3 PCLKB	2 ICLK	
0008 83A3h	RSPI1	RSPI status register	SPSR	8	8	2, 3 PCLKB	2 ICLK	
0008 83A4h	RSPI1	RSPI data register	SPDR	32	16, 32	2, 3 PCLKB	2 ICLK	
0008 83A8h	RSPI1	RSPI sequence control register	SPSCR	8	8	2, 3 PCLKB	2 ICLK	
0008 83A9h	RSPI1	RSPI sequence status register	SPSSR	8	8	2, 3 PCLKB	2 ICLK	
0008 83AAh	RSPI1	RSPI bit rate register	SPBR	8	8	2, 3 PCLKB	2 ICLK	
0008 83ABh	RSPI1	RSPI data control register	SPDCR	8	8	2, 3 PCLKB	2 ICLK	
0008 83ACh	RSPI1	RSPI clock delay register	SPCKD	8	8	2, 3 PCLKB	2 ICLK	
0008 83ADh	RSPI1	RSPI slave select negation delay register	SSLND	8	8	2, 3 PCLKB	2 ICLK	
0008 83AEh	RSPI1	RSPI next-access delay register	SPND	8	8	2, 3 PCLKB	2 ICLK	
0008 83AFh	RSPI1	RSPI control register 2	SPCR2	8	8	2, 3 PCLKB	2 ICLK	
0008 83B0h	RSPI1	RSPI command register 0	SPCMD0	16	16	2, 3 PCLKB	2 ICLK	
0008 83B2h	RSPI1	RSPI command register 1	SPCMD1	16	16	2, 3 PCLKB	2 ICLK	
0008 83B4h	RSPI1	RSPI command register 2	SPCMD2	16	16	2, 3 PCLKB	2 ICLK	
0008 83B6h	RSPI1	RSPI command register 3	SPCMD3	16	16	2, 3 PCLKB	2 ICLK	
0008 83B8h	RSPI1	RSPI command register 4	SPCMD4	16	16	2, 3 PCLKB	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (26/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 A0A6h	SCI5	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK	SCIc, SCId
0008 A0A7h	SCI5	Serial extended mode register	SEMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0A8h	SCI5	Noise filter setting register	SNFR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0A9h	SCI5	I ² C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK	
0008 A0AAh	SCI5	I ² C mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK	
0008 A0ABh	SCI5	I ² C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK	
0008 A0ACh	SCI5	I ² C status register	SISR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0ADh	SCI5	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0C0h	SCI6	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0C1h	SCI6	Bit rate register	BRR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0C2h	SCI6	Serial control register	SCR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0C3h	SCI6	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0C4h	SCI6	Serial status register	SSR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0C5h	SCI6	Receive data register	RDR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0C6h	SCI6	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0C7h	SCI6	Serial extended mode register	SEMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0C8h	SCI6	Noise filter setting register	SNFR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0C9h	SCI6	I ² C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK	
0008 A0CAh	SCI6	I ² C mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK	
0008 A0CBh	SCI6	I ² C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK	
0008 A0CCh	SCI6	I ² C status register	SISR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0CDh	SCI6	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0E0h	SCI7	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0E1h	SCI7	Bit rate register	BRR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0E2h	SCI7	Serial control register	SCR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0E3h	SCI7	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0E4h	SCI7	Serial status register	SSR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0E5h	SCI7	Receive data register	RDR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0E6h	SCI7	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0E7h	SCI7	Serial extended mode register	SEMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0E8h	SCI7	Noise filter setting register	SNFR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0E9h	SCI7	I ² C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK	
0008 A0EAh	SCI7	I ² C mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK	
0008 A0EBh	SCI7	I ² C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK	
0008 A0ECh	SCI7	I ² C status register	SISR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0EDh	SCI7	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A100h	SCI8	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A101h	SCI8	Bit rate register	BRR	8	8	2, 3 PCLKB	2 ICLK	
0008 A102h	SCI8	Serial control register	SCR	8	8	2, 3 PCLKB	2 ICLK	
0008 A103h	SCI8	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK	
0008 A104h	SCI8	Serial status register	SSR	8	8	2, 3 PCLKB	2 ICLK	
0008 A105h	SCI8	Receive data register	RDR	8	8	2, 3 PCLKB	2 ICLK	
0008 A106h	SCI8	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A107h	SCI8	Serial extended mode register	SEMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A108h	SCI8	Noise filter setting register	SNFR	8	8	2, 3 PCLKB	2 ICLK	
0008 A109h	SCI8	I ² C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK	
0008 A10Ah	SCI8	I ² C mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK	
0008 A10Bh	SCI8	I ² C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK	
0008 A10Ch	SCI8	I ² C status register	SISR	8	8	2, 3 PCLKB	2 ICLK	
0008 A10Dh	SCI8	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A120h	SCI9	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK	

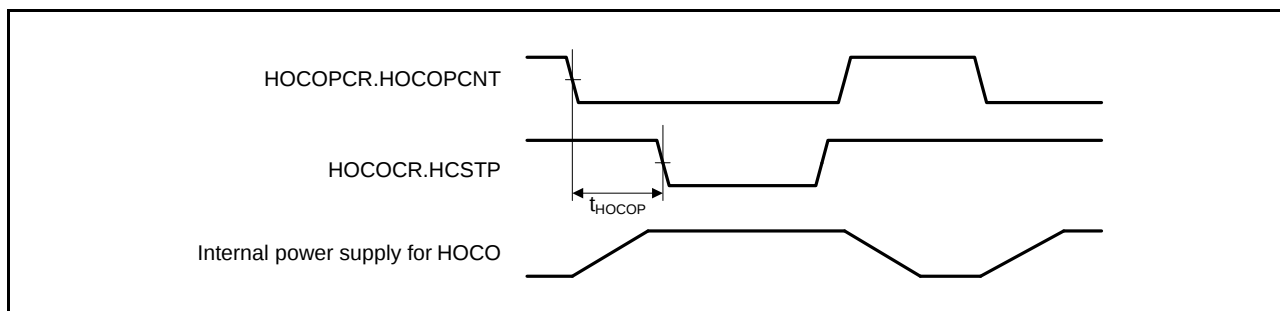


Figure 5.9 HOCO Power Supply Control Timing

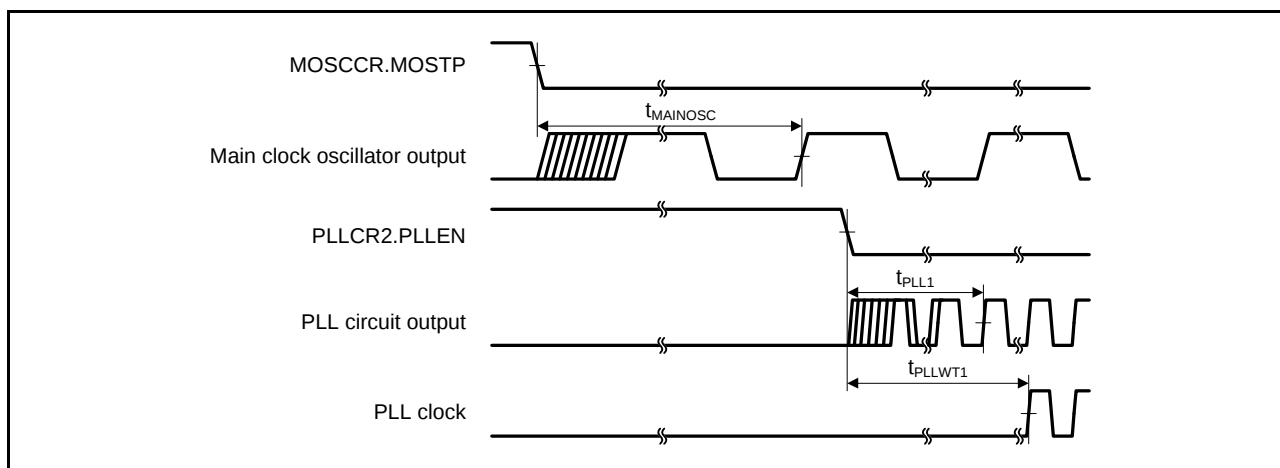


Figure 5.10 PLL Clock Oscillation Start Timing (PLL is Operated after Main Clock Oscillation Has Settled)

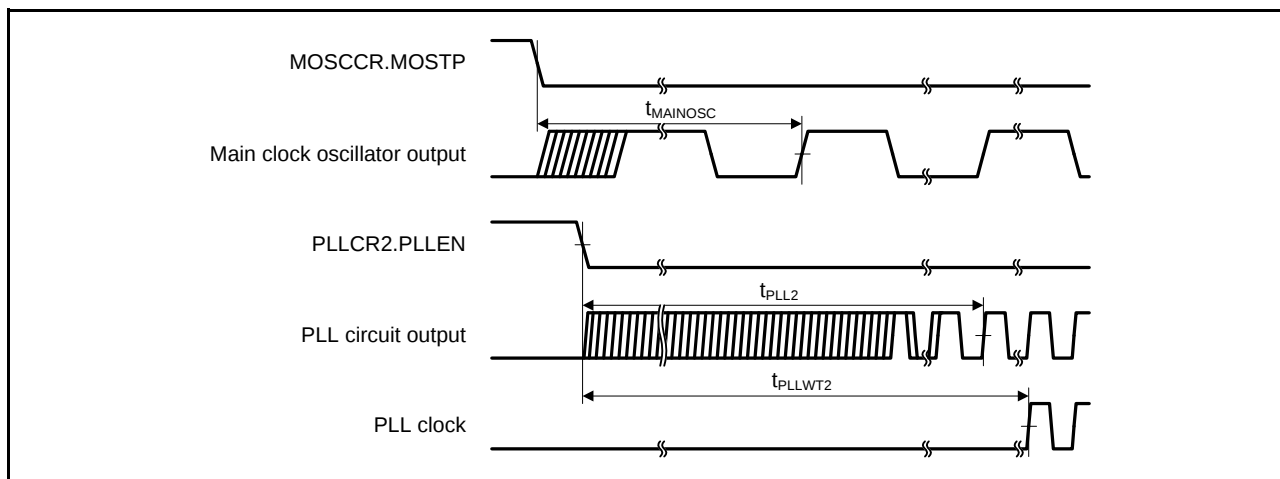


Figure 5.11 PLL Clock Oscillation Start Timing (PLL is Operated before Main Clock Oscillation Has Settled)

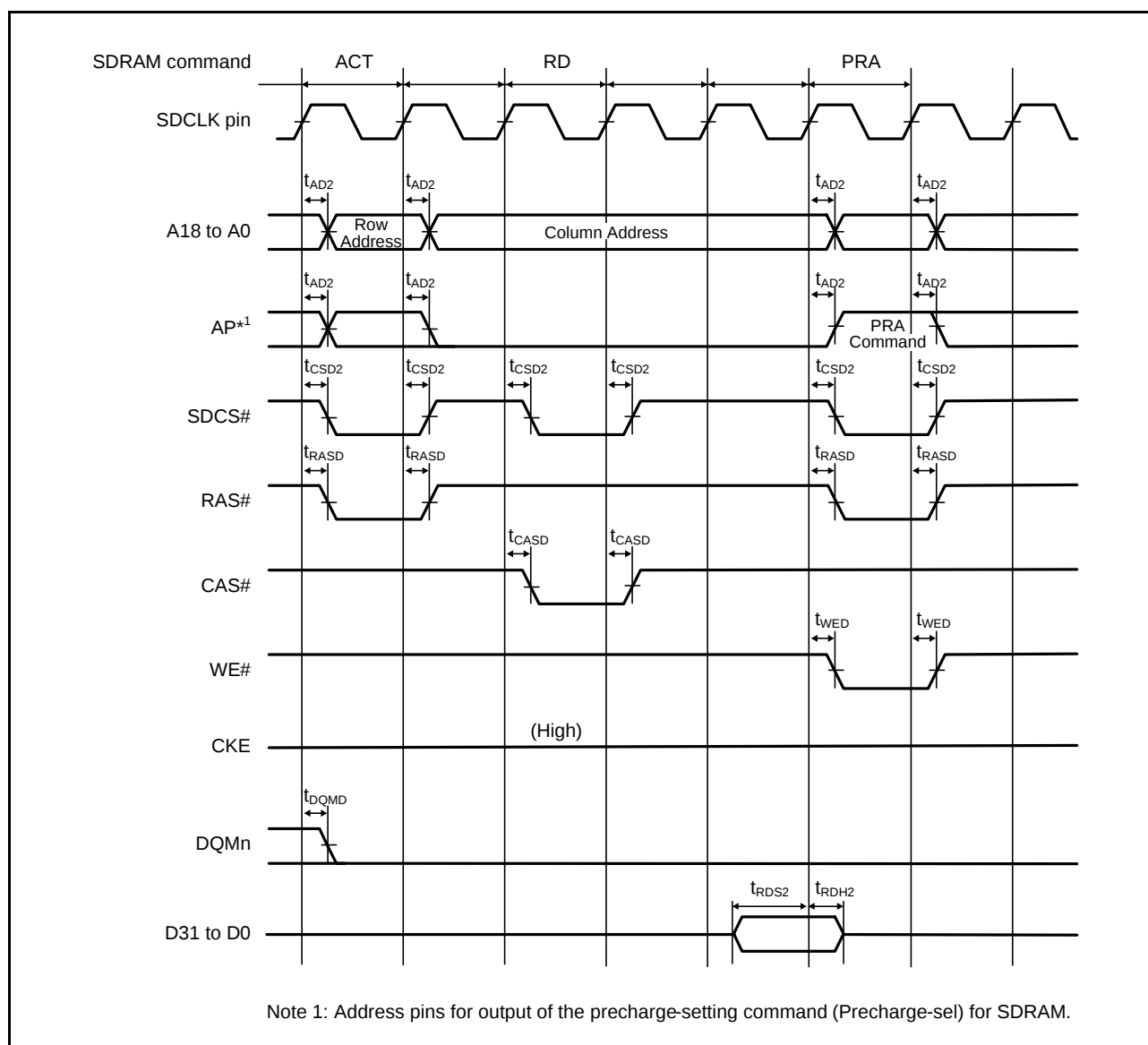


Figure 5.24 SDRAM Space Single Read Bus Timing

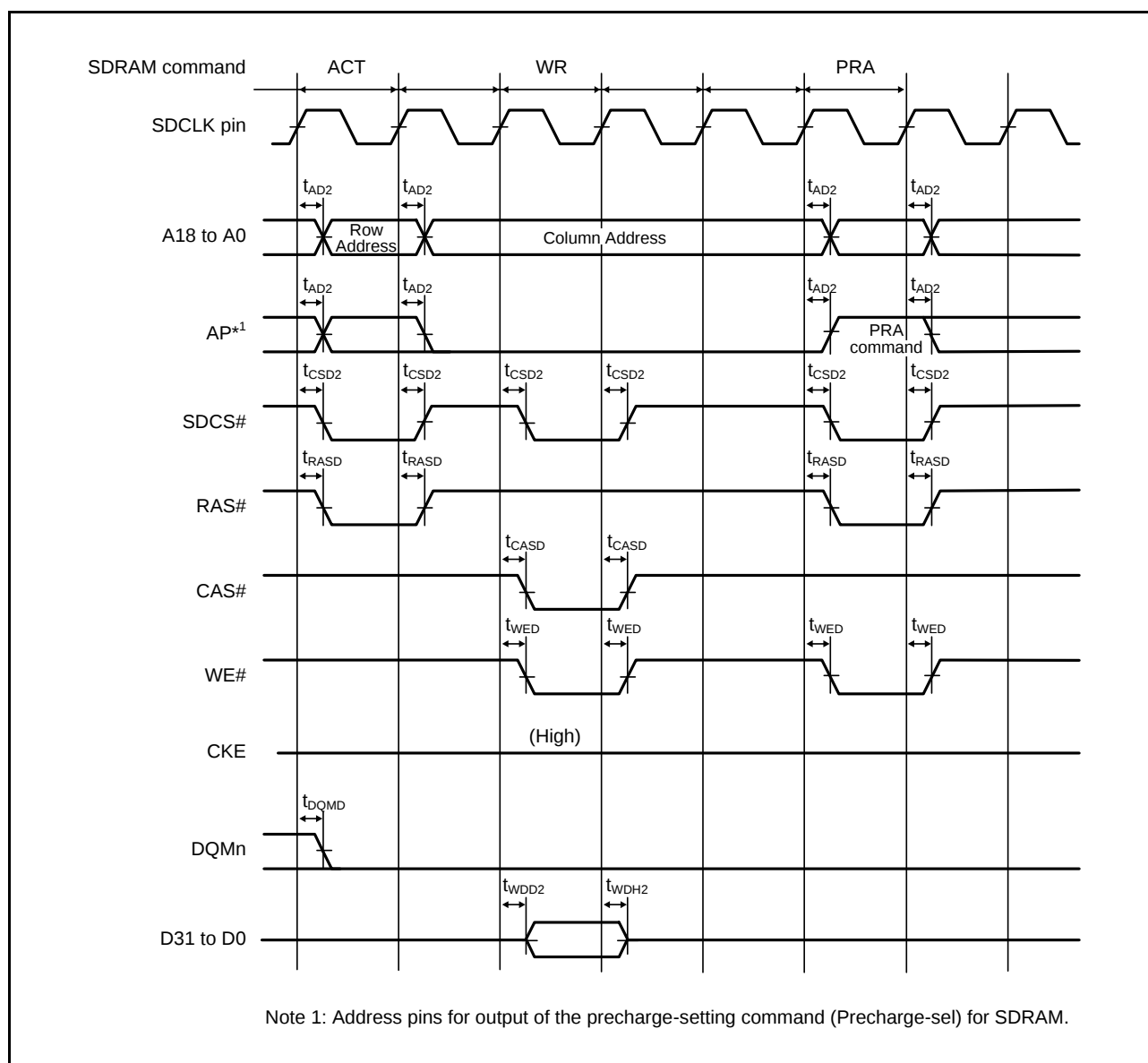


Figure 5.25 SDRAM Space Single Write Bus Timing

5.3.7 Timing of On-Chip Peripheral Modules

Table 5.19 Timing of On-Chip Peripheral Modules (1)

Conditions: VCC = AVCC0 = VREFH = VCC_USB = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0,
VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V
PCLK = 8 to 50 MHz
T_a = T_{opr}
High drive output is selected by the drive capacity control register.

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
I/O ports	Input data pulse width		t _{PRW}	1.5	—	t _{Pcyc}	Figure 5.34
MTU/TPU	Input capture input pulse width	Single-edge setting	t _{TICW}	1.5	—	t _{Pcyc}	Figure 5.35
		Both-edge setting		2.5	—		
	Timer clock pulse width	Single-edge setting	t _{TCKWH} , t _{TCKWL}	1.5	—	t _{Pcyc}	Figure 5.36
		Both-edge setting		2.5	—		
		Phase counting mode		2.5	—		
POE	POE# input pulse width		t _{POEW}	1.5	—	t _{Pcyc}	Figure 5.37
8-bit timer	Timer clock pulse width	Single-edge setting	t _{TMCWH} , t _{TMCWL}	1.5	—	t _{Pcyc}	Figure 5.38
		Both-edge setting		2.5	—		
SCI	Input clock cycle	Asynchronous	t _{Scyc}	4	—	t _{Pcyc}	Figure 5.39
		Clock synchronous		6	—		
	Input clock pulse width		t _{SCKW}	0.4	0.6	t _{Scyc}	Figure 5.40
	Input clock rise time		t _{SCKr}	—	20	ns	
	Input clock fall time		t _{SCKf}	—	20	ns	
	Output clock cycle	Asynchronous	t _{Scyc}	16	—	t _{Pcyc}	
		Clock synchronous		4	—		
	Output clock pulse width		t _{SCKW}	0.4	0.6	t _{Scyc}	
	Output clock rise time		t _{SCKr}	—	20	ns	
	Output clock fall time		t _{SCKf}	—	20	ns	
	Transmit data delay time	Clock synchronous	t _{TXD}	—	40	ns	
	Receive data setup time	Clock synchronous	t _{RXS}	40	—	ns	
	Receive data hold time	Clock synchronous	t _{RXH}	40	—	ns	
A/D converter	10-bit A/D converter trigger input pulse width		t _{TRGW}	1.5	—	t _{Pcyc}	Figure 5.41
	12-bit A/D converter trigger input pulse width			1.5	—		

Note 1. t_{Pcyc}: PCLK cycle

Table 5.24 Timing of On-Chip Peripheral Modules (6)

Conditions: VCC = AVCC0 = VREFH = VCC_USB = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0

VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V

PCLK = 8 to 50 MHz

 $T_a = T_{opr}$

High drive output is selected by the drive capacity control register.

Item		Symbol	Min.*1, *2	Max.*1	Unit	Test Conditions
RIIC (Fast-mode+) ICFER.FMPE = 1	SCL input cycle time	t_{SCL}	$6(12) \times t_{IICcyc} + 240$	—	ns	Figure 5.47
	SCL input high pulse width	t_{SCLH}	$3(6) \times t_{IICcyc} + 120$	—	ns	
	SCL input low pulse width	t_{SCLL}	$3(6) \times t_{IICcyc} + 120$	—	ns	
	SCL, SDA input rise time	t_{Sr}	—	120	ns	
	SCL, SDA input fall time	t_{Sf}	—	120	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	$1(4) \times t_{IICcyc}$	ns	
	SDA input bus free time	t_{BUF}	$3(6) \times t_{IICcyc} + 120$	—	ns	
	Start condition input hold time	t_{STAH}	$t_{IICcyc} + 120$	—	ns	
	Restart condition input setup time	t_{STAS}	120	—	ns	
	Stop condition input setup time	t_{STOS}	120	—	ns	
	Data input setup time	t_{SDAS}	$t_{IICcyc} + 120$	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	550	pF	
Simple IIC (Standard-mode)	SDA input rise time	t_{Sr}	—	1000	ns	
	SDA input fall time	t_{Sf}	—	300	ns	
	SDA input spike pulse removal time	t_{SP}	0	$4 \times t_{IICcyc}$	ns	
	Data input setup time	t_{SDAS}	250	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
Simple IIC (Fast-mode)	SCL, SDA input rise time	t_{Sr}	$20 + 0.1C_b$	300	ns	
	SCL, SDA input fall time	t_{Sf}	$20 + 0.1C_b$	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	$4 \times t_{IICcyc}$	ns	
	Data input setup time	t_{SDAS}	100	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

Note: t_{IICcyc} : RIIC internal reference clock (IIC ϕ) Cycle, t_{Pcyc} : PCLK cycle

Note 1. The value in parentheses is used when ICMR3.NF[1:0] are set to 11b while a digital filter is enabled with ICFER.NFE = 1.

Note 2. C_b indicates the total capacity of the bus line.

5.4 USB Characteristics

Table 5.27 On-Chip USB Full-Speed Characteristics (DP and DM Pin Characteristics)

Conditions: $V_{CC} = AV_{CC0} = V_{REFH} = V_{CC_USB} = 3.0$ to 3.6 V, $V_{REFH0} = 3.0$ V to AV_{CC0}

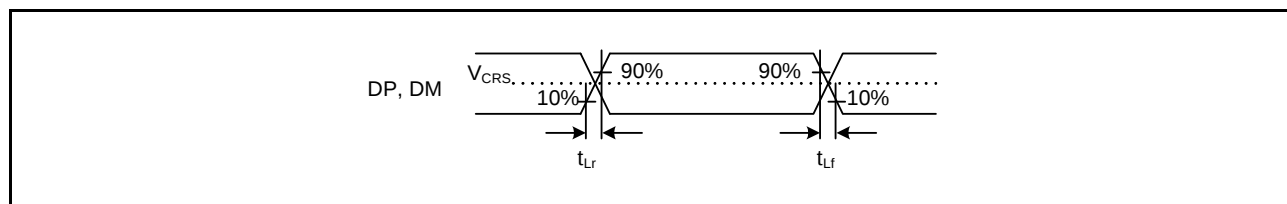
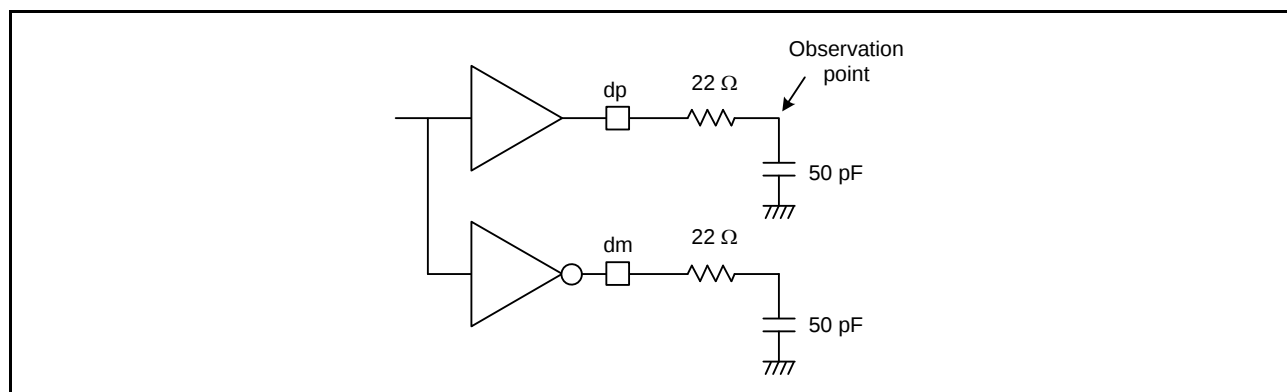
$V_{SS} = AV_{SS0} = V_{REFL}/V_{REFL0} = V_{SS_USB} = 0$ V

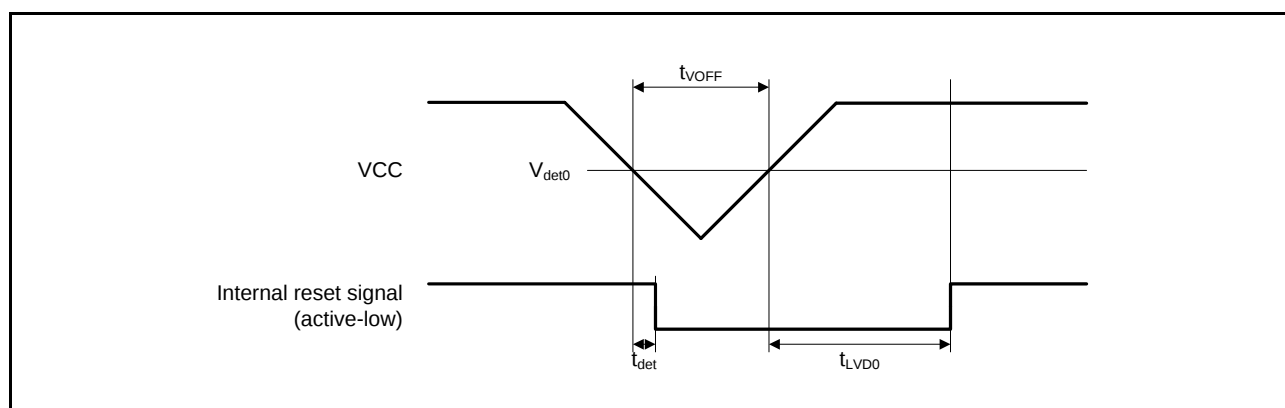
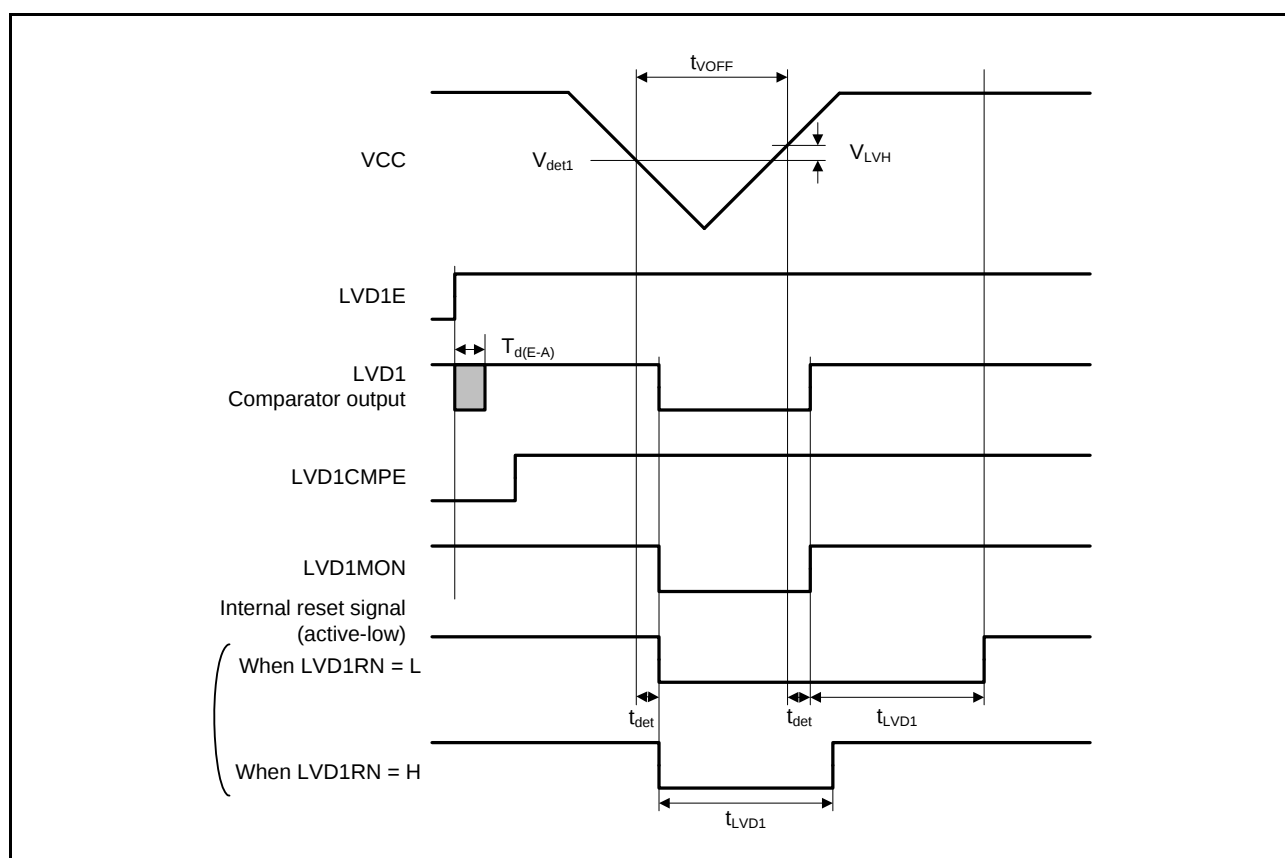
$PCLK = 24$ to 50 MHz

$T_a = T_{opr}$

High drive output is selected by the drive capacity control register.

	Item	Symbol	Min.	Max.	Unit	Test Conditions
Input characteristics	Input high level voltage	V_{IH}	2.0	—	V	
	Input low level voltage	V_{IL}	—	0.8	V	
	Differential input sensitivity	V_{DI}	0.2	—	V	DP – DM
	Differential common mode range	V_{CM}	0.8	2.5	V	
Output characteristics	Output high level voltage	V_{OH}	2.8	3.6	V	$I_{OH} = -200 \mu A$
	Output low level voltage	V_{OL}	0.0	0.3	V	$I_{OL} = 2$ mA
	Cross-over voltage	V_{CRS}	1.3	2.0	V	
	Rise time	t_{Lr}	4	20	ns	
	Fall time	t_{Lf}	4	20	ns	
	Rise/fall time ratio	t_{Lr} / t_{Lf}	90	111.11	%	t_{Lr} / t_{Lf}
	Output resistance	Z_{DRV}	28	44	Ω	$R_s = 22 \Omega$ included


Figure 5.61 DP and DM Output Timing (Full-Speed)

Figure 5.62 Test Circuit (Full-Speed)

Figure 5.64 Voltage Detection Circuit Timing (V_{det0})Figure 5.65 Voltage Detection Circuit Timing (V_{det1})

Appendix 1. Package Dimensions

Information on the latest version of the package dimensions or mountings has been displayed in “Packages” on Renesas Electronics Corporation website.

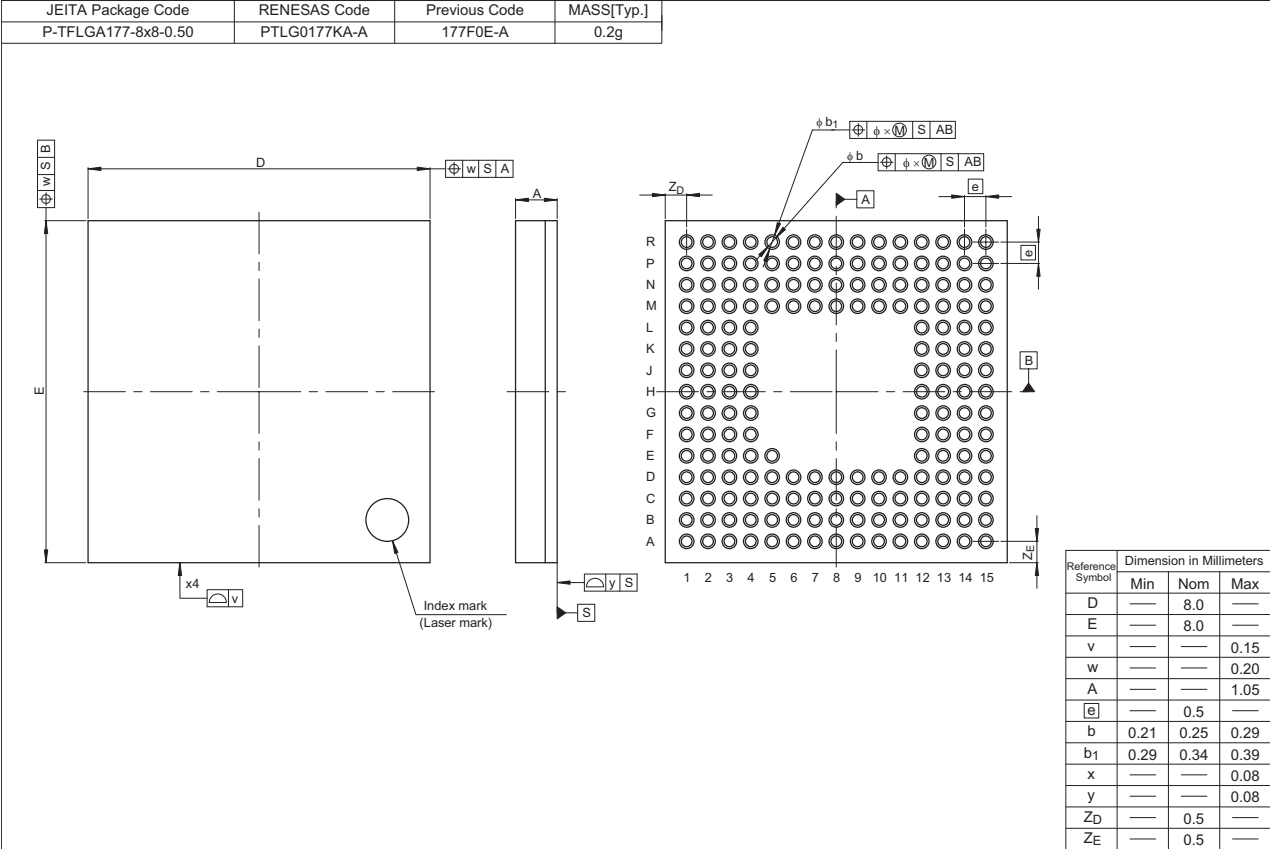


Figure A 177-pin TFLGA (PTLG0177KA-A)

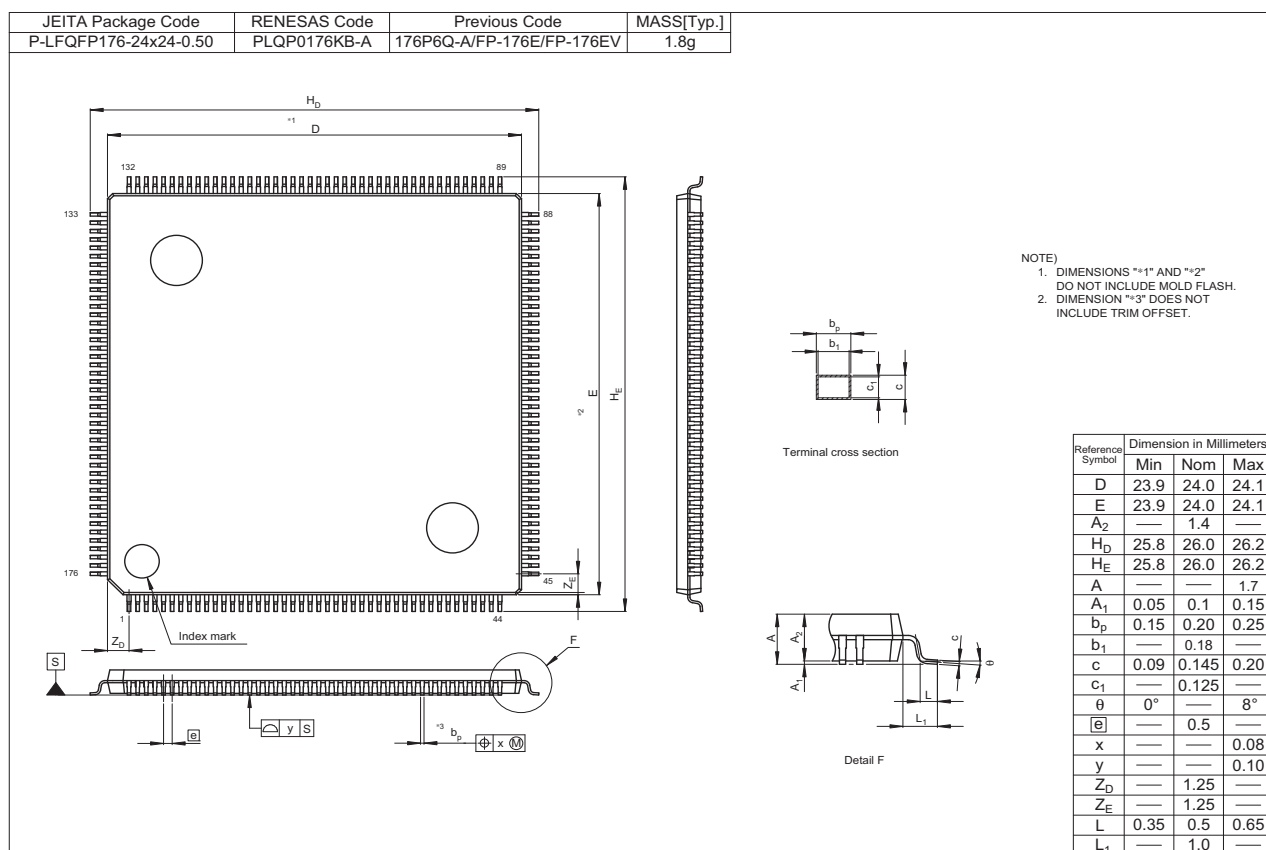


Figure C 176-pin LQFP (PLQP0176KB-A)

Rev.	Date	Description	
		Page	Summary
1.70	Oct 08. 2013	80 to 127	Table 4.1 List of I/O Registers (Address Order), changed
		5. Electrical Characteristics	
		131, 132	Table 5.4 DC Characteristics (3), changed, Note. 9, Note. 10, added
		133	Table 5.6 Permissible Output Currents, changed
		139	Table 5.12 Clock Timing (Sub-Clock Related), Note 3, added
		167	Table 5.25 Timing of On-Chip Peripheral Modules (8), added
		175	Figure 5.58 PDC Timing, added
		175	Figure 5.59 PDC Input Clock Characteristic, added
		176	Figure 5.60 PDC Output Clock Characteristic, added
		178	Table 5.27 10-Bit A/D Conversion Characteristics, changed
		179	Table 5.28 12-Bit A/D Conversion Characteristics, changed
		185	Table 5.35 ROM (Flash Memory for Code Storage) Characteristics (1), added
		185	Table 5.36 ROM (Flash Memory for Code Storage) Characteristics (2), changed
		186	Table 5.37 E2 Flash Characteristics (1), added
		186	Table 5.38 E2 Flash Characteristics (2), changed
		Appendix 1. Package Dimensions	
		197	Figure H 64-pin TFLGA (PTLG0064JA-A), added