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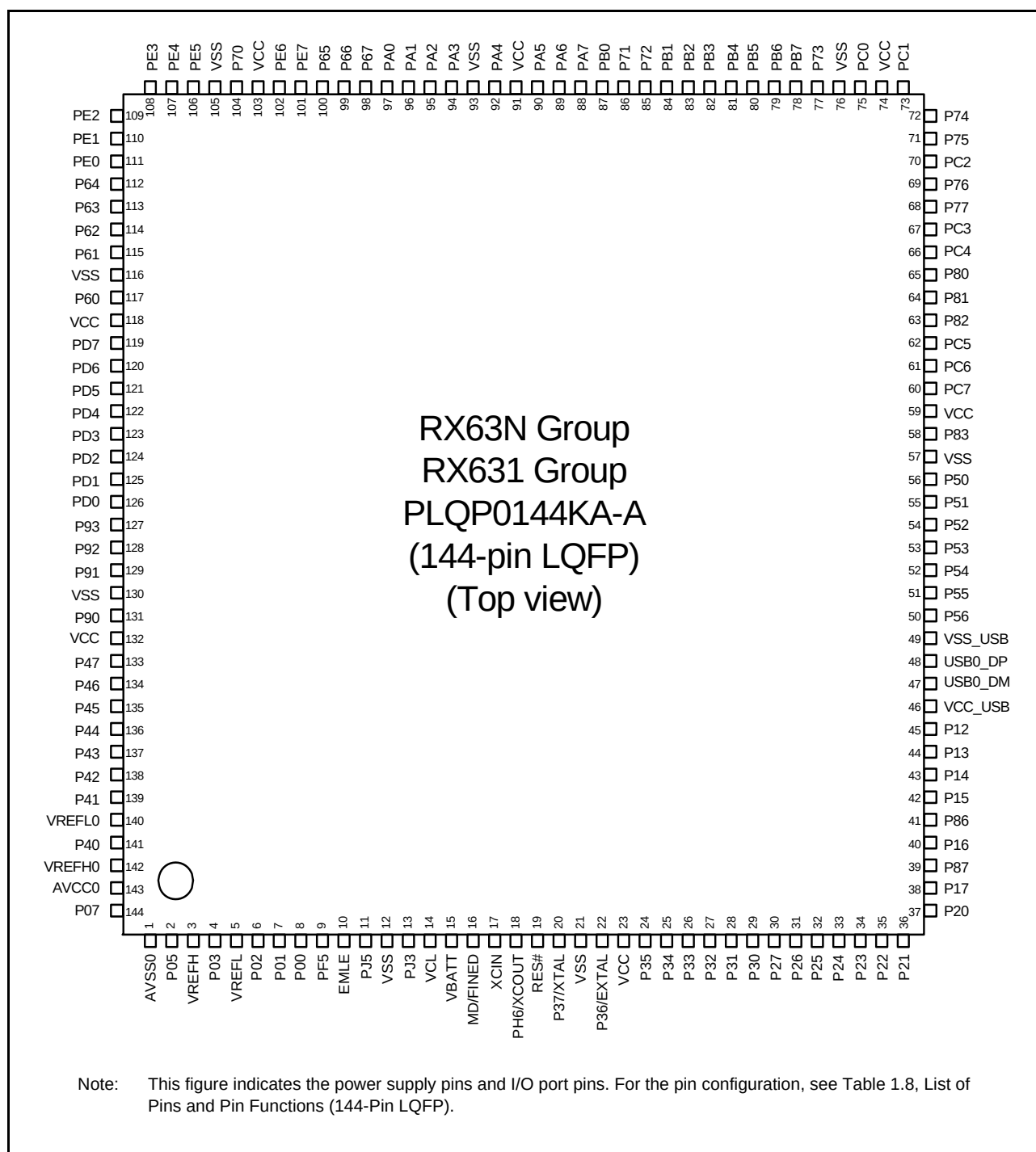
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Details

Product Status	Obsolete
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, I ² C, LINbus, SCI, SPI, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	30
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f5631nddfl-v0

**Figure 1.7 Pin Assignment (144-Pin LQFP)**

RX63N Group, RX631 Group
PTLG0100JA-A (100-pin TFLGA)
(Top view)

	A	B	C	D	E	F	G	H	J	K	
10	PE2	PE3	PE4	PA0	PA3	VSS	VCC	PB7	PC1	PC2	10
9	PE1	PD7	PE5	PA1	PA5	PA7	PB1	PB6	PC0	PC3	9
8	PE0	PD6	PD5	PE7	PA4	PB0	PB4	PC6	PC4	PC5	8
7	PD4	PD3	PD2	PE6	PA6	PB2	PB5	PC7	P50	P51	7
6	PD0	PD1	P47	P46	PA2	PB3	P52	P54	VCC_ USB	USB0_ DP	6
5	P43	P44	P42	P45	P41	P12	P53	P55	VSS_ USB	USB0_ DM	5
4	VREFL0	P40	VREFH0	VBATT	P34	P32	P27	P15	P13	P14	4
3	P07	AVCC0	PJ3	MD/ FINED	RES#	P35	P30	P16	P17	P20	3
2	VREFH	AVSS0	VREFL	XCOUT	VSS	VCC	P31	P25	P21	P22	2
1	P05	EMLE	VCL	XCIN	XTAL	EXTAL	P33	P26	P24	P23	1
	A	B	C	D	E	F	G	H	J	K	

Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.10, List of Pins and Pin Functions (100-Pin LQFP).

Figure 1.8 Pin Assignment (100-Pin TFLGA)

Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (3/5)

Pin Number 177-Pin TFLGA 176-Pin LFBGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SC1c, SC1d, RSPI, RIIC, CAN, IEB, USB, and PDC)	Interrupt	S12AD, AD, DA
H3	RES#						
H4		P35				NMI	
H12		PA4	A4	MTIC5U/MTCLKA/ TIOCA1/TMRI0/PO20	ET_MDC/TXD5/SMOSI5/ SSDA5/SSLA0	IRQ5-DS	
H13		PA3	A3	MTIOC0D/MTCLKD/ TIOC0D/TCLKB/PO19	ET_MDIO/RXD5/SMISO5/ SSCL5	IRQ6-DS	
H14		PA2	A2	PO18	RXD5/SMISO5/SSCL5/ SSLA3		
H15	TRDATA3	PG7	D31				
J1	EXTAL	P36					
J2	VCC						
J3		P34		MTIOC0A/TMCI3/PO12/ POE2#	SCK6/SCK0/ USB_DPRPD	IRQ4	
J4	TMS	PF3					
J12		PA5	A5	TIOC0B1/PO21	ET_LINKSTA/RSPCKA		
J13	VSS						
J14		PA7	A7	TIOC0B2/PO23	ET_WOL/MISOA		
J15		PA6	A6	MTIC5V/MTCLKB/ TIOCA2/TMCI3/PO22/ POE2#	ET_EXOUT/CTS5#/ RTS5#/#SS5#/#MOSIA		
K1		P33		MTIOC0D/TIOC0D/ TMRI3/PO11/POE3#	RXD6/RXD0/SMISO6/ SMISO0/SSCL6/SSCL0/ CRX0/PCKO	IRQ3-DS	
K2		P32		MTIOC0C/TIOC0C/TMO3/ PO10/RTCOU/RTIC2	TXD6/TXD0/SMOSI6/ SMOSI0/SSDA6/SSDA0/ CTX0/USB0_VBUSEN/ VSYNC	IRQ2-DS	
K3	TDI	PF2			RXD1/SMISO1/SSCL1		
K4	TCK/FINEC	PF1			SCK1		
K12		PB2	A10	TIOC0C3/TCLKC/PO26	ET_RX_CLK/REF50CK/ CTS4#/#RTS4#/#CTS6#/ RTS6#/#SS4#/#SS6#		
K13		P71	CS1#		ET_MDIO		
K14	VCC						
K15		PB0	A8	MTIC5W/TIOCA3/PO24	ET_ERXD1/RMII_RXD1/ RXD4/RXD6/SMISO4/ SMISO6/SSCL4/SSCL6/ RSPCKA	IRQ12	
L1		P31		MTIOC4D/TMCI2/PO9/ RTIC1	CTS1#/#RTS1#/#SS1#/ SSLB0/USB0_DPUPE	IRQ1-DS	
L2		P30		MTIOC4B/TMRI3/PO8/ RTIC0/POE8#	RXD1/SMISO1/SSCL1/ MISOB/USB0_DRPD	IRQ0-DS	
L3	TDO	PF0			TXD1/SMOSI1/SSDA1		
L4		P25	CS5#/#EDACK1	MTIOC4C/MTCLKB/ TIOCA4/PO5	RXD3/SMISO3/SSCL3/ USB_DPRPD/HSYNC		ADTRG0#
L12		PB6	A14	MTIOC3D/TIOCA5/PO30	ET_ETXD1/RMII_TXD1/ RXD9/SMISO9/SSCL9		
L13		PB3	A11	MTIOC0A/MTIOC4A/ TIOC0D/TCLKD/TMO0/ PO27/POE3#	ET_RX_ER/RMII_RX_ER/ SCK4/SCK6		
L14		PB1	A9	MTIOC0C/MTIOC4C/ TIOC0B3/TMCI0/PO25	ET_ERXD0/RMII_RXD0/ TXD4/TXD6/SMOSI4/ SMOSI6/SSDA4/SSDA6	IRQ4-DS	
L15		P72	CS2#		ET_MDC		
M1		P27	CS7#	MTIOC2B/TMCI3/PO7	SCK1/RSPCKB		

Table 1.8 List of Pins and Pin Functions (144-Pin LQFP) (3/5)

Pin No. 144-pin LQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timers (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SC1c, SC1d, RSPI, RIIC, CAN, IEB, USB, and PDC)	Interrupt	S12AD AD DA
64	TRDATA1	P81	EDACK0	MTIOC3D/PO27	RXD10/SMISO10/ SSCL10/ET_ETXD0/ RMII_TXD0		
65	TRDATA0	P80	EDREQ0	MTIOC3B/PO26	SCK10/ET_TX_EN/ RMII_TXD_EN		
66		PC4	A20/CS3#	MTIOC3D/MTCLKC/ TIOCC6/TCLKE/ TMC11/PO25/POE0#	SCK5/CTS8#/RTS8#/ SS8#/SSLA0/ ET_TX_CLK		
67		PC3	A19	MTIOC4D/TCLKB/ PO24	TXD5/SMOSI5/SSDA5/ IETXD/ET_TX_ER		
68		P77	CS7#	PO23	TXD11/SMOSI11/ SSDA11/ET_RX_ER/ RMII_RX_ER		
69		P76	CS6#	PO22	RXD11/SMISO11/ SSCL11/ET_RX_CLK/ REF50CK		
70		PC2	A18	MTIOC4B/TCLKA/ PO21	RXD5/SMISO5/SSCL5/ SSLA3/IERXD/ ET_RX_DV		
71		P75	CS5#	PO20	SCK11/ET_ERXD0/ RMII_RXD0		
72		P74	CS4#	PO19	CTS11#/RTS11#/ SS11#/ET_ERXD1/ RMII_RXD1		
73		PC1	A17	MTIOC3A/TCLKD/ PO18	SCK5/SSLA2/SDA3/ ET_ERXD2	IRQ12	
74	VCC						
75		PC0	A16	MTIOC3C/TCLKC/ PO17	CTS5#/RTS5#/SS5#/ SSLA1/SCL3/ ET_ERXD3	IRQ14	
76	VSS						
77		P73	CS3#	PO16	ET_WOL		
78		PB7	A15	MTIOC3B/TIOCB5/ PO31	TXD9/SMOSI9/SSDA9/ ET_CRS/ RMII_CRS_DV		
79		PB6	A14	MTIOC3D/TIOCA5/ PO30	RXD9/SMISO9/SSCL9/ ET_ETXD1/RMII_TXD1		
80		PB5	A13	MTIOC2A/MTIOC1B/ TIOCB4/TMRI1/PO29/ POE1#	SCK9/ET_ETXD0/ RMII_TXD0		
81		PB4	A12	TIOCA4/PO28	CTS9#/RTS9#/SS9#/ ET_TX_EN/ RMII_TXD_EN		
82		PB3	A11	MTIOC0A/MTIOC4A/ TIOCD3/TCLKD/TMO0/ PO27/POE3#	SCK4/SCK6/ ET_RX_ER/ RMII_RX_ER		
83		PB2	A10	TIOCC3/TCLKC/PO26	CTS4#/RTS4#/CTS6#/ RTS6#/SS4#/SS6#/ ET_RX_CLK/REF50CK		
84		PB1	A9	MTIOC0C/MTIOC4C/ TIOCB3/TMC10/PO25	TXD4/TXD6/SMOSI4/ SMOSI6/SSDA4/ SSDA6/ET_ERXD0/ RMII_RXD0	IRQ4-DS	
85		P72	CS2#		ET_MDC		
86		P71	CS1#		ET_MDIO		
87		PB0	A8	MTIC5W/TIOCA3/ PO24	RXD4/RXD6/SMISO4/ SMISO6/SSCL4/ SSCL6/RSPCKA/ T_ERXD1/RMII_RXD1	IRQ12	
88		PA7	A7	TIOCB2/PO23	MISOA/ET_WOL		

Table 1.10 List of Pins and Pin Functions (100-Pin LQFP) (4/4)

Pin No. 100-pin LQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC	Timers (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SC1c, SC1d, RSPI, RIIC, CAN, IEB, USB)	Interrupt	S12AD AD DA
94	VREFL0						
95		P40				IRQ8-DS	AN000
96	VREFH0						
97	AVCC0						
98		P07				IRQ15	ADTRG0#
99	AVSS0						
100		P05				IRQ13	DA1

Note 1. Enabled only for the ROM capacity of 768 Kbytes or more

Note 2. The BCLK function is multiplexed with the I/O port function for pin P53, so the port function is not available if the external bus is enabled.

Table 1.13 List of Pins and Pin Functions (48-Pin LQFP) (1/2)

Pin Number 48-Pin LQFP	Power Supply Clock System Control	I/O Port	Timer (MTU2a, TPUa, TMR, PPG, POE2a)	Communications (SC1c, SC1d, RSPI, RIIC, CAN, IEB, USB)	Interrupt	S12ADa, DAa
1	VCL					
2	MD/FINED					
3	RES#					
4	XTAL	P37				
5	VSS					
6	EXTAL	P36				
7	VCC					
8		P35			NMI	
9		P31	MTIOC4D/TMC12/PO9	CTS1#/RTS1#/SS1#/ SSLB0/USB0_DPUPE	IRQ1-DS	
10		P30	MTIOC4B/TMR13/PO8/ POE8#	RXD1/SMISO1/SSCL1/ MISOB/USB0_DRPD	IRQ0-DS	
11	FINEC	P27	MTIOC2B/TMC13/PO7	SCK1/RSPCKB		
12		P26	MTIOC2A/TMO1/PO6	TXD1/SMOSI1/SSDA1/ MOSIB/USB0_VBUSEN		
13		P17	MTIOC3A/MTIOC3B/ TIOCB0/TCLKD/TMO1/ PO15/POE8#	SCK1/MISOA/SDA2-DS/ IETXD	IRQ7	
14		P16	MTIOC3C/MTIOC3D/ TIOCB1/TCLKC/TMO2/ PO14	TXD1/SMOSI1/SSDA1/ MOSIA/SCL2-DS/IERXD/ USB0_VBUS/ USB0_VBUSEN/ USB0_OVRCURB	IRQ6	ADTRG0#
15		P15	MTIOC0B/MTCLKB/ TIOCB2/TCLKB/TMC12/ PO13	RXD1/SMISO1/SSCL1/ CRX1-DS	IRQ5	
16		P14	MTIOC3A/MTCLKA/ TIOCB5/TCLKA/TMR12/ PO15	CTS1#/RTS1#/SS1#/ CTX1/USB0_DPUPE/ USB0_OVRCURA	IRQ4	
17	VCC_USB					
18				USB0_DM		
19				USB0_DP		
20	VSS_USB					
21		PC7	MTIOC3A/MTCLKB/ TMO2 /PO31	TXD8/SMOSI8/SSDA8/ MISOA	IRQ14	
22		PC6	MTIOC3C/MTCLKA/ TMC12/PO30	RXD8/SMISO8/SSCL8/ MOSIA/USB0_EXICEN	IRQ13	
23		PC5	MTIOC3B/MTCLKD/ TMR12/PO29	SCK8/RSPCKA/USB0_ID		
24		PC4	MTIOC3D/MTCLKC/ TMC11/PO25/POE0#	SCK5/CTS8#/RTS8#/SS8#/ /SSLA0/ USB0_DPRPD		
25		PB5/ PC3	MTIOC2A/MTIOC1B/ TIOCB4/TMR11/PO29/ POE1#			
26		PB3/ PC2	MTIOC0A/MTIOC4A/ TIOC3D/TCLKD/TMO0/ PO27/POE3#	SCK6		
27		PB1/ PC1	MTIOC0C/MTIOC4C/ TIOCB3/TMC10/PO25	TXD6/SMOSI6/SSDA6	IRQ4-DS	
28	VCC					

2.3 Register Associated with DSP Instructions

(1) Accumulator (ACC)

The accumulator (ACC) is a 64-bit register used for DSP instructions. The accumulator is also used for the multiply and multiply-and-accumulate instructions; EMUL, EMULU, FMUL, MUL, and RMPA, in which case the prior value in the accumulator is modified by execution of the instruction.

Use the MVTACHI and MVTACLO instructions for writing to the accumulator. The MVTACHI and MVTACLO instructions write data to the higher-order 32 bits (bits 63 to 32) and the lower-order 32 bits (bits 31 to 0), respectively. Use the MVFACHI and MVFACMI instructions for reading data from the accumulator. The MVFACHI and MVFACMI instructions read data from the higher-order 32 bits (bits 63 to 32) and the middle 32 bits (bits 47 to 16), respectively.

Table 4.1 List of I/O Registers (Address Order) (7/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 7096h	ICU	Interrupt request register 150	IR150	8	8	2	ICLK	ICUb
0008 7097h	ICU	Interrupt request register 151	IR151	8	8	2	ICLK	
0008 7098h	ICU	Interrupt request register 152	IR152	8	8	2	ICLK	
0008 7099h	ICU	Interrupt request register 153	IR153	8	8	2	ICLK	
0008 709Ah	ICU	Interrupt request register 154	IR154	8	8	2	ICLK	
0008 709Bh	ICU	Interrupt request register 155	IR155	8	8	2	ICLK	
0008 709Ch	ICU	Interrupt request register 156	IR156	8	8	2	ICLK	
0008 709Dh	ICU	Interrupt request register 157	IR157	8	8	2	ICLK	
0008 709Eh	ICU	Interrupt request register 158	IR158	8	8	2	ICLK	
0008 709Fh	ICU	Interrupt request register 159	IR159	8	8	2	ICLK	
0008 70A0h	ICU	Interrupt request register 160	IR160	8	8	2	ICLK	
0008 70A1h	ICU	Interrupt request register 161	IR161	8	8	2	ICLK	
0008 70A2h	ICU	Interrupt request register 162	IR162	8	8	2	ICLK	
0008 70A3h	ICU	Interrupt request register 163	IR163	8	8	2	ICLK	
0008 70A4h	ICU	Interrupt request register 164	IR164	8	8	2	ICLK	
0008 70A5h	ICU	Interrupt request register 165	IR165	8	8	2	ICLK	
0008 70A6h	ICU	Interrupt request register 166	IR166	8	8	2	ICLK	
0008 70A7h	ICU	Interrupt request register 167	IR167	8	8	2	ICLK	
0008 70AAh	ICU	Interrupt request register 170	IR170	8	8	2	ICLK	
0008 70ABh	ICU	Interrupt request register 171	IR171	8	8	2	ICLK	
0008 70ACh	ICU	Interrupt request register 172	IR172	8	8	2	ICLK	
0008 70ADh	ICU	Interrupt request register 173	IR173	8	8	2	ICLK	
0008 70AEh	ICU	Interrupt request register 174	IR174	8	8	2	ICLK	
0008 70AFh	ICU	Interrupt request register 175	IR175	8	8	2	ICLK	
0008 70B0h	ICU	Interrupt request register 176	IR176	8	8	2	ICLK	
0008 70B1h	ICU	Interrupt request register 177	IR177	8	8	2	ICLK	
0008 70B2h	ICU	Interrupt request register 178	IR178	8	8	2	ICLK	
0008 70B3h	ICU	Interrupt request register 179	IR179	8	8	2	ICLK	
0008 70B4h	ICU	Interrupt request register 180	IR180	8	8	2	ICLK	
0008 70B5h	ICU	Interrupt request register 181	IR181	8	8	2	ICLK	
0008 70B6h	ICU	Interrupt request register 182	IR182	8	8	2	ICLK	
0008 70B7h	ICU	Interrupt request register 183	IR183	8	8	2	ICLK	
0008 70B8h	ICU	Interrupt request register 184	IR184	8	8	2	ICLK	
0008 70B9h	ICU	Interrupt request register 185	IR185	8	8	2	ICLK	
0008 70BAh	ICU	Interrupt request register 186	IR186	8	8	2	ICLK	
0008 70BBh	ICU	Interrupt request register 187	IR187	8	8	2	ICLK	
0008 70BCh	ICU	Interrupt request register 188	IR188	8	8	2	ICLK	
0008 70BDh	ICU	Interrupt request register 189	IR189	8	8	2	ICLK	
0008 70BEh	ICU	Interrupt request register 190	IR190	8	8	2	ICLK	
0008 70BFh	ICU	Interrupt request register 191	IR191	8	8	2	ICLK	
0008 70C0h	ICU	Interrupt request register 192	IR192	8	8	2	ICLK	
0008 70C1h	ICU	Interrupt request register 193	IR193	8	8	2	ICLK	
0008 70C2h	ICU	Interrupt request register 194	IR194	8	8	2	ICLK	
0008 70C3h	ICU	Interrupt request register 195	IR195	8	8	2	ICLK	
0008 70C4h	ICU	Interrupt request register 196	IR196	8	8	2	ICLK	
0008 70C5h	ICU	Interrupt request register 197	IR197	8	8	2	ICLK	
0008 70C6h	ICU	Interrupt request register 198	IR198	8	8	2	ICLK	
0008 70C7h	ICU	Interrupt request register 199	IR199	8	8	2	ICLK	
0008 70C8h	ICU	Interrupt request register 200	IR200	8	8	2	ICLK	
0008 70C9h	ICU	Interrupt request register 201	IR201	8	8	2	ICLK	
0008 70CAh	ICU	Interrupt request register 202	IR202	8	8	2	ICLK	

Table 4.1 List of I/O Registers (Address Order) (14/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 7400h	ICU	DMAC activation request select register 0	DMRSR0	8	8	2 ICLK		ICUb
0008 7404h	ICU	DMAC activation request select register 1	DMRSR1	8	8	2 ICLK		
0008 7408h	ICU	DMAC activation request select register 2	DMRSR2	8	8	2 ICLK		
0008 740Ch	ICU	DMAC activation request select register 3	DMRSR3	8	8	2 ICLK		
0008 7500h	ICU	IRQ control register 0	IRQCR0	8	8	2 ICLK		
0008 7501h	ICU	IRQ control register 1	IRQCR1	8	8	2 ICLK		
0008 7502h	ICU	IRQ control register 2	IRQCR2	8	8	2 ICLK		
0008 7503h	ICU	IRQ control register 3	IRQCR3	8	8	2 ICLK		
0008 7504h	ICU	IRQ control register 4	IRQCR4	8	8	2 ICLK		
0008 7505h	ICU	IRQ control register 5	IRQCR5	8	8	2 ICLK		
0008 7506h	ICU	IRQ control register 6	IRQCR6	8	8	2 ICLK		
0008 7507h	ICU	IRQ control register 7	IRQCR7	8	8	2 ICLK		
0008 7508h	ICU	IRQ control register 8	IRQCR8	8	8	2 ICLK		
0008 7509h	ICU	IRQ control register 9	IRQCR9	8	8	2 ICLK		
0008 750Ah	ICU	IRQ control register 10	IRQCR10	8	8	2 ICLK		
0008 750Bh	ICU	IRQ control register 11	IRQCR11	8	8	2 ICLK		
0008 750Ch	ICU	IRQ control register 12	IRQCR12	8	8	2 ICLK		
0008 750Dh	ICU	IRQ control register 13	IRQCR13	8	8	2 ICLK		
0008 750Eh	ICU	IRQ control register 14	IRQCR14	8	8	2 ICLK		
0008 750Fh	ICU	IRQ control register 15	IRQCR15	8	8	2 ICLK		
0008 7510h	ICU	IRQ pin digital filter enable register 0	IRQFLTE0	8	8	2 ICLK		
0008 7511h	ICU	IRQ pin digital filter enable register 1	IRQFLTE1	8	8	2 ICLK		
0008 7514h	ICU	IRQ pin digital filter setting register 0	IRQFLTC0	16	16	2 ICLK		
0008 7516h	ICU	IRQ pin digital filter setting register 1	IRQFLTC1	16	16	2 ICLK		
0008 7580h	ICU	Non-maskable interrupt status register	NMISR	8	8	2 ICLK		
0008 7581h	ICU	Non-maskable interrupt enable register	NMIER	8	8	2 ICLK		
0008 7582h	ICU	Non-maskable interrupt status clear register	NMICLR	8	8	2 ICLK		
0008 7583h	ICU	NMI pin interrupt control register	NMICR	8	8	2 ICLK		
0008 7590h	ICU	NMI pin digital filter enable register	NMIFLTE	8	8	2 ICLK		
0008 7594h	ICU	NMI pin digital filter setting register	NMIFLTC	16	16	2 ICLK		
0008 8000h	CMT	Compare match timer start register 0	CMSTR0	16	16	2, 3 PCLKB	2 ICLK	CMT
0008 8002h	CMT0	Compare match timer control register	CMCR	16	16	2, 3 PCLKB	2 ICLK	
0008 8004h	CMT0	Compare match timer counter	CMCNT	16	16	2, 3 PCLKB	2 ICLK	
0008 8006h	CMT0	Compare match timer constant register	CMCOR	16	16	2, 3 PCLKB	2 ICLK	
0008 8008h	CMT1	Compare match timer control register	CMCR	16	16	2, 3 PCLKB	2 ICLK	
0008 800Ah	CMT1	Compare match timer counter	CMCNT	16	16	2, 3 PCLKB	2 ICLK	
0008 800Ch	CMT1	Compare match timer constant register	CMCOR	16	16	2, 3 PCLKB	2 ICLK	
0008 8010h	CMT	Compare match timer start register 1	CMSTR1	16	16	2, 3 PCLKB	2 ICLK	
0008 8012h	CMT2	Compare match timer control register	CMCR	16	16	2, 3 PCLKB	2 ICLK	
0008 8014h	CMT2	Compare match timer counter	CMCNT	16	16	2, 3 PCLKB	2 ICLK	
0008 8016h	CMT2	Compare match timer constant register	CMCOR	16	16	2, 3 PCLKB	2 ICLK	
0008 8018h	CMT3	Compare match timer control register	CMCR	16	16	2, 3 PCLKB	2 ICLK	
0008 801Ah	CMT3	Compare match timer counter	CMCNT	16	16	2, 3 PCLKB	2 ICLK	
0008 801Ch	CMT3	Compare match timer constant register	CMCOR	16	16	2, 3 PCLKB	2 ICLK	
0008 8020h	WDT	WDT refresh register	WDTRR	8	8	2, 3 PCLKB	2 ICLK	WDTA
0008 8022h	WDT	WDT control register	WDTCR	16	16	2, 3 PCLKB	2 ICLK	
0008 8024h	WDT	WDT status register	WDTSR	16	16	2, 3 PCLKB	2 ICLK	
0008 8026h	WDT	WDT reset control register	WDTRCR	8	8	2, 3 PCLKB	2 ICLK	
0008 8030h	IWDT	IWDT refresh register	IWDTRR	8	8	2, 3 PCLKB	2 ICLK	
0008 8032h	IWDT	IWDT control register	IWDTCR	16	16	2, 3 PCLKB	2 ICLK	
0008 8034h	IWDT	IWDT status register	IWDTSR	16	16	2, 3 PCLKB	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (29/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 C000h	PORT0	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C001h	PORT1	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C002h	PORT2	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C003h	PORT3	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C004h	PORT4	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C005h	PORT5	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C006h	PORT6	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C007h	PORT7	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C008h	PORT8	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C009h	PORT9	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C00Ah	PORTA	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C00Bh	PORTB	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C00Ch	PORTC	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C00Dh	PORTD	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C00Eh	PORTE	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C00Fh	PORTF	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C010h	PORTG	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C012h	PORTJ	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C020h	PORT0	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C021h	PORT1	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C022h	PORT2	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C023h	PORT3	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C024h	PORT4	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C025h	PORT5	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C026h	PORT6	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C027h	PORT7	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C028h	PORT8	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C029h	PORT9	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C02Ah	PORTA	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C02Bh	PORTB	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C02Ch	PORTC	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C02Dh	PORTD	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C02Eh	PORTE	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C02Fh	PORTF	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C030h	PORTG	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C032h	PORTJ	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C040h	PORT0	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C041h	PORT1	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C042h	PORT2	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C043h	PORT3	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C044h	PORT4	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C045h	PORT5	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (35/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 C344h	ICU	Group 1 interrupt enable register	GEN01	32	32	1 to 2PCLKB	2 ICLK	ICUb
0008 C348h	ICU	Group 2 interrupt enable register	GEN02	32	32	1 to 2PCLKB	2 ICLK	
0008 C34Ch	ICU	Group 3 interrupt enable register	GEN03	32	32	1 to 2PCLKB	2 ICLK	
0008 C350h	ICU	Group 4 interrupt enable register	GEN04	32	32	1 to 2PCLKB	2 ICLK	
0008 C354h	ICU	Group 5 interrupt enable register	GEN05	32	32	1 to 2PCLKB	2 ICLK	
0008 C358h	ICU	Group 6 interrupt enable register	GEN06	32	32	1 to 2PCLKB	2 ICLK	
0008 C370h	ICU	Group 12 interrupt enable register	GEN12	32	32	1 to 2PCLKB	2 ICLK	
0008 C380h	ICU	Group 0 interrupt clear register	GCR00	32	32	1 to 2PCLKB	2 ICLK	
0008 C384h	ICU	Group 1 interrupt clear register	GCR01	32	32	1 to 2PCLKB	2 ICLK	
0008 C388h	ICU	Group 2 interrupt clear register	GCR02	32	32	1 to 2PCLKB	2 ICLK	
0008 C38Ch	ICU	Group 3 interrupt clear register	GCR03	32	32	1 to 2PCLKB	2 ICLK	
0008 C390h	ICU	Group 4 interrupt clear register	GCR04	32	32	1 to 2PCLKB	2 ICLK	
0008 C394h	ICU	Group 5 interrupt clear register	GCR05	32	32	1 to 2PCLKB	2 ICLK	
0008 C398h	ICU	Group 6 interrupt clear register	GCR06	32	32	1 to 2PCLKB	2 ICLK	
0008 C3C0h	ICU	Unit select register	SEL	32	32	1 to 2PCLKB	2 ICLK	
0008 C400h	RTC	64-Hz counter	R64CNT	8	8	2, 3 PCLKB	2 ICLK	RTCa
0008 C402h	RTC	Second counter	RSECCNT	8	8	2, 3 PCLKB	2 ICLK	
0008 C404h	RTC	Minute counter	RMINCNT	8	8	2, 3 PCLKB	2 ICLK	
0008 C406h	RTC	Hour counter	RHRCNT	8	8	2, 3 PCLKB	2 ICLK	
0008 C408h	RTC	Day-of-week counter	RWKCNT	8	8	2, 3 PCLKB	2 ICLK	
0008 C40Ah	RTC	Date counter	RDAYCNT	8	8	2, 3 PCLKB	2 ICLK	
0008 C40Ch	RTC	Month counter	RMONCNT	8	8	2, 3 PCLKB	2 ICLK	
0008 C40Eh	RTC	Year counter	RYRCNT	16	16	2, 3 PCLKB	2 ICLK	
0008 C410h	RTC	Second alarm register	RSECAR	8	8	2, 3 PCLKB	2 ICLK	
0008 C412h	RTC	Minute alarm register	RMINAR	8	8	2, 3 PCLKB	2 ICLK	
0008 C414h	RTC	Hour alarm register	RHRAR	8	8	2, 3 PCLKB	2 ICLK	
0008 C416h	RTC	Day-of-week alarm register	RWKAR	8	8	2, 3 PCLKB	2 ICLK	
0008 C418h	RTC	Date alarm register	RDAYAR	8	8	2, 3 PCLKB	2 ICLK	
0008 C41Ah	RTC	Month alarm register	RMONAR	8	8	2, 3 PCLKB	2 ICLK	
0008 C41Ch	RTC	Year alarm register	RYRAR	16	16	2, 3 PCLKB	2 ICLK	
0008 C41Eh	RTC	Year alarm enable register	RYRAREN	8	8	2, 3 PCLKB	2 ICLK	
0008 C422h	RTC	RTC control register 1	RCR1	8	8	2, 3 PCLKB	2 ICLK	
0008 C424h	RTC	RTC control register 2	RCR2	8	8	2, 3 PCLKB	2 ICLK	
0008 C426h	RTC	RTC control register 3	RCR3	8	8	2, 3 PCLKB	2 ICLK	
0008 C428h	RTC	RTC control register 4	RCR4	8	8	2, 3 PCLKB	2 ICLK	
0008 C42Ah	RTC	Frequency register H	RFRH	16	16	2, 3 PCLKB	2 ICLK	
0008 C42Ch	RTC	Frequency register L	RFRL	16	16	2, 3 PCLKB	2 ICLK	
0008 C42Eh	RTC	Time error adjustment register	RADJ	8	8	2, 3 PCLKB	2 ICLK	
0008 C440h	RTC	Time capture control register 0	RTCCR0	8	8	2, 3 PCLKB	2 ICLK	
0008 C442h	RTC	Time capture control register 1	RTCCR1	8	8	2, 3 PCLKB	2 ICLK	
0008 C444h	RTC	Time capture control register 2	RTCCR2	8	8	2, 3 PCLKB	2 ICLK	
0008 C452h	RTC	Second capture register 0	RSECCP0	8	8	2, 3 PCLKB	2 ICLK	
0008 C454h	RTC	Minute capture register 0	RMINCP0	8	8	2, 3 PCLKB	2 ICLK	

5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Table 5.1 Absolute Maximum Ratings

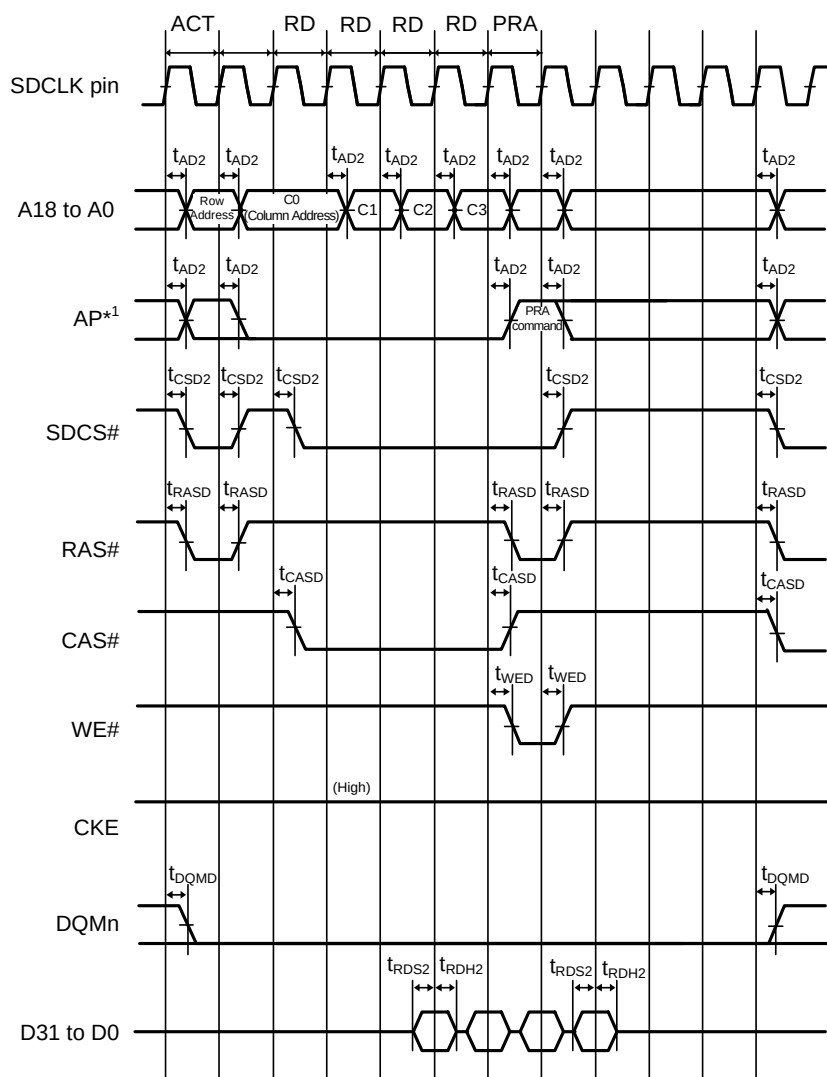
Conditions: $V_{SS} = AVSS0 = VREFL/VREFL0 = VSS_USB = 0\text{ V}$

Item		Symbol	Value	Unit
Power supply voltage		V_{CC}, V_{CC_USB}	-0.3 to +4.6	V
V_{BATT} power supply voltage		V_{BATT}	-0.3 to +4.6	V
Input voltage (except for ports for 5 V tolerant*1)		V_{in}	-0.3 to $V_{CC} + 0.3$	V
Input voltage (ports for 5 V tolerant*1)		V_{in}	-0.3 to +5.8	V
Reference power supply voltage		V_{REFH}	-0.3 to $V_{CC} + 0.3$	V
Analog power supply voltage		$AVCC^{*2}$	-0.3 to +4.6	V
Analog input voltage		V_{AN}	-0.3 to $V_{CC} + 0.3$	V
Operating temperature	D version	T_{opr}	-40 to +85	°C
	G version		-40 to +105	°C
Storage temperature		T_{stg}	-55 to +125	°C

Caution: Permanent damage to the LSI may result if absolute maximum ratings are exceeded.

Note 1. Ports 07, 12 to 17, 20, 21, 30 to 33, 67, and C0 to C3 are 5 V tolerant.

Note 2. Connect $AVCC0$ to V_{CC} . When neither the A/D converter nor the D/A converter is in use, do not leave the $AVCC0$, V_{REFH} / V_{REFH0} , $AVSS0$, and V_{REFL} / V_{REFL0} pins open. Connect the $AVCC0$ and V_{REFH} / V_{REFH0} pins to V_{CC} , and the $AVSS0$ and V_{REFL} / V_{REFL0} pins to V_{SS} , respectively.



Note 1: Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

Figure 5.26 SDRAM Space Multiple Read Bus Timing

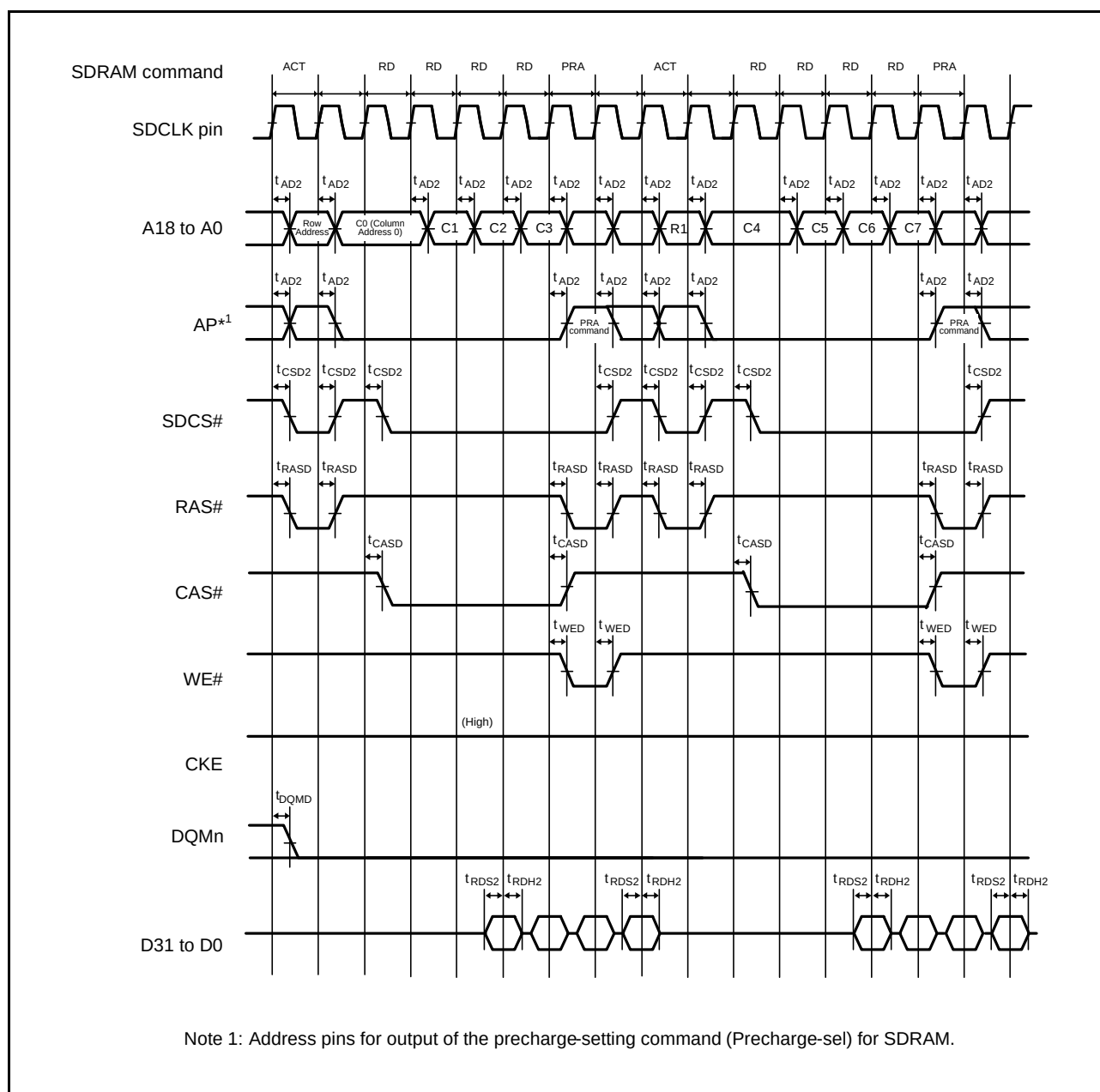


Figure 5.28 SDRAM Space Multiple Read Line Stride Bus Timing

Table 5.24 Timing of On-Chip Peripheral Modules (6)

Conditions: VCC = AVCC0 = VREFH = VCC_USB = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0

VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V

PCLK = 8 to 50 MHz

 $T_a = T_{opr}$

High drive output is selected by the drive capacity control register.

Item		Symbol	Min.*1, *2	Max.*1	Unit	Test Conditions
RIIC (Fast-mode+) ICFER.FMPE = 1	SCL input cycle time	t_{SCL}	$6(12) \times t_{IICcyc} + 240$	—	ns	Figure 5.47
	SCL input high pulse width	t_{SCLH}	$3(6) \times t_{IICcyc} + 120$	—	ns	
	SCL input low pulse width	t_{SCLL}	$3(6) \times t_{IICcyc} + 120$	—	ns	
	SCL, SDA input rise time	t_{Sr}	—	120	ns	
	SCL, SDA input fall time	t_{Sf}	—	120	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	$1(4) \times t_{IICcyc}$	ns	
	SDA input bus free time	t_{BUF}	$3(6) \times t_{IICcyc} + 120$	—	ns	
	Start condition input hold time	t_{STAH}	$t_{IICcyc} + 120$	—	ns	
	Restart condition input setup time	t_{STAS}	120	—	ns	
	Stop condition input setup time	t_{STOS}	120	—	ns	
	Data input setup time	t_{SDAS}	$t_{IICcyc} + 120$	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	550	pF	
Simple IIC (Standard-mode)	SDA input rise time	t_{Sr}	—	1000	ns	
	SDA input fall time	t_{Sf}	—	300	ns	
	SDA input spike pulse removal time	t_{SP}	0	$4 \times t_{IICcyc}$	ns	
	Data input setup time	t_{SDAS}	250	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
Simple IIC (Fast-mode)	SCL, SDA input rise time	t_{Sr}	$20 + 0.1C_b$	300	ns	
	SCL, SDA input fall time	t_{Sf}	$20 + 0.1C_b$	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	$4 \times t_{IICcyc}$	ns	
	Data input setup time	t_{SDAS}	100	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

Note: t_{IICcyc} : RIIC internal reference clock (IIC ϕ) Cycle, t_{Pcyc} : PCLK cycle

Note 1. The value in parentheses is used when ICMR3.NF[1:0] are set to 11b while a digital filter is enabled with ICFER.NFE = 1.

Note 2. C_b indicates the total capacity of the bus line.

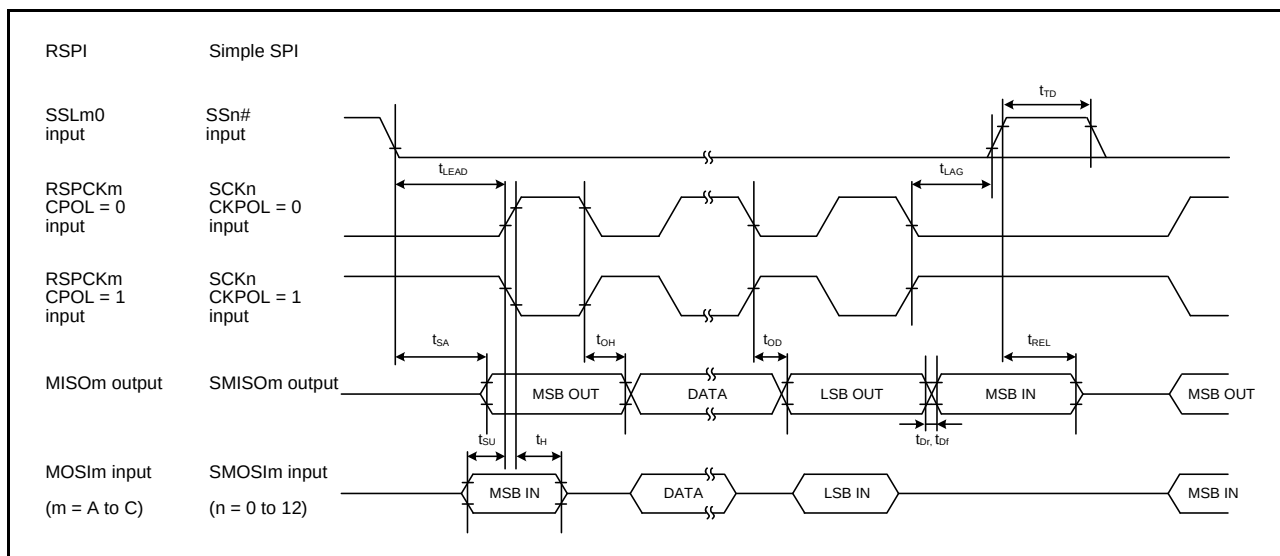


Figure 5.45 RSPi Timing (Slave, CPHA = 0) and Simple SPI Timing (Slave, CKPH = 1)

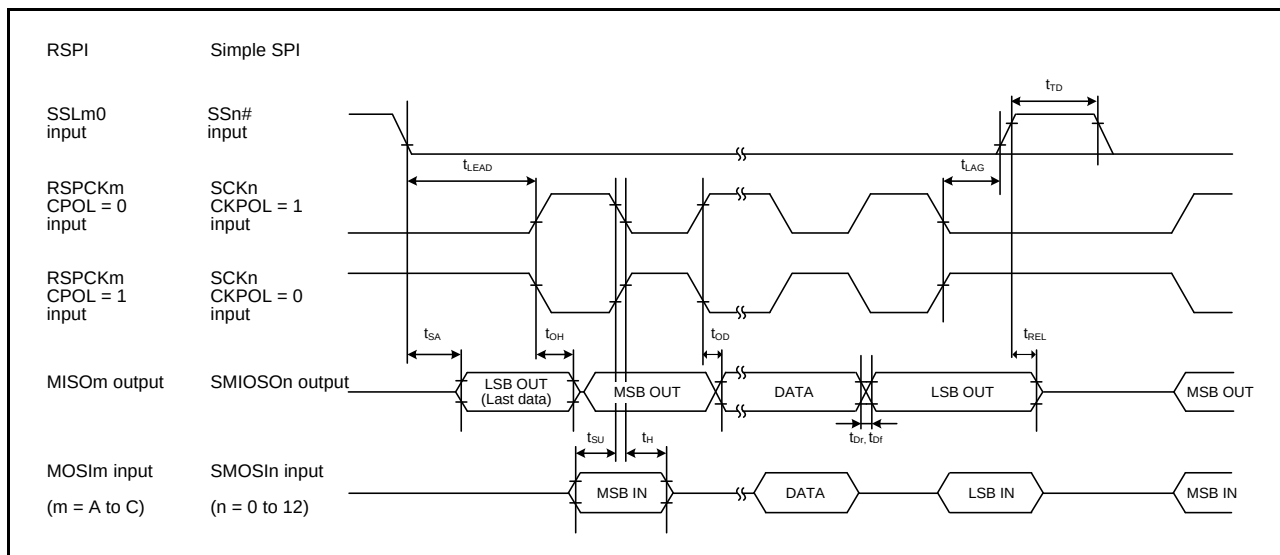


Figure 5.46 RSPi Timing (Slave, CPHA = 1) and Simple SPI Timing (Slave, CKPH = 0)

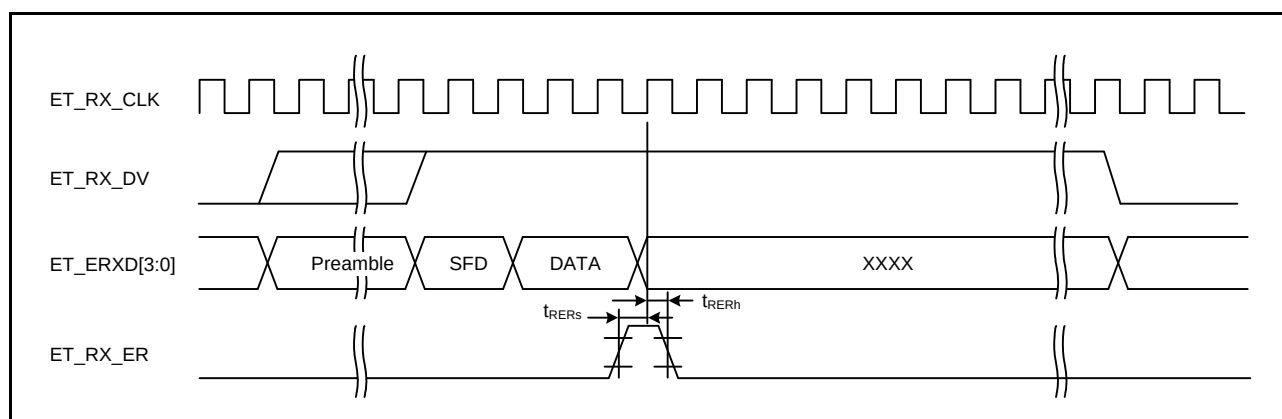


Figure 5.56 MII Reception Timing (Error Occurrence)

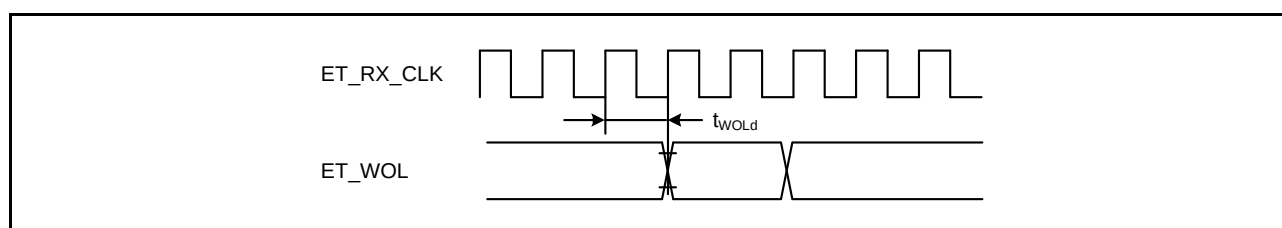


Figure 5.57 WOL Output Timing (MII)

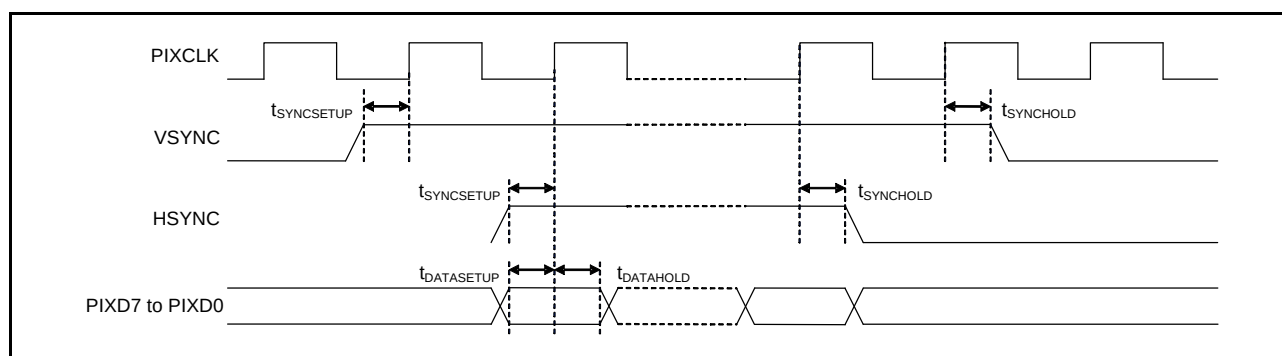


Figure 5.58 PDC Timing

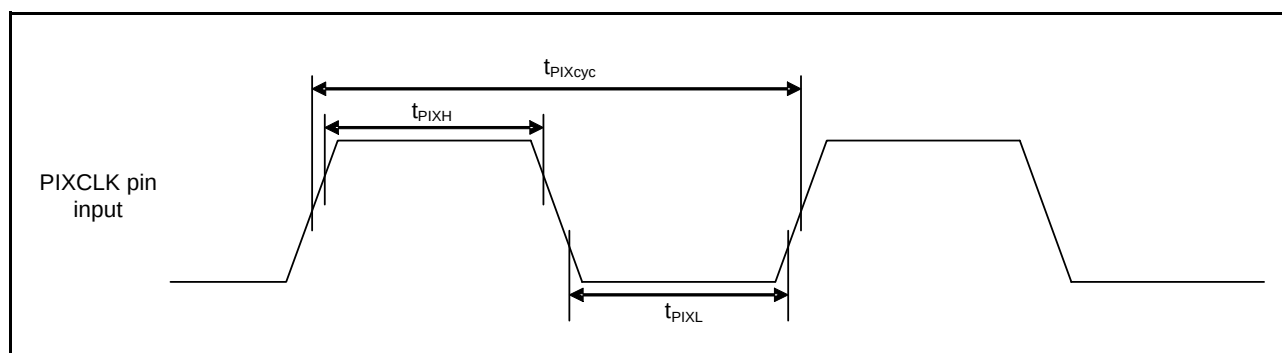


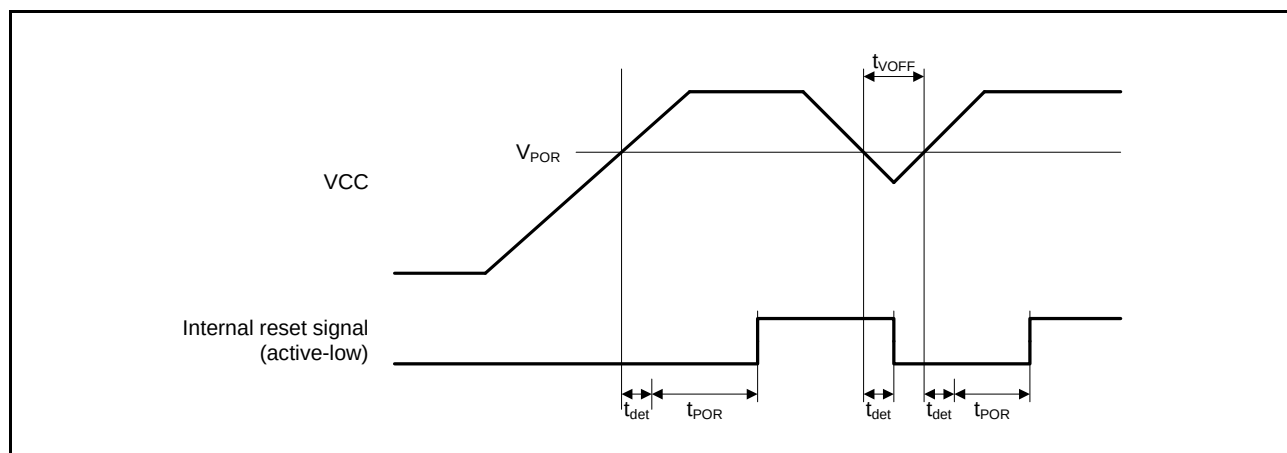
Figure 5.59 PDC Input Clock Characteristic

5.8 Power-on Reset Circuit and Voltage Detection Circuit Characteristics

Table 5.33 Power-on Reset Circuit and Voltage Detection Circuit CharacteristicsConditions: $V_{CC} = AV_{CC0} = V_{REFH} = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, $V_{REFH0} = 2.7$ V to AV_{CC0} $V_{SS} = AV_{SS0} = V_{REFL}/V_{REFL0} = V_{SS_USB} = 0$ V $T_a = T_{opr}$

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage detection level	Power-on reset (POR)	Low power consumption function disabled	V _{POR}	2.5	2.6	2.7	V	Figure 5.63
		Low power consumption function enabled		2.0	2.35	2.7		
	Voltage detection circuit (LVD0)		V _{det0}	2.7	2.80	2.9		Figure 5.64
	Voltage detection circuit (LVD1)		V _{det1_A}	2.75	2.95	3.15		Figure 5.65
	Voltage detection circuit (LVD2)		V _{det2_A}	2.75	2.95	3.15		Figure 5.66
Internal reset time	Power-on reset time		t _{POR}	—	4.6	—	ms	Figure 5.63
	LVD0 reset time		t _{LVD0}	—	4.6	—		Figure 5.64
	LVD1 reset time		t _{LVD1}	—	0.9	—		Figure 5.65
	LVD2 reset time		t _{LVD2}	—	0.9	—		Figure 5.66
Minimum VCC down time			t _{VOFF}	200	—	—	μs	Figure 5.63 and Figure 5.64
Response delay time			t _{det}	—	—	200	μs	Figure 5.63 to Figure 5.66
LVD operation stabilization time (after LVD is enabled)			Td _(E-A)	—	—	3	μs	Figure 5.65 and Figure 5.66
Hysteresis width (LVD1 and LVD2)			V _{LVH}	—	80	—	mV	

Note: The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR} , V_{det1} , and V_{det2} for the POR/ LVD.

**Figure 5.63 Power-on Reset Timing**

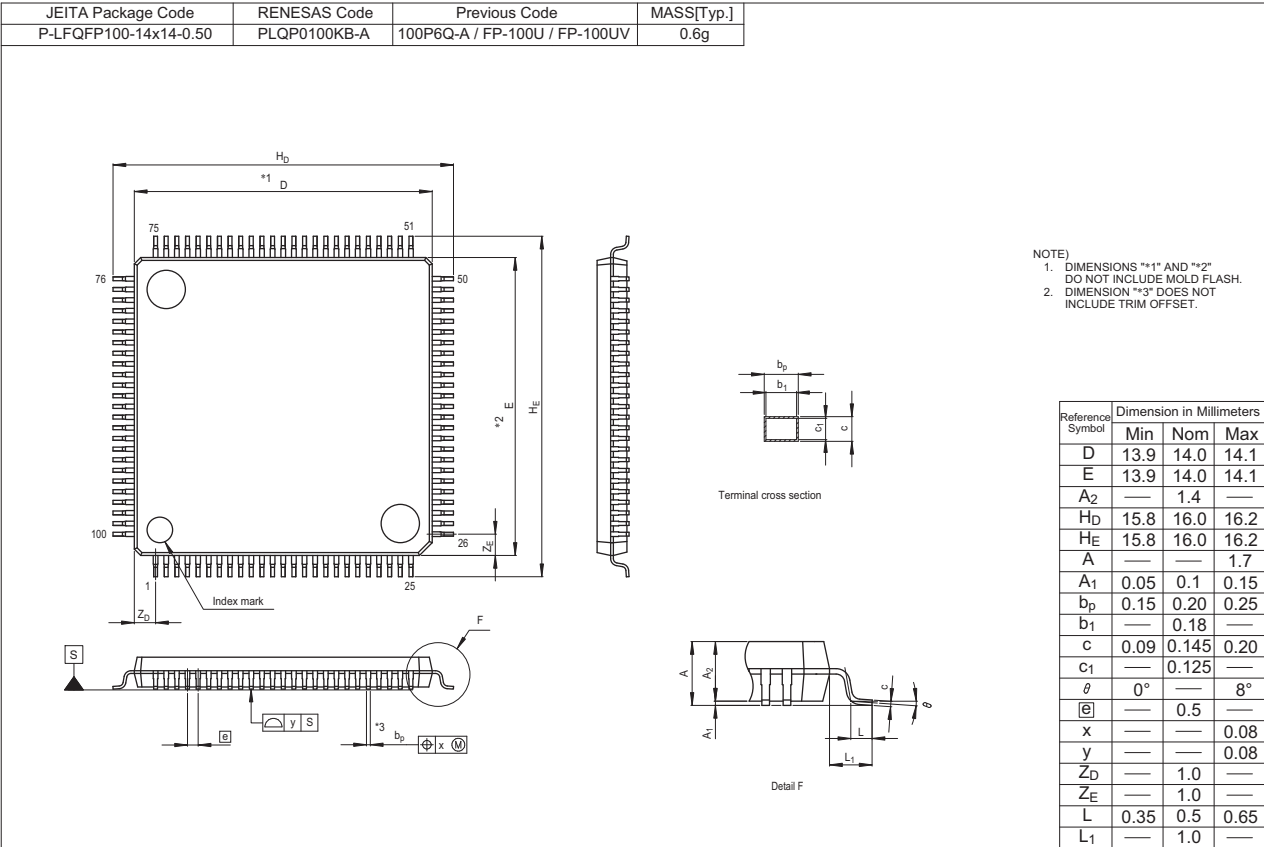


Figure G 100-pin LQFP (PLQP0100KB-A)

Rev.	Date	Description	
		Page	Summary
1.60	Mar 13. 2013	Feature	
		1	Changed
		1. Overview	
		2 to 7	Table 1.1 Outline of Specifications: changed, note added
		8	Table 1.2 Comparison of Functions for Different Packages in the RX63N/RX631 Group, changed
		9 to 15	Table 1.3 List of Products, changed
		16	Figure 1.1 How to Read the Product Part No., changed
		17	Figure 1.2 Block Diagram, changed
		24 to 32	Figure 1.3 to Figure 1.11 Pin Assignment: note, added
		53 to 57	Table 1.9 List of Pins and Pin Functions (100-Pin TFLGA), added
		62 to 64	Table 1.11 List of Pins and Pin Functions (64-Pin LQFP), added
		65, 66	Table 1.12 List of Pins and Pin Functions (48-Pin LQFP), added
		3. Address Space	
		71	Figure 3.1 Memory Map in Each Operating Mode, changed
		4. I/O Registers	
		75 to 120	Table 4.1 List of I/O Registers (Address Order), changed
		5. Electrical Characteristics	
		All	Characteristics and timing conditions in the tables, changed
		124, 125	Table 5.4 DC Characteristics (3), changed
		126	Table 5.5 DC Characteristics (4), changed
		127	5.3 AC Characteristics, changed
		130, 131	Table 5.11, Clock Timing (Except for Sub-Clock Related): Condition and the table, changed, note, added
		132	Table 5.12 Clock Timing (Sub-Clock Related): Condition and the table, changed, note, added
		176	Table 5.33 Battery Backup Function Characteristics: Condition, changed
		Appendix 1. Package Dimensions	
		189	Figure H 64-pin LQFP (PLQP0064KB-A), added
		190	Figure I 48-pin LQFP (PLQP0048KB-A), added
1.70	Oct 08. 2013	Features	
		1	changed
		1. Overview	
		2 to 7	Table 1.1 Outline of Specifications, General I/O ports, Packages, changed, Parallel data capture unit (PDC), added.
		8	Table 1.2 Comparison of Functions for Different Packages in the RX63N/RX631 Group, 64-pin LQFP, changed, 64-pin TFLGA, Parallel data capture unit (PDC), added.
		9 to 16	Table 1.3 List of Products, changed.
		17	Figure 1.1 How to Read the Product Part No., changed
		18	Figure 1.2 Block Diagram, changed
		19 to 24	Table 1.4 Pin Functions, changed, Parallel data capture unit (PDC), added
		32	Figure 1.10 Pin Assignment (64-Pin TFLGA), added
		35 to 40	Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA), changed
		41 to 45	Table 1.6 List of Pin and Pin Functions (176-Pin LQFP), changed
		46 to 50	Table 1.7 List of Pins and Pin Functions (145-Pin TFLGA), changed
		51 to 55	Table 1.8 List of Pins and Pin Functions (144-Pin LQFP), changed
		65 to 66	Table 1.11 List of Pins and Pin Functions (64-Pin TFLGA), added
		3. Address Space	
		76	Figure 3.1 Memory Map in Each Operating Mode, changed
		4. I/O Registers	
		79	(4) Restrictions in Relation to RMPA and String-Manipulation Instructions, added