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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

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Details

Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, I ² C, LINbus, SCI, SPI, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	30
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f5631pddfl-v0

Table 1.1 Outline of Specifications (6/6)

Classification	Module/Function	Description
Communication function	Parallel data capture unit (PDC)	1 channel - Communicates with an image sensor or other external I/Os and transfer parallel data such as an image output from those devices to internal RAM or external address spaces (CS space and SDRAM space) through DTC or DMAC.
12-bit A/D converter (S12ADa)		1 unit (1 unit x 21 channels) 12-bit resolution - Conversion time: 1.0 μs per channel (in operation with PCLK at 50 MHz) - Operating mode - Scan mode (single scan mode or continuous scan mode) - Sample-and-hold function - Reference voltage generation - Three ways to start A/D conversion - Conversion can be started by software, a conversion start trigger from a timer (MTU, TPU, or TMR), or an external trigger signal. - A/D conversion of the temperature sensor output
10-bit A/D converter (ADb)		1 unit (1 unit x 8 channels) 10-bit resolution - Conversion time: 1.0 μs per channel (in operation with PCLK at 50 MHz) - Operating mode - Scan mode (single scan mode or continuous scan mode) - External amplifier connection mode - Sample-and-hold function - Three ways to start A/D conversion - Conversion can be started by software, a conversion start trigger from a timer (MTU, TPU, or TMR), or an external trigger signal.
D/A converter (DAa)		2 channels 10-bit resolution - Output voltage: 0 V to VREFH
Temperature sensor		1 channel - Precision: $\pm 1^{\circ}\text{C}$ - The voltage of the temperature is converted into a digital value by the 12-bit A/D converter.
CRC calculator (CRC)		- CRC code generation for arbitrary amounts of data in 8-bit units - Select any of three generating polynomials: $X^8 + X^2 + X + 1$, $X^{16} + X^{15} + X^2 + 1$, or $X^{16} + X^{12} + X^5 + 1$. - Generation of CRC codes for use with LSB-first or MSB-first communications is selectable
Unique ID		A 16-byte device-specific ID (only for the G version)
Data encryption unit (DEU)*1		- AES encryption and decryption functions 128/192/256-bit key length - ECB/CBC mode
Operating frequency		Up to 100 MHz
Power supply voltage		VCC = AVCC0 = VREFH = VCC_USB = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0, V _{BATT} = 2.0 V to 3.6 V (for products with 100 or more pins), V _{BATT} = 2.3 V to 3.6 V (for the 64-pin product)
Operating temperature		D version: -40 to +85°C, G version: -40 to +105°C*2
Package		177-pin TFLGA (PTLG0177KA-A) 176-pin LFBGA (PLBG0176GA-A) 176-pin LQFP (PLQP0176KB-A) 145-pin TFLGA (PTLG0145KA-A) 144-pin LQFP (PLQP0144KA-A) 100-pin TFLGA (PTLG0100JA-A) (in the planning stage) 100-pin LQFP (PLQP0100KB-A) 64-pin TFLGA (PTLG0064JA-A) 64-pin LQFP (PLQP0064KB-A) 48-pin LQFP (PLQP0048KB-A)
On-chip debugging system		- E1 emulator (JTAG and FINE interfaces) - E20 emulator (JTAG interface)

Note 1. Please contact our sales office for more information.

Note 2. Please contact us if you are using a G version.

Table 1.3 List of Products (2/8)

Group	Part No.	Package	ROM Capacity	RAM Capacity	E2 Data Flash	Operating Frequency (Max.)	Operating Temp. Range
RX63N (D version)	R5F563NDDDLK	PTLG0145KA-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NBCDLK	PTLG0145KA-A	1 Mbyte	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NBDDLK	PTLG0145KA-A	1 Mbyte	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NACDLK	PTLG0145KA-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NADDLK	PTLG0145KA-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NFHDFB	PLQP0144KA-A	2 Mbytes	256 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NFDDFB	PLQP0144KA-A	2 Mbytes	256 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NKHDFB	PLQP0144KA-A*1	2 Mbytes	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NKDDFB	PLQP0144KA-A	2 Mbytes	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NECDFB	PLQP0144KA-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NEDDFB	PLQP0144KA-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NJHDFB	PLQP0144KA-A*1	1.5 Mbytes	256 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NJDDFB	PLQP0144KA-A*1	1.5 Mbytes	256 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NGHDFB	PLQP0144KA-A*1	1.5 Mbytes	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NGDDFB	PLQP0144KA-A*1	1.5 Mbytes	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NDCDFB	PLQP0144KA-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NDDDFB	PLQP0144KA-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NYHDFB	PLQP0144KA-A	1 Mbyte	256 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NYDDFB	PLQP0144KA-A	1 Mbyte	256 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NWHDFB	PLQP0144KA-A	1 Mbyte	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NWDDFB	PLQP0144KA-A	1 Mbyte	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NBCDFB	PLQP0144KA-A	1 Mbyte	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NBDDFB	PLQP0144KA-A	1 Mbyte	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NACDFB	PLQP0144KA-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NADDFB	PLQP0144KA-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NECDLJ	PTLG0100JA-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NEDDLJ	PTLG0100JA-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NDCDLJ	PTLG0100JA-A*1	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NDDDLJ	PTLG0100JA-A*1	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NBCDLJ	PTLG0100JA-A	1 Mbyte	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NBDDLJ	PTLG0100JA-A	1 Mbyte	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NACDLJ	PTLG0100JA-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NADDLJ	PTLG0100JA-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NFHDFP	PLQP0100KB-A	2 Mbytes	256 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NFDDFP	PLQP0100KB-A	2 Mbytes	256 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NKHDFP	PLQP0100KB-A*1	2 Mbytes	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NKDDFP	PLQP0100KB-A	2 Mbytes	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NECDFP	PLQP0100KB-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NEDDFP	PLQP0100KB-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NJHDFP	PLQP0100KB-A*1	1.5 Mbytes	256 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NJDDFP	PLQP0100KB-A*1	1.5 Mbytes	256 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NGHDFP	PLQP0100KB-A*1	1.5 Mbytes	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NGDDFP	PLQP0100KB-A*1	1.5 Mbytes	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NDCDFP	PLQP0100KB-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NDDDFP	PLQP0100KB-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C

1.5 Pin Assignments

Figure 1.5 to Figure 1.12 show the pins assignments. Table 1.5 to Table 1.13 show the list of pins and pin functions. Power pins and I/O ports are shown in the pin assignment diagrams.

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	
15	PE2	PE3	P70	P65	P67	VSS	VCC	PG7	PA6	PB0	P72	PB4	VSS	VCC	PC1	15
14	PE1	PE0	VSS	PE7	PG3	PA0	PA1	PA2	PA7	VCC	PB1	PB5	P73	P75	P74	14
13	P63	P64	PE4	VCC	PG2	PG4	PG6	PA3	VSS	P71	PB3	PB7	PC0	PC2	P76	13
12	P60	VSS	P62	PE5	PE6	P66	PG5	PA4	PA5	PB2	PB6	P77	PC3	PC4	P80	12
11	PD6	PG1	VCC	P61	RX63N Group RX631 Group PTLG0177KA-A (177-pin TFLGA) (Top perspective view)							P81	P82	PC6	VCC	11
10	P97	PD4	PG0	PD7								PC5	PC7	P83	VSS	10
9	VCC	P96	PD3	PD5								P50	P51	P52	P84	9
8	P94	PD1	PD2	VSS								P53	VCC_USB	USB1_DP	USB1_DM	8
7	VSS	P92	PD0	P95								P54	P55	VSS_USB	USB0_DP	7
6	VCC	P91	P90	P93	NC							P56	P57	VCC_USB	USB0_DM	6
5	P46	P47	P45	P44								P13	P12	P10	P11	5
4	P42	P41	P43	P00	VSS	BSCANP	PF4	P35	PF3	PF1	P25	P86	P15	P14	P85	4
3	VREFL0	P40	VREFH0	P03	PF5	PJ3	MD/FINED	RES#	P34	PF2	PF0	P24	P22	P87	P16	3
2	AVCC0	P07	VREFH	P02	EMLE	VCL	XCOUT	VSS	VCC	P32	P30	P26	P23	P17	P20	2
1	AVSS0	P05	VREFL	P01	PJ5	VBATT	XCIN	XTAL	EXTAL	P33	P31	P27	VCC	VSS	P21	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	

Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.5, List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA).

Figure 1.3 Pin Assignment (177-Pin TFLGA)

Table 1.6 List of Pin and Pin Functions (176-Pin LQFP) (4/5)

Pin Number	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SCIC, SCID, RSPI, RIIC, CAN, IEB, USB, and PDC)	Interrupt	S12AD, AD, DA
100		PB1	A9	MTIOC0C/MTIOC4C/ TIOCB3/TMCI0/PO25	ET_ERXD0/RMII_RXD0/ TXD4/TXD6/SMOSI4/ SMOSI6/SSDA4/SSDA6	IRQ4-DS	
101		P72	CS2#		ET_MDC		
102		P71	CS1#		ET_MDIO		
103	VCC						
104		PB0	A8	MTIC5W/TIOCA3/PO24	ET_ERXD1/RMII_RXD1/ RXD4/RXD6/SMISO4/ SMISO6/SSCL4/SSCL6/ RSPCKA	IRQ12	
105	VSS						
106		PA7	A7	TIOCB2/PO23	ET_WOL/MISOA		
107		PA6	A6	MTIC5V/MTCLKB/ TIOCA2/TMCI3/PO22/ POE2#	ET_EXOUT/CTS5#/ RTS5#/SS5#/MOSIA		
108		PA5	A5	TIOCB1/PO21	ET_LINKSTA/RSPCKA		
109		PA4	A4	MTIC5U/MTCLKA/ TIOCA1/TMRI0/PO20	ET_MDC/TXD5/SMOSI5/ SSDA5/SSLA0	IRQ5-DS	
110		PA3	A3	MTIOC0D/MTCLKD/ TIOCD0/TCLKB/PO19	ET_MDIO/RXD5/SMISO5/ SSCL5	IRQ6-DS	
111	TRDATA3	PG7	D31				
112		PA2	A2	PO18	RXD5/SMISO5/SSCL5/ SSLA3		
113	TRDATA2	PG6	D30				
114		PA1	A1/DQM3	MTIOC0B/MTCLKC/ TIOCB0/PO17	ET_WOL/SCK5/SSLA2	IRQ11	
115	VCC						
116	TRCLK	PG5	D29				
117	VSS						
118		PA0	A0/BC0#/DQM2	MTIOC4A/TIOCA0/PO16	ET_TX_EN/ RMII_TXD_EN/SSLA1		
119	TRSYNC	PG4	D28				
120		P67	CS7#/DQM1		CRX2*2	IRQ15	
121	TRDATA1	PG3	D27				
122		P66	CS6#/DQM0		CTX2*2		
123	TRDATA0	PG2	D26				
124		P65	CS5#/CKE				
125		PE7	D15[A15/D15]	TIOCB11	MISOB	IRQ7	AN5
126		PE6	D14[A14/D14]	TIOCA11	MOSIB	IRQ6	AN4
127	VCC						
128	SDCLK	P70					
129	VSS						
130		PE5	D13[A13/D13]	MTIOC4C/MTIOC2B/ TIOCB10	ET_RX_CLK/REF50CK/ RSPCKB	IRQ5	AN3
131		PE4	D12[A12/D12]	MTIOC4D/MTIOC1A/ TIOCA10/PO28	ET_ERXD2/SSLB0		AN2
132		PE3	D11[A11/D11]	MTIOC4B/TIOCB9/PO26/ POE8#	ET_ERXD3/CTS12#/ RTS12#/SS12#/MISOB		AN1
133		PE2	D10[A10/D10]	MTIOC4A/TIOCA9/PO23	RXD12/SMISO12/ SSCL12/RXD12/SSLB3/ MOSIB	IRQ7-DS	AN0
134		PE1	D9[A9/D9]	MTIOC4C/TIOCD9/PO18	TXD12/SMOSI12/ SSDA12/TXD12/ SIOX12/SSLB2/RSPCKB		ANEX1
135		PE0	D8[A8/D8]	TIOCC9	SCK12/SSLB1		ANEX0

Table 1.9 List of Pins and Pin Functions (100-Pin TFLGA) (4/5)

Pin No. 100-pin TFLGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC	Timers (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SCIC, SCID, RSPI, RIIC, CAN, IEB, USB)	Interrupt	S12AD AD DA
H4		P15		MTIOC0B/ MTCLKB/ TIOCB2/ TCLKB/TMCI2/ PO13	RXD1/SCK3/ SMISO1/SSCL1/ CRX1-DS	IRQ5	
H5		P55	WAIT#/ EDREQ0	MTIOC4D/ TMO3	CRX1/ET_EXOUT	IRQ10	
H6		P54	ALE/EDACK0	MTIOC4B/ TMCI1	CTS2#/RTS2#/ SS2#/CTX1/ ET_LINKSTA		
H7		PC7	A23/CS0#	MTIOC3A/ MTCLKB/ TMO2/PO31	TXD8/SMOSI8/ SSDA8/MISOA/ ET_COL	IRQ14	
H8		PC6	A22/CS1#	MTIOC3C/ MTCLKA/ TMCI2/PO30	RXD8/SMISO8/ SSCL8/MOSIA/ ET_ETXD3	IRQ13	
H9		PB6	A14	MTIOC3D/ TIOCA5/PO30	RXD9/SMISO9/ SSCL9/ET_ETXD1/ RMII_TXD1		
H10		PB7	A15	MTIOC3B/ TIOCB5/PO31	TXD9/SMOSI9/ SSDA9/ET_CRS/ RMII_CRS_DV		
J1		P24	CS4#/ EDREQ1	MTIOC4A/ MTCLKA/ TIOCB4/ TMRI1/PO4	SCK3/ USB0_VBUSEN		
J2		P21		MTIOC1B/ TIOCA3/ TMCI0/PO1	RXD0/SMISO0/ SSCL0/ USB0_EXICEN	IRQ9	
J3		P17		MTIOC3A/ MTIOC3B/ TIOCB0/ TCLKD/TMO1/ PO15/POE8#	SCK1/TXD3/ SMOSI3/SSDA3/ MISOA/SDA2-DS/ IETXD	IRQ7	ADTRG#
J4		P13		MTIOC0B/ TIOCA5/TMO3/ PO13	TXD2/SMOSI2/ SSDA2/SDA0[FM+]	IRQ3	ADTRG#
J5	VSS_USB						
J6	VCC_USB						
J7		P50	WR0#/WR#		TXD2/SMOSI2/ SSDA2/SSLB1		
J8		PC4	A20/CS3#	MTIOC3D/ MTCLKC/ TMCI1/PO25/ POE0#	SCK5/CTS8#/ RTS8#/SS8#/ SSLA0/ET_TX_CLK		
J9		PC0	A16	MTIOC3C/ TCLKC/PO17	CTS5#/RTS5#/ SS5#/SSLA1/ ET_ERXD3	IRQ14	
J10		PC1	A17	MTIOC3A/ TCLKD/PO18	SCK5/SSLA2/ ET_ERXD2	IRQ12	
K1		P23	EDACK0	MTIOC3D/ MTCLKD/ TIOCD3/PO3	TXD3/CTS0#/ RTS0#/SMOSI3/ SS0#/SSDA3/ USB0_DPUPE		

Table 4.1 List of I/O Registers (Address Order) (10/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 719Ch	ICU	DTC activation enable register 156	DTCER156	8	8	2	ICLK	ICUb
0008 719Dh	ICU	DTC activation enable register 157	DTCER157	8	8	2	ICLK	
0008 719Eh	ICU	DTC activation enable register 158	DTCER158	8	8	2	ICLK	
0008 719Fh	ICU	DTC activation enable register 159	DTCER159	8	8	2	ICLK	
0008 71A0h	ICU	DTC activation enable register 160	DTCER160	8	8	2	ICLK	
0008 71A1h	ICU	DTC activation enable register 161	DTCER161	8	8	2	ICLK	
0008 71A2h	ICU	DTC activation enable register 162	DTCER162	8	8	2	ICLK	
0008 71A3h	ICU	DTC activation enable register 163	DTCER163	8	8	2	ICLK	
0008 71A4h	ICU	DTC activation enable register 164	DTCER164	8	8	2	ICLK	
0008 71A5h	ICU	DTC activation enable register 165	DTCER165	8	8	2	ICLK	
0008 71AAh	ICU	DTC activation enable register 170	DTCER170	8	8	2	ICLK	
0008 71ABh	ICU	DTC activation enable register 171	DTCER171	8	8	2	ICLK	
0008 71ADh	ICU	DTC activation enable register 173	DTCER173	8	8	2	ICLK	
0008 71AEh	ICU	DTC activation enable register 174	DTCER174	8	8	2	ICLK	
0008 71B0h	ICU	DTC activation enable register 176	DTCER176	8	8	2	ICLK	
0008 71B1h	ICU	DTC activation enable register 177	DTCER177	8	8	2	ICLK	
0008 71B3h	ICU	DTC activation enable register 179	DTCER179	8	8	2	ICLK	
0008 71B4h	ICU	DTC activation enable register 180	DTCER180	8	8	2	ICLK	
0008 71B7h	ICU	DTC activation enable register 183	DTCER183	8	8	2	ICLK	
0008 71B8h	ICU	DTC activation enable register 184	DTCER184	8	8	2	ICLK	
0008 71BBh	ICU	DTC activation enable register 187	DTCER187	8	8	2	ICLK	
0008 71BCh	ICU	DTC activation enable register 188	DTCER188	8	8	2	ICLK	
0008 71BFh	ICU	DTC activation enable register 191	DTCER191	8	8	2	ICLK	
0008 71C0h	ICU	DTC activation enable register 192	DTCER192	8	8	2	ICLK	
0008 71C3h	ICU	DTC activation enable register 195	DTCER195	8	8	2	ICLK	
0008 71C4h	ICU	DTC activation enable register 196	DTCER196	8	8	2	ICLK	
0008 71C6h	ICU	DTC activation enable register 198	DTCER198	8	8	2	ICLK	
0008 71C7h	ICU	DTC activation enable register 199	DTCER199	8	8	2	ICLK	
0008 71C8h	ICU	DTC activation enable register 200	DTCER200	8	8	2	ICLK	
0008 71C9h	ICU	DTC activation enable register 201	DTCER201	8	8	2	ICLK	
0008 71CAh	ICU	DTC activation enable register 202	DTCER202	8	8	2	ICLK	
0008 71CBh	ICU	DTC activation enable register 203	DTCER203	8	8	2	ICLK	
0008 71CEh	ICU	DTC activation enable register 206	DTCER206	8	8	2	ICLK	
0008 71CFh	ICU	DTC activation enable register 207	DTCER207	8	8	2	ICLK	
0008 71D0h	ICU	DTC activation enable register 208	DTCER208	8	8	2	ICLK	
0008 71D6h	ICU	DTC activation enable register 214	DTCER214	8	8	2	ICLK	
0008 71D7h	ICU	DTC activation enable register 215	DTCER215	8	8	2	ICLK	
0008 71D9h	ICU	DTC activation enable register 217	DTCER217	8	8	2	ICLK	
0008 71DAh	ICU	DTC activation enable register 218	DTCER218	8	8	2	ICLK	
0008 71DCh	ICU	DTC activation enable register 220	DTCER220	8	8	2	ICLK	
0008 71DDh	ICU	DTC activation enable register 221	DTCER221	8	8	2	ICLK	
0008 71DFh	ICU	DTC activation enable register 223	DTCER223	8	8	2	ICLK	
0008 71E0h	ICU	DTC activation enable register 224	DTCER224	8	8	2	ICLK	
0008 71E2h	ICU	DTC activation enable register 226	DTCER226	8	8	2	ICLK	
0008 71E3h	ICU	DTC activation enable register 227	DTCER227	8	8	2	ICLK	
0008 71E5h	ICU	DTC activation enable register 229	DTCER229	8	8	2	ICLK	
0008 71E6h	ICU	DTC activation enable register 230	DTCER230	8	8	2	ICLK	
0008 71E8h	ICU	DTC activation enable register 232	DTCER232	8	8	2	ICLK	
0008 71E9h	ICU	DTC activation enable register 233	DTCER233	8	8	2	ICLK	
0008 71EBh	ICU	DTC activation enable register 235	DTCER235	8	8	2	ICLK	
0008 71ECh	ICU	DTC activation enable register 236	DTCER236	8	8	2	ICLK	

Table 4.1 List of I/O Registers (Address Order) (17/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 81A8h	TPU8	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 81AAh	TPU8	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	
0008 81B0h	TPU9	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK	
0008 81B1h	TPU9	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK	
0008 81B2h	TPU9	Timer I/O control register H	TIORH	8	8	2, 3 PCLKB	2 ICLK	
0008 81B3h	TPU9	Timer I/O control register L	TIORL	8	8	2, 3 PCLKB	2 ICLK	
0008 81B4h	TPU9	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK	
0008 81B5h	TPU9	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK	
0008 81B6h	TPU9	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	
0008 81B8h	TPU9	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	
0008 81BAh	TPU9	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	
0008 81BCh	TPU9	Timer general register C	TGRC	16	16	2, 3 PCLKB	2 ICLK	
0008 81BEh	TPU9	Timer general register D	TGRD	16	16	2, 3 PCLKB	2 ICLK	
0008 81C0h	TPU10	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK	
0008 81C1h	TPU10	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK	
0008 81C2h	TPU10	Timer I/O control register	TIOR	8	8	2, 3 PCLKB	2 ICLK	
0008 81C4h	TPU10	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK	
0008 81C5h	TPU10	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK	
0008 81C6h	TPU10	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	
0008 81C8h	TPU10	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	
0008 81CAh	TPU10	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	
0008 81D0h	TPU11	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK	
0008 81D1h	TPU11	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK	
0008 81D2h	TPU11	Timer I/O control register	TIOR	8	8	2, 3 PCLKB	2 ICLK	
0008 81D4h	TPU11	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK	
0008 81D5h	TPU11	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK	
0008 81D6h	TPU11	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	
0008 81D8h	TPU11	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	
0008 81DAh	TPU11	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	
0008 81E6h	PPG0	PPG output control register	PCR	8	8	2, 3 PCLKB	2 ICLK	PPG
0008 81E7h	PPG0	PPG output mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 81E8h	PPG0	Next data enable register H	NDERH	8	8	2, 3 PCLKB	2 ICLK	
0008 81E9h	PPG0	Next data enable register L	NDERL	8	8	2, 3 PCLKB	2 ICLK	
0008 81EAh	PPG0	Output data register H	PODRH	8	8	2, 3 PCLKB	2 ICLK	
0008 81EBh	PPG0	Output data register L	PODRL	8	8	2, 3 PCLKB	2 ICLK	
0008 81ECh ^{*1}	PPG0	Next data register H	NDRH	8	8	2, 3 PCLKB	2 ICLK	
0008 81EDh ^{*2}	PPG0	Next data register L	NDRL	8	8	2, 3 PCLKB	2 ICLK	
0008 81EEh ^{*1}	PPG0	Next data register H	NDRH2	8	8	2, 3 PCLKB	2 ICLK	
0008 81EFh ^{*2}	PPG0	Next data register L	NDRL2	8	8	2, 3 PCLKB	2 ICLK	
0008 81F0h	PPG1	PPG trigger select register	PTRSLR	8	8	2, 3 PCLKB	2 ICLK	
0008 81F6h	PPG1	PPG output control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 81F7h	PPG1	PPG output mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 81F8h	PPG1	Next data enable register H	NDERH	8	8	2, 3 PCLKB	2 ICLK	
0008 81F9h	PPG1	Next data enable register L	NDERL	8	8	2, 3 PCLKB	2 ICLK	
0008 81FAh	PPG1	Output data register H	PODRH	8	8	2, 3 PCLKB	2 ICLK	
0008 81FBh	PPG1	Output data register L	PODRL	8	8	2, 3 PCLKB	2 ICLK	
0008 81FCh ^{*3}	PPG1	Next data register H	NDRH	8	8	2, 3 PCLKB	2 ICLK	PPG
0008 81FDh ^{*4}	PPG1	Next data register L	NDRL	8	8	2, 3 PCLKB	2 ICLK	
0008 81FEh ^{*3}	PPG1	Next data register H	NDRH2	8	8	2, 3 PCLKB	2 ICLK	
0008 81FFh ^{*4}	PPG1	Next data register L	NDRL2	8	8	2, 3 PCLKB	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (44/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
000A 0230h	USB1	Interrupt enable register 0	INTENB0	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 0236h	USB1	BRDY interrupt enable register	BRDYENB	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 0238h	USB1	NRDY interrupt enable register	NRDYENB	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 023Ah	USB1	BEMP interrupt enable register	BEMPENB	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 023Ch	USB1	SOF output configuration register	SOFCFG	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 0240h	USB1	Interrupt status register 0	INTSTS0	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 0246h	USB1	BRDY interrupt status register	BRDYSTS	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 0248h	USB1	NRDY interrupt status register	NRDYSTS	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	USBa
000A 024Ah	USB1	BEMP interrupt status register	BEMPSTS	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 024Ch	USB1	Frame number register	FRMNUM	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	

Table 4.1 List of I/O Registers (Address Order) (45/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK $\geq$ PCLK	ICLK<PCLK	
000A 024Eh	USB1	Device state changing register	DVCHGR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 0250h	USB1	USB address register	USBADDR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 0254h	USB1	USB request type register	USBREQ	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 0256h	USB1	USB request value register	USBVAL	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 0258h	USB1	USB request index register	USBINDX	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 025Ah	USB1	USB request length register	USBLENG	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	USBa
000A 025Ch	USB1	DCP configuration register	DCPCFG	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 025Eh	USB1	DCP maximum packet size register	DCPMAXP	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 0260h	USB1	DCP control register	DCPCTR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 0264h	USB1	Pipe window select register	PIPESEL	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	

5.3.2 Clock Timing

Table 5.12 Clock Timing (Except for Sub-Clock Related)

Conditions: VCC = AVCC0 = VREFH = VCC_USB = V_{BATT} = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0,
VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V, T_a = T_{opr}

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
BCLK pin output cycle time	Packages with 177 to 144 pins	t _{Bcyc}	20	—	—	ns	Figure 5.3	
	Packages with 100 pins or less		40	—	—	ns		
BCLK pin output high pulse width		t _{CH}	5	—	—	ns		
BCLK pin output low pulse width		t _{CL}	5	—	—	ns		
BCLK pin output rising time		t _{Cr}	—	—	5	ns		
BCLK pin output falling time		t _{Cf}	—	—	5	ns		
SDCLK pin output cycle time	only 177 to 144 pin	t _{Bcyc}	20	—	—	ns		
SDCLK pin output high pulse width		t _{CH}	5	—	—	ns		
SDCLK pin output low pulse width		t _{CH}	5	—	—	ns		
SDCLK pin output rising time		t _{CH}	—	—	5	ns		
SDCLK pin output falling time		t _{CH}	—	—	5	ns		
EXTAL external clock input cycle time		t _{EXcyc}	50	—	—	ns		Figure 5.4
EXTAL external clock input high pulse width		t _{EXH}	20	—	—	ns		
EXTAL external clock input low pulse width		t _{EXL}	20	—	—	ns		
EXTAL external clock rising time		t _{EXr}	—	—	5	ns		
EXTAL external clock falling time		t _{EXf}	—	—	5	ns		
EXTAL external clock input wait time*1		t _{EXWT}	1	—	—	ms		
Main clock frequency		f _{MAIN}	4	—	16	MHz	Figure 5.5	
Main clock oscillator start-up time		t _{MAINOSC}	—	—	—*3	ms		
Main clock oscillation stabilization wait time		t _{MAINOSCWT}	—	—	—*4	ms		
LOCO and IWDTCCLK clock cycle time		t _{cyc}	6.96	8	9.4	μs		
LOCO and IWDTCCLK clock oscillation frequency		f _{LOCO}	106.25	125	143.75	kHz		
LOCO and IWDTCCLK clock oscillation stabilization wait time		t _{LOCOWT}	—	—	20	μs	Figure 5.6	
HOCO clock oscillator oscillation frequency		f _{HOCO}	45	50	55	MHz		
HOCO clock oscillation stabilization wait time 1*2		t _{HOCOWT1}	—	—	1.8	ms	Figure 5.7	
HOCO clock oscillation stabilization wait time 2		t _{HOCOWT2}	—	—	2.0	ms	Figure 5.8	
HOCO clock power supply settling time		t _{HOCOP}	—	—	1	ms	Figure 5.9	
PLL clock frequency		f _{PLL}	104	—	200	MHz		
PLL lock time	PLL operation started after main clock oscillation has settled	t _{PLL1}	—	—	500	μs	Figure 5.10	
PLL clock oscillation stabilization wait time		t _{PLLWT1}	—	—	—*5	ms		
PLL lock time	PLL operation started before main clock oscillation has settled	t _{PLL2}	—	—	t _{MAINOSC} + t _{PLL1}	ms	Figure 5.11	
PLL clock oscillation stabilization wait time		t _{PLLWT2}	—	—	—*5	ms		

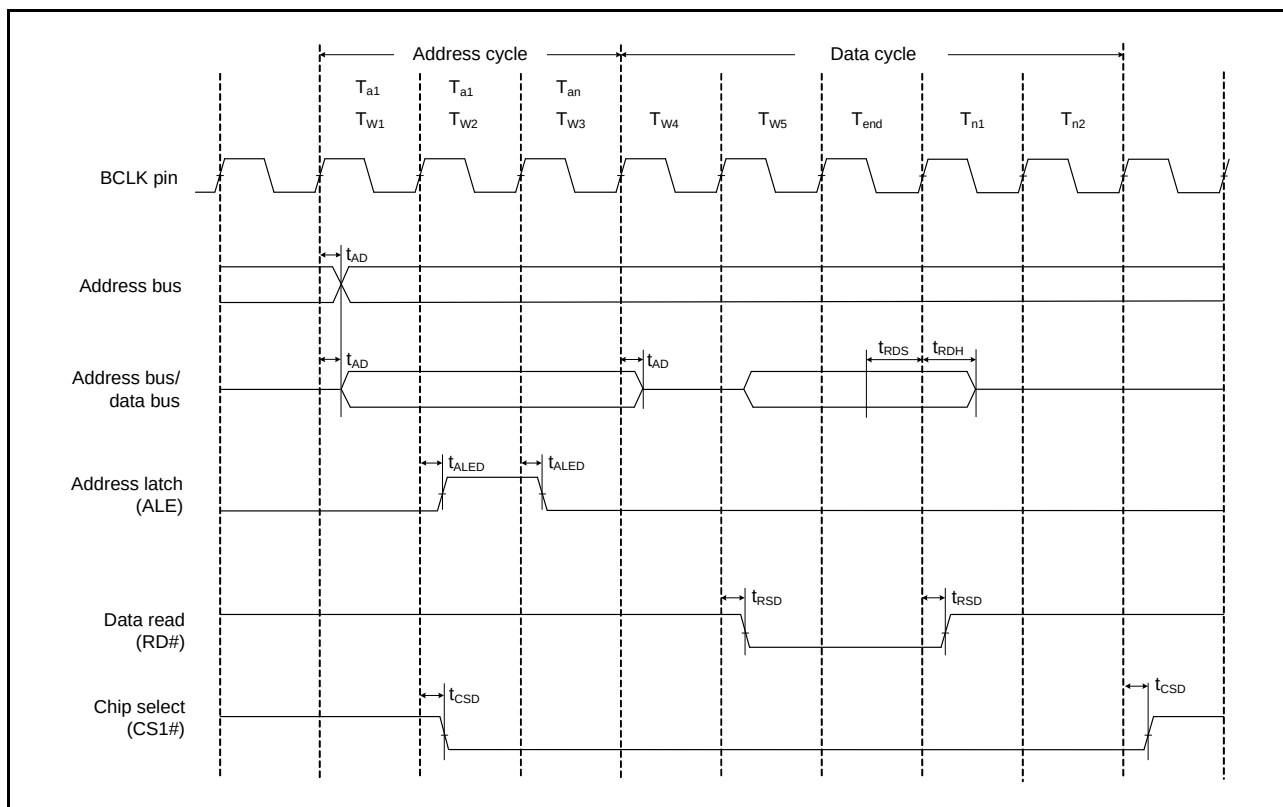


Figure 5.17 Address/Data Multiplexed Bus Read Access Timing

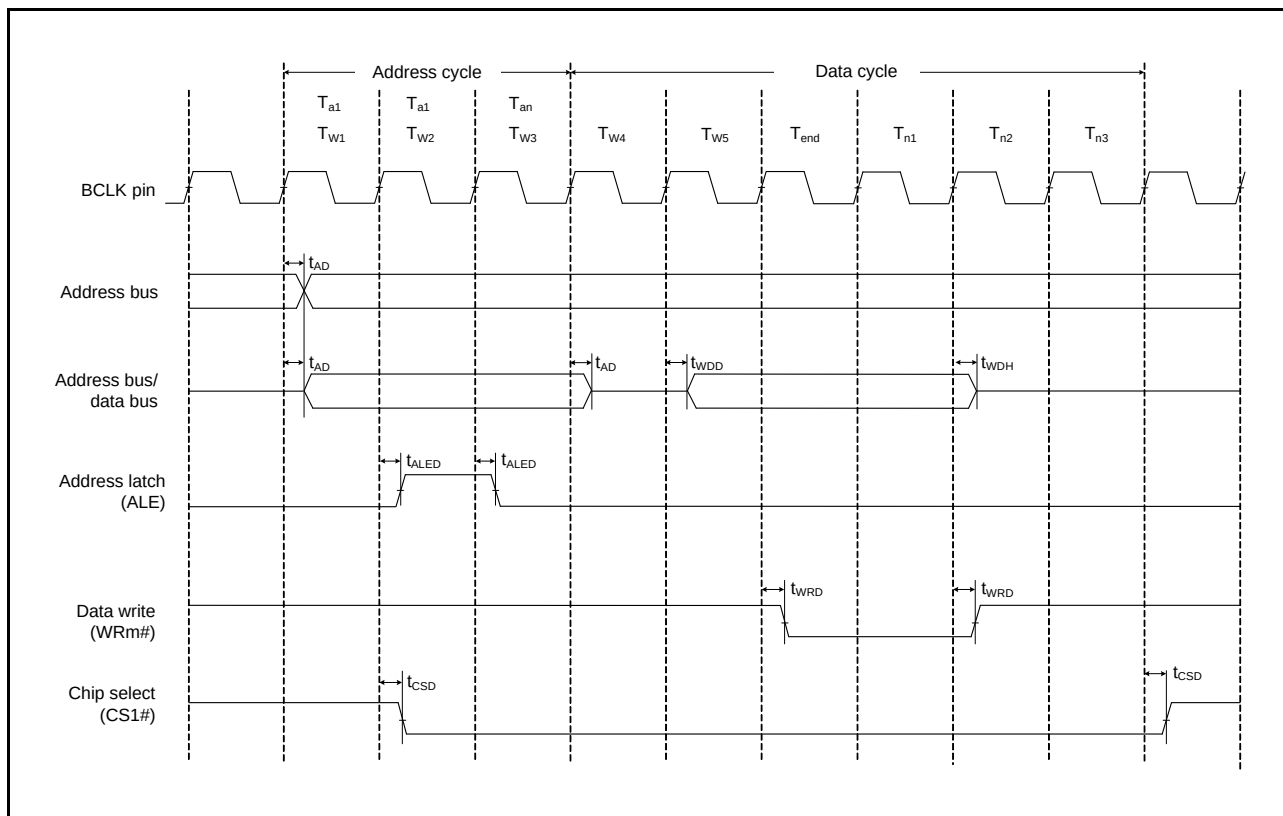


Figure 5.18 Address/Data Multiplexed Bus Write Access Timing

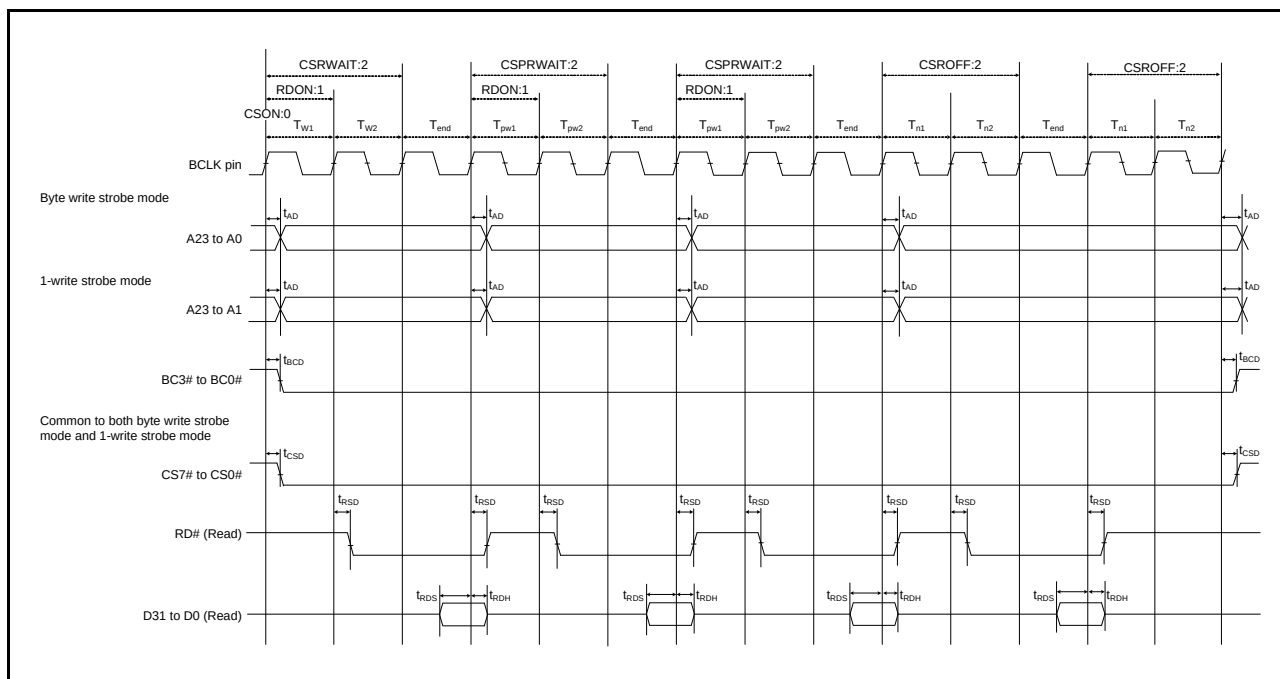


Figure 5.21 External Bus Timing/Page Read Cycle (Bus Clock Synchronized)

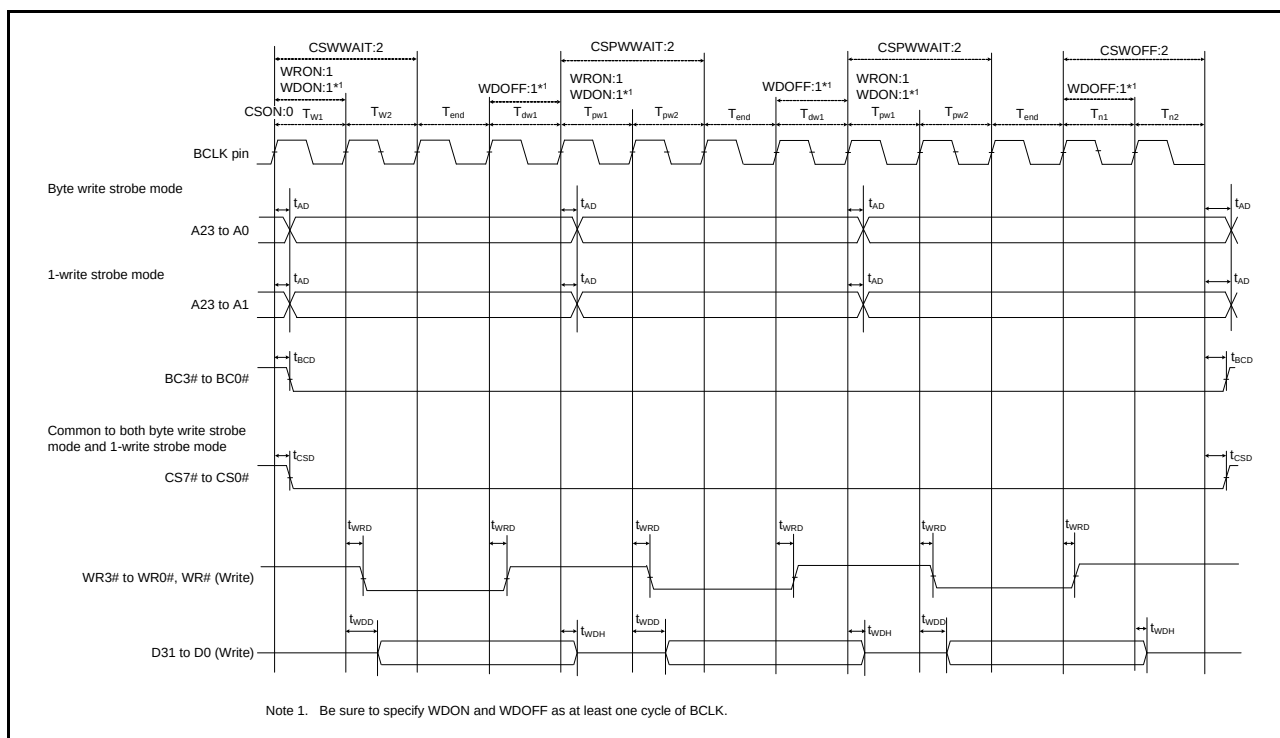


Figure 5.22 External Bus Timing/Page Write Cycle (Bus Clock Synchronized)

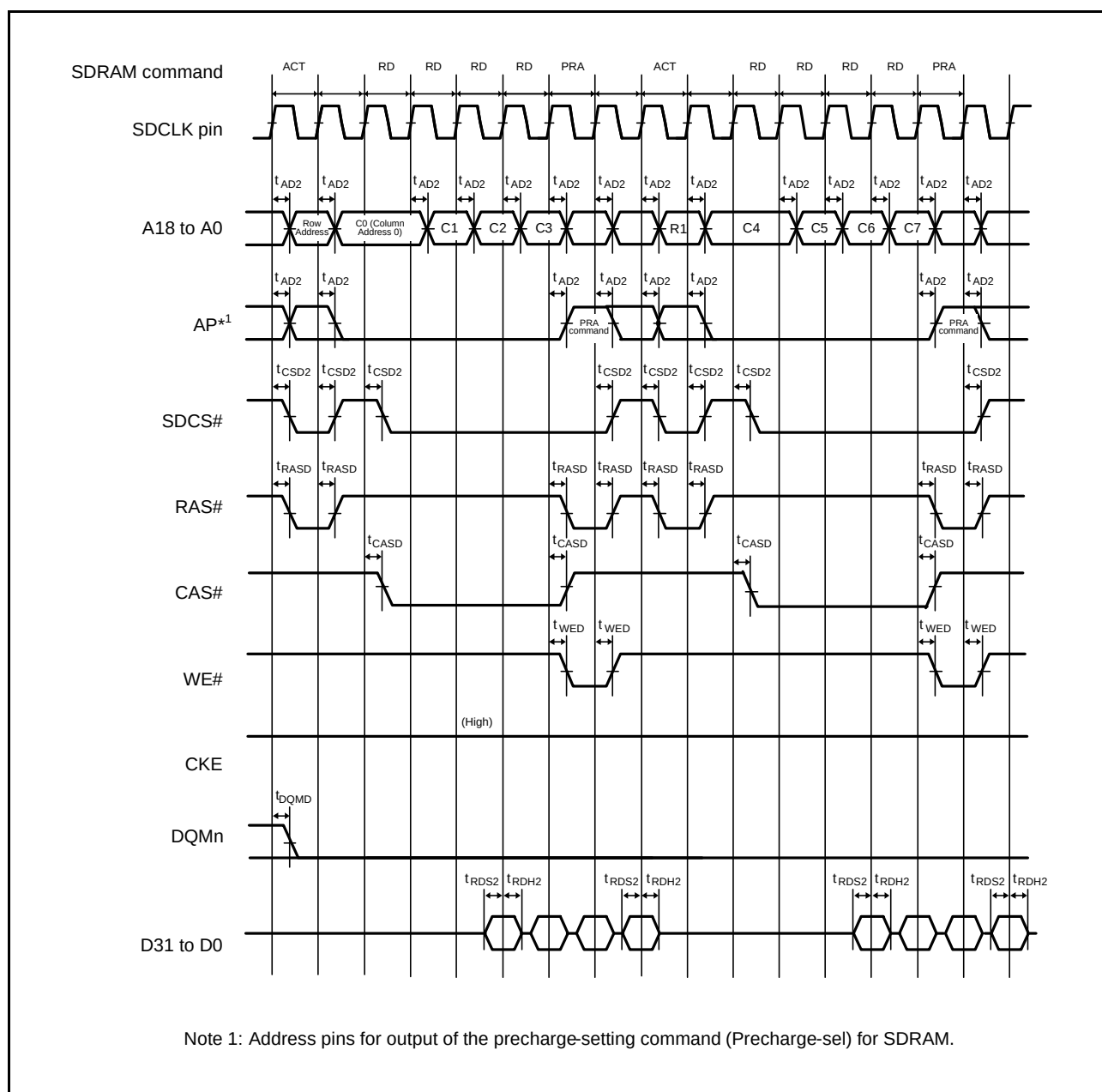
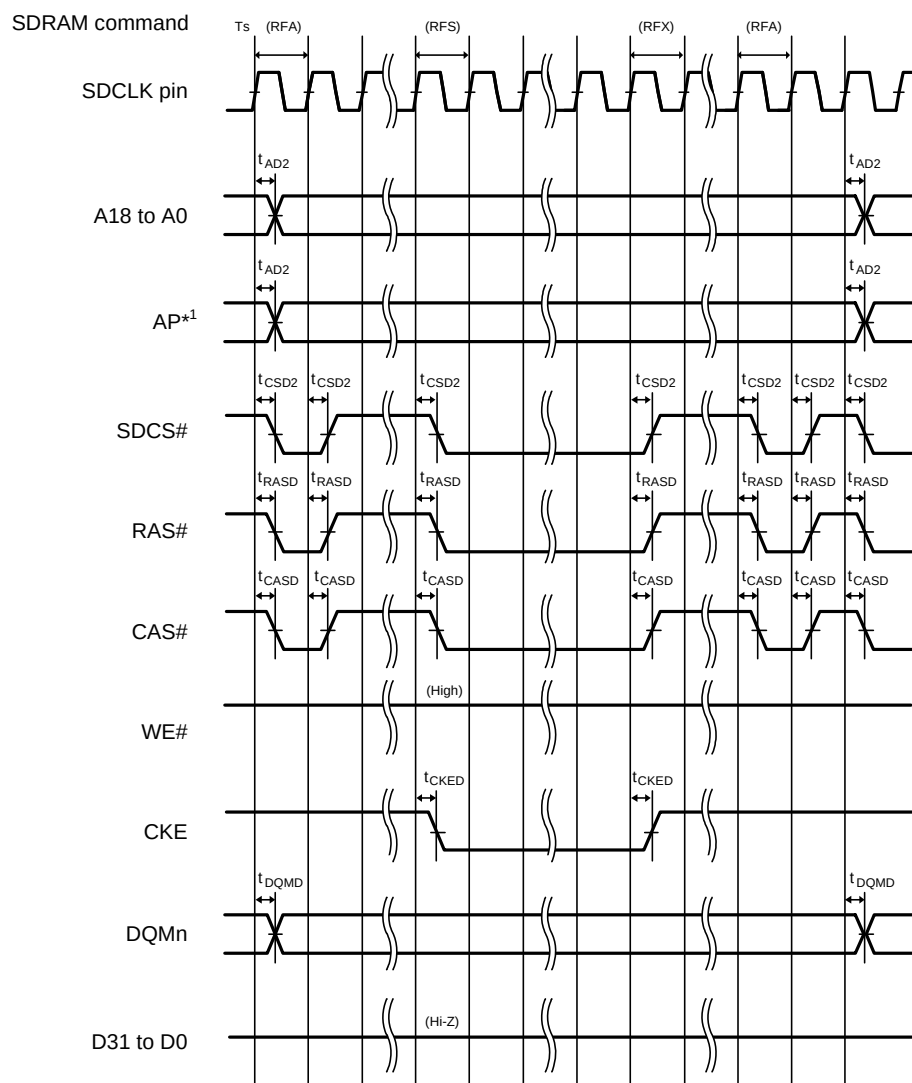


Figure 5.28 SDRAM Space Multiple Read Line Stride Bus Timing



Note 1: Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

Figure 5.30 SDRAM Space Self-Refresh Bus Timing

Table 5.21 Timing of On-Chip Peripheral Modules (3)

Conditions: $V_{CC} = AVCC0 = VREFH = VCC_USB = 2.7$ to 3.6 V*1, $VREFH0 = 2.7$ V to $AVCC0$ *1,
 $VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0$ V,
 $PCLK = 8$ to 50 MHz,
 $T_a = T_{opr}$
 High drive output is selected by the drive capacity control register.

Item				Symbol	Min.	Max.	Unit*2	Test Conditions
RSPI	Data output delay time	Master	Packages with 177 to 144 pins	t_{OD}	—	18	ns	Figure 5.43 to Figure 5.46 C = 30pF
			Packages with 100 pins or less		—	30		
		Slave	Packages with 177 to 144 pins		—	$3 \times t_{Pcyc} + 40$		
			Packages with 100 pins or less		—	$3 \times t_{Pcyc} + 50$		
	Data output hold time	Master		t_{OH}	0	—	ns	
		Slave			0	—		
	Successive transmission delay time	Master		t_{TD}	$t_{SPcyc} + 2 \times t_{Pcyc}$	$8 \times t_{SPcyc} + 2 \times t_{Pcyc}$	ns	
		Slave			$4 \times t_{Pcyc}$	—		
	MOSI and MISO rise/fall time	Output	Packages with 177 to 144 pins	t_{Dr}, t_{Df}	—	5	ns	
			Packages with 100 pins or less		—	10		
		Input			—	1	μs	
	SSL rise/fall time	Output	Packages with 177 to 144 pins	t_{SSLr}, t_{SSLf}	—	5	ns	
			Packages with 100 pins or less		—	10		
		Input			—	1	μs	
Slave access time				t_{SA}	—	4	t_{Pcyc}	Figure 5.45 and Figure 5.46 C = 30pF
Slave output release time				t_{REL}	—	3	t_{Pcyc}	

Note 1. When operation at 3.0 V or a lower voltage is needed, please contact a Renesas sales office.

Note 2. t_{Pcyc} : PCLK cycle

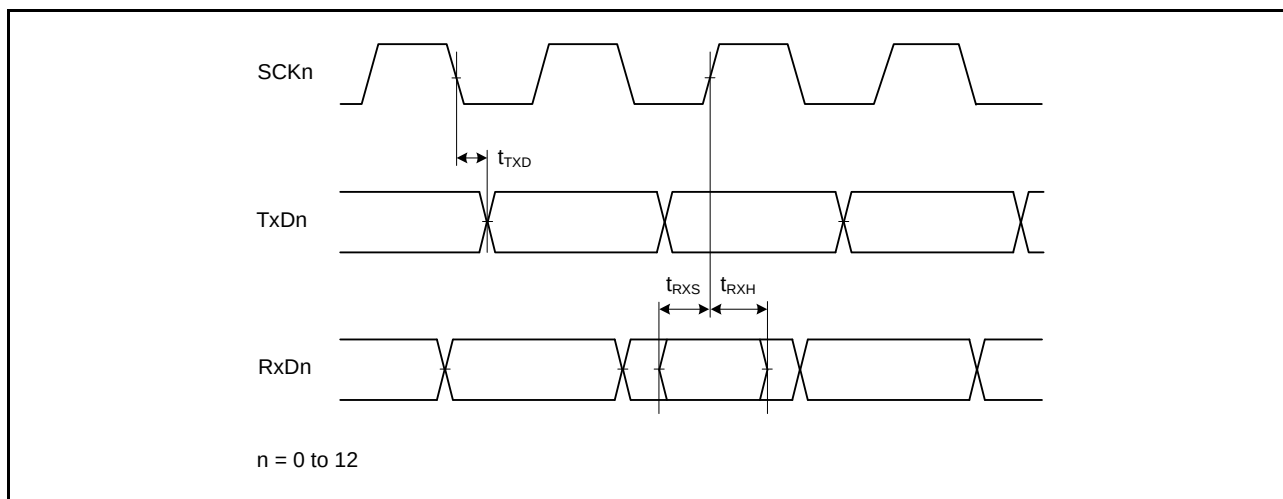


Figure 5.40 SCI Input/Output Timing: Clock Synchronous Mode

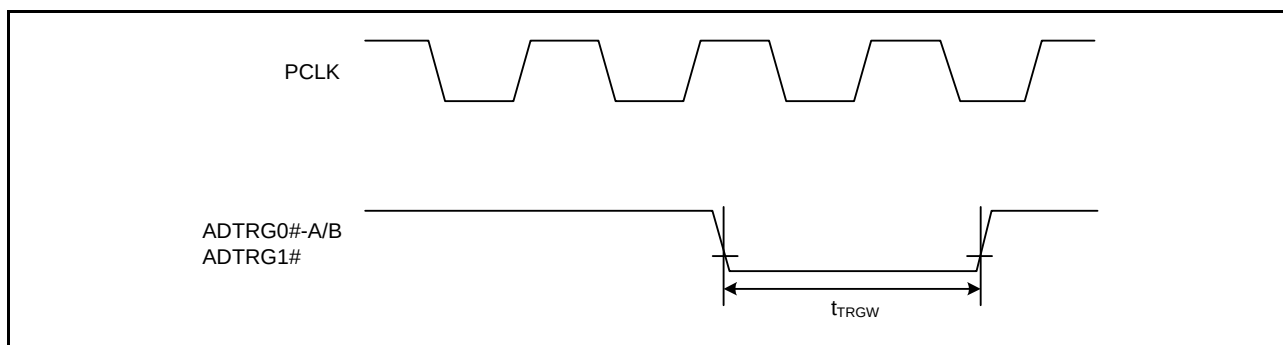


Figure 5.41 A/D Converter External Trigger Input Timing

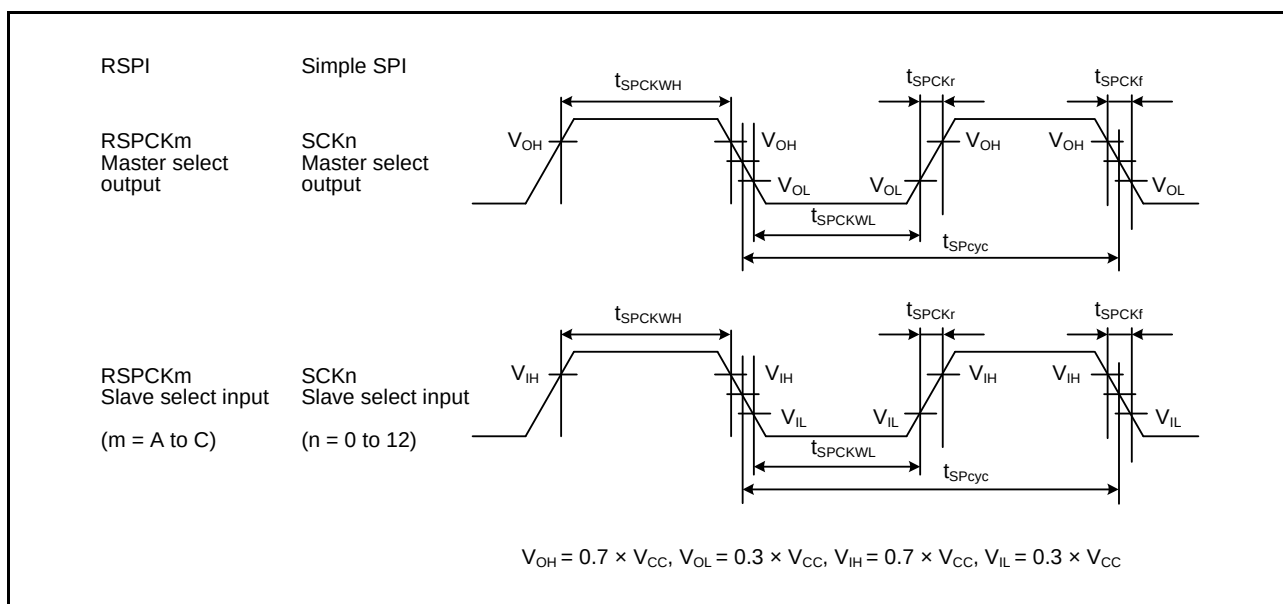


Figure 5.42 RSPI Clock Timing and Simple SPI Clock Timing

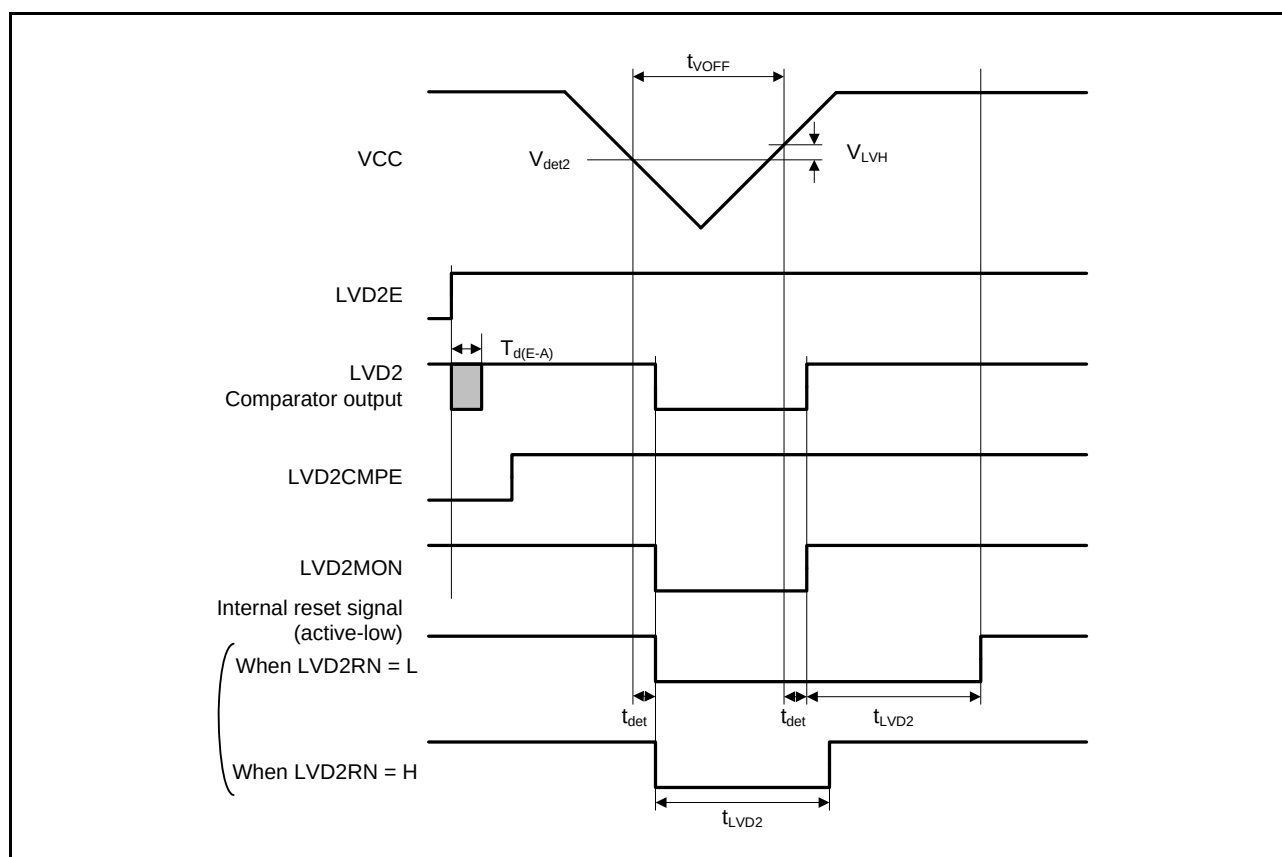


Figure 5.66 Voltage Detection Circuit Timing (V_{det2})

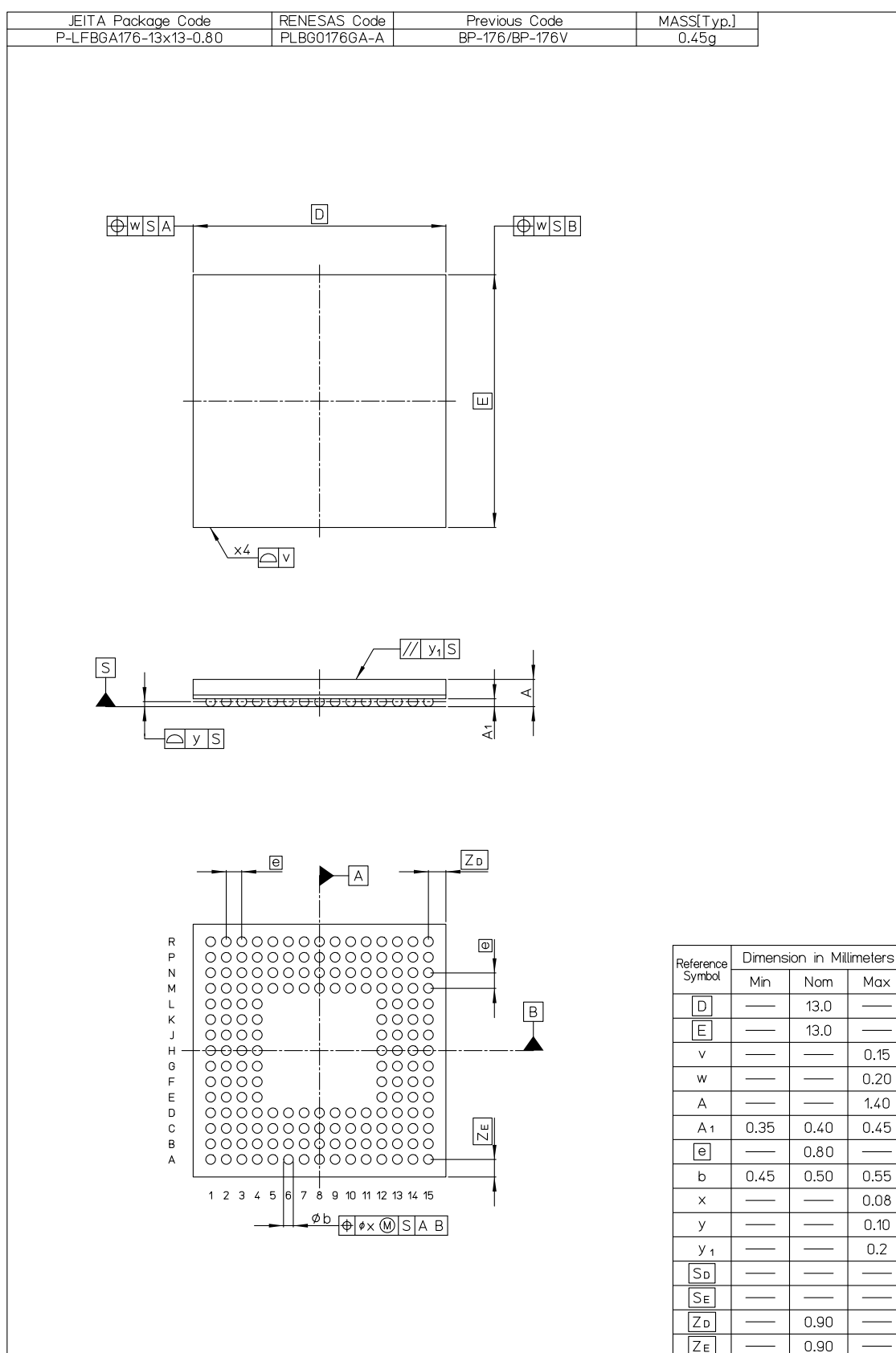


Figure B 176-pin LFBGA (PLBG0176GA-A)

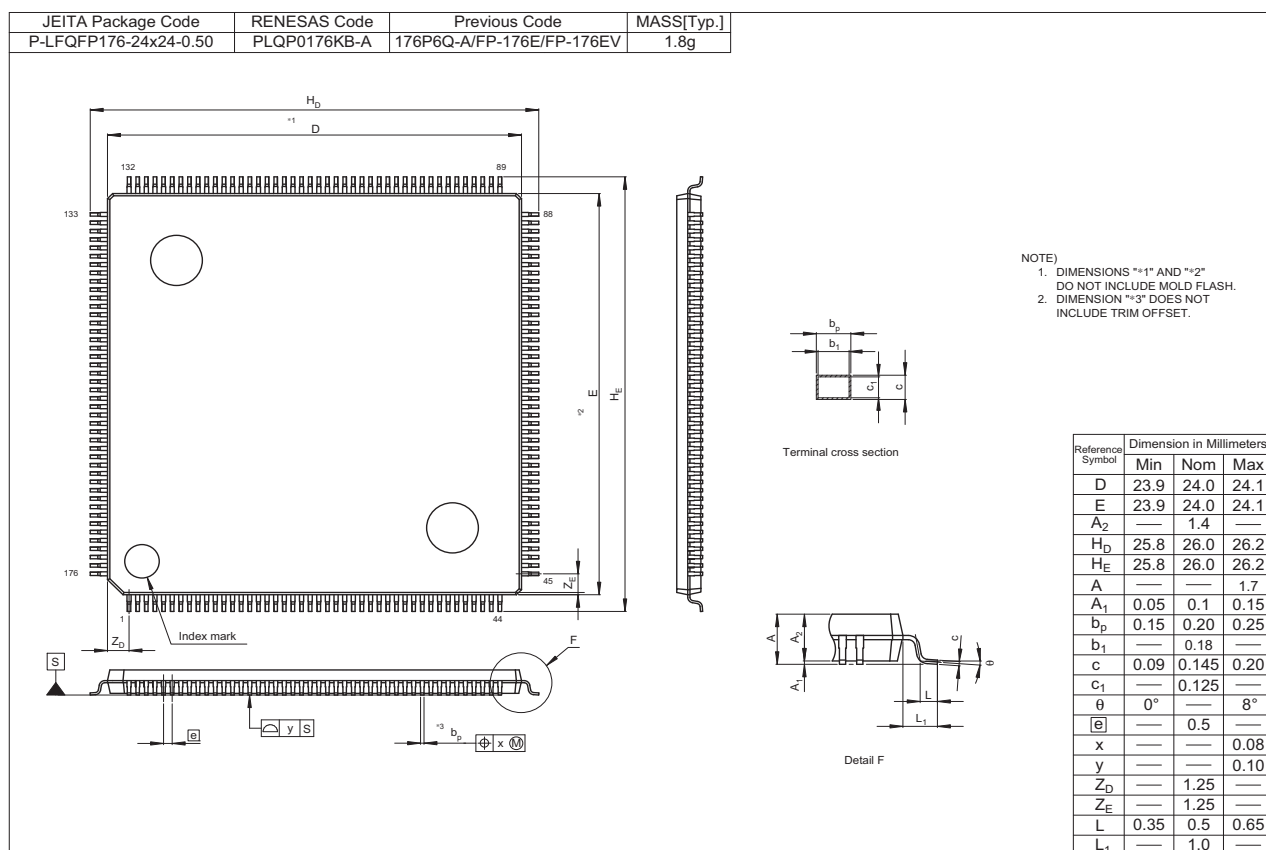


Figure C 176-pin LQFP (PLQP0176KB-A)

REVISION HISTORY	RX63N Group, RX631 Group Datasheet
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Rev.	Date	Description	
		Page	Summary
0.50	May 13, 2011	—	First Edition issued
0.90	Dec 27, 2011	All	— Package added (177-pin TFLGA, 176-pin LFBGA, 145-pin TFLGA), module name changed — Interrupt Controller (ICUb) module name changed 1. Overview 2 to 6 Table 1.1 Outline of Specifications, Reset, Realtime clock, Temperature sensor, Power supply voltage, changed 8 to 10 Table 1.3 List of Products, changed 10 Figure 1.1 How to Read the Product Part No., changed 12 to 17 Table 1.4 Pin Functions, BSCANP pin added 18 Figure 1.3 Pin Assignment (176-Pin TFLGA), added 19 Figure 1.4 Pin Assignment (176-Pin LFBGA), added 20 Figure 1.5 Pin Assignment (176-Pin LQFP), pin 18 changed 21 Figure 1.6 Pin Assignment (144-Pin TFLGA), added 22 Figure 1.7 Pin Assignment (144-Pin LQFP), pin 16 changed 23 Figure 1.8 Pin Assignment (100-Pin LQFP), pin 7 changed 24 to 28 Table 1.5 List of Pins and Pin Functions (177-pin TFLGA, 176-pin LFBGA), added 34 to 38 Table 1.7 List of Pins and Pin Functions (145-Pin TFLGA), added 4. I/O Registers 56 to 99 Table 5.1 List of I/O Registers, changed Appendix 2. Package Dimensions 100 Figure A. 177-pin TFLGA (PTLG0177KA-A), added 101 Figure B. 176-pin LFBGA (PLBG0176GA-A), added 103 Figure D. 145-pin TFLGA (PTLG0145KA-A), added 105 Figure F. 100-pin TFLGA (PTLG0100KA-A), added
1.00	Jun 06, 2012	1. Overview	2 to 6 Table 1.1 Outline of Specifications: CPU, ROM, RAM, E2 DataFlash, clock generation circuit, temperature sensor, power supply voltage, changed. Low power consumption, deleted 8 to 10 Table 1.3 List of Products, changed 11 Figure 1.2 Block Diagram, changed 12 Table 1.4 Pin Functions, description of VCC, changed 24 to 28 Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA): SDRAMC, added to table header; BCLK in pin number line M8, moved to Power Supply Clock System Control column 29 to 33 Table 1.6 List of Pin and Pin Functions (176-Pin LQFP): SDRAMC, added to table header; BCLK in pin number line 68, moved to Power Supply Clock System Control column 34 to 38 Table 1.7 List of Pin and Pin Functions (145-Pin TFLGA): SDRAMC, added to table header; MOSIB, added to pin number line D13; T_ERXD1 in pin number line H12, changed to ET_ERXD1; PO8, added to pin number line J4; BCLK in pin number line K6, moved to Power Supply Clock System Control column 39 to 43 Table 1.8 List of Pins and Pin Functions (144-Pin LQFP): SDRAMC, added to table header; PO8, added to pin number line 29; BCLK in pin number line 53, moved to Power Supply Clock System Control column; T_ERXD1 in pin number 87, changed to ET_ERXD1; MOSIB, added to pin number line 102 44 to 47 Table 1.9 List of Pins and Pin Functions (100-Pin LQFP): BCLK in pin number line 41, moved to Power Supply Clock System Control column 4. I/O Registers 57, 58 Table 4.1, MPU registers, added 5. Electrical Characteristics 105 to 163 Added