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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

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Details

Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I ² C, LINbus, SCI, SPI, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	133
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b, 21x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LFQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f5631wddfc-v0

Table 1.1 Outline of Specifications (5/6)

Classification	Module/Function	Description
Communication function	Ethernet controller (ETHERC)	- Input and output of Ethernet/IEEE 802.3 frames - Transfer at 10 or 100 Mbps - Full- and half-duplex modes - MII (Media Independent Interface) or RMII (Reduced Media Independent Interface) as defined in IEEE 802.3u - Detection of Magic Packets^{TM*1} or output of a "wake-on-LAN" signal (WOL) - Compliance with flow control as defined in IEEE 802.3x standards Note 1. Magic PacketTM is a registered trademark of Advanced Micro Devices, Inc.
	DMA controller for Ethernet controller (EDMAC)	- Alleviation of CPU loads by the descriptor control method - Transmission FIFO: 2 Kbytes; Reception FIFO: 2 Kbytes
	USB 2.0 host/function module (USBa)	- Includes a UDC (USB Device Controller) and transceiver for USB 2.0 - Host/function module: one port, function module: one port - Compliance with the USB 2.0 specification - Transfer rate: Full speed (12 Mbps) - Self-power mode and bus-power mode are selectable - OTG (On the Go) operation is possible - Incorporates 2 Kbytes of RAM as a transfer buffer
	Serial communications interfaces (SCIC, SCId)	13 channels (SCIC: 12 channels + SCId: 1 channel) - SCIC - Serial communications modes: Asynchronous, clock synchronous, and smart-card interface - Multi-processor function - On-chip baud rate generator allows selection of the desired bit rate - Choice of LSB-first or MSB-first transfer - Average transfer rate clock can be input from TMR timers for SCI5, SCI6, and SCI12 - Simple I²C - Simple SPI - SCId (The following functions are added to SCIC) - Supports the serial communications protocol, which contains the start frame and information frame - Supports the LIN format
	I ² C bus interfaces (RIIC)	4 channels (one of them is FM+) - Communication formats - I²C bus format/SMBus format - Supports the multi-master - Max. transfer rate: 1 Mbps (channel 0)
	IEBus (IEB)	1 channel - Supports protocol control for the IEBus - Half-duplex asynchronous transfer - Multi-master operation - Broadcast communications function - Two selectable modes, differentiated by transfer rate
	CAN module (CAN)	3 channels - Compliance with the ISO11898-1 specification (standard frame and extended frame) 32 mailboxes each
	Serial peripheral interfaces (SPI)	3 channels - RSPI transfer facility - Using the MOSI (master out, slave in), MISO (master in, slave out), SSL (slave select), and RSPCK (RSPI clock) signals enables serial transfer through SPI operation (four lines) or clock-synchronous operation (three lines) - Capable of handling serial transfer as a master or slave - Data formats - Switching between MSB first and LSB first - The number of bits in each transfer can be changed to any number of bits from 8 to 16, or to 20, 24, or 32 bits. 128-bit buffers for transmission and reception - Up to four frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits) - Buffered structure - Double buffers for both transmission and reception

Table 1.3 List of Products (3/8)

Group	Part No.	Package	ROM Capacity	RAM Capacity	E2 Data Flash	Operating Frequency (Max.)	Operating Temp. Range
RX63N (D version)	R5F563NYHDFP	PLQP0100KB-A	1 Mbyte	256 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NYDDFP	PLQP0100KB-A	1 Mbyte	256 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NWHDFP	PLQP0100KB-A	1 Mbyte	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NWDDFP	PLQP0100KB-A	1 Mbyte	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NWGDFP	PLQP0100KB-A*1	1 Mbyte	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NWCDFP	PLQP0100KB-A*1	1 Mbyte	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NBCDFP	PLQP0100KB-A	1 Mbyte	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NBDDFP	PLQP0100KB-A	1 Mbyte	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NACDFP	PLQP0100KB-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NADDFP	PLQP0100KB-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
RX63N (G version) *2	R5F563NFHGFC	PLQP0176KB-A	2 Mbytes	256 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NFDGFC	PLQP0176KB-A	2 Mbytes	256 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NKDGFC	PLQP0176KB-A	2 Mbytes	192 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NEDGFC	PLQP0176KB-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NDDGFC	PLQP0176KB-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NYHGFC	PLQP0176KB-A	1 Mbyte	256 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NYDGFC	PLQP0176KB-A	1 Mbyte	256 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NWHGFC	PLQP0176KB-A	1 Mbyte	192 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NWDGFC	PLQP0176KB-A	1 Mbyte	192 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NBDGFC	PLQP0176KB-A	1 Mbyte	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NADGFC	PLQP0176KB-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NFHGF	PLQP0144KA-A	2 Mbytes	256 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NFDGF	PLQP0144KA-A	2 Mbytes	256 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NKDGF	PLQP0144KA-A	2 Mbytes	192 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NEDGF	PLQP0144KA-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NDDGF	PLQP0144KA-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NYHGF	PLQP0144KA-A	1 Mbyte	256 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NYDGF	PLQP0144KA-A	1 Mbyte	256 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NWHGF	PLQP0144KA-A	1 Mbyte	192 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NWDGF	PLQP0144KA-A	1 Mbyte	192 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NBDGF	PLQP0144KA-A	1 Mbyte	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NADGF	PLQP0144KA-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NFHGF	PLQP0100KB-A	2 Mbytes	256 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NFDGF	PLQP0100KB-A	2 Mbytes	256 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NKDGF	PLQP0100KB-A	2 Mbytes	192 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NEDGF	PLQP0100KB-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NDDGF	PLQP0100KB-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NYHGF	PLQP0100KB-A	1 Mbyte	256 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NYDGF	PLQP0100KB-A	1 Mbyte	256 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NWHGF	PLQP0100KB-A	1 Mbyte	192 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NWDGF	PLQP0100KB-A	1 Mbyte	192 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NBDGF	PLQP0100KB-A	1 Mbyte	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NADGF	PLQP0100KB-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
RX631 (D version)	R5F5631ECDLC	PTLG0177KA-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631EDDLC	PTLG0177KA-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C

	A	B	C	D	E	F	G	H	J	K	L	M	N	
13	PE3	PE4	VSS	PE6	P67	PA2	PA4	PA7	PB1	PB5	VSS	VCC	P74	13
12	PE1	PE2	P70	PE5	P65	PA1	VCC	PB0	PB2	PB6	P73	PC1	P75	12
11	P62	P61	PE0	VCC	P66	VSS	PA6	P71	PB4	PB7	PC2	PC0	PC3	11
10	VSS	VCC	P63	PE7	PA0	PA3	PA5	P72	PB3	P76	PC4	P77	P82	10
9	PD6	PD4	PD7	P64	RX63N Group RX631 Group PTLG0145KA-A (145-pin TFLGA) (Top perspective view)					P80	PC5	P81	PC7	9
8	PD2	PD0	PD3	P60						VCC	P83	PC6	VSS	8
7	P92	P91	PD1	PD5						P51	P52	P50	P55	7
6	P90	P47	VSS	P93						P53	P56	VSS_ USB	USB0_ DP	6
5	P45	P43	P46	VCC	P44					P54	P13	VCC_ USB	USB0_ DM	5
4	P42	VREFL0	P41	P01	EMLE	VBATT	BSCANP	P35	P30	P15	P24	P12	P14	4
3	P40	P05	VREFH0	P03	PJ5	PJ3	MD/ FINED	VSS	P32	P31	P16	P86	P87	3
2	P07	AVCC0	P02	PF5	VCL	XCOUT	RES#	VCC	P33	P26	P23	P17	P20	2
1	AVSS0	VREFH	VREFL	P00	VSS	XCIN	XTAL	EXTAL	P34	P27	P25	P22	P21	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	

Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.7, List of Pins and Pin Functions (145-Pin TFLGA).

Figure 1.6 Pin Assignment (145-Pin TFLGA)

Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (2/5)

Pin Number 177-Pin TFLGA 176-Pin LFBGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SCIC, SCID, RSPI, RIIC, CAN, IEB, USB, and PDC)	Interrupt	S12AD, AD, DA
C14	VSS						
C15	SDCLK	P70					
D1		P01		TMC10	RXD6/SMISO6/SSCL6	IRQ9	AN019
D2		P02		TMC11	SCK6	IRQ10	AN020
D3		P03				IRQ11	DA0
D4		P00		TMRI0	TXD6/SMOSI6/SSDA6	IRQ8	AN018
D5		P44				IRQ12-DS	AN004
D6		P93	A19/D19		CTS7#/RTS7#/SS7#		AN017
D7		P95	A21/D21				
D8	VSS						
D9		PD5	D5[A5/D5]	MTIC5W/POE2#	SSLC1	IRQ5	AN013
D10		PD7	D7[A7/D7]	MTIC5U/POE0#	SSLC3	IRQ7	AN7
D11		P61	CS1#/SDCS#				
D12		PE5	D13[A13/D13]	MTIOC4C/MTIOC2B/ TIOCB10	ET_RX_CLK/REF50CK/ RSPCKB	IRQ5	AN3
D13	VCC						
D14		PE7	D15[A15/D15]	TIOCB11	MISOB	IRQ7	AN5
D15		P65	CS5#/CKE				
E1		PJ5					
E2	EMLE						
E3		PF5				IRQ4	
E4	VSS						
E5*1	NC						
E12		PE6	D14[A14/D14]	TIOCA11	MOSIB	IRQ6	AN4
E13	TRDATA0	PG2	D26				
E14	TRDATA1	PG3	D27				
E15		P67	CS7#/DQM1		CRX2*3	IRQ15	
F1	VBATT						
F2	VCL						
F3		PJ3		MTIOC3C	CTS6#/RTS6#/CTS0#/ RTS0#/SS6#/SS0#		
F4	BSCANP						
F12		P66	CS6#/DQM0		CTX2*3		
F13	TRSYNC	PG4	D28				
F14		PA0	A0/BC0#/DQM2	MTIOC4A/TIOCA0/PO16	ET_TX_EN/ RMII_TXD_EN/SSLA1		
F15	VSS						
G1	XCIN						
G2	XCOUT						
G3	MD/FINED						
G4	TRST#	PF4					
G12	TRCLK	PG5	D29				
G13	TRDATA2	PG6	D30				
G14		PA1	A1/DQM3	MTIOC0B/MTCLKC/ TIOCB0/PO17	ET_WOL/SCK5/SSLA2	IRQ11	
G15	VCC						
H1	XTAL	P37					
H2	VSS						

Note 3. Enabled only for the ROM capacity: 2 Mbytes/1.5 Mbytes

Table 1.6 List of Pin and Pin Functions (176-Pin LQFP) (3/5)

Pin Number	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SCIC, SCID, RSPI, RIIC, CAN, IEB, USB, and PDC)	Interrupt	S12AD, AD, DA
72		P50	WR0#/WR#		TXD2/SMOSI2/SSDA2/ SSLB1		
73	VSS						
74		P83	EDACK1	MTIOC4C	ET_CRS/RMII_CRS_DV/ CTS10#/RTS10#/SS10#		
75	VCC						
76		PC7	A23/CS0#	MTIOC3A/MTCLKB/ TIOCB6/TMO2/PO31	ET_COL/TXD8/SMOSI8/ SSDA8/MISOA	IRQ14	
77		PC6	A22/CS1#	MTIOC3C/MTCLKA/ TIOCA6/TMCI2/PO30	ET_ETXD3/RXD8/ SMISO8/SSCL8/MOSIA	IRQ13	
78		PC5	A21/CS2#/ WAIT#	MTIOC3B/MTCLKD/ TIOCD6/TCLKF/TMRI2/ PO29	ET_ETXD2/SCK8/ RSPCKA		
79		P82	EDREQ1	MTIOC4A/PO28	ET_ETXD1/RMII_TXD1/ TXD10/SMOSI10/SSDA10		
80		P81	EDACK0	MTIOC3D/PO27	ET_ETXD0/RMII_TXD0/ RXD10/SMISO10/SSCL10		
81		P80	EDREQ0	MTIOC3B/PO26	ET_TX_EN/ RMII_TXD_EN/SCK10		
82		PC4	A20/CS3#	MTIOC3D/MTCLKC/ TIOCC6/TCLKE/TMCI1/ PO25/POE0#	ET_TX_CLK/SCK5/ CTS8#/RTS8#/SS8#/ SSLA0		
83		PC3	A19	MTIOC4D/TCLKB/PO24	ET_TX_ER/TXD5/ SMOSI5/SSDA5/IETXD		
84		P77	CS7#	PO23	ET_RX_ER/RMII_RX_ER/ TXD11/SMOSI11/SSDA11		
85		P76	CS6#	PO22	ET_RX_CLK/REF50CK/ RXD11/SMISO11/SSCL11		
86		PC2	A18	MTIOC4B/TCLKA/PO21	ET_RX_DV/RXD5/ SMISO5/SSCL5/SSLA3/ IERXD		
87		P75	CS5#	PO20	ET_ERXD0/RMII_RXD0/ SCK11		
88		P74	CS4#	PO19	ET_ERXD1/RMII_RXD1/ CTS11#/RTS11#/SS11#		
89		PC1	A17	MTIOC3A/TCLKD/PO18	ET_ERXD2/SCK5/SSLA2/ SDA3	IRQ12	
90	VCC						
91		PC0	A16	MTIOC3C/TCLKC/PO17	ET_ERXD3/CTS5#/ RTS5#/SS5#/SSLA1/ SCL3	IRQ14	
92	VSS						
93		P73	CS3#	PO16	ET_WOL		
94		PB7	A15	MTIOC3B/TIOCB5/PO31	ET_CRS/RMII_CRS_DV/ TXD9/SMOSI9/SSDA9		
95		PB6	A14	MTIOC3D/TIOCA5/PO30	ET_ETXD1/RMII_TXD1/ RXD9/SMISO9/SSCL9		
96		PB5	A13	MTIOC2A/MTIOC1B/ TIOCB4/TMRI1/PO29/ POE1#	ET_ETXD0/RMII_TXD0/ SCK9		
97		PB4	A12	TIOCA4/PO28	ET_TX_EN/ RMII_TXD_EN/CTS9#/ RTS9#/SS9#		
98		PB3	A11	MTIOC0A/MTIOC4A/ TIOCD3/TCLKD/TMO0/ PO27/POE3#	ET_RX_ER/RMII_RX_ER/ SCK4/SCK6		
99		PB2	A10	TIOCC3/TCLKC/PO26	ET_RX_CLK/REF50CK/ CTS4#/RTS4#/CTS6#/ RTS6#/SS4#/SS6#		

Table 1.8 List of Pins and Pin Functions (144-Pin LQFP) (1/5)

Pin No. 144-pin LQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timers (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SC1c, SC1d, RSPI, RIIC, CAN, IEB, USB, and PDC)	Interrupt	S12AD AD DA
1	AVSS0						
2		P05				IRQ13	DA1
3	VREFH						
4		P03				IRQ11	DA0
5	VREFL						
6		P02		TMC11	SCK6	IRQ10	AN020
7		P01		TMC10	RXD6/SMISO6/SSCL6	IRQ9	AN019
8		P00		TMR10	TXD6/SMOSI6/SSDA6	IRQ8	AN018
9		PF5				IRQ4	
10	EMLE						
11		PJ5					
12	VSS						
13		PJ3		MTIOC3C	CTS6#/RTS6#/CTS0#/ RTS0#/SS6#/SS0#		
14	VCL						
15	VBATT						
16	MD/FINED						
17	XCIN						
18	XCOUT						
19	RES#						
20	XTAL	P37					
21	VSS						
22	EXTAL	P36					
23	VCC						
24		P35				NMI	
25	TRST#	P34		MTIOC0A/TMC13/ PO12/POE2#	SCK6/SCK0/ USB0_DPRPD	IRQ4	
26		P33		MTIOC0D/TIOC0D/ TMR13/PO11/POE3#	RXD6/RXD0/SMISO6/ SMISO0/SSCL6/ SSCL0/CRX0/PCKO	IRQ3-DS	
27		P32		MTIOC0C/TIOC0C/ TMO3/PO10/RTCOUT/ RTCIC2	TXD6/TXD0/SMOSI6/ SMOSI0/SSDA6/ SSDA0/CTX0/ USB0_VBUSEN/ VSYNC	IRQ2-DS	
28	TMS	P31		MTIOC4D/TMC12/PO9/ RTCIC1	CTS1#/RTS1#/SS1#/ SSLB0/USB0_DPUPE	IRQ1-DS	
29	TDI	P30		MTIOC4B/TMR13/PO8/ RTCIC0/POE8#	RXD1/SMISO1/SSCL1/ MISOB/USB0_DRPD	IRQ0-DS	
30	TCK/FINEC	P27	CS7#	MTIOC2B/TMC13/PO7	SCK1/RSPCKB		
31	TDO	P26	CS6#	MTIOC2A/TMO1/PO6	TXD1/CTS3#/RTS3#/ SMOSI1/SS3#/SSDA1/ MOSIB		
32		P25	CS5#/EDACK1	MTIOC4C/MTCLKB/ TIOCA4/PO5	RXD3/SMISO3/SSCL3/ USB0_DPRPD/HSYNC		ADTRG0#
33		P24	CS4#/EDREQ1	MTIOC4A/MTCLKA/ TIOCB4/TMR11/PO4	SCK3/USB0_VBUSEN/ PIXCLK		
34		P23	EDACK0	MTIOC3D/MTCLKD/ TIOC3D/PO3	TXD3/CTS0#/RTS0#/ SMOSI3/SS0#/SSDA3/ USB0_DPUPE/PIXD7		
35		P22	EDREQ0	MTIOC3B/MTCLKC/ TIOCC3/TMO0/PO2	SCK0/USB0_DRPD/ PIXD6		

Table 1.11 List of Pins and Pin Functions (64-Pin TFLGA) (2/2)

Pin No. 64-pin TFLGA	Power Supply Clock System Control	I/O Port	Timers (MTU2a, TPUa, TMR, PPG, RTCa, POE2a)	Communications (SClC, SClD, RSPI, RIIC, CAN, IEB, USB)	Interrupt	S12ADa, DAa
E4	TMS	P16	MTIOC3C/MTIOC3D/ TIOCB1/TCLKC/TMO2/ RTCOUT	TXD1/SMOSI1/SSDA1/ MOSIA/SCL2-DS/IERXD/ USB0_VBUS/ USB0_VBUSEN/ USB0_OVRCURB	IRQ6	ADTRG0#
E5		PC4	MTIOC3D/MTCLKC/TMC1/ PO25/POE0#	SCK5/SSLA0/ USB0_DPRPD		
E6	VCC					
E7	VSS					
E8		PB0	MTIC5W/TIOCA3/PO24	RXD6/SMISO6/SSCL6/ RSPCKA	IRQ12	
F1	VCC					
F2		P35			NMI	
F3		P31	MTIOC4D/TMC12/RTCIC1	CTS1#/RTS1#/SS1#/ SSLB0/USB0_DPUPE	IRQ1-DS	
F4		PC5	MTIOC3B/MTCLKD/TMR12/ PO29	RSPCKA/USB0_ID		
F5		P15	MTIOC0B/MTCLKB/ TIOCB2/TCLKB/TMC12	RXD1/SMISO1/SSCL1/ CRX1-DS/USB1_DPUPE	IRQ5	
F6		PB1	MTIOC0C/MTIOC4C/ TIOCB3/TMC10/PO25	TXD6/SMOSI6/SSDA6	IRQ4-DS	
F7		PB5	MTIOC2A/MTIOC1B/ TIOCB4/TMR11/PO29/ POE1#	SCK9		
F8		PB3	MTIOC0A/MTIOC4A/ TIOC3D/TCLKD/TMO0/ PO27/POE3#	SCK6		
G1	EXTAL	P36				
G2	TDO	P26	MTIOC2A/TMO1	TXD1/SMOSI1/SSDA1/ MOSIB/USB0_VBUSEN		
G3	VCC_USB					
G4	VSS_USB					
G5	VCC_USB					
G6		PC6	MTIOC3C/MTCLKA/TMC12/ PO30	MOSIA/USB0_EXICEN	IRQ13	
G7		PC3	MTIOC4D/TCLKB/PO24	TXD5/SMOSI5/SSDA5/ SDA2/IETXD		
G8		PB6	MTIOC3D/TIOCA5/PO30	RXD9/SMISO9/SSCL9		
H1	XTAL	P37				
H2	TRST#	P17	MTIOC3A/MTIOC3B/ TIOCB0/TCLKD/TMO1/ POE8#	SCK1/MISOA/SDA2-DS/ IETXD/USB1_VBUS	IRQ7	
H3				USB0_DM		
H4				USB0_DP		
H5				USB1_DM		
H6				USB1_DP		
H7		PC2	MTIOC4B/TCLKA/PO21	RXD5/SMISO5/SSCL5/ SSLA3/SCL2/IERXD		
H8		PB7	MTIOC3B/TIOCB5/PO31	TXD9/SMOSI9/SSDA9		

Table 1.12 List of Pins and Pin Functions (64-Pin LQFP) (1/3)

Pin Number 64-Pin LQFP	Power Supply Clock System Control	I/O Port	Timer (MTU2a, TPUa, TMR, PPG, RTCa, POE2a)	Timer Communications (SC1c, SC1d, RSPI, RIIC, CAN, IEB, USB)	Interrupt	S12ADa, DAa
1	EMLE					
2	VCL					
3	MD/FINED					
4	XCIN					
5	XCOUT					
6	RES#					
7	XTAL	P37				
8	VSS					
9	EXTAL	P36				
10	VCC					
11		P35			NMI	
12	VBATT					
13		P31	MTIOC4D/TMC12/PO9/ RTCIC1	CTS1#/RTS1#/SS1#/ SSLB0/USB0_DPUPE	IRQ1-DS	
14	TDI	P30	MTIOC4B/TMRI3/PO8/ POE8#/RTCIC0	RXD1/SMISO1/SSCL1/ MISOB/USB0_DRPD	IRQ0-DS	
15	TCK/FINEC	P27	MTIOC2B/TMC13/PO7	SCK1/RSPCKB		
16	TDO	P26	MTIOC2A/TMO1/PO6	TXD1/SMOSI1/SSDA1/ MOSIB/USB0_VBUSEN		
17	TRST#	P17	MTIOC3A/MTIOC3B/ TIOCB0/TCLKD/TMO1/ PO15/POE8#	SCK1/MISOA/ SDA2-DS/IETXD	IRQ7	
18	TMS	P16	MTIOC3C/MTIOC3D/ TIOCB1/TCLKC/TMO2/ PO14/RTCOUT	TXD1/SMOSI1/SSDA1/ MOSIA/SCL2-DS/IERXD/ USB0_VBUS/ USB0_VBUSEN/ USB0_OVRCURB	IRQ6	ADTRG0#
19		P15	MTIOC0B/MTCLKB/ TIOCB2/TCLKB/TMC12/ PO13	RXD1/SMISO1/SSCL1/ CRX1-DS	IRQ5	
20		P14	MTIOC3A/MTCLKA/ TIOCB5/TCLKA/TMRI2/ PO15	CTS1#/RTS1#/SS1#/ CTX1/USB0_DPUPE/ USB0_OVRCURA	IRQ4	
21	VCC_USB					
22				USB0_DM		
23				USB0_DP		
24	VSS_USB					
25		P55	MTIOC4D/TMO3	CRX1	IRQ10	
26		P54	MTIOC4B/TMC11	CTX1		
27		PC7	MTIOC3A/ MTCLKB/TMO2 /PO31	TXD8/SMOSI8/SSDA8/ MISOA	IRQ14	
28		PC6	MTIOC3C/MTCLKA/ TMC12/PO30	RXD8/SMISO8/SSCL8/ MOSIA/USB0_EXICEN	IRQ13	
29		PC5	MTIOC3B/MTCLKD/ TMRI2/PO29	SCK8/RSPCKA/USB0_ID		
30		PC4	MTIOC3D/MTCLKC/ TMC11/PO25/POE0#	SCK5/CTS8#/RTS8#/SS8#/ SSLA0/USB0_DPRPD		
31		PC3	MTIOC4D/TCLKB/ PO24	TXD5/SMOSI5/SSDA5/ IETXD		

Table 4.1 List of I/O Registers (Address Order) (8/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 70CBh	ICU	Interrupt request register 203	IR203	8	8	2	ICLK	ICUb
0008 70D6h	ICU	Interrupt request register 214	IR214	8	8	2	ICLK	
0008 70D7h	ICU	Interrupt request register 215	IR215	8	8	2	ICLK	
0008 70D8h	ICU	Interrupt request register 216	IR216	8	8	2	ICLK	
0008 70D9h	ICU	Interrupt request register 217	IR217	8	8	2	ICLK	
0008 70DAh	ICU	Interrupt request register 218	IR218	8	8	2	ICLK	
0008 70DBh	ICU	Interrupt request register 219	IR219	8	8	2	ICLK	
0008 70DCh	ICU	Interrupt request register 220	IR220	8	8	2	ICLK	
0008 70DDh	ICU	Interrupt request register 221	IR221	8	8	2	ICLK	
0008 70DEh	ICU	Interrupt request register 222	IR222	8	8	2	ICLK	
0008 70DFh	ICU	Interrupt request register 223	IR223	8	8	2	ICLK	
0008 70E0h	ICU	Interrupt request register 224	IR224	8	8	2	ICLK	
0008 70E1h	ICU	Interrupt request register 225	IR225	8	8	2	ICLK	
0008 70E2h	ICU	Interrupt request register 226	IR226	8	8	2	ICLK	
0008 70E3h	ICU	Interrupt request register 227	IR227	8	8	2	ICLK	
0008 70E4h	ICU	Interrupt request register 228	IR228	8	8	2	ICLK	
0008 70E5h	ICU	Interrupt request register 229	IR229	8	8	2	ICLK	
0008 70E6h	ICU	Interrupt request register 230	IR230	8	8	2	ICLK	
0008 70E7h	ICU	Interrupt request register 231	IR231	8	8	2	ICLK	
0008 70E8h	ICU	Interrupt request register 232	IR232	8	8	2	ICLK	
0008 70E9h	ICU	Interrupt request register 233	IR233	8	8	2	ICLK	
0008 70EAh	ICU	Interrupt request register 234	IR234	8	8	2	ICLK	
0008 70EBh	ICU	Interrupt request register 235	IR235	8	8	2	ICLK	
0008 70ECh	ICU	Interrupt request register 236	IR236	8	8	2	ICLK	
0008 70EDh	ICU	Interrupt request register 237	IR237	8	8	2	ICLK	
0008 70EEh	ICU	Interrupt request register 238	IR238	8	8	2	ICLK	
0008 70EFh	ICU	Interrupt request register 239	IR239	8	8	2	ICLK	
0008 70F0h	ICU	Interrupt request register 240	IR240	8	8	2	ICLK	
0008 70F1h	ICU	Interrupt request register 241	IR241	8	8	2	ICLK	
0008 70F2h	ICU	Interrupt request register 242	IR242	8	8	2	ICLK	
0008 70F3h	ICU	Interrupt request register 243	IR243	8	8	2	ICLK	
0008 70F4h	ICU	Interrupt request register 244	IR244	8	8	2	ICLK	
0008 70F5h	ICU	Interrupt request register 245	IR245	8	8	2	ICLK	
0008 70F6h	ICU	Interrupt request register 246	IR246	8	8	2	ICLK	
0008 70F7h	ICU	Interrupt request register 247	IR247	8	8	2	ICLK	
0008 70F8h	ICU	Interrupt request register 248	IR248	8	8	2	ICLK	
0008 70F9h	ICU	Interrupt request register 249	IR249	8	8	2	ICLK	
0008 70FAh	ICU	Interrupt request register 250	IR250	8	8	2	ICLK	
0008 70FBh	ICU	Interrupt request register 251	IR251	8	8	2	ICLK	
0008 70FCh	ICU	Interrupt request register 252	IR252	8	8	2	ICLK	
0008 70FDh	ICU	Interrupt request register 253	IR253	8	8	2	ICLK	
0008 711Bh	ICU	DTC activation enable register 027	DTCER027	8	8	2	ICLK	
0008 711Ch	ICU	DTC activation enable register 028	DTCER028	8	8	2	ICLK	
0008 711Dh	ICU	DTC activation enable register 029	DTCER029	8	8	2	ICLK	
0008 711Eh	ICU	DTC activation enable register 030	DTCER030	8	8	2	ICLK	
0008 711Fh	ICU	DTC activation enable register 031	DTCER031	8	8	2	ICLK	
0008 7121h	ICU	DTC activation enable register 033	DTCER033	8	8	2	ICLK	
0008 7122h	ICU	DTC activation enable register 034	DTCER034	8	8	2	ICLK	
0008 7124h	ICU	DTC activation enable register 036	DTCER036	8	8	2	ICLK	
0008 7125h	ICU	DTC activation enable register 037	DTCER037	8	8	2	ICLK	
0008 7127h	ICU	DTC activation enable register 039	DTCER039	8	8	2	ICLK	

Table 4.1 List of I/O Registers (Address Order) (34/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 C1B1h	MPC	PE1 pin function control register	PE1PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1B2h	MPC	PE2 pin function control register	PE2PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1B3h	MPC	PE3 pin function control register	PE3PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1B4h	MPC	PE4 pin function control register	PE4PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1B5h	MPC	PE5 pin function control register	PE5PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1B6h	MPC	PE6 pin function control register	PE6PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1B7h	MPC	PE7 pin function control register	PE7PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1B8h	MPC	PF0 pin function control register	PF0PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1B9h	MPC	PF1 pin function control register	PF1PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1BAh	MPC	PF2 pin function control register	PF2PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1BDh	MPC	PF5 pin function control register	PF5PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1D3h	MPC	PJ3 pin function control register	PJ3PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C280h	SYSTEM	Deep standby control register	DPSBYCR	8	8	4, 5 PCLKB	2, 3 ICLK	Low Power Consumption
0008 C282h	SYSTEM	Deep standby interrupt enable register 0	DPSIER0	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C283h	SYSTEM	Deep standby interrupt enable register 1	DPSIER1	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C284h	SYSTEM	Deep standby interrupt enable register 2	DPSIER2	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C285h	SYSTEM	Deep standby interrupt enable register 3	DPSIER3	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C286h	SYSTEM	Deep standby interrupt flag register 0	DPSIFR0	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C287h	SYSTEM	Deep standby interrupt flag register 1	DPSIFR1	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C288h	SYSTEM	Deep standby interrupt flag register 2	DPSIFR2	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C289h	SYSTEM	Deep standby interrupt flag register 3	DPSIFR3	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C28Ah	SYSTEM	Deep standby interrupt edge register 0	DPSIEGR0	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C28Bh	SYSTEM	Deep standby interrupt edge register 1	DPSIEGR1	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C28Ch	SYSTEM	Deep standby interrupt edge register 2	DPSIEGR2	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C28Dh	SYSTEM	Deep standby interrupt edge register 3	DPSIEGR3	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C290h	SYSTEM	Reset status register 0	RSTSR0	8	8	4, 5 PCLKB	2, 3 ICLK	Resets
0008 C291h	SYSTEM	Reset status register 1	RSTSR1	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C293h	SYSTEM	Main clock oscillator forced oscillation control register	MOFCR	8	8	4, 5 PCLKB	2, 3 ICLK	Clock Generation Circuit
0008 C294h	SYSTEM	High-speed on-chip oscillator power supply control register	HOCOPCR	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C296h	FLASH	Flash write erase protection register	FWEPROR	8	8	4, 5 PCLKB	2, 3 ICLK	ROM
0008 C297h	SYSTEM	Voltage monitoring circuit control register	LVCMPCR	8	8	4, 5 PCLKB	2, 3 ICLK	LVDA
0008 C298h	SYSTEM	Voltage detection level select register	LVDLVL	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C29Ah	SYSTEM	Voltage monitoring 1 circuit control register 0	LVD1CR0	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C29Bh	SYSTEM	Voltage monitoring 2 circuit control register 0	LVD2CR0	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C2A0h to 0008 C2BFh	SYSTEM	Deep standby backup register 0 to 31	DPSBKR0 to 31	8	8	4, 5 PCLKB	2, 3 ICLK	Low Power Consumption
0008 C300h	ICU	Group 0 interrupt source register	GRP00	32	32	1 to 2PCLKB	2 ICLK	ICUb
0008 C304h	ICU	Group 1 interrupt source register	GRP01	32	32	1 to 2PCLKB	2 ICLK	
0008 C308h	ICU	Group 2 interrupt source register	GRP02	32	32	1 to 2PCLKB	2 ICLK	
0008 C30Ch	ICU	Group 3 interrupt source register	GRP03	32	32	1 to 2PCLKB	2 ICLK	
0008 C310h	ICU	Group 4 interrupt source register	GRP04	32	32	1 to 2PCLKB	2 ICLK	
0008 C314h	ICU	Group 5 interrupt source register	GRP05	32	32	1 to 2PCLKB	2 ICLK	
0008 C318h	ICU	Group 6 interrupt source register	GRP06	32	32	1 to 2PCLKB	2 ICLK	
0008 C330h	ICU	Group 12 interrupt source register	GRP12	32	32	1 to 2PCLKB	2 ICLK	
0008 C340h	ICU	Group 0 interrupt enable register	GEN00	32	32	1 to 2PCLKB	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (49/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
000C 0100h	ETHERC	ETHERC mode register	ECMR	32	32	5, 6 PCLKA	—	ETHERC
000C 0108h	ETHERC	Receive frame length register	RFLR	32	32	5, 6 PCLKA	—	
000C 0110h	ETHERC	ETHERC status register	ECSR	32	32	5, 6 PCLKA	—	
000C 0118h	ETHERC	ETHERC interrupt permission register	ECSIPR	32	32	5, 6 PCLKA	—	
000C 0120h	ETHERC	PHY interface register	PIR	32	32	5, 6 PCLKA	—	
000C 0128h	ETHERC	PHY status register	PSR	32	32	5, 6 PCLKA	—	
000C 0140h	ETHERC	Random number generation counter upper limit setting register	RDMLR	32	32	5, 6 PCLKA	—	
000C 0150h	ETHERC	IPG register	IPGR	32	32	5, 6 PCLKA	—	
000C 0154h	ETHERC	Automatic PAUSE frame register	APR	32	32	5, 6 PCLKA	—	
000C 0158h	ETHERC	Manual PAUSE frame register	MPR	32	32	5, 6 PCLKA	—	
000C 0160h	ETHERC	PAUSE Frame receive counter register	RFCF	32	32	5, 6 PCLKA	—	
000C 0164h	ETHERC	Automatic PAUSE frame retransmit count register	TPAUSER	32	32	5, 6 PCLKA	—	
000C 0168h	ETHERC	PAUSE frame retransmit counter register	TPAUSECR	32	32	5, 6 PCLKA	—	
000C 016Ch	ETHERC	Broadcast frame receive count setting register	BCFR	32	32	5, 6 PCLKA	—	
000C 01C0h	ETHERC	MAC address high register	MAHR	32	32	5, 6 PCLKA	—	
000C 01C8h	ETHERC	MAC address low register	MALR	32	32	5, 6 PCLKA	—	
000C 01D0h	ETHERC	Transmit retry over counter register	TROCR	32	32	5, 6 PCLKA	—	
000C 01D4h	ETHERC	Delayed collision detect counter register	CDCR	32	32	5, 6 PCLKA	—	
000C 01D8h	ETHERC	Lost carrier counter register	LCCR	32	32	5, 6 PCLKA	—	
000C 01DCh	ETHERC	Carrier not detect counter register	CNDCR	32	32	5, 6 PCLKA	—	
000C 01E4h	ETHERC	CRC error frame receive counter register	CEFCR	32	32	5, 6 PCLKA	—	
000C 01E8h	ETHERC	Frame receive error counter register	FRECR	32	32	5, 6 PCLKA	—	
000C 01ECh	ETHERC	Too-short frame receive counter register	TSFRCR	32	32	5, 6 PCLKA	—	
000C 01F0h	ETHERC	Too-long frame receive counter register	TLFRCR	32	32	5, 6 PCLKA	—	
000C 01F4h	ETHERC	Residual-bit frame receive counter register	RFCR	32	32	5, 6 PCLKA	—	
000C 01F8h	ETHERC	Multicast address frame receive counter register	MAFCR	32	32	5, 6 PCLKA	—	

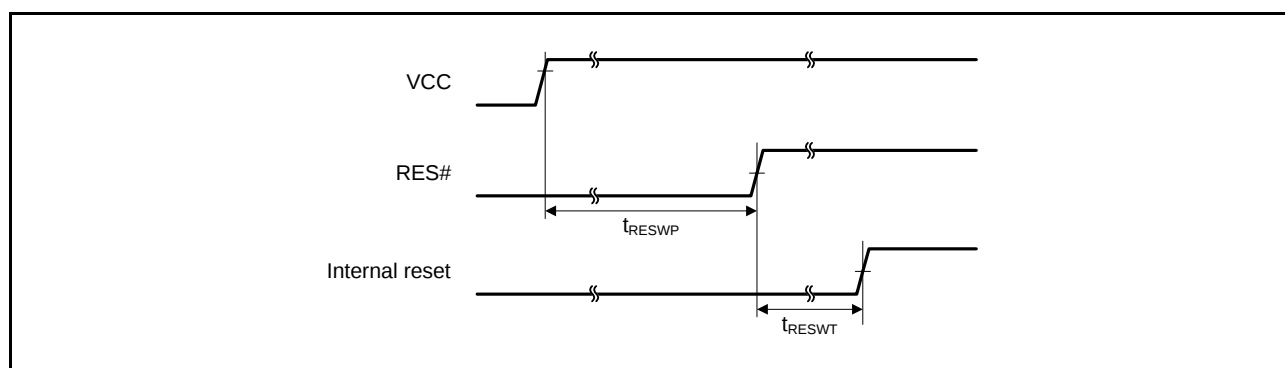


Figure 5.1 Reset Input Timing at Power-On

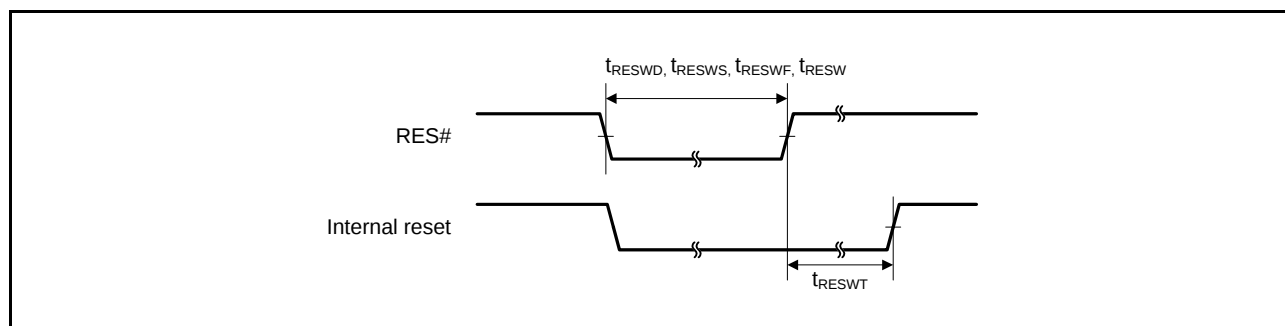


Figure 5.2 Reset Input Timing

5.3.2 Clock Timing

Table 5.12 Clock Timing (Except for Sub-Clock Related)

Conditions: VCC = AVCC0 = VREFH = VCC_USB = V_{BATT} = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0,
VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V, T_a = T_{opr}

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BCLK pin output cycle time	Packages with 177 to 144 pins	t _{Bcyc}	20	—	—	ns	Figure 5.3
	Packages with 100 pins or less		40	—	—	ns	
BCLK pin output high pulse width		t _{CH}	5	—	—	ns	
BCLK pin output low pulse width		t _{CL}	5	—	—	ns	
BCLK pin output rising time		t _{Cr}	—	—	5	ns	
BCLK pin output falling time		t _{Cf}	—	—	5	ns	
SDCLK pin output cycle time	only 177 to 144 pin	t _{Bcyc}	20	—	—	ns	
SDCLK pin output high pulse width		t _{CH}	5	—	—	ns	
SDCLK pin output low pulse width		t _{CH}	5	—	—	ns	
SDCLK pin output rising time		t _{CH}	—	—	5	ns	
SDCLK pin output falling time		t _{CH}	—	—	5	ns	
EXTAL external clock input cycle time		t _{EXcyc}	50	—	—	ns	Figure 5.4
EXTAL external clock input high pulse width		t _{EXH}	20	—	—	ns	
EXTAL external clock input low pulse width		t _{EXL}	20	—	—	ns	
EXTAL external clock rising time		t _{EXr}	—	—	5	ns	
EXTAL external clock falling time		t _{EXf}	—	—	5	ns	
EXTAL external clock input wait time*1		t _{EXWT}	1	—	—	ms	
Main clock frequency		f _{MAIN}	4	—	16	MHz	
Main clock oscillator start-up time		t _{MAINOSC}	—	—	—*3	ms	Figure 5.5
Main clock oscillation stabilization wait time		t _{MAINOSCWT}	—	—	—*4	ms	
LOCO and IWDTCCLK clock cycle time		t _{cyc}	6.96	8	9.4	μs	
LOCO and IWDTCCLK clock oscillation frequency		f _{LOCO}	106.25	125	143.75	kHz	
LOCO and IWDTCCLK clock oscillation stabilization wait time		t _{LOCOWT}	—	—	20	μs	Figure 5.6
HOCO clock oscillator oscillation frequency		f _{HOCO}	45	50	55	MHz	
HOCO clock oscillation stabilization wait time 1*2		t _{HOCOWT1}	—	—	1.8	ms	Figure 5.7
HOCO clock oscillation stabilization wait time 2		t _{HOCOWT2}	—	—	2.0	ms	Figure 5.8
HOCO clock power supply settling time		t _{HOCOP}	—	—	1	ms	Figure 5.9
PLL clock frequency		f _{PLL}	104	—	200	MHz	
PLL lock time	PLL operation started after main clock oscillation has settled	t _{PLL1}	—	—	500	μs	Figure 5.10
PLL clock oscillation stabilization wait time		t _{PLLWT1}	—	—	—*5	ms	
PLL lock time	PLL operation started before main clock oscillation has settled	t _{PLL2}	—	—	t _{MAINOSC} + t _{PLL1}	ms	Figure 5.11
PLL clock oscillation stabilization wait time		t _{PLLWT2}	—	—	—*5	ms	

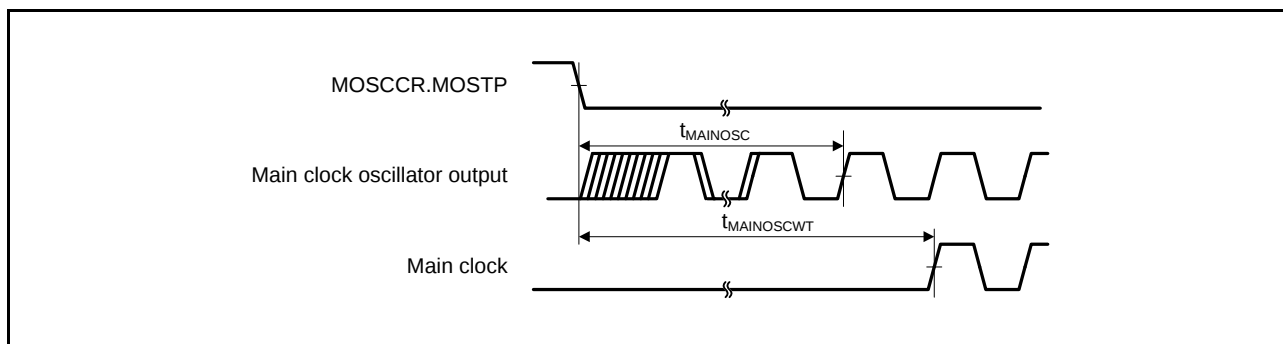


Figure 5.5 Main Clock Oscillation Start Timing

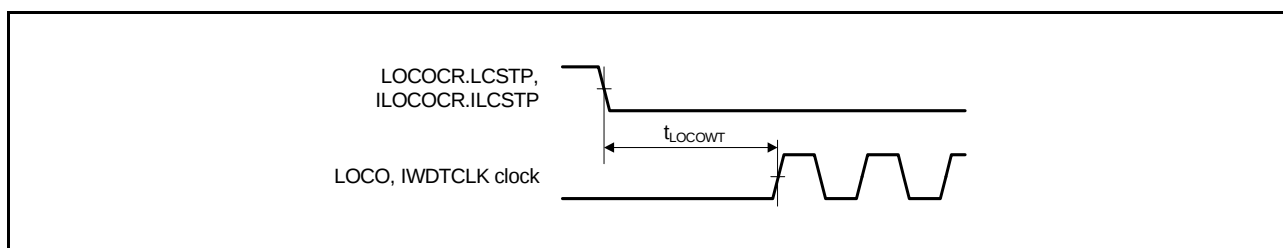


Figure 5.6 LOCO, IWDTCCLK Oscillation Start Timing

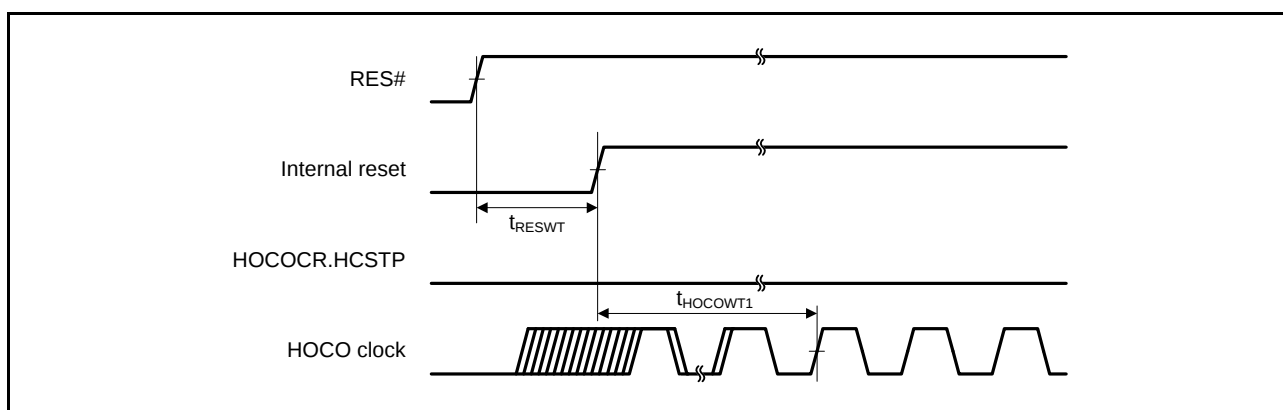


Figure 5.7 HOCO Oscillation Start Timing (After Reset is Canceled by Setting the OFS1.HOCOEN Bit to 0)

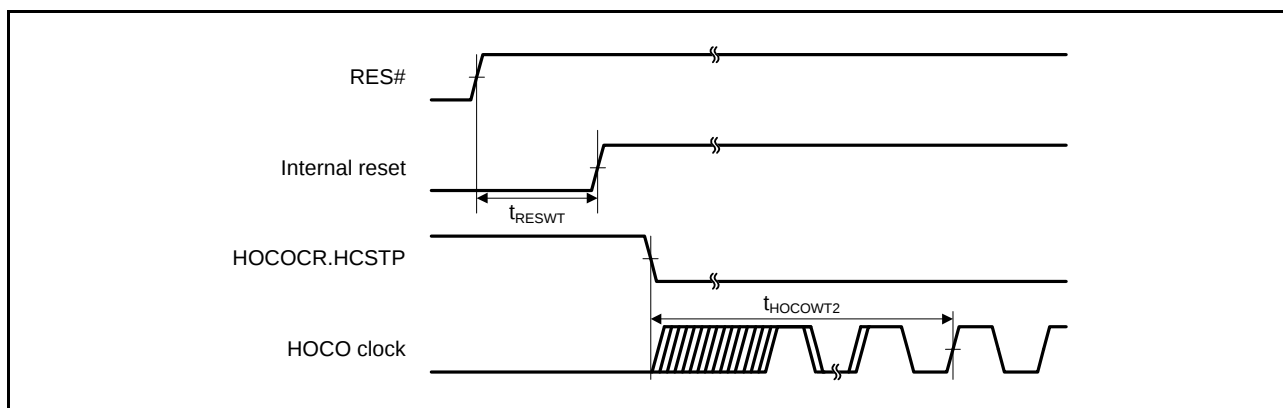


Figure 5.8 HOCO Clock Oscillation Start Timing (Oscillation is Started by Setting the HOCOCR.HCSTP Bit)

5.3.5 Bus Timing

Table 5.16 Bus Timing (packages with 177 to 144 pins)

Conditions: $V_{CC} = AVCC0 = VREFH = VCC_USB = 2.7$ to 3.6 V, $VREFH0 = 2.7$ V to $AVCC0$,
 $VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0$ V,
 $ICLK = 8$ to 100 MHz, $BCLK$ pin = 8 to 50 MHz, $SDCLK$ pin = 8 to 50 MHz, $T_a = T_{opr}$
 Output load conditions: $V_{OH} = VCC \times 0.5$, $V_{OL} = VCC \times 0.5$, $I_{OH} = -1.0$ mA, $I_{OL} = 1.0$ mA, $C = 30$ pF
 High drive output is selected by the drive capacity control register.

Item	Symbol	Min.	Max.	Unit	Test Conditions
Address delay time	t_{AD}	—	15	ns	Figure 5.17 to Figure 5.22
Byte control delay time	t_{BCD}	—	15	ns	
CS# delay time	t_{CSD}	—	15	ns	
ALE delay time	t_{ALED}	—	20	ns	
RD# delay time	t_{RSD}	—	15	ns	
Read data setup time	t_{RDS}	15	—	ns	
Read data hold time	t_{RDH}	0	—	ns	
WR# delay time	t_{WRD}	—	15	ns	
Write data delay time	t_{WDD}	—	15	ns	
Write data hold time	t_{WDH}	0	—	ns	
WAIT# setup time	t_{WTS}	15	—	ns	Figure 5.23
WAIT# hold time	t_{WTH}	0	—	ns	
Address delay time 2 (SDRAM)	t_{AD2}	1	15	ns	Figure 5.24 to Figure 5.30
CS# delay time 2 (SDRAM)	t_{CSD2}	1	15	ns	
DQM delay time (SDRAM)	t_{DQMD}	1	15	ns	
CKE delay time (SDRAM)	t_{CKED}	1	15	ns	
Read data setup time 2 (SDRAM)	t_{RDS2}	12	—	ns	
Read data hold time 2 (SDRAM)	t_{RDH2}	0	—	ns	
Write data delay time 2 (SDRAM)	t_{WDD2}	—	15	ns	
Write data hold time 2 (SDRAM)	t_{WDH2}	1	—	ns	
WE# delay time (SDRAM)	t_{WED}	1	15	ns	
RAS# delay time (SDRAM)	t_{RASD}	1	15	ns	
CAS# delay time (SDRAM)	t_{CASD}	1	15	ns	

Table 5.17 Bus Timing (packages with 100 pins or less)

Conditions: $V_{CC} = AVCC0 = VREFH = VCC_USB = 2.7$ to 3.6 V, $VREFH0 = 2.7$ V to $AVCC0$,

$VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0$ V,

$ICLK = 8$ to 100 MHz, $BCLK$ pin = 8 to 50 MHz, $T_a = T_{opr}$

Output load conditions: $V_{OH} = VCC \times 0.5$, $V_{OL} = VCC \times 0.5$, $I_{OH} = -1.0$ mA, $I_{OL} = 1.0$ mA, $C = 30$ pF

High drive output is selected by the drive capacity control register.

Item	Symbol	Min.	Max.	Unit	Test Conditions
Address delay time	t_{AD}	—	20	ns	Figure 5.17 to Figure 5.22
Byte control delay time	t_{BCD}	—	20	ns	
CS# delay time	t_{CSD}	—	20	ns	
ALE delay time	t_{ALED}	—	20	ns	
RD# delay time	t_{RSD}	—	20	ns	
Read data setup time	t_{RDS}	15	—	ns	
Read data hold time	t_{RDH}	0	—	ns	
WR# delay time	t_{WRD}	—	20	ns	
Write data delay time	t_{WDD}	—	20	ns	
Write data hold time	t_{WDH}	0	—	ns	
WAIT# setup time	t_{WTS}	15	—	ns	Figure 5.23
WAIT# hold time	t_{WTH}	0	—	ns	

Table 5.25 Timing of On-Chip Peripheral Modules (7)

Conditions: VCC = AVCC0 = VREFH = VCC_USB = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0

VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V

ICLK = 12.5 to 100 MHz, T_a = T_{opr}

High drive output is selected by the drive capacity control register.

Item		Symbol	Min.	Max.	Unit	Test Conditions
ETHERC(RMII)	REF50CK cycle time	T _{ck}	20	—	ns	Figure 5.48 to Figure 5.51
	REF50CK frequency Typ. 50 MHz	—	—	50 + 100ppm	MHz	
	REF50CK duty	—	35	65	%	
	REF50CK rise/fall time	T _{ckr/ckf}	0.5	3.5	ns	
	RMII_XXXX*1 output delay time	T _{co}	2.5	15.0	ns	
	RMII_XXXX*2 setup time	T _{su}	3	—	ns	
	RMII_XXXX*2 hold time	T _{hd}	1	—	ns	
	RMII_XXXX*1, *2 rise/fall time	Tr/Tf	0.5	6	ns	
	ET_WOL output delay time	t _{WOLd}	1	23.5	ns	Figure 5.52
ETHERC(MII)	ET_TX_CLK cycle time	t _{Tcyc}	40	—	ns	—
	ET_TX_EN output delay time	t _{TEND}	1	20	ns	Figure 5.53
	ET_ETXD0 to ET_ETXD3 output delay time	t _{MTDd}	1	20	ns	
	ET_CRs setup time	t _{CRSs}	10	—	ns	
	ET_CRs hold time	t _{CRSh}	10	—	ns	
	ET_COL setup time	t _{COLs}	10	—	ns	Figure 5.54
	ET_COL hold time	t _{COLh}	10	—	ns	
	ET_RX_CLK cycle time	t _{TRcyc}	40	—	ns	—
	ET_RX_DV setup time	t _{RDVs}	10	—	ns	Figure 5.55
	ET_RX_DV hold time	t _{RDVh}	10	—	ns	
	ET_ERXD0 to ET_ERXD3 setup time	t _{MRDs}	10	—	ns	
	ET_ERXD0 to ET_ERXD3 hold time	t _{MRDh}	10	—	ns	
	ET_RX_ER setup time	t _{RERs}	10	—	ns	Figure 5.56
	ET_RX_ER hold time	t _{RESh}	10	—	ns	
	ET_WOL output delay time	t _{WOLd}	1	23.5	ns	Figure 5.57

Note 1. RMII_TXD_EN, RMII_TXD1, RMII_TXD0.

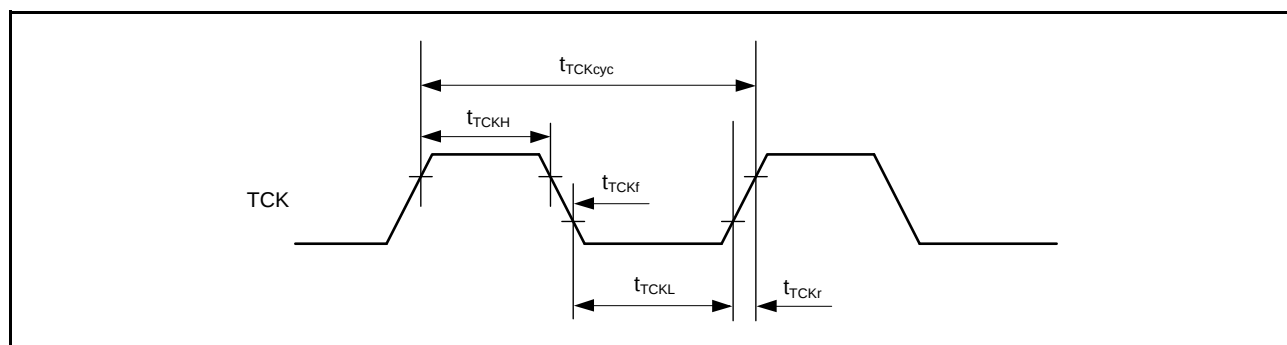
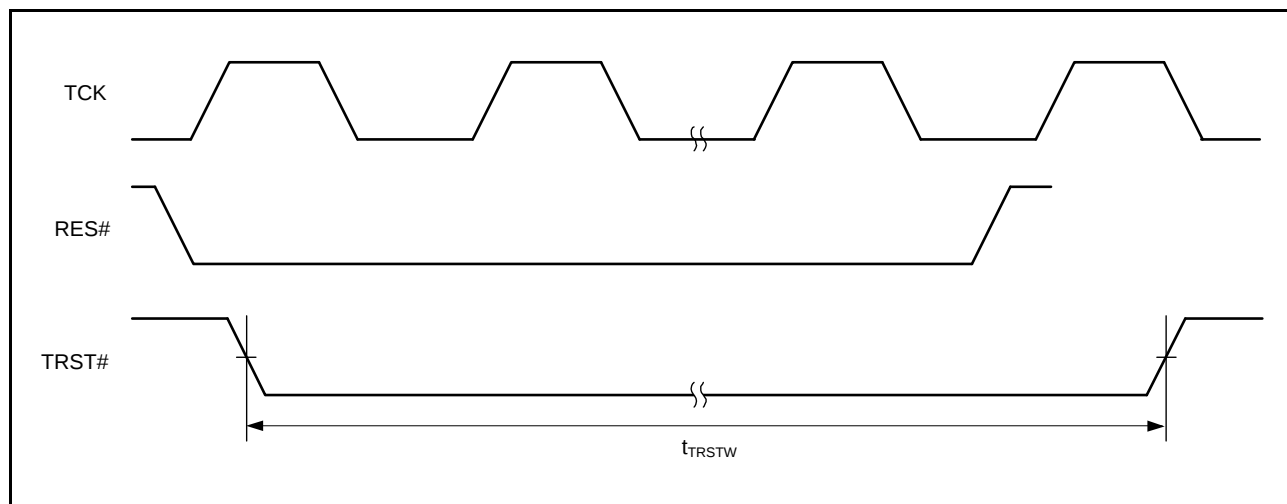
Note 2. RMII_CRs_DV, RMII_RXD1, RMII_RXD0, RMII_RX_ER

5.13 Boundary Scan

Table 5.40 Boundary Scan

Conditions: $V_{CC} = AVCC0 = VREFH = VCC_USB = 2.7$ to $3.6V$, $VREFH0 = 2.7V$ to $AVCC0$
 $VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0V$
 $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
TCK clock cycle time	t_{TCKcyc}	100	—	—	ns	Figure 5.70
TCK clock high pulse width	t_{TCKH}	45	—	—	ns	
TCK clock low pulse width	t_{TCKL}	45	—	—	ns	
TCK clock rise time	t_{TCKr}	—	—	5	ns	
TCK clock fall time	t_{TCKf}	—	—	5	ns	
TRST# pulse width	t_{TRSTW}	20	—	—	t_{TCKcyc}	Figure 5.71
TMS setup time	t_{TMSS}	20	—	—	ns	Figure 5.72
TMS hold time	t_{TMSH}	20	—	—	ns	
TDI setup time	t_{TDIS}	20	—	—	ns	
TDI hold time	t_{TDIH}	20	—	—	ns	
TDO data delay time	t_{TDOD}	—	—	40	ns	


Figure 5.70 Boundary Scan TCK Timing

Figure 5.71 Boundary Scan TRST# Timing

Classifications

- Items with Technical Update document number: Changes according to the corresponding issued Technical Update
- Items without Technical Update document number: Minor changes that do not require Technical Update to be issued

Rev.	Date	Description		Classification
		Page	Summary	
1.80	May 13. 2014	Features		TN-RX*-A092A/J
		1	Operating temp. range chaged, Unique ID added	
		1. Overview		
		2 to 7	Table 1.1 Outline of Specifications: Operating temperature changed, Unique ID and Note 2, added	
		8	Table 1.2 Comparison of Functions for Different Packages: Unique ID, added	
		9 to 16	Table 1.3 List of Products, changed and Note 2, added	
		17	Figure 1.1 How to Read the Product Part Number: Operating temperature range, changed	
		19, 23	Table 1.4 Pin Functions: VBATT and USB power pins, changed	
		3. Address Space		
		76	Figure 3.1 Memory Map in Each Operating Mode, changed	TN-RX*-A081A/E
		77	Figure 3.2 Correspondence between External Address Spaces and CS Areas (In On-Chip ROM Disabled Extended Mode), changed	TN-RX*-A081A/E
		5. Electrical Characteristics		TN-RX*-A097A/J
		130	Table 5.1 Absolute Maximum Ratings: Operating temperature, changed	
		131	Table 5.2 DC Characteristics (1): Note 1, chaged	
		133 to 134	Table 5.4 DC Characteristics (3) (for D and G Versions (-40 ≤ Ta ≤ +85°C)): Title	
		135 to 136	Table 5.5 DC Characteristics (4) (for G Version (-85 < Ta ≤ +105°C)), added	
		1921	Table 5.12 Clock Timing (Except for Sub-Clock Related): LOCO changed to LOCO and IWDTCCLKB	
		144	Figure 5.6 LOCO, IWDTCCLK Clock Oscillation Start Timing, added	
		189	Figure 5.68 Battery Backup Function Characteristics changed	

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