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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Discontinued at Digi-Key
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I ² C, LINbus, SCI, SPI, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	111
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b, 21x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LFQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f5631whdfb-v0

Table 1.1 Outline of Specifications (2/6)

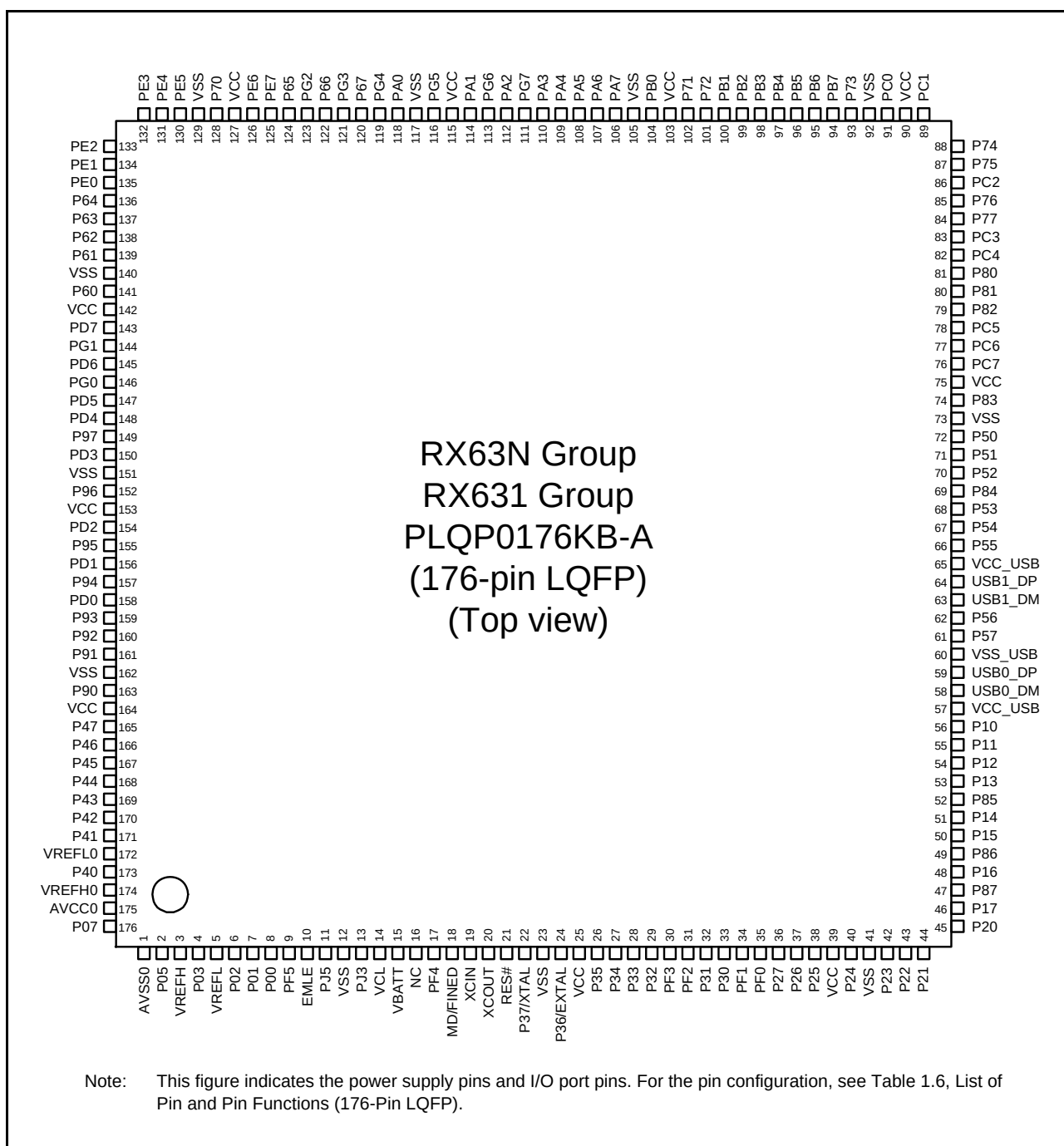
Classification	Module/Function	Description
Low power consumption	Low power consumption facilities	• Module stop function • Four low power consumption modes Sleep mode, all-module clock stop mode, software standby mode, and deep software standby mode • Battery backup function
Interrupt	Interrupt controller (ICUb)	• Peripheral function interrupts: 187 sources • External interrupts: 16 (pins IRQ0 to IRQ15) • Software interrupts: One source • Non-maskable interrupts: 6 sources • Sixteen levels specifiable for the order of priority
External bus extension		• The external address space can be divided into nine areas (CS0 to CS7, SDCS), each with independent control of access settings. Capacity of each area: 16 Mbytes (CS0 to CS7), 128 Mbytes (SDCS) A chip-select signal (CS0# to CS7#, SDCS#) can be output for each area. Each area is specifiable as an 8-, 16-, or 32-bit bus space. The data arrangement in each area is selectable as little or big endian (only for data). • SDRAM interface connectable • Bus format: Separate bus, multiplex bus • Wait control • Write buffer facility
DMA	DMA controller (DMAC)	• 4 channels • Three transfer modes: Normal transfer, repeat transfer, and block transfer • Activation sources: Software trigger, external interrupts, and interrupt requests from peripheral functions
	EXDMA controller (EXDMACa)	• 2 channels • Four transfer modes: Normal transfer, repeat transfer, block transfer, and cluster transfer • Single-address transfer enabled with the EDAKn signal • Capable of direct data transfer to TFT LCD panels • Activation sources: Software trigger, external DMA requests (EDREQn), and interrupt requests from peripheral functions
	Data transfer controller (DTCa)	• Three transfer modes: Normal transfer, repeat transfer, and block transfer • Activation sources: External interrupts and interrupt requests from peripheral functions

Table 1.3 List of Products (4/8)

Group	Part No.	Package	ROM Capacity	RAM Capacity	E2 Data Flash	Operating Frequency (Max.)	Operating Temp. Range
RX631 (D version)	R5F5631DCDLC	PTLG0177KA-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631DDDL	PTLG0177KA-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631BDDL	PTLG0177KA-A	1 Mbyte	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631BCDLC	PTLG0177KA-A	1 Mbyte	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631ACDLC	PTLG0177KA-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631ADDLC	PTLG0177KA-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56318CDLC	PTLG0177KA-A	512 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56318DDL	PTLG0177KA-A	512 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56317CDLC	PTLG0177KA-A	384 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56317DDL	PTLG0177KA-A	384 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56316CDLC	PTLG0177KA-A	256 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56316DDL	PTLG0177KA-A	256 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631ECDBG	PLBG0176GA-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631EDDBG	PLBG0176GA-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631DCDBG	PLBG0176GA-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631DDDBG	PLBG0176GA-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631BCDBG	PLBG0176GA-A	1 Mbyte	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631BDDBG	PLBG0176GA-A	1 Mbyte	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631ACDBG	PLBG0176GA-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631ADDBG	PLBG0176GA-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56318CDBG	PLBG0176GA-A	512 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56318DDBG	PLBG0176GA-A	512 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56317CDBG	PLBG0176GA-A	384 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56317DDBG	PLBG0176GA-A	384 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56316CDBG	PLBG0176GA-A	256 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56316DDBG	PLBG0176GA-A	256 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631FHDFC	PLQP0176KB-A	2 Mbytes	256 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631FDDFC	PLQP0176KB-A	2 Mbytes	256 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631KHDFC	PLQP0176KB-A*1	2 Mbytes	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631KDDFC	PLQP0176KB-A	2 Mbytes	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631ECDFC	PLQP0176KB-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631EDDFC	PLQP0176KB-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631JHDFC	PLQP0176KB-A*1	1.5 Mbytes	256 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631JDDFC	PLQP0176KB-A*1	1.5 Mbytes	256 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631GHDFC	PLQP0176KB-A*1	1.5 Mbytes	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631GDDFC	PLQP0176KB-A*1	1.5 Mbytes	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631DCDFC	PLQP0176KB-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631DDDFC	PLQP0176KB-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631YHDFC	PLQP0176KB-A	1 Mbyte	256 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631YDDFC	PLQP0176KB-A	1 Mbyte	256 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631WHDFC	PLQP0176KB-A	1 Mbyte	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631WDDFC	PLQP0176KB-A	1 Mbyte	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631BCDFC	PLQP0176KB-A	1 Mbyte	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631BDDFC	PLQP0176KB-A	1 Mbyte	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631ACDFC	PLQP0176KB-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C

Table 1.3 List of Products (7/8)

Group	Part No.	Package	ROM Capacity	RAM Capacity	E2 Data Flash	Operating Frequency (Max.)	Operating Temp. Range
RX631 (D version)	R5F5631NDDFM	PLQP0064KB-A	384 Kbytes	64 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631MCDFM	PLQP0064KB-A	256 Kbytes	64 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631MDDFM	PLQP0064KB-A	256 Kbytes	64 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631PCDFL	PLQP0048KB-A	512 Kbytes	64 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631PDDFL	PLQP0048KB-A	512 Kbytes	64 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631NCDFL	PLQP0048KB-A	384 Kbytes	64 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631NDDFL	PLQP0048KB-A	384 Kbytes	64 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631MCDFL	PLQP0048KB-A	256 Kbytes	64 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631MDDFL	PLQP0048KB-A	256 Kbytes	64 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56318SDLC	PTLG0177KA-A	512 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56317SDLC	PTLG0177KA-A	384 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56316SDLC	PTLG0177KA-A	256 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56318SDBG	PLBG0176GA-A*1	512 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56317SDBG	PLBG0176GA-A*1	384 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56316SDBG	PLBG0176GA-A*1	256 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56318SDFC	PLQP0176KB-A*1	512 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56317SDFC	PLQP0176KB-A*1	384 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56316SDFC	PLQP0176KB-A*1	256 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56318SDLK	PTLG0145KA-A	512 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56317SDLK	PTLG0145KA-A	384 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56316SDLK	PTLG0145KA-A	256 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56318SDFB	PLQP144KA-A*1	512 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56317SDFB	PLQP144KA-A*1	384 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56316SDFB	PLQP144KA-A*1	256 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631PFDLH	PTLG0064JA-A	512 Kbytes	64 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631MFDLH	PTLG0064JA-A*1	256 Kbytes	64 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5S56310CDFC	PLQP0176KB-A	0 bytes	128 Kbytes	0 bytes	100 MHz	-40 to +85°C
RX631 (G version) *2	R5F5631FDGFC	PLQP0176KB-A	2 Mbytes	256 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631KDGFC	PLQP0176KB-A	2 Mbytes	192 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631EDGFC	PLQP0176KB-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631DDGFC	PLQP0176KB-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631YDGFC	PLQP0176KB-A	1 Mbyte	256 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631WDGFC	PLQP0176KB-A	1 Mbyte	192 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631BDGFC	PLQP0176KB-A	1 Mbyte	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631ADGFC	PLQP0176KB-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F56318SGFC	PLQP0176KB-A	512 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F56318DGFC	PLQP0176KB-A	512 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F56317SGFC	PLQP0176KB-A	384 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F56317DGFC	PLQP0176KB-A	384 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F56316SGFC	PLQP0176KB-A	256 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F56316DGFC	PLQP0176KB-A	256 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631FDGFB	PLQP0144KA-A	2 Mbytes	256 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631KDGFB	PLQP0144KA-A	2 Mbytes	192 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631EDGFB	PLQP0144KA-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631JDGFB	PLQP0144KA-A	1.5 Mbytes	256 Kbytes	32 Kbytes	100 MHz	-40 to +105°C

**Figure 1.5 Pin Assignment (176-Pin LQFP)**

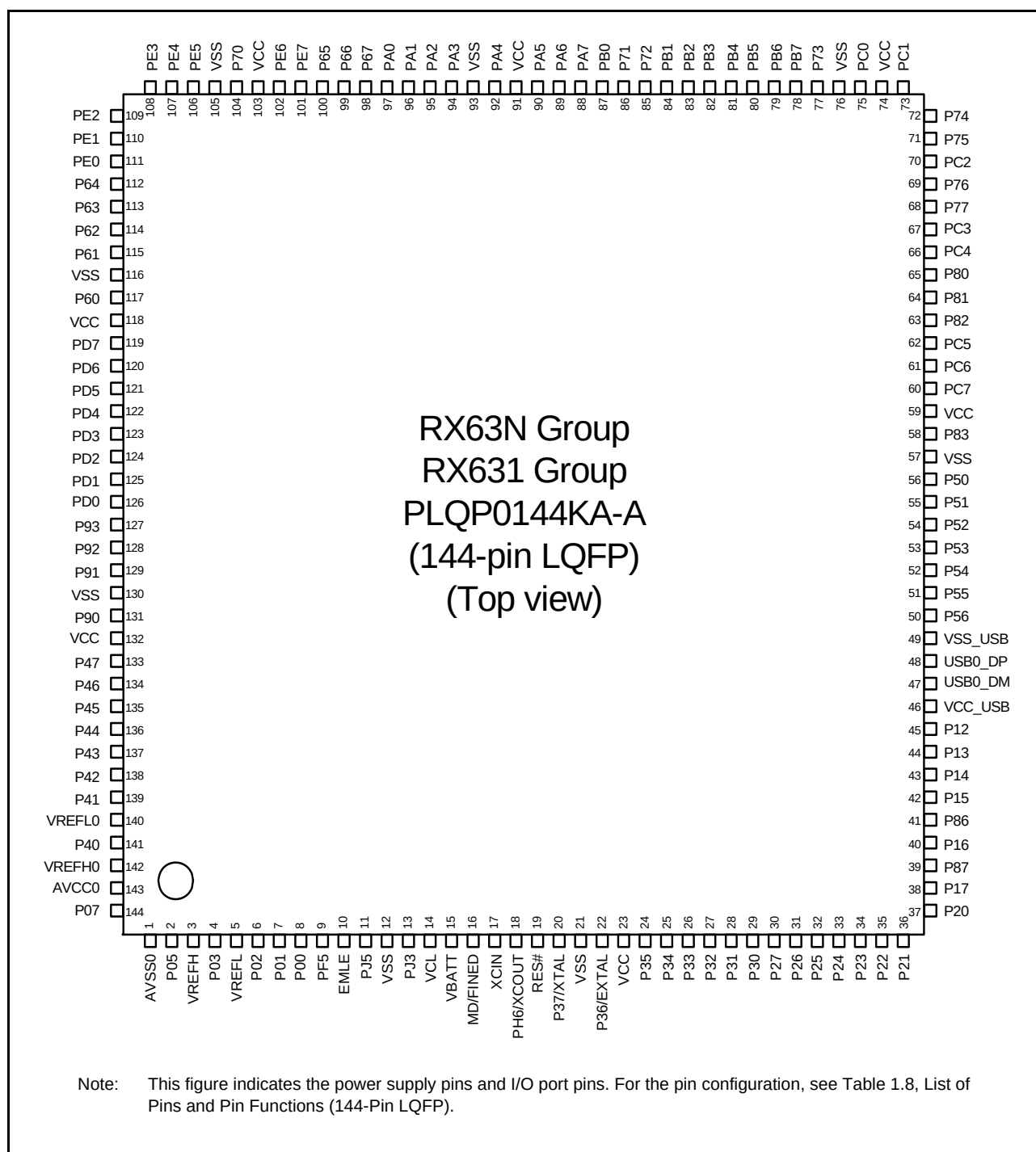
**Figure 1.7 Pin Assignment (144-Pin LQFP)**

Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (3/5)

Pin Number 177-Pin TFLGA 176-Pin LFBGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SC1c, SC1d, RSPI, RIIC, CAN, IEB, USB, and PDC)	Interrupt	S12AD, AD, DA
H3	RES#						
H4		P35				NMI	
H12		PA4	A4	MTIC5U/MTCLKA/ TIOCA1/TMRI0/PO20	ET_MDC/TXD5/SMOSI5/ SSDA5/SSLA0	IRQ5-DS	
H13		PA3	A3	MTIOC0D/MTCLKD/ TIOC0D/TCLKB/PO19	ET_MDIO/RXD5/SMISO5/ SSCL5	IRQ6-DS	
H14		PA2	A2	PO18	RXD5/SMISO5/SSCL5/ SSLA3		
H15	TRDATA3	PG7	D31				
J1	EXTAL	P36					
J2	VCC						
J3		P34		MTIOC0A/TMCI3/PO12/ POE2#	SCK6/SCK0/ USB_DPRPD	IRQ4	
J4	TMS	PF3					
J12		PA5	A5	TIOC0B1/PO21	ET_LINKSTA/RSPCKA		
J13	VSS						
J14		PA7	A7	TIOC0B2/PO23	ET_WOL/MISOA		
J15		PA6	A6	MTIC5V/MTCLKB/ TIOCA2/TMCI3/PO22/ POE2#	ET_EXOUT/CTS5#/ RTS5#SS5#MOSIA		
K1		P33		MTIOC0D/TIOC0D/ TMRI3/PO11/POE3#	RXD6/RXD0/SMISO6/ SMISO0/SSCL6/SSCL0/ CRX0/PCKO	IRQ3-DS	
K2		P32		MTIOC0C/TIOC0C/TMO3/ PO10/RTCOU/RTIC2	TXD6/TXD0/SMOSI6/ SMOSI0/SSDA6/SSDA0/ CTX0/USB0_VBUSEN/ VSYNC	IRQ2-DS	
K3	TDI	PF2			RXD1/SMISO1/SSCL1		
K4	TCK/FINEC	PF1			SCK1		
K12		PB2	A10	TIOC0C3/TCLKC/PO26	ET_RX_CLK/REF50CK/ CTS4#RTS4#CTS6#/ RTS6#SS4#SS6#		
K13		P71	CS1#		ET_MDIO		
K14	VCC						
K15		PB0	A8	MTIC5W/TIOCA3/PO24	ET_ERXD1/RMII_RXD1/ RXD4/RXD6/SMISO4/ SMISO6/SSCL4/SSCL6/ RSPCKA	IRQ12	
L1		P31		MTIOC4D/TMCI2/PO9/ RTIC1	CTS1#RTS1#SS1#/ SSLB0/USB0_DPUPE	IRQ1-DS	
L2		P30		MTIOC4B/TMRI3/PO8/ RTIC0/POE8#	RXD1/SMISO1/SSCL1/ MISOB/USB0_DRPD	IRQ0-DS	
L3	TDO	PF0			TXD1/SMOSI1/SSDA1		
L4		P25	CS5#/EDACK1	MTIOC4C/MTCLKB/ TIOCA4/PO5	RXD3/SMISO3/SSCL3/ USB_DPRPD/HSYNC		ADTRG0#
L12		PB6	A14	MTIOC3D/TIOCA5/PO30	ET_ETXD1/RMII_TXD1/ RXD9/SMISO9/SSCL9		
L13		PB3	A11	MTIOC0A/MTIOC4A/ TIOC0D/TCLKD/TMO0/ PO27/POE3#	ET_RX_ER/RMII_RX_ER/ SCK4/SCK6		
L14		PB1	A9	MTIOC0C/MTIOC4C/ TIOC0B3/TMCI0/PO25	ET_ERXD0/RMII_RXD0/ TXD4/TXD6/SMOSI4/ SMOSI6/SSDA4/SSDA6	IRQ4-DS	
L15		P72	CS2#		ET_MDC		
M1		P27	CS7#	MTIOC2B/TMCI3/PO7	SCK1/RSPCKB		

Table 1.6 List of Pin and Pin Functions (176-Pin LQFP) (3/5)

Pin Number	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SCIC, SCID, RSPI, RIIC, CAN, IEB, USB, and PDC)	Interrupt	S12AD, AD, DA
72		P50	WR0#/WR#		TXD2/SMOSI2/SSDA2/ SSLB1		
73	VSS						
74		P83	EDACK1	MTIOC4C	ET_CRS/RMII_CRS_DV/ CTS10#/RTS10#/SS10#		
75	VCC						
76		PC7	A23/CS0#	MTIOC3A/MTCLKB/ TIOCB6/TMO2/PO31	ET_COL/TXD8/SMOSI8/ SSDA8/MISOA	IRQ14	
77		PC6	A22/CS1#	MTIOC3C/MTCLKA/ TIOCA6/TMCI2/PO30	ET_ETXD3/RXD8/ SMISO8/SSCL8/MOSIA	IRQ13	
78		PC5	A21/CS2#/ WAIT#	MTIOC3B/MTCLKD/ TIOCD6/TCLKF/TMRI2/ PO29	ET_ETXD2/SCK8/ RSPCKA		
79		P82	EDREQ1	MTIOC4A/PO28	ET_ETXD1/RMII_TXD1/ TXD10/SMOSI10/SSDA10		
80		P81	EDACK0	MTIOC3D/PO27	ET_ETXD0/RMII_TXD0/ RXD10/SMISO10/SSCL10		
81		P80	EDREQ0	MTIOC3B/PO26	ET_TX_EN/ RMII_TXD_EN/SCK10		
82		PC4	A20/CS3#	MTIOC3D/MTCLKC/ TIOCC6/TCLKE/TMCI1/ PO25/POE0#	ET_TX_CLK/SCK5/ CTS8#/RTS8#/SS8#/ SSLA0		
83		PC3	A19	MTIOC4D/TCLKB/PO24	ET_TX_ER/TXD5/ SMOSI5/SSDA5/IETXD		
84		P77	CS7#	PO23	ET_RX_ER/RMII_RX_ER/ TXD11/SMOSI11/SSDA11		
85		P76	CS6#	PO22	ET_RX_CLK/REF50CK/ RXD11/SMISO11/SSCL11		
86		PC2	A18	MTIOC4B/TCLKA/PO21	ET_RX_DV/RXD5/ SMISO5/SSCL5/SSLA3/ IERXD		
87		P75	CS5#	PO20	ET_ERXD0/RMII_RXD0/ SCK11		
88		P74	CS4#	PO19	ET_ERXD1/RMII_RXD1/ CTS11#/RTS11#/SS11#		
89		PC1	A17	MTIOC3A/TCLKD/PO18	ET_ERXD2/SCK5/SSLA2/ SDA3	IRQ12	
90	VCC						
91		PC0	A16	MTIOC3C/TCLKC/PO17	ET_ERXD3/CTS5#/ RTS5#/SS5#/SSLA1/ SCL3	IRQ14	
92	VSS						
93		P73	CS3#	PO16	ET_WOL		
94		PB7	A15	MTIOC3B/TIOCB5/PO31	ET_CRS/RMII_CRS_DV/ TXD9/SMOSI9/SSDA9		
95		PB6	A14	MTIOC3D/TIOCA5/PO30	ET_ETXD1/RMII_TXD1/ RXD9/SMISO9/SSCL9		
96		PB5	A13	MTIOC2A/MTIOC1B/ TIOCB4/TMRI1/PO29/ POE1#	ET_ETXD0/RMII_TXD0/ SCK9		
97		PB4	A12	TIOCA4/PO28	ET_TX_EN/ RMII_TXD_EN/CTS9#/ RTS9#/SS9#		
98		PB3	A11	MTIOC0A/MTIOC4A/ TIOCD3/TCLKD/TMO0/ PO27/POE3#	ET_RX_ER/RMII_RX_ER/ SCK4/SCK6		
99		PB2	A10	TIOCC3/TCLKC/PO26	ET_RX_CLK/REF50CK/ CTS4#/RTS4#/CTS6#/ RTS6#/SS4#/SS6#		

Table 1.6 List of Pin and Pin Functions (176-Pin LQFP) (4/5)

Pin Number 176-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SCIC, SCID, RSPI, RIIC, CAN, IEB, USB, and PDC)	Interrupt	S12AD, AD, DA
100		PB1	A9	MTIOC0C/MTIOC4C/ TIOCB3/TMCI0/PO25	ET_ERXD0/RMII_RXD0/ TXD4/TXD6/SMOSI4/ SMOSI6/SSDA4/SSDA6	IRQ4-DS	
101		P72	CS2#		ET_MDC		
102		P71	CS1#		ET_MDIO		
103	VCC						
104		PB0	A8	MTIC5W/TIOCA3/PO24	ET_ERXD1/RMII_RXD1/ RXD4/RXD6/SMISO4/ SMISO6/SSCL4/SSCL6/ RSPCKA	IRQ12	
105	VSS						
106		PA7	A7	TIOCB2/PO23	ET_WOL/MISOA		
107		PA6	A6	MTIC5V/MTCLKB/ TIOCA2/TMCI3/PO22/ POE2#	ET_EXOUT/CTS5#/ RTS5#/SS5#/MOSIA		
108		PA5	A5	TIOCB1/PO21	ET_LINKSTA/RSPCKA		
109		PA4	A4	MTIC5U/MTCLKA/ TIOCA1/TMRI0/PO20	ET_MDC/TXD5/SMOSI5/ SSDA5/SSLA0	IRQ5-DS	
110		PA3	A3	MTIOC0D/MTCLKD/ TIOCD0/TCLKB/PO19	ET_MDIO/RXD5/SMISO5/ SSCL5	IRQ6-DS	
111	TRDATA3	PG7	D31				
112		PA2	A2	PO18	RXD5/SMISO5/SSCL5/ SSLA3		
113	TRDATA2	PG6	D30				
114		PA1	A1/DQM3	MTIOC0B/MTCLKC/ TIOCB0/PO17	ET_WOL/SCK5/SSLA2	IRQ11	
115	VCC						
116	TRCLK	PG5	D29				
117	VSS						
118		PA0	A0/BC0#/DQM2	MTIOC4A/TIOCA0/PO16	ET_TX_EN/ RMII_TXD_EN/SSLA1		
119	TRSYNC	PG4	D28				
120		P67	CS7#/DQM1		CRX2*2	IRQ15	
121	TRDATA1	PG3	D27				
122		P66	CS6#/DQM0		CTX2*2		
123	TRDATA0	PG2	D26				
124		P65	CS5#/CKE				
125		PE7	D15[A15/D15]	TIOCB11	MISOB	IRQ7	AN5
126		PE6	D14[A14/D14]	TIOCA11	MOSIB	IRQ6	AN4
127	VCC						
128	SDCLK	P70					
129	VSS						
130		PE5	D13[A13/D13]	MTIOC4C/MTIOC2B/ TIOCB10	ET_RX_CLK/REF50CK/ RSPCKB	IRQ5	AN3
131		PE4	D12[A12/D12]	MTIOC4D/MTIOC1A/ TIOCA10/PO28	ET_ERXD2/SSLB0		AN2
132		PE3	D11[A11/D11]	MTIOC4B/TIOCB9/PO26/ POE8#	ET_ERXD3/CTS12#/ RTS12#/SS12#/MISOB		AN1
133		PE2	D10[A10/D10]	MTIOC4A/TIOCA9/PO23	RXD12/SMISO12/ SSCL12/RXD12/SSLB3/ MOSIB	IRQ7-DS	AN0
134		PE1	D9[A9/D9]	MTIOC4C/TIOCD9/PO18	TXD12/SMOSI12/ SSDA12/TXD12/ SIOX12/SSLB2/RSPCKB		ANEX1
135		PE0	D8[A8/D8]	TIOCC9	SCK12/SSLB1		ANEX0

Table 1.8 List of Pins and Pin Functions (144-Pin LQFP) (1/5)

Pin No. 144-pin LQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timers (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SC1c, SC1d, RSPI, RIIC, CAN, IEB, USB, and PDC)	Interrupt	S12AD AD DA
1	AVSS0						
2		P05				IRQ13	DA1
3	VREFH						
4		P03				IRQ11	DA0
5	VREFL						
6		P02		TMC11	SCK6	IRQ10	AN020
7		P01		TMC10	RXD6/SMISO6/SSCL6	IRQ9	AN019
8		P00		TMR10	TXD6/SMOSI6/SSDA6	IRQ8	AN018
9		PF5				IRQ4	
10	EMLE						
11		PJ5					
12	VSS						
13		PJ3		MTIOC3C	CTS6#/RTS6#/CTS0#/ RTS0#/SS6#/SS0#		
14	VCL						
15	VBATT						
16	MD/FINED						
17	XCIN						
18	XCOUT						
19	RES#						
20	XTAL	P37					
21	VSS						
22	EXTAL	P36					
23	VCC						
24		P35				NMI	
25	TRST#	P34		MTIOC0A/TMC13/ PO12/POE2#	SCK6/SCK0/ USB0_DPRPD	IRQ4	
26		P33		MTIOC0D/TIOC0D/ TMR13/PO11/POE3#	RXD6/RXD0/SMISO6/ SMISO0/SSCL6/ SSCL0/CRX0/PCKO	IRQ3-DS	
27		P32		MTIOC0C/TIOC0C/ TMO3/PO10/RTCOUT/ RTCIC2	TXD6/TXD0/SMOSI6/ SMOSI0/SSDA6/ SSDA0/CTX0/ USB0_VBUSEN/ VSYNC	IRQ2-DS	
28	TMS	P31		MTIOC4D/TMC12/PO9/ RTCIC1	CTS1#/RTS1#/SS1#/ SSLB0/USB0_DPUPE	IRQ1-DS	
29	TDI	P30		MTIOC4B/TMR13/PO8/ RTCIC0/POE8#	RXD1/SMISO1/SSCL1/ MISOB/USB0_DRPD	IRQ0-DS	
30	TCK/FINEC	P27	CS7#	MTIOC2B/TMC13/PO7	SCK1/RSPCKB		
31	TDO	P26	CS6#	MTIOC2A/TMO1/PO6	TXD1/CTS3#/RTS3#/ SMOSI1/SS3#/SSDA1/ MOSIB		
32		P25	CS5#/EDACK1	MTIOC4C/MTCLKB/ TIOCA4/PO5	RXD3/SMISO3/SSCL3/ USB0_DPRPD/HSYNC		ADTRG0#
33		P24	CS4#/EDREQ1	MTIOC4A/MTCLKA/ TIOCB4/TMR11/PO4	SCK3/USB0_VBUSEN/ PIXCLK		
34		P23	EDACK0	MTIOC3D/MTCLKD/ TIOC3D/PO3	TXD3/CTS0#/RTS0#/ SMOSI3/SS0#/SSDA3/ USB0_DPUPE/PIXD7		
35		P22	EDREQ0	MTIOC3B/MTCLKC/ TIOCC3/TMO0/PO2	SCK0/USB0_DRPD/ PIXD6		

Table 1.9 List of Pins and Pin Functions (100-Pin TFLGA) (2/5)

Pin No. 100-pin TFLGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC	Timers (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SCIC, SCID, RSPI, RIIC, CAN, IEB, USB)	Interrupt	S12AD AD DA
D2	XCOUT						
D3	MD/FINED						
D4	VBATT						
D5		P45				IRQ13-DS	AN005
D6		P46				IRQ14-DS	AN006
D7		PE6	D14[A14/D14]		MOSIB	IRQ6	AN4
D8		PE7	D15[A15/D15]		MISOB	IRQ7	AN5
D9		PA1	A1	MTIOC0B/ MTCLKC/ TIOCBO/PO17	SCK5/SSLA2/ ET_WOL	IRQ11	
D10		PA0	A0/BC0#	MTIOC4A/ TIOCA0/PO16	SSLA1/ET_TX_EN/ RMII_TXD_EN		
E1	XTAL	P37					
E2	VSS						
E3	RES#						
E4	TRST#	P34		MTIOC0A/ TMC13/PO12/ POE2#	SCK6/SCK0/ USB0_DPRPD	IRQ4	
E5		P41				IRQ9-DS	AN001
E6		PA2	A2	PO18	RXD5/SMISO5/ SSCL5/SSLA3		
E7		PA6	A6	MTIC5V/ MTCLKB/ TIOCA2/ TMC13/PO22/ POE2#	CTS5#/RTS5#/ SS5#/MOSIA/ ET_EXOUT		
E8		PA4	A4	MTIC5U/ MTCLKA/ TIOCA1/ TMRI0/PO20	TXD5/SMOSI5/ SSDA5/SSLA0/ ET_MDC	IRQ5-DS	
E9		PA5	A5	TIOCBI/PO21	RSPCKA/ ET_LINKSTA		
E10		PA3	A3	MTIOC0D/ MTCLKD/ TIOCDO/ TCLKB/PO19	RXD5/SMISO5/ SSCL5/ET_MDIO	IRQ6-DS	
F1	EXTAL	P36					
F2	VCC						
F3		P35				NMI	
F4		P32		MTIOC0C/ TIOCC0/TMO3/ PO10/ RTCOUT/ RTCIC2	TXD6/TXD0/ SMOSI6/SMOSI0/ SSDA6/SSDA0/ CTX0*1/ USB0_VBUSEN	IRQ2-DS	
F5		P12		TMC11	RXD2/SMISO2/ SSCL2/SCL0[FM+]	IRQ2	
F6		PB3	A11	MTIOC0A/ MTIOC4A/ TIOCDO/ TCLKD/TMO0/ PO27/POE3#	SCK6/ET_RX_ER/ RMII_RX_ER		

3. Address Space

3.1 Address Space

This LSI has a 4-Gbyte address space, consisting of the range of addresses from 0000 0000h to FFFF FFFFh. That is, linear access to an address space of up to 4 Gbytes is possible, and this contains both program and data areas.

Figure 3.1 shows the memory maps in the respective operating modes. Accessible areas will differ according to the operating mode and states of control bits.

Table 4.1 List of I/O Registers (Address Order) (14/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function	
						ICLK>PCLK	ICLK<PCLK		
0008 7400h	ICU	DMAC activation request select register 0	DMRSR0	8	8	2 ICLK		ICUb	
0008 7404h	ICU	DMAC activation request select register 1	DMRSR1	8	8	2 ICLK			
0008 7408h	ICU	DMAC activation request select register 2	DMRSR2	8	8	2 ICLK			
0008 740Ch	ICU	DMAC activation request select register 3	DMRSR3	8	8	2 ICLK			
0008 7500h	ICU	IRQ control register 0	IRQCR0	8	8	2 ICLK			
0008 7501h	ICU	IRQ control register 1	IRQCR1	8	8	2 ICLK			
0008 7502h	ICU	IRQ control register 2	IRQCR2	8	8	2 ICLK			
0008 7503h	ICU	IRQ control register 3	IRQCR3	8	8	2 ICLK			
0008 7504h	ICU	IRQ control register 4	IRQCR4	8	8	2 ICLK			
0008 7505h	ICU	IRQ control register 5	IRQCR5	8	8	2 ICLK			
0008 7506h	ICU	IRQ control register 6	IRQCR6	8	8	2 ICLK			
0008 7507h	ICU	IRQ control register 7	IRQCR7	8	8	2 ICLK			
0008 7508h	ICU	IRQ control register 8	IRQCR8	8	8	2 ICLK			
0008 7509h	ICU	IRQ control register 9	IRQCR9	8	8	2 ICLK			
0008 750Ah	ICU	IRQ control register 10	IRQCR10	8	8	2 ICLK			
0008 750Bh	ICU	IRQ control register 11	IRQCR11	8	8	2 ICLK			
0008 750Ch	ICU	IRQ control register 12	IRQCR12	8	8	2 ICLK			
0008 750Dh	ICU	IRQ control register 13	IRQCR13	8	8	2 ICLK			
0008 750Eh	ICU	IRQ control register 14	IRQCR14	8	8	2 ICLK			
0008 750Fh	ICU	IRQ control register 15	IRQCR15	8	8	2 ICLK			
0008 7510h	ICU	IRQ pin digital filter enable register 0	IRQFLTE0	8	8	2 ICLK			
0008 7511h	ICU	IRQ pin digital filter enable register 1	IRQFLTE1	8	8	2 ICLK			
0008 7514h	ICU	IRQ pin digital filter setting register 0	IRQFLTC0	16	16	2 ICLK			
0008 7516h	ICU	IRQ pin digital filter setting register 1	IRQFLTC1	16	16	2 ICLK			
0008 7580h	ICU	Non-maskable interrupt status register	NMISR	8	8	2 ICLK			
0008 7581h	ICU	Non-maskable interrupt enable register	NMIER	8	8	2 ICLK			
0008 7582h	ICU	Non-maskable interrupt status clear register	NMICLR	8	8	2 ICLK			
0008 7583h	ICU	NMI pin interrupt control register	NMICR	8	8	2 ICLK			
0008 7590h	ICU	NMI pin digital filter enable register	NMIFLTE	8	8	2 ICLK			
0008 7594h	ICU	NMI pin digital filter setting register	NMIFLTC	16	16	2 ICLK			
0008 8000h	CMT	Compare match timer start register 0	CMSTR0	16	16	2, 3 PCLKB	2 ICLK	CMT	
0008 8002h	CMT0	Compare match timer control register	CMCR	16	16	2, 3 PCLKB	2 ICLK		
0008 8004h	CMT0	Compare match timer counter	CMCNT	16	16	2, 3 PCLKB	2 ICLK		
0008 8006h	CMT0	Compare match timer constant register	CMCOR	16	16	2, 3 PCLKB	2 ICLK		
0008 8008h	CMT1	Compare match timer control register	CMCR	16	16	2, 3 PCLKB	2 ICLK		
0008 800Ah	CMT1	Compare match timer counter	CMCNT	16	16	2, 3 PCLKB	2 ICLK		
0008 800Ch	CMT1	Compare match timer constant register	CMCOR	16	16	2, 3 PCLKB	2 ICLK		
0008 8010h	CMT	Compare match timer start register 1	CMSTR1	16	16	2, 3 PCLKB	2 ICLK		
0008 8012h	CMT2	Compare match timer control register	CMCR	16	16	2, 3 PCLKB	2 ICLK		
0008 8014h	CMT2	Compare match timer counter	CMCNT	16	16	2, 3 PCLKB	2 ICLK		
0008 8016h	CMT2	Compare match timer constant register	CMCOR	16	16	2, 3 PCLKB	2 ICLK		
0008 8018h	CMT3	Compare match timer control register	CMCR	16	16	2, 3 PCLKB	2 ICLK		
0008 801Ah	CMT3	Compare match timer counter	CMCNT	16	16	2, 3 PCLKB	2 ICLK		
0008 801Ch	CMT3	Compare match timer constant register	CMCOR	16	16	2, 3 PCLKB	2 ICLK		
0008 8020h	WDT	WDT refresh register	WDTRR	8	8	2, 3 PCLKB	2 ICLK		WDTA
0008 8022h	WDT	WDT control register	WDTCR	16	16	2, 3 PCLKB	2 ICLK		
0008 8024h	WDT	WDT status register	WDTSR	16	16	2, 3 PCLKB	2 ICLK		
0008 8026h	WDT	WDT reset control register	WDTRCR	8	8	2, 3 PCLKB	2 ICLK		
0008 8030h	IWDT	IWDT refresh register	IWDTRR	8	8	2, 3 PCLKB	2 ICLK		
0008 8032h	IWDT	IWDT control register	IWDTCR	16	16	2, 3 PCLKB	2 ICLK		
0008 8034h	IWDT	IWDT status register	IWDTSR	16	16	2, 3 PCLKB	2 ICLK		

Table 4.1 List of I/O Registers (Address Order) (20/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 8368h	RIIC3	I ² C bus status register 1	ICSR1	8	8	2, 3 PCLKB	2 ICLK	RSPI
0008 8369h	RIIC3	I ² C bus status register 2	ICSR2	8	8	2, 3 PCLKB	2 ICLK	
0008 836Ah	RIIC3	Slave address register L0	SARL0	8	8	2, 3 PCLKB	2 ICLK	
0008 836Bh	RIIC3	Slave address register U0	SARU0	8	8	2, 3 PCLKB	2 ICLK	
0008 836Ch	RIIC3	Slave address register L1	SARL1	8	8	2, 3 PCLKB	2 ICLK	
0008 836Dh	RIIC3	Slave address register U1	SARU1	8	8	2, 3 PCLKB	2 ICLK	
0008 836Eh	RIIC3	Slave address register L2	SARL2	8	8	2, 3 PCLKB	2 ICLK	
0008 836Fh	RIIC3	Slave address register U2	SARU2	8	8	2, 3 PCLKB	2 ICLK	
0008 8370h	RIIC3	I ² C bus bit rate low-level register	ICBRL	8	8	2, 3 PCLKB	2 ICLK	
0008 8371h	RIIC3	I ² C bus bit rate high-level register	ICBRH	8	8	2, 3 PCLKB	2 ICLK	
0008 8372h	RIIC3	I ² C bus transmit data register	ICDRT	8	8	2, 3 PCLKB	2 ICLK	
0008 8373h	RIIC3	I ² C bus receive data register	ICDRR	8	8	2, 3 PCLKB	2 ICLK	
0008 8380h	RSPI0	RSPI control register	SPCR	8	8	2, 3 PCLKB	2 ICLK	
0008 8381h	RSPI0	RSPI slave select polarity register	SSLP	8	8	2, 3 PCLKB	2 ICLK	
0008 8382h	RSPI0	RSPI pin control register	SPPCR	8	8	2, 3 PCLKB	2 ICLK	
0008 8383h	RSPI0	RSPI status register	SPSR	8	8	2, 3 PCLKB	2 ICLK	
0008 8384h	RSPI0	RSPI data register	SPDR	32	16, 32	2, 3 PCLKB	2 ICLK	
0008 8388h	RSPI0	RSPI sequence control register	SPSCR	8	8	2, 3 PCLKB	2 ICLK	
0008 8389h	RSPI0	RSPI sequence status register	SPSSR	8	8	2, 3 PCLKB	2 ICLK	
0008 838Ah	RSPI0	RSPI bit rate register	SPBR	8	8	2, 3 PCLKB	2 ICLK	
0008 838Bh	RSPI0	RSPI data control register	SPDCR	8	8	2, 3 PCLKB	2 ICLK	
0008 838Ch	RSPI0	RSPI clock delay register	SPCKD	8	8	2, 3 PCLKB	2 ICLK	
0008 838Dh	RSPI0	RSPI slave select negation delay register	SSLND	8	8	2, 3 PCLKB	2 ICLK	
0008 838Eh	RSPI0	RSPI next-access delay register	SPND	8	8	2, 3 PCLKB	2 ICLK	
0008 838Fh	RSPI0	RSPI control register 2	SPCR2	8	8	2, 3 PCLKB	2 ICLK	
0008 8390h	RSPI0	RSPI command register 0	SPCMD0	16	16	2, 3 PCLKB	2 ICLK	
0008 8392h	RSPI0	RSPI command register 1	SPCMD1	16	16	2, 3 PCLKB	2 ICLK	
0008 8394h	RSPI0	RSPI command register 2	SPCMD2	16	16	2, 3 PCLKB	2 ICLK	
0008 8396h	RSPI0	RSPI command register 3	SPCMD3	16	16	2, 3 PCLKB	2 ICLK	
0008 8398h	RSPI0	RSPI command register 4	SPCMD4	16	16	2, 3 PCLKB	2 ICLK	
0008 839Ah	RSPI0	RSPI command register 5	SPCMD5	16	16	2, 3 PCLKB	2 ICLK	RSPI
0008 839Ch	RSPI0	RSPI command register 6	SPCMD6	16	16	2, 3 PCLKB	2 ICLK	
0008 839Eh	RSPI0	RSPI command register 7	SPCMD7	16	16	2, 3 PCLKB	2 ICLK	
0008 83A0h	RSPI1	RSPI control register	SPCR	8	8	2, 3 PCLKB	2 ICLK	
0008 83A1h	RSPI1	RSPI slave select polarity register	SSLP	8	8	2, 3 PCLKB	2 ICLK	
0008 83A2h	RSPI1	RSPI pin control register	SPPCR	8	8	2, 3 PCLKB	2 ICLK	
0008 83A3h	RSPI1	RSPI status register	SPSR	8	8	2, 3 PCLKB	2 ICLK	
0008 83A4h	RSPI1	RSPI data register	SPDR	32	16, 32	2, 3 PCLKB	2 ICLK	
0008 83A8h	RSPI1	RSPI sequence control register	SPSCR	8	8	2, 3 PCLKB	2 ICLK	
0008 83A9h	RSPI1	RSPI sequence status register	SPSSR	8	8	2, 3 PCLKB	2 ICLK	
0008 83AAh	RSPI1	RSPI bit rate register	SPBR	8	8	2, 3 PCLKB	2 ICLK	
0008 83ABh	RSPI1	RSPI data control register	SPDCR	8	8	2, 3 PCLKB	2 ICLK	
0008 83ACh	RSPI1	RSPI clock delay register	SPCKD	8	8	2, 3 PCLKB	2 ICLK	
0008 83ADh	RSPI1	RSPI slave select negation delay register	SSLND	8	8	2, 3 PCLKB	2 ICLK	
0008 83AEh	RSPI1	RSPI next-access delay register	SPND	8	8	2, 3 PCLKB	2 ICLK	
0008 83AFh	RSPI1	RSPI control register 2	SPCR2	8	8	2, 3 PCLKB	2 ICLK	
0008 83B0h	RSPI1	RSPI command register 0	SPCMD0	16	16	2, 3 PCLKB	2 ICLK	
0008 83B2h	RSPI1	RSPI command register 1	SPCMD1	16	16	2, 3 PCLKB	2 ICLK	
0008 83B4h	RSPI1	RSPI command register 2	SPCMD2	16	16	2, 3 PCLKB	2 ICLK	
0008 83B6h	RSPI1	RSPI command register 3	SPCMD3	16	16	2, 3 PCLKB	2 ICLK	
0008 83B8h	RSPI1	RSPI command register 4	SPCMD4	16	16	2, 3 PCLKB	2 ICLK	

Table 5.3 DC Characteristics (2)

Conditions: $V_{CC} = AVCC0 = VREFH = VCC_USB = 2.7$ to 3.6 V, $VREFH0 = 2.7$ V to $AVCC0$,
 $VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0$ V, $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Output high voltage	All output pins	V_{OH}	$V_{CC} - 0.5$	—	V	$I_{OH} = -1$ mA
Output low voltage	All output pins (except for RIIC pins, and ETHERC)	V_{OL}	—	0.5	V	$I_{OL} = 1.0$ mA
	RIIC pins	—	—	0.4	V	$I_{OL} = 3.0$ mA
		—	—	0.6		$I_{OL} = 6.0$ mA
	RIIC pins (only P12 and P13 in channel 0)	V_{OL}	—	0.4	V	$I_{OL} = 15.0$ mA (ICFER.FMPE = 1)
		—	0.4	—		$I_{OL} = 20.0$ mA (ICFER.FMPE = 1)
	ETHERC	V_{OL}	—	0.4	V	$I_{OL} = 1.0$ mA
Input leakage current	RES#, MD pin, EMLE*1, NMI	$ I_{in} $	—	1.0	μ A	$V_{in} = 0$ V $V_{in} = V_{CC}$
Three-state leakage current (off state)	Other than ports for 5 V tolerant	$ I_{TSI} $	—	1.0	μ A	$V_{in} = 0$ V $V_{in} = V_{CC}$
	Ports for 5 V tolerant		—	5.0		$V_{in} = 0$ V $V_{in} = 5.5$ V
Input pull-up MOS current	Ports 0 to 2, 30 to 34, 36, 37, 4 to G, J3, J5	I_p	-10	—	-300	μ A $V_{CC} = 2.7$ to 3.6 V $V_{in} = 0$ V
Input capacitance	All input pins (except for ports 12, 13, 16, 17, 20, 21, 4, C0, C1, and EMLE)	C_{in}	—	—	15	pF $V_{in} = 0$ V $f = 1$ MHz $T_a = 25^\circ\text{C}$
	Ports 12, 13, 16, 17, 20, 21, 4, C0, C1, EMLE		—	—	30	
Input pull-down MOS current	EMLE, BSCANP	I_p	10	—	300	μ A $V_{in} = V_{CC}$

Note 1. The input leakage current value at the EMLE pin is only when $V_{in} = 0$ V.

Table 5.6 DC Characteristics (4)

Conditions: $V_{CC} = AVCC0 = VREFH = VCC_USB = 2.7$ to 3.6 V, $VREFH0 = 2.7$ V to $AVCC0$,
 $VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0$ V, $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Permissible total power consumption*1	P_d	—	—	380	mW	*2

Note 1. This is the total power consumption of the chip as a whole (including the power consumed by the output buffers).

Note 2. Contact a Renesas sales office or agent regarding further details of the conditions of measurement.

Table 5.7 Permissible Output Currents

Conditions: $V_{CC} = AVCC0 = VREFH = VCC_USB = 2.7$ to 3.6 V, $VREFH0 = 2.7$ V to $AVCC0$,
 $VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0$ V, $T_a = T_{opr}$

Item			Symbol	Min.	Typ.	Max.	Unit
Permissible output low current (average value per pin)	All output pins*1	Normal drive	I_{OL}	—	—	2.0	mA
	All output pins*2	High drive	I_{OL}			3.8	mA
Permissible output low current (max. value per pin)	All output pins*1	Normal drive	I_{OL}	—	—	4.0	mA
	All output pins*2	High drive	I_{OL}			7.6	mA
Permissible output low current (total)	Total of all output pins		ΣI_{OL}	—	—	80	mA
Permissible output high current (average value per pin)	All output pins*1	Normal drive	I_{OH}	—	—	−2.0	mA
	USB_DPUPE pin*2	High drive	I_{OH}	—	—	−3.8	mA
Permissible output high current (max. value per pin)	All output pins*1	Normal drive	I_{OH}	—	—	−4.0	mA
	All output pins*2	High drive	I_{OH}	—	—	−7.6	mA
Permissible output high current (total)	Total of all output pins		ΣI_{OH}	—	—	−80	mA

Caution: To protect the LSI's reliability, the output current values should not exceed the values in this table.

Note 1. This is the value when normal driving ability is set with a pin for which normal driving ability is selectable.

Note 2. This is the value when high driving ability is set with a pin for which normal driving ability is selectable or the value of the pin to which high driving ability is fixed.

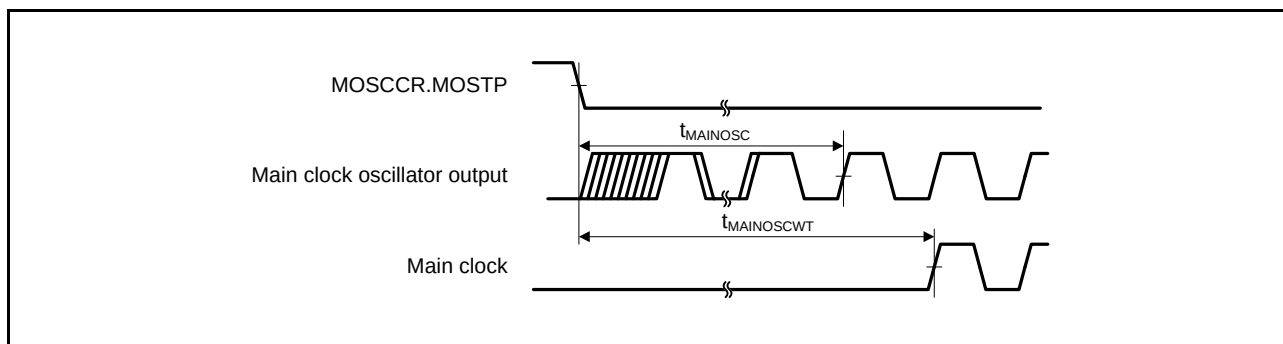


Figure 5.5 Main Clock Oscillation Start Timing

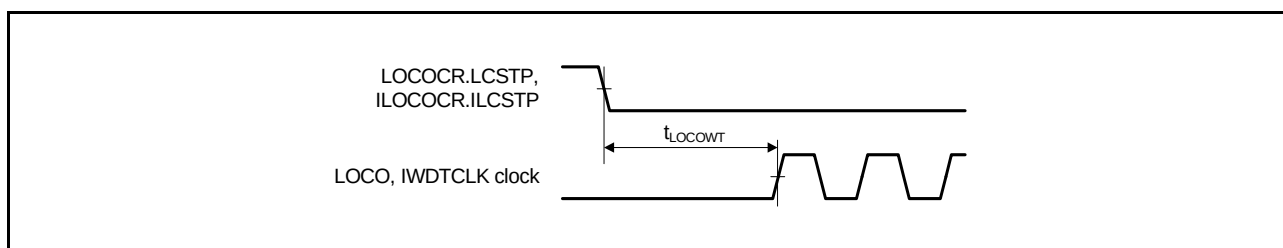


Figure 5.6 LOCO, IWDTCCLK Oscillation Start Timing

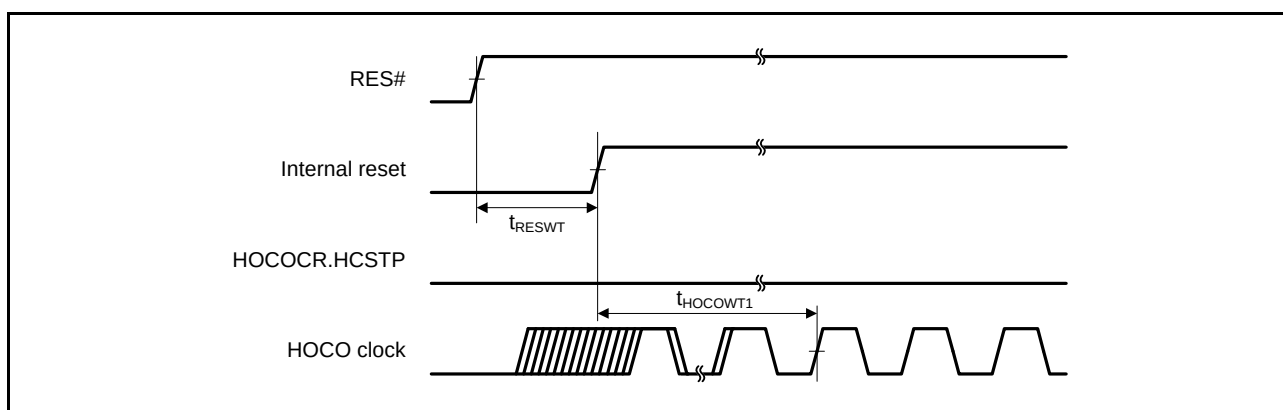


Figure 5.7 HOCO Oscillation Start Timing (After Reset is Canceled by Setting the OFS1.HOCOEN Bit to 0)

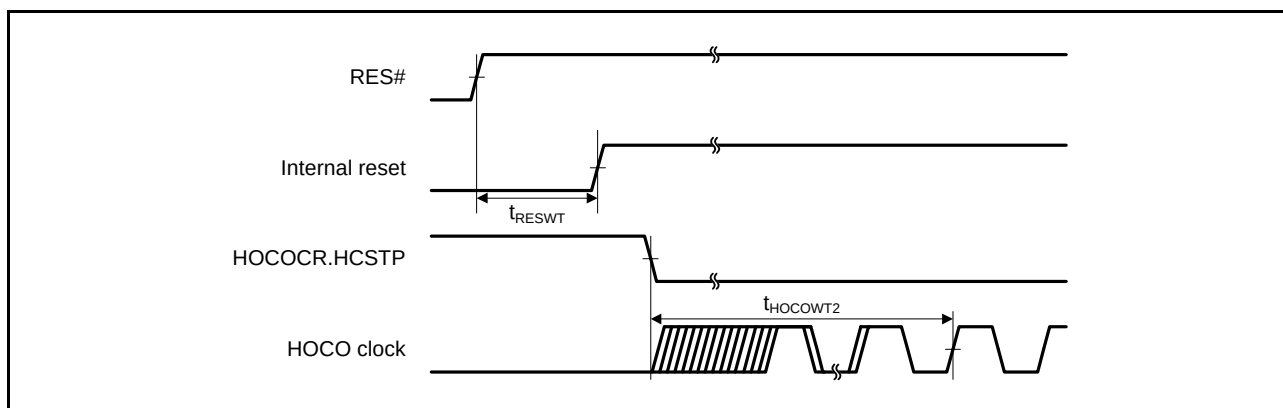


Figure 5.8 HOCO Clock Oscillation Start Timing (Oscillation is Started by Setting the HOCOEN.HCSTP Bit)

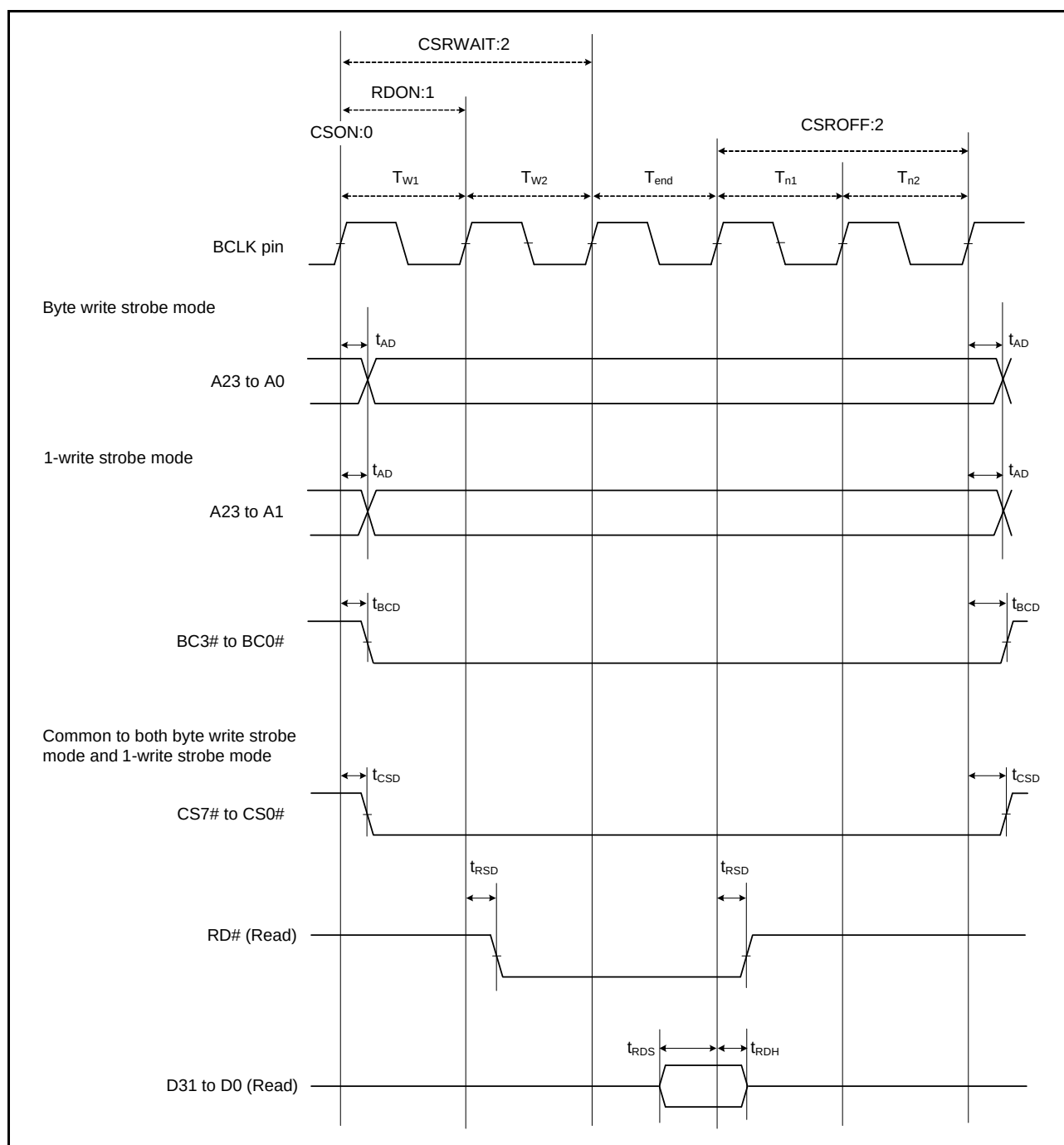


Figure 5.19 External Bus Timing/Normal Read Cycle (Bus Clock Synchronized)

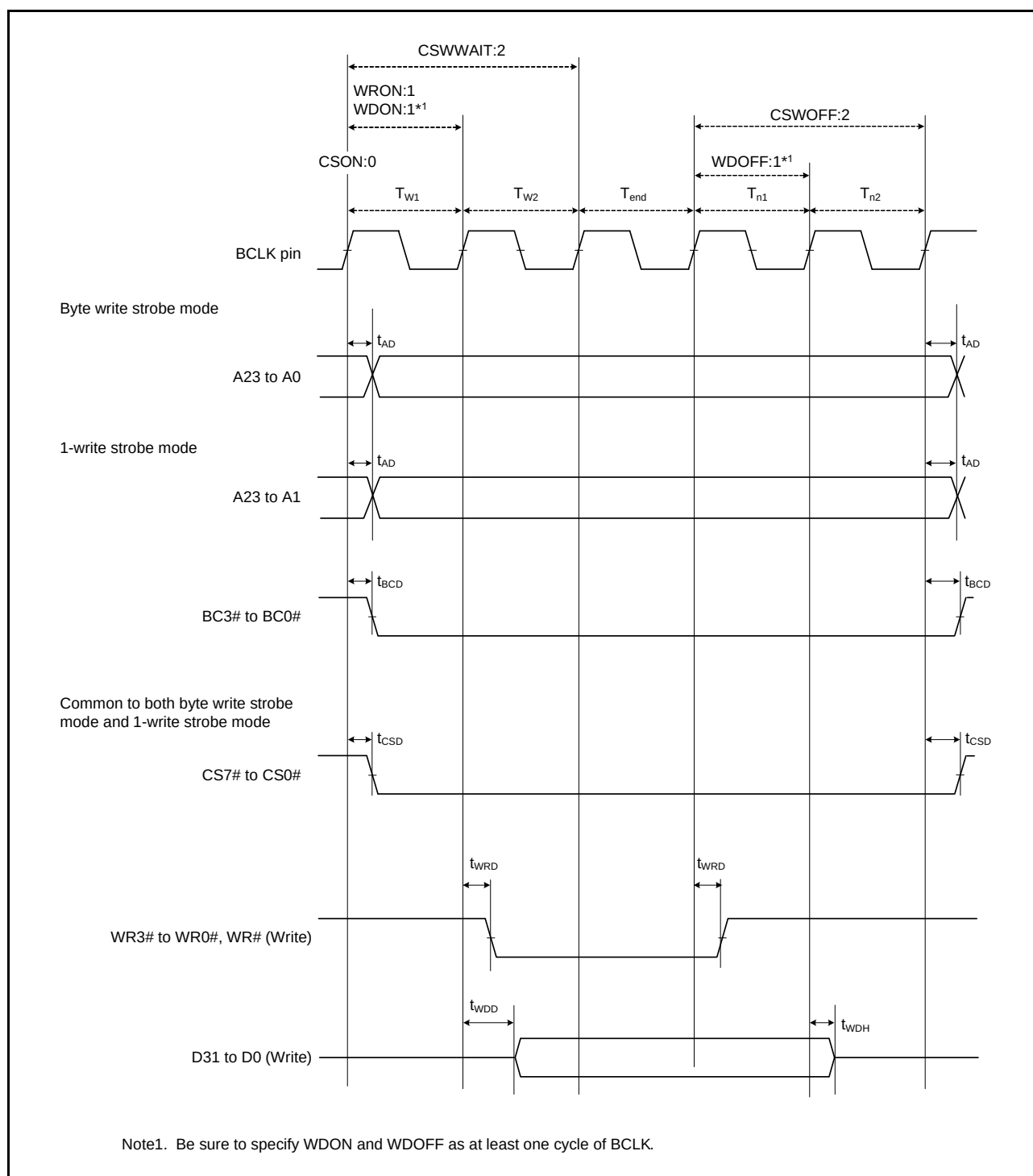


Figure 5.20 External Bus Timing/Normal Write Cycle (Bus Clock Synchronized)

5.3.6 EXDMAC Timing

Table 5.18 EXDMAC Timing

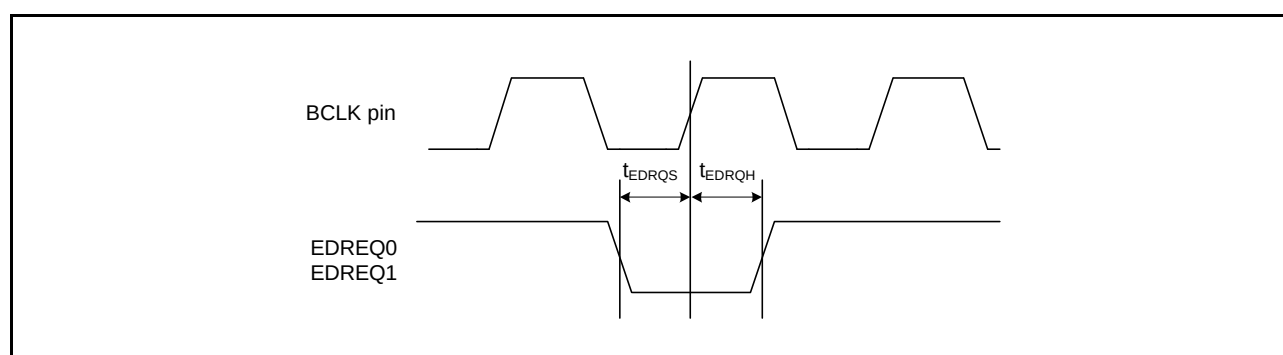
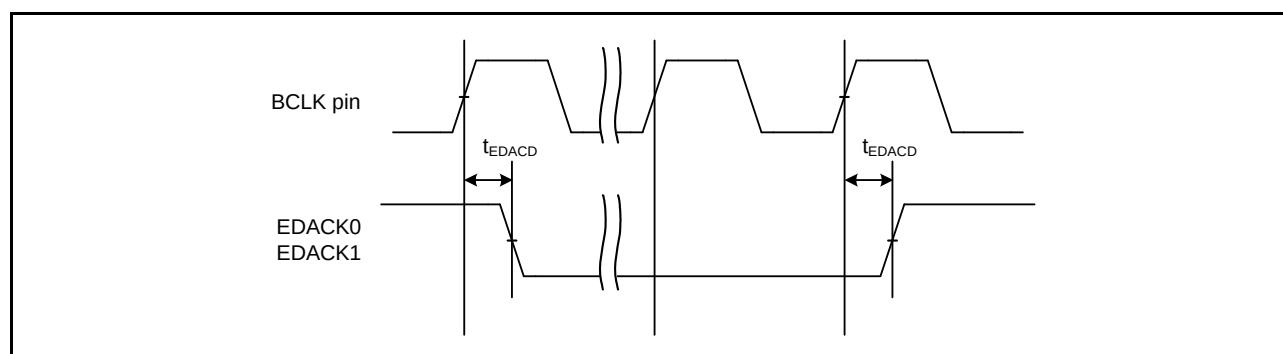
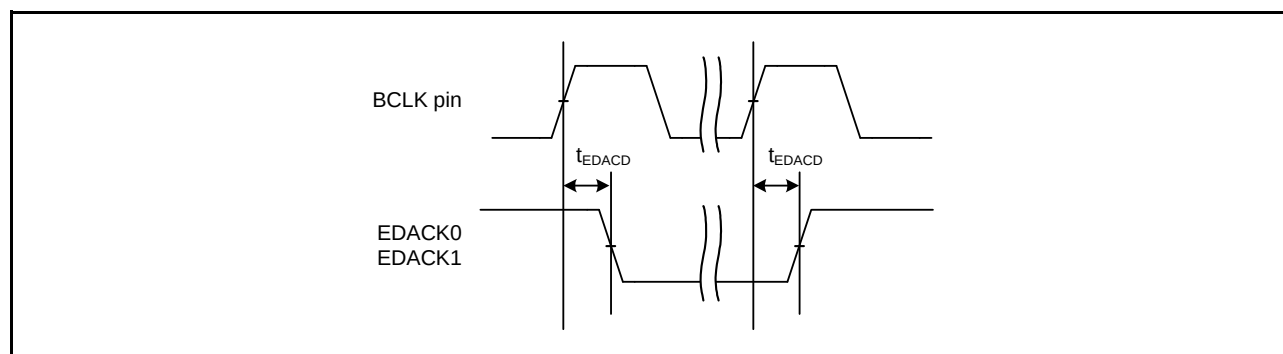
Conditions: $V_{CC} = AV_{CC0} = V_{REFH} = V_{CC_USB} = 2.7$ to 3.6 V, $V_{REFH0} = 2.7$ V to AV_{CC0} ,

$V_{SS} = AV_{SS0} = V_{REFL}/V_{REFL0} = V_{SS_USB} = 0$ V

$ICLK = 8$ to 100 MHz, $PCLK = 8$ to 50 MHz, $BCLK$ pin = 8 to 100 MHz, $SDCLK$ pin = 8 to 50 MHz, $T_a = T_{opr}$

High drive output is selected by the drive capacity control register

	Item	Symbol	Min.	Max.	Unit	Test Conditions
EXDMAC	EDREQ setup time	t_{EDRQS}	20	—	ns	Figure 5.31
	EDREQ hold time	t_{EDRQH}	5	—	ns	Figure 5.32 and Figure 5.33
	EDACK delay time	t_{EDACD}	—	15	ns	Figure 5.33

**Figure 5.31 EDREQ0 and EDREQ1 Input Timing****Figure 5.32 EDACK0 and EDACK1 Single-Address Transfer Timing (for a CS Area)****Figure 5.33 EDACK0 and EDACK1 Single-Address Transfer Timing (for SDRAM)**

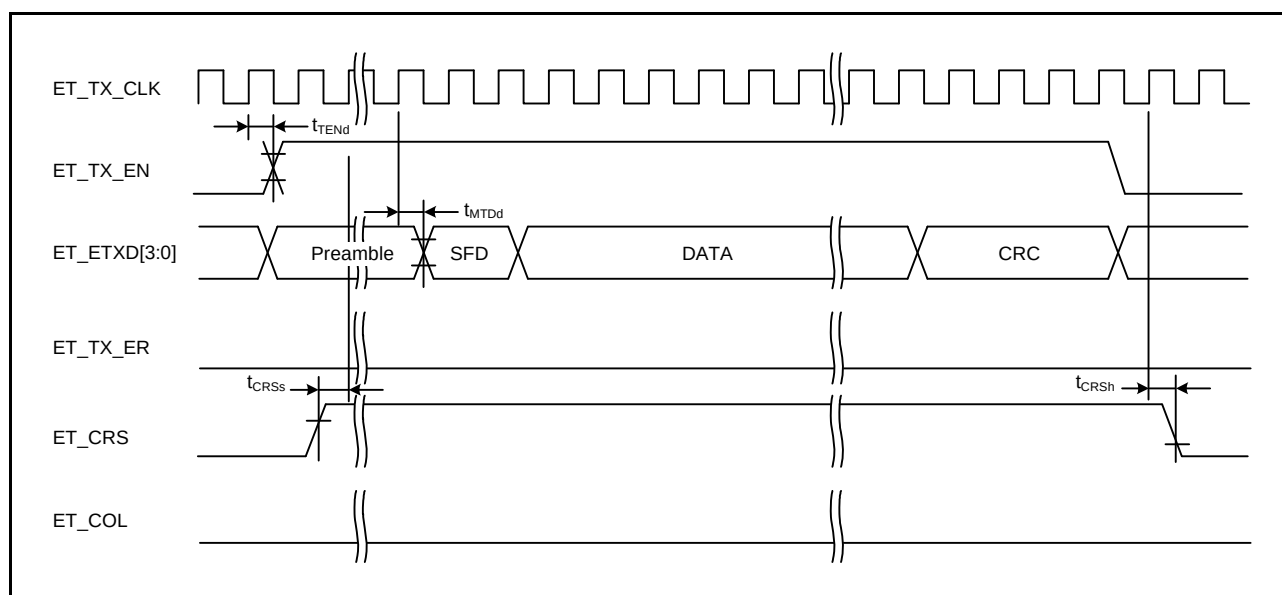


Figure 5.53 MII Transmission Timing (Normal Operation)

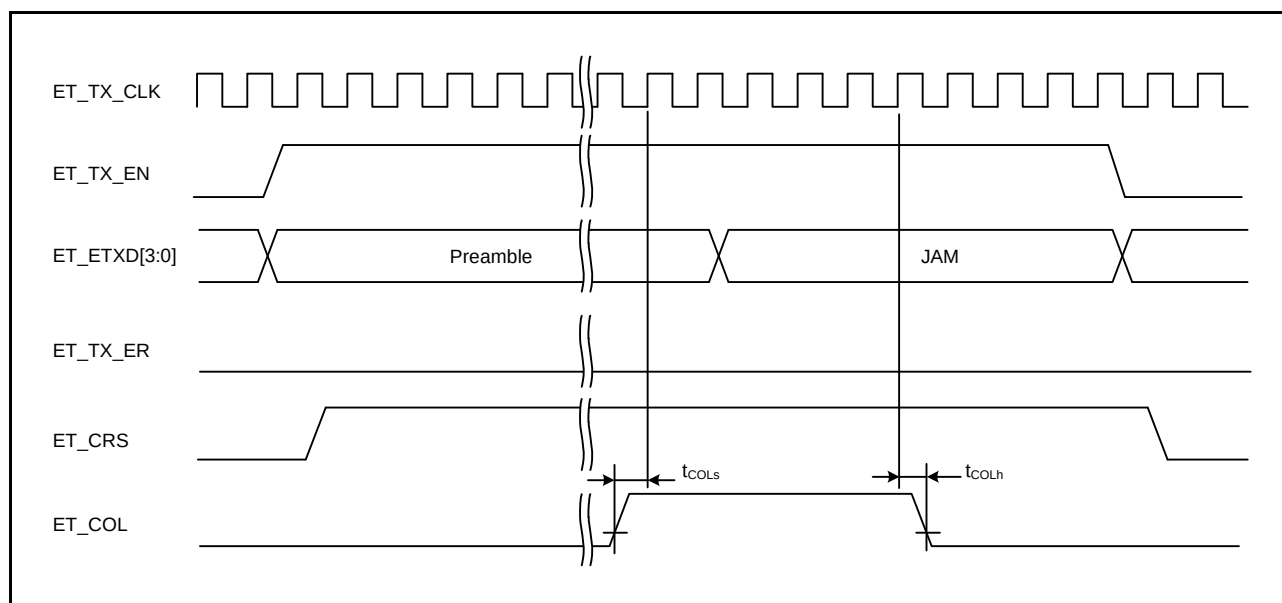


Figure 5.54 MII Transmission Timing (Conflict Occurrence)

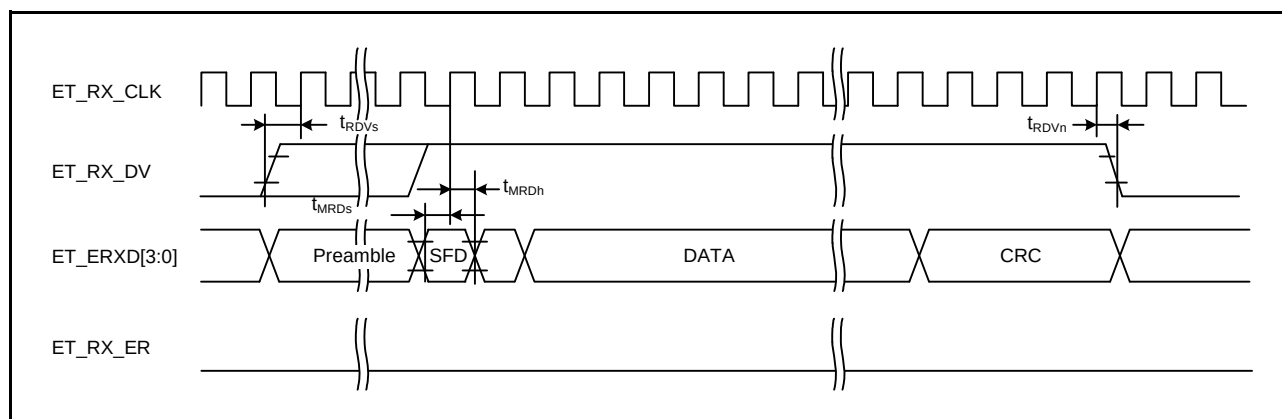


Figure 5.55 MII Reception Timing (Normal Operation)