Renesas Electronics America Inc - R5F5631YDDFB#V0 Datasheet

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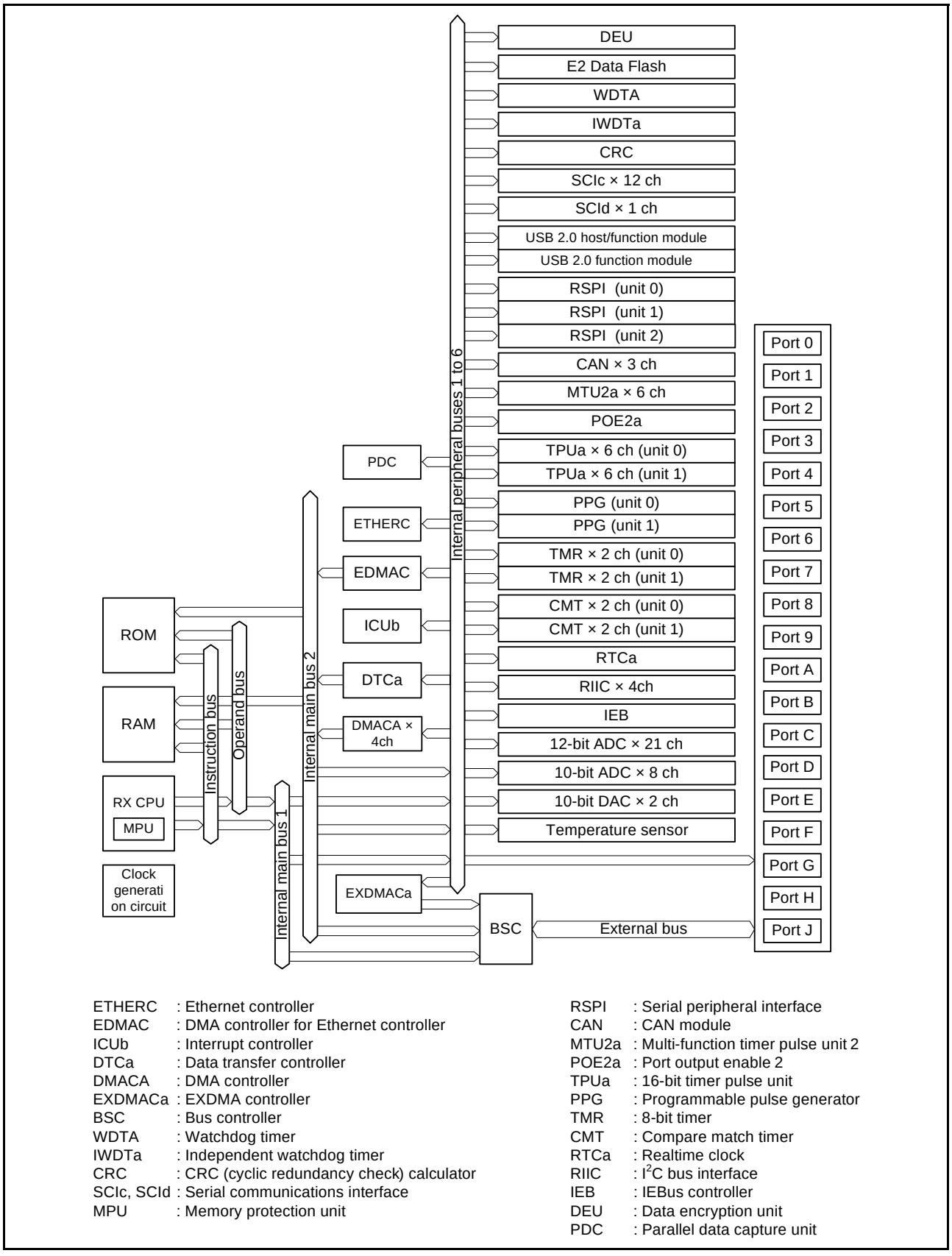
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SCI, SPI, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	111
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b, 21x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LFQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f5631yddfb-v0

1.3 Block Diagram

Figure 1.2 shows a block diagram.



ETHERC : Ethernet controller
EDMAC : DMA controller for Ethernet controller
ICUb : Interrupt controller
DTCa : Data transfer controller
DMACA : DMA controller
EXDMACa : EXDMA controller
BSC : Bus controller
WDTA : Watchdog timer
IWDTa : Independent watchdog timer
CRC : CRC (cyclic redundancy check) calculator
SCIc, SCId : Serial communications interface
MPU : Memory protection unit

RSPI : Serial peripheral interface
CAN : CAN module
MTU2a : Multi-function timer pulse unit 2
POE2a : Port output enable 2
TPUa : 16-bit timer pulse unit
PPG : Programmable pulse generator
TMR : 8-bit timer
CMT : Compare match timer
RTCa : Realtime clock
RIIC : I^2C bus interface
IEB : IEBus controller
DEU : Data encryption unit
PDC : Parallel data capture unit

Figure 1.2 Block Diagram

1.4 Pin Functions

Table 1.4 lists the pin functions.

Table 1.4 Pin Functions (1/6)

Classifications	Pin Name	I/O	Description
Power supply	VCC	Input	Power supply pin. Connect it to the system power supply. Connect this pin to VSS via a 0.1-μF capacitor. The capacitor should be placed close to the pin.
	VCL	Input	Connect this pin to VSS via a 0.1-μF capacitor. The capacitor should be placed close to the pin.
	VSS	Input	Ground pin. Connect it to the system power supply (0 V).
	VBATT	Input	Backup power pin. When the battery backup function is not to be used, connect it to the VCC pin.
Clock	XTAL	Output	Pins for a crystal resonator. An external clock signal can be input through the EXTAL pin.
	EXTAL	Input	
	BCLK	Output	Outputs the external bus clock for external devices.
	SDCLK	Output	Outputs the clock dedicated for the SDRAM.
	XCOUT	Output	Input/output pins for the subclock oscillator. Connect a crystal resonator between XCOUT and XCIN.
	XCIN	Input	
Operating mode control	MD	Input	Pins for setting the operating mode. The signal levels on these pins must not be changed during operation.
System control	RES#	Input	Reset signal input pin. This LSI enters the reset state when this signal goes low.
	EMLE	Input	Input pin for the on-chip emulator enable signal. When the on-chip emulator is used, this pin should be driven high. When not used, it should be driven low.
	BSCANP	Input	Boundary scan enable pin. Boundary scan is enabled when this pin goes high. When not used, it should be driven low.
On-chip emulator	FINEC	Input	Fine interface clock pin
	FINED	I/O	Fine interface pin
	TRST#	Input	On-chip emulator or boundary scan pins. When the EMLE pin is driven high, these pins are dedicated for the on-chip emulator.
	TMS	Input	
	TDI	Input	
	TCK	Input	
	TDO	Output	
	TRCLK	Output	This pin outputs the clock for synchronization with the trace data.
	TRSYNC	Output	This pin indicates that output from the TRDATA0 to TRDATA3 pins is valid.
	TRDATA0 to TRDATA3	Output	These pins output the trace information.
Address bus	A0 to A23	Output	Output pins for the address.
Data bus	D0 to D31	I/O	Input and output pins for the bidirectional data bus.
Multiplexed bus	A0/D0 to A15/D15	I/O	Address/data multiplexed bus

Table 1.4 Pin Functions (6/6)

Classifications	Pin Name	I/O	Description
Analog power supply	AVCC0	Input	Analog voltage supply pin for the 12-bit A/D converter. Connect this pin to VCC if the 12-bit A/D converter is not to be used.
	AVSS0	Input	Analog ground pin for the 12-bit A/D converter. Connect this pin to VSS if the 12-bit A/D converter is not to be used.
	VREFH0	Input	Analog reference voltage supply pin for the 12-bit A/D converter. Connect this pin to VCC if the 12-bit A/D converter is not to be used.
	VREFL0	Input	Analog reference ground pin for the 12-bit A/D converter. Connect this pin to VSS if the 12-bit A/D converter is not to be used.
	VREFH	Input	Reference voltage input pin for the 10-bit A/D converter and D/A converter. This is used as the analog power supply for the respective modules. Connect this pin to VCC if neither the 10-bit A/D converter nor the D/A converter is in use.
	VREFL	Input	Reference ground pin for the 10-bit A/D converter and D/A converter. This is used as the analog ground for the respective modules. Set this pin to the same potential as the VSS pin.
I/O ports	P00 to P03, P05, P07	I/O	6-bit input/output pins.
	P10 to P17	I/O	8-bit input/output pins.
	P20 to P27	I/O	8-bit input/output pins.
	P30 to P37	I/O	8-bit input/output pins. (P35 is an input pin)
	P40 to P47	I/O	8-bit input/output pins.
	P50 to P57	I/O	8-bit input/output pins.
	P60 to P67	I/O	8-bit input/output pins.
	P70 to P77	I/O	8-bit input/output pins.
	P80 to P87	I/O	8-bit input/output pins.
	P90 to P97	I/O	8-bit input/output pins.
	PA0 to PA7	I/O	8-bit input/output pins.
	PB0 to PB7	I/O	8-bit input/output pins.
	PC0 to PC7	I/O	8-bit input/output pins.
	PD0 to PD7	I/O	8-bit input/output pins.
	PE0 to PE7	I/O	8-bit input/output pins.
	PF0 to PF5	I/O	6-bit input/output pins.
	PG0 to PG7	I/O	8-bit input/output pins.
	PJ3, PJ5	I/O	2-bit input/output pins.

Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (2/5)

Pin Number 177-Pin TFLGA 176-Pin LFBGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SCIc, SCId, RSPI, RIIC, CAN, IEB, USB, and PDC)	Interrupt	S12AD, AD, DA
C14	VSS						
C15	SDCLK	P70					
D1		P01		TMCI0	RXD6/SMISO6/SSCL6	IRQ9	AN019
D2		P02		TMCI1	SCK6	IRQ10	AN020
D3		P03				IRQ11	DA0
D4		P00		TMRI0	TXD6/SMOSI6/SSDA6	IRQ8	AN018
D5		P44				IRQ12-DS	AN004
D6		P93	A19/D19		CTS7#/RTS7#/SS7#		AN017
D7		P95	A21/D21				
D8	VSS						
D9		PD5	D5[A5/D5]	MTIC5W/POE2#	SSLC1	IRQ5	AN013
D10		PD7	D7[A7/D7]	MTIC5U/POE0#	SSLC3	IRQ7	AN7
D11		P61	CS1#/SDCS#				
D12		PE5	D13[A13/D13]	MTIOC4C/MTIOC2B/ TIOCB10	ET_RX_CLK/REF50CK/ RSPCKB	IRQ5	AN3
D13	VCC						
D14		PE7	D15[A15/D15]	TIOCB11	MISOB	IRQ7	AN5
D15		P65	CS5#/CKE				
E1		PJ5					
E2	EMLE						
E3		PF5				IRQ4	
E4	VSS						
E5*1	NC						
E12		PE6	D14[A14/D14]	TIOCA11	MOSIB	IRQ6	AN4
E13	TRDATA0	PG2	D26				
E14	TRDATA1	PG3	D27				
E15		P67	CS7#/DQM1		CRX2*3	IRQ15	
F1	VBATT						
F2	VCL						
F3		PJ3		MTIOC3C	CTS6#/RTS6#/CTS0#/ RTS0#/SS6#/SS0#		
F4	BSCANP						
F12		P66	CS6#/DQM0		CTX2*3		
F13	TRSYNC	PG4	D28				
F14		PA0	A0/BC0#/DQM2	MTIOC4A/TIOCA0/PO16	ET_TX_EN/ RMII_TXD_EN/SSLA1		
F15	VSS						
G1	XCIN						
G2	XCOUT						
G3	MD/FINED						
G4	TRST#	PF4					
G12	TRCLK	PG5	D29				
G13	TRDATA2	PG6	D30				
G14		PA1	A1/DQM3	MTIOC0B/MTCLKC/ TIOCB0/PO17	ET_WOL/SCK5/SSLA2	IRQ11	
G15	VCC						
H1	XTAL	P37					
H2	VSS						

Table 1.6 List of Pin and Pin Functions (176-Pin LQFP) (1/5)

Pin Number 176-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SCIc, SCId, RSPI, RIIC, CAN, IEB, USB, and PDC)	Interrupt	S12AD, AD, DA
1	AVSS0						
2		P05				IRQ13	DA1
3	VREFH						
4		P03				IRQ11	DA0
5	VREFL						
6		P02		TMCI1	SCK6	IRQ10	AN020
7		P01		TMCI0	RXD6/SMISO6/SSCL6	IRQ9	AN019
8		P00		TMRI0	TXD6/SMOSI6/SSDA6	IRQ8	AN018
9		PF5				IRQ4	
10	EMLE						
11		PJ5					
12	VSS						
13		PJ3		MTIOC3C	CTS6#/RTS6#/CTS0#/ RTS0#/SS6#/SS0#		
14	VCL						
15	VBATT						
16	NC						
17	TRST#	PF4					
18	MD/FINED						
19	XCIN						
20	XCOUT						
21	RES#						
22	XTAL	P37					
23	VSS						
24	EXTAL	P36					
25	VCC						
26		P35				NMI	
27		P34		MTIOC0A/TMCI3/PO12/ POE2#	SCK6/SCK0/ USB0_DPRPD	IRQ4	
28		P33		MTIOC0D/TIOCD0/ TMRI3/PO11/POE3#	RXD6/RXD0/SMISO6/ SMISO0/SSCL6/SSCL0/ CRX0/PCKO	IRQ3-DS	
29		P32		MTIOC0C/TIOCC0/TMO3/ PO10/RTCOUT/RTCIC2	TXD6/TXD0/SMOSI6/ SMOSI0/SSDA6/SSDA0/ CTX0/USB0_VBUSEN/ VSYNC	IRQ2-DS	
30	TMS	PF3					
31	TDI	PF2			RXD1/SMISO1/SSCL1		
32		P31		MTIOC4D/TMCI2/PO9/ RTCIC1	CTS1#/RTS1#/SS1#/ SSLB0/USB0_DPUPE	IRQ1-DS	
33		P30		MTIOC4B/TMRI3/PO8/ RTCIC0/POE8#	RXD1/SMISO1/SSCL1/ MISOB/USB0_DRPD	IRQ0-DS	
34	TCK/FINEC	PF1			SCK1		
35	TDO	PF0			TXD1/SMOSI1/SSDA1		
36		P27	CS7#	MTIOC2B/TMCI3/PO7	SCK1/RSPCKB		
37		P26	CS6#	MTIOC2A/TMO1/PO6	TXD1/CTS3#/RTS3# SMOSI1/SS3#/SSDA1/ MOSIB		
38		P25	CS5#/EDACK1	MTIOC4C/MTCLKB/ TIOCA4/PO5	RXD3/SMISO3/SSCL3/ USB0_DPRPD/HSYNC		ADTRG0#
39	VCC						
40		P24	CS4#/EDREQ1	MTIOC4A/MTCLKA/ TIOCB4/TMRI1/PO4	SCK3/USB0_VBUSEN/ PIXCLK		

Table 1.6 List of Pin and Pin Functions (176-Pin LQFP) (4/5)

Pin Number 176-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SCIc, SCId, RSPI, RIIC, CAN, IEB, USB, and PDC)	Interrupt	S12AD, AD, DA
100		PB1	A9	MTIOC0C/MTIOC4C/ TIOCB3/TMCI0/PO25	ET_ERXD0/RMII_RXD0/ TXD4/TXD6/SMOSI4/ SMOSI6/SSDA4/SSDA6	IRQ4-DS	
101		P72	CS2#		ET_MDC		
102		P71	CS1#		ET_MDIO		
103	VCC						
104		PB0	A8	MTIC5W/TIOCA3/PO24	ET_ERXD1/RMII_RXD1/ RXD4/RXD6/SMISO4/ SMISO6/SSCL4/SSCL6/ RSPCKA	IRQ12	
105	VSS						
106		PA7	A7	TIOCB2/PO23	ET_WOL/MISOA		
107		PA6	A6	MTIC5V/MTCLKB/ TIOCA2/TMCI3/PO22/ POE2#	ET_EXOUT/CTS5#/ RTS5#/SS5#/MOSIA		
108		PA5	A5	TIOCB1/PO21	ET_LINKSTA/RSPCKA		
109		PA4	A4	MTIC5U/MTCLKA/ TIOCA1/TMRI0/PO20	ET_MDC/TXD5/SMOSI5/ SSDA5/SSLA0	IRQ5-DS	
110		PA3	A3	MTIOC0D/MTCLKD/ TIOCD0/TCLKB/PO19	ET_MDIO/RXD5/SMISO5/ SSCL5	IRQ6-DS	
111	TRDATA3	PG7	D31				
112		PA2	A2	PO18	RXD5/SMISO5/SSCL5/ SSLA3		
113	TRDATA2	PG6	D30				
114		PA1	A1/DQM3	MTIOC0B/MTCLKC/ TIOCB0/PO17	ET_WOL/SCK5/SSLA2	IRQ11	
115	VCC						
116	TRCLK	PG5	D29				
117	VSS						
118		PA0	A0/BC0#/DQM2	MTIOC4A/TIOCA0/PO16	ET_TX_EN/ RMII_TXD_EN/SSLA1		
119	TRSYNC	PG4	D28				
120		P67	CS7#/DQM1		CRX2*2	IRQ15	
121	TRDATA1	PG3	D27				
122		P66	CS6#/DQM0		CTX2*2		
123	TRDATA0	PG2	D26				
124		P65	CS5#/CKE				
125		PE7	D15[A15/D15]	TIOCB11	MISOB	IRQ7	AN5
126		PE6	D14[A14/D14]	TIOCA11	MOSIB	IRQ6	AN4
127	VCC						
128	SDCLK	P70					
129	VSS						
130		PE5	D13[A13/D13]	MTIOC4C/MTIOC2B/ TIOCB10	ET_RX_CLK/REF50CK/ RSPCKB	IRQ5	AN3
131		PE4	D12[A12/D12]	MTIOC4D/MTIOC1A/ TIOCA10/PO28	ET_ERXD2/SSLB0		AN2
132		PE3	D11[A11/D11]	MTIOC4B/TIOCB9/PO26/ POE8#	ET_ERXD3/CTS12#/ RTS12#/SS12#/MISOB		AN1
133		PE2	D10[A10/D10]	MTIOC4A/TIOCA9/PO23	RXD12/SMISO12/ SSCL12/RXDX12/SSLB3/ MOSIB	IRQ7-DS	AN0
134		PE1	D9[A9/D9]	MTIOC4C/TIOCD9/PO18	TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12/SSLB2/RSPCKB		ANEX1
135		PE0	D8[A8/D8]	TIOCC9	SCK12/SSLB1		ANEX0

Table 4.1 List of I/O Registers (Address Order) (17/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 81A8h	TPU8	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 81AAh	TPU8	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	
0008 81B0h	TPU9	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK	
0008 81B1h	TPU9	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK	
0008 81B2h	TPU9	Timer I/O control register H	TIORH	8	8	2, 3 PCLKB	2 ICLK	
0008 81B3h	TPU9	Timer I/O control register L	TIORL	8	8	2, 3 PCLKB	2 ICLK	
0008 81B4h	TPU9	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK	
0008 81B5h	TPU9	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK	
0008 81B6h	TPU9	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	
0008 81B8h	TPU9	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	
0008 81BAh	TPU9	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	
0008 81BCh	TPU9	Timer general register C	TGRC	16	16	2, 3 PCLKB	2 ICLK	
0008 81BEh	TPU9	Timer general register D	TGRD	16	16	2, 3 PCLKB	2 ICLK	
0008 81C0h	TPU10	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK	
0008 81C1h	TPU10	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK	
0008 81C2h	TPU10	Timer I/O control register	TIOR	8	8	2, 3 PCLKB	2 ICLK	
0008 81C4h	TPU10	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK	
0008 81C5h	TPU10	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK	
0008 81C6h	TPU10	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	
0008 81C8h	TPU10	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	
0008 81CAh	TPU10	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	
0008 81D0h	TPU11	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK	
0008 81D1h	TPU11	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK	
0008 81D2h	TPU11	Timer I/O control register	TIOR	8	8	2, 3 PCLKB	2 ICLK	
0008 81D4h	TPU11	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK	
0008 81D5h	TPU11	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK	
0008 81D6h	TPU11	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	
0008 81D8h	TPU11	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	
0008 81DAh	TPU11	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	
0008 81E6h	PPG0	PPG output control register	PCR	8	8	2, 3 PCLKB	2 ICLK	PPG
0008 81E7h	PPG0	PPG output mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 81E8h	PPG0	Next data enable register H	NDERH	8	8	2, 3 PCLKB	2 ICLK	
0008 81E9h	PPG0	Next data enable register L	NDERL	8	8	2, 3 PCLKB	2 ICLK	
0008 81EAh	PPG0	Output data register H	PODRH	8	8	2, 3 PCLKB	2 ICLK	
0008 81EBh	PPG0	Output data register L	PODRL	8	8	2, 3 PCLKB	2 ICLK	
0008 81ECh*1	PPG0	Next data register H	NDRH	8	8	2, 3 PCLKB	2 ICLK	
0008 81EDh*2	PPG0	Next data register L	NDRL	8	8	2, 3 PCLKB	2 ICLK	
0008 81EEh*1	PPG0	Next data register H	NDRH2	8	8	2, 3 PCLKB	2 ICLK	
0008 81EFh*2	PPG0	Next data register L	NDRL2	8	8	2, 3 PCLKB	2 ICLK	
0008 81F0h	PPG1	PPG trigger select register	PTRSLR	8	8	2, 3 PCLKB	2 ICLK	
0008 81F6h	PPG1	PPG output control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 81F7h	PPG1	PPG output mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 81F8h	PPG1	Next data enable register H	NDERH	8	8	2, 3 PCLKB	2 ICLK	
0008 81F9h	PPG1	Next data enable register L	NDERL	8	8	2, 3 PCLKB	2 ICLK	
0008 81FAh	PPG1	Output data register H	PODRH	8	8	2, 3 PCLKB	2 ICLK	
0008 81FBh	PPG1	Output data register L	PODRL	8	8	2, 3 PCLKB	2 ICLK	
0008 81FCh*3	PPG1	Next data register H	NDRH	8	8	2, 3 PCLKB	2 ICLK	
0008 81FDh*4	PPG1	Next data register L	NDRL	8	8	2, 3 PCLKB	2 ICLK	
0008 81FEh*3	PPG1	Next data register H	NDRH2	8	8	2, 3 PCLKB	2 ICLK	PPG
0008 81FFh*4	PPG1	Next data register L	NDRL2	8	8	2, 3 PCLKB	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (25/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 A02Bh	SCI1	I²C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK	SCIc, SCId
0008 A02Ch	SCI1	I²C status register	SISR	8	8	2, 3 PCLKB	2 ICLK	
0008 A02Dh	SCI1	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A040h	SCI2	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A041h	SCI2	Bit rate register	BRR	8	8	2, 3 PCLKB	2 ICLK	
0008 A042h	SCI2	Serial control register	SCR	8	8	2, 3 PCLKB	2 ICLK	
0008 A043h	SCI2	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK	
0008 A044h	SCI2	Serial status register	SSR	8	8	2, 3 PCLKB	2 ICLK	
0008 A045h	SCI2	Receive data register	RDR	8	8	2, 3 PCLKB	2 ICLK	
0008 A046h	SCI2	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A047h	SCI2	Serial extended mode register	SEM	8	8	2, 3 PCLKB	2 ICLK	
0008 A048h	SCI2	Noise filter setting register	SNFR2	8	8	2, 3 PCLKB	2 ICLK	
0008 A049h	SCI2	I²C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK	
0008 A04Ah	SCI2	I²C mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK	
0008 A04Bh	SCI2	I²C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK	
0008 A04Ch	SCI2	I²C status register	SISR	8	8	2, 3 PCLKB	2 ICLK	
0008 A04Dh	SCI2	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A060h	SCI3	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A061h	SCI3	Bit rate register	BRR	8	8	2, 3 PCLKB	2 ICLK	
0008 A062h	SCI3	Serial control register	SCR	8	8	2, 3 PCLKB	2 ICLK	
0008 A063h	SCI3	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK	
0008 A064h	SCI3	Serial status register	SSR	8	8	2, 3 PCLKB	2 ICLK	
0008 A065h	SCI3	Receive data register	RDR	8	8	2, 3 PCLKB	2 ICLK	
0008 A066h	SCI3	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A067h	SCI3	Serial extended mode register	SEMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A068h	SCI3	Noise filter setting register	SNFR	8	8	2, 3 PCLKB	2 ICLK	
0008 A069h	SCI3	I²C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK	
0008 A06Ah	SCI3	I²C mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK	
0008 A06Bh	SCI3	I²C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK	
0008 A06Ch	SCI3	I²C status register	SISR	8	8	2, 3 PCLKB	2 ICLK	
0008 A06Dh	SCI3	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A080h	SCI4	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A081h	SCI4	Bit rate register	BRR	8	8	2, 3 PCLKB	2 ICLK	
0008 A082h	SCI4	Serial control register	SCR	8	8	2, 3 PCLKB	2 ICLK	
0008 A083h	SCI4	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK	
0008 A084h	SCI4	Serial status register	SSR	8	8	2, 3 PCLKB	2 ICLK	
0008 A085h	SCI4	Receive data register	RDR	8	8	2, 3 PCLKB	2 ICLK	
0008 A086h	SCI4	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A087h	SCI4	Serial extended mode register	SEMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A088h	SCI4	Noise filter setting register	SNFR	8	8	2, 3 PCLKB	2 ICLK	
0008 A089h	SCI4	I²C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK	
0008 A08Ah	SCI4	I²C mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK	
0008 A08Bh	SCI4	I²C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK	
0008 A08Ch	SCI4	I²C status register	SISR	8	8	2, 3 PCLKB	2 ICLK	
0008 A08Dh	SCI4	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0A0h	SCI5	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0A1h	SCI5	Bit rate register	BRR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0A2h	SCI5	Serial control register	SCR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0A3h	SCI5	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0A4h	SCI5	Serial status register	SSR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0A5h	SCI5	Receive data register	RDR	8	8	2, 3 PCLKB	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (29/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 C000h	PORT0	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C001h	PORT1	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C002h	PORT2	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C003h	PORT3	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C004h	PORT4	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C005h	PORT5	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C006h	PORT6	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C007h	PORT7	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C008h	PORT8	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C009h	PORT9	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C00Ah	PORTA	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C00Bh	PORTB	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C00Ch	PORTC	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C00Dh	PORTD	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C00Eh	PORTE	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C00Fh	PORTF	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C010h	PORTG	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C012h	PORTJ	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C020h	PORT0	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C021h	PORT1	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C022h	PORT2	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C023h	PORT3	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C024h	PORT4	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C025h	PORT5	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C026h	PORT6	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C027h	PORT7	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C028h	PORT8	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C029h	PORT9	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C02Ah	PORTA	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C02Bh	PORTB	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C02Ch	PORTC	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C02Dh	PORTD	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C02Eh	PORTE	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C02Fh	PORTF	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C030h	PORTG	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C032h	PORTJ	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C040h	PORT0	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C041h	PORT1	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C042h	PORT2	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C043h	PORT3	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C044h	PORT4	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C045h	PORT5	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (30/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 C046h	PORT6	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C047h	PORT7	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C048h	PORT8	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C049h	PORT9	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C04Ah	PORTA	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C04Bh	PORTB	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C04Ch	PORTC	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C04Dh	PORTD	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C04Eh	PORTE	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C04Fh	PORTF	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C050h	PORTG	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C052h	PORTJ	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C060h	PORT0	Port input data register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C061h	PORT1	Port input data register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C062h	PORT2	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C063h	PORT3	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C064h	PORT4	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C065h	PORT5	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C066h	PORT6	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C067h	PORT7	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C068h	PORT8	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C069h	PORT9	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C06Ah	PORTA	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C06Bh	PORTB	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C06Ch	PORTC	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C06Dh	PORTD	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C06Eh	PORTE	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C06Fh	PORTF	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C070h	PORTG	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C072h	PORTJ	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C080h	PORT0	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C081h	PORT0	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C082h	PORT1	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C083h	PORT1	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C084h	PORT2	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C085h	PORT2	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C086h	PORT3	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C087h	PORT3	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C088h	PORT4	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C089h	PORT4	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C08Ah	PORT5	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C08Bh	PORT5	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C08Ch	PORT6	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C08Dh	PORT6	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C08Eh	PORT7	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C08Fh	PORT7	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C090h	PORT8	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C091h	PORT8	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C092h	PORT9	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C093h	PORT9	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C094h	PORTA	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (31/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 C095h	PORTA	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C096h	PORTB	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C097h	PORTB	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C098h	PORTC	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C099h	PORTC	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C09Ah	PORTD	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C09Bh	PORTD	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C09Ch	PORTE	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C09Dh	PORTE	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C09Eh	PORTF	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C09Fh	PORTF	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C0A0h	PORTG	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C0A1h	PORTG	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C0A4h	PORTJ	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C0A5h	PORTJ	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C0C0h	PORT0	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0C1h	PORT1	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0C2h	PORT2	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0C3h	PORT3	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0C4h	PORT4	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0C5h	PORT5	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0C6h	PORT6	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0C7h	PORT7	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0C8h	PORT8	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0C9h	PORT9	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0CAh	PORTA	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0CBh	PORTB	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0CCh	PORTC	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0CDh	PORTD	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0CEh	PORTE	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0CFh	PORTF	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0D0h	PORTG	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0D2h	PORTJ	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0E0h	PORT0	Drive ability control register	DSCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0E2h	PORT2	Drive ability control register	DSCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0E5h	PORT5	Drive ability control register	DSCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0E9h	PORT9	Drive ability control register	DSCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0EAh	PORTA	Drive ability control register	DSCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0EBh	PORTB	Drive ability control register	DSCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0ECh	PORTC	Drive ability control register	DSCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0EDh	PORTD	Drive ability control register	DSCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0EEh	PORTE	Drive ability control register	DSCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0F0h	PORTG	Drive ability control register	DSCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C100h	MPC	CS output enable register	PFCSE	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C102h	MPC	CS output pin select register 0	PFCSS0	8	8	2, 3 PCLKB	2 ICLK	
0008 C103h	MPC	CS output pin select register 1	PFCSS1	8	8	2, 3 PCLKB	2 ICLK	
0008 C104h	MPC	Address output enable register 0	PFAOE0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C105h	MPC	Address output enable register 1	PFAOE1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C106h	MPC	External bus control register 0	PFBCR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C107h	MPC	External bus control register 1	PFBCR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C10Eh	MPC	Ethernet control resister 1	PFENET	8	8	2, 3 PCLKB	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (40/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
000A 0054h	USB0	USB request type register	USBREQ	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	
000A 0056h	USB0	USB request value register	USBVAL	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	
000A 0058h	USB0	USB request index register	USBINDX	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	
000A 005Ah	USB0	USB request length register	USBLENG	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	
000A 005Ch	USB0	DCP configuration register	DCPCFG	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	
000A 005Eh	USB0	DCP maximum packet size register	DCPMAXP	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	
000A 0060h	USB0	DCP control register	DCPCTR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	
000A 0064h	USB0	Pipe window select register	PIPESEL	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	USBa
000A 0068h	USB0	Pipe configuration register	PIPECFG	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	
000A 006Ch	USB0	Pipe maximum packet size register	PIPEMAXP	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. Measured with clocks supplied to the peripheral functions. This does not include the BGO operation.
Note 3. I_{CC} depends on f (ICLK) as follows. (ICLK:PCLK:BCLK:BCLK pin = 8:4:4:2)
I_{CC} Max. = 0.87 × f + 13 (max. operation in high-speed operating mode)
I_{CC} Typ. = 0.35 × f + 5 (normal operation in high-speed operating mode)
I_{CC} Typ. = 1.0 × f + 3 (low-speed operating mode 1)
I_{CC} Max. = 0.53 × f + 12 (sleep mode)
Note 4. This does not include the BGO operation.
Note 5. This is the increase for programming or erasure of the ROM or flash memory for data storage during program execution.
Note 6. Supply of the clock signal to peripherals is stopped in this state. This does not include the BGO operation.
Note 7. The reference power supply current is included in the power supply current value for 10-bit A/D conversion and D/A conversion.
Note 8. When V_{BATT} is used
Note 9. The current values for 10-bit A/D converter and 10-bit D/A converter are included in the current from the VREFH pin.
Note 10. The values are the sum of I_{AVCC0} and I_{VREFH}.

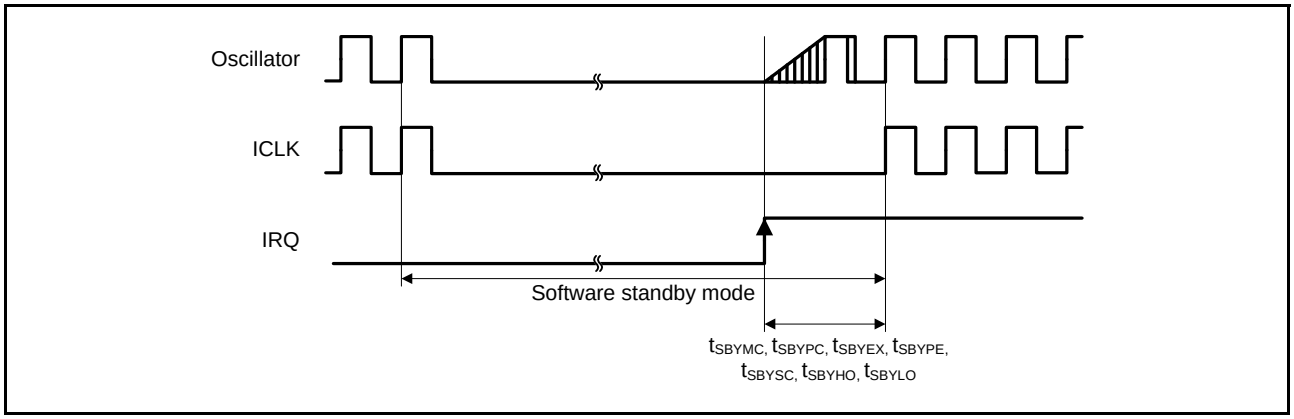


Figure 5.13 Software Standby Mode Cancellation Timing

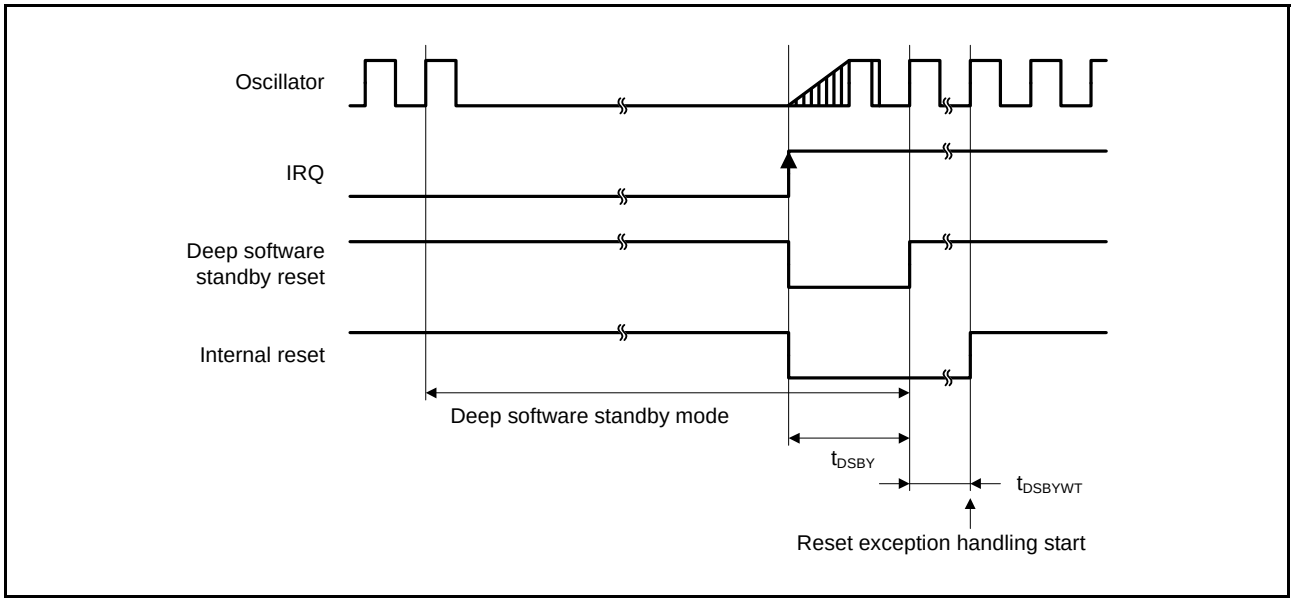


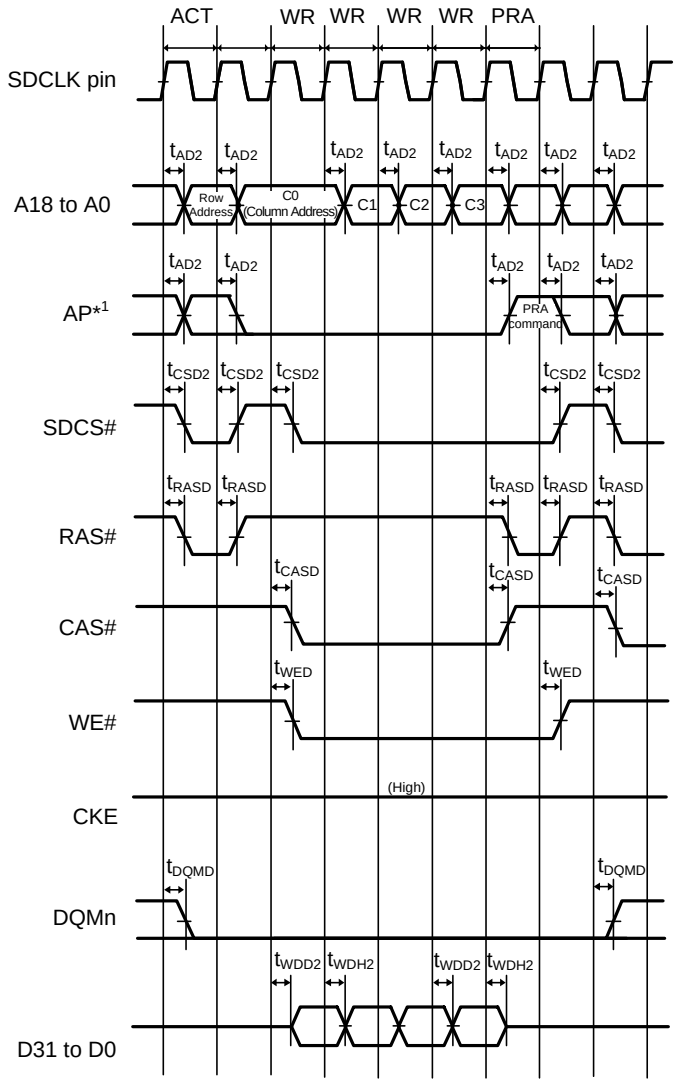
Figure 5.14 Deep Software Standby Mode Cancellation Timing

5.3.4 Control Signal Timing

Table 5.15 Control Signal Timing

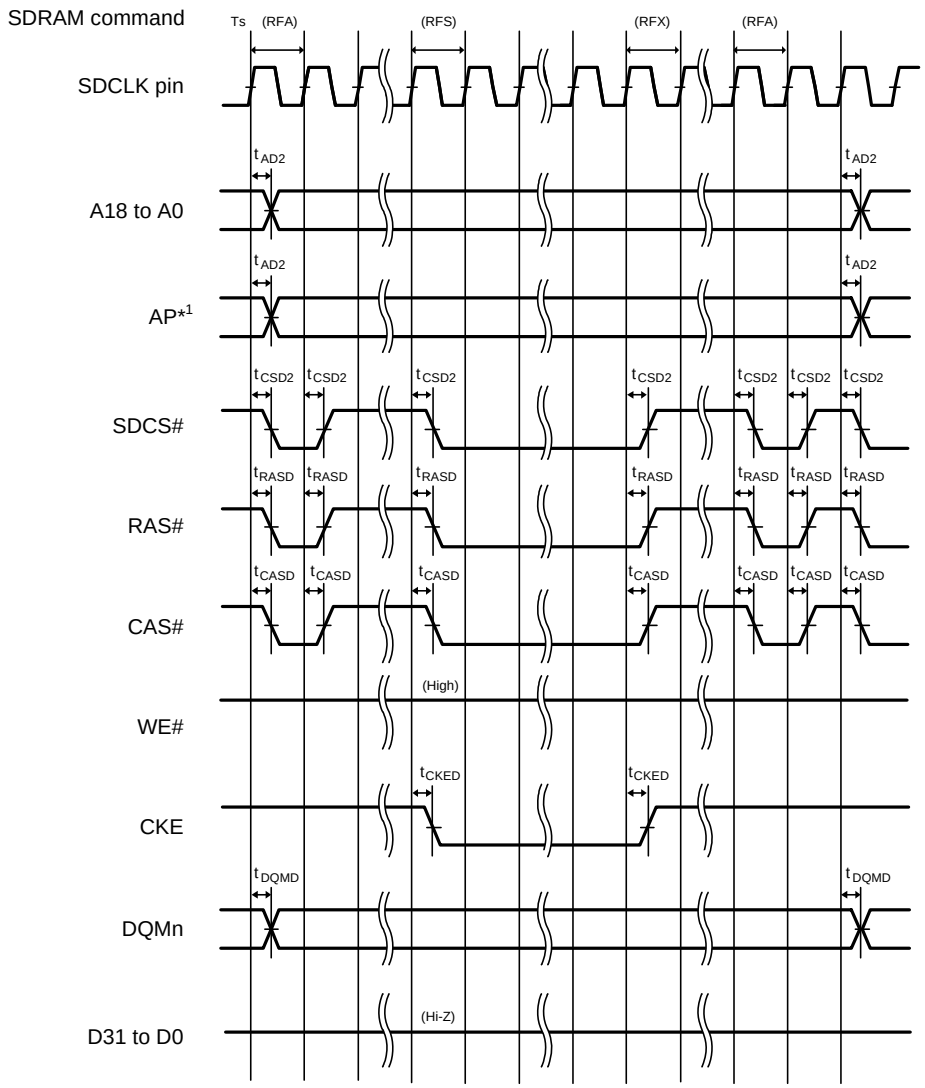
Conditions: VCC = AVCC0 = VREFH = VCC_USB = V_{BATT} = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0,
VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V, $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
NMI pulse width	t_{NMIW}	200	—	—	ns	tc (PCLK) × 2 ≤ 200 ns Figure 5.15
		tc (PCLK) × 2				tc (PCLK) × 2 > 200 ns Figure 5.15
IRQ pulse width	t_{IRQW}	200	—	—	ns	tc (PCLK) × 2 ≤ 200 ns Figure 5.16
		tc (PCLK) × 2				tc (PCLK) × 2 > 200 ns Figure 5.16



Note 1: Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

Figure 5.27 SDRAM Space Multiple Write Bus Timing



Note 1: Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

Figure 5.30 SDRAM Space Self-Refresh Bus Timing

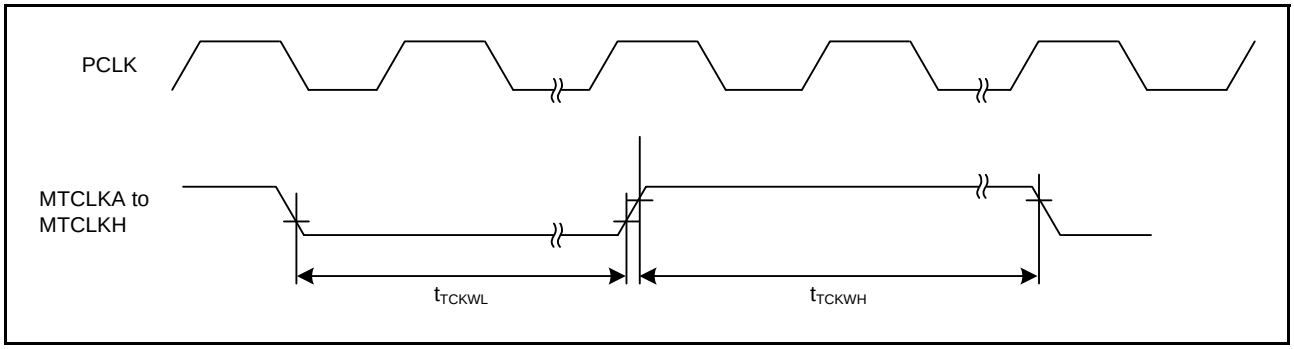


Figure 5.36 MTU Clock Input Timing

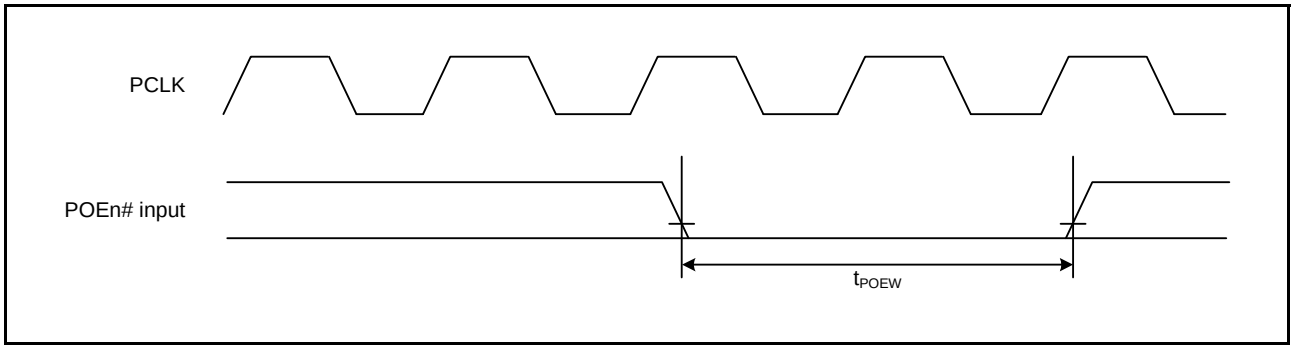


Figure 5.37 POE# Input Timing

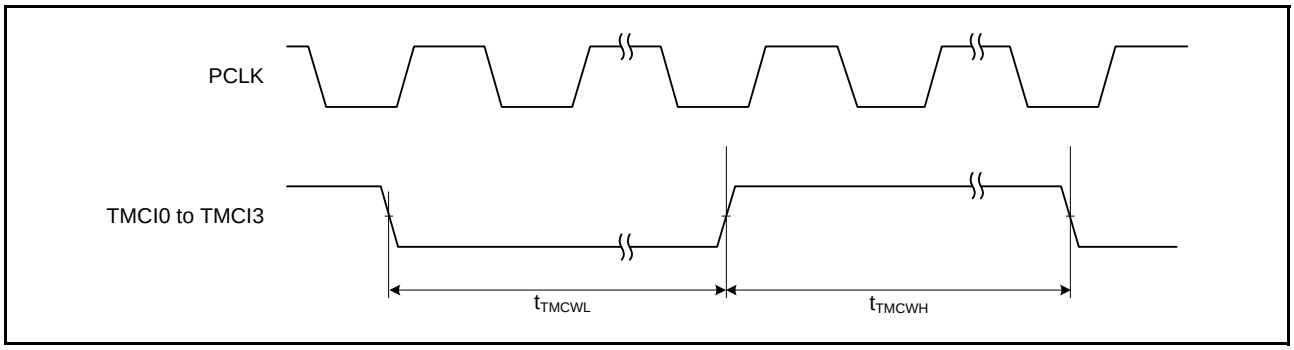


Figure 5.38 8-Bit Timer Clock Input Timing

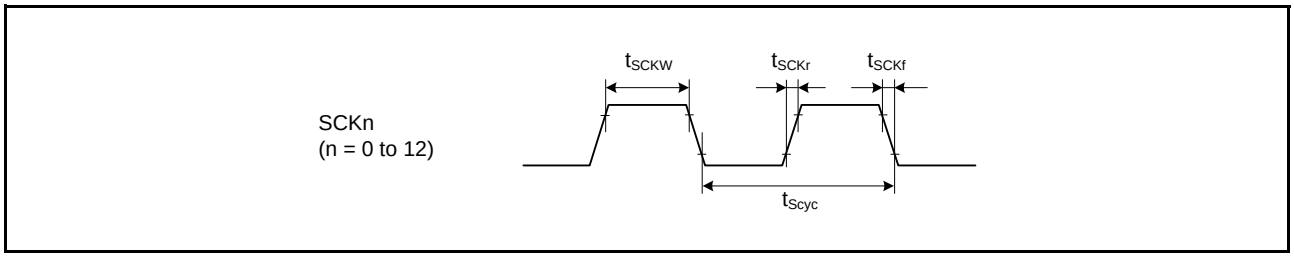
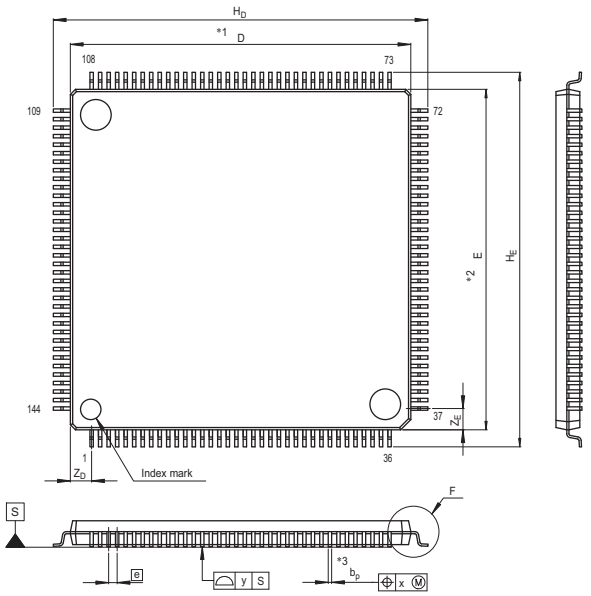
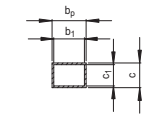


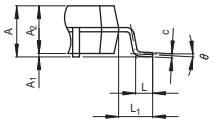
Figure 5.39 SCK Clock Input Timing

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP144-20x20-0.50	PLQP0144KA-A	144P6Q-A / FP-144L / FP-144LV	1.2g





Terminal cross section



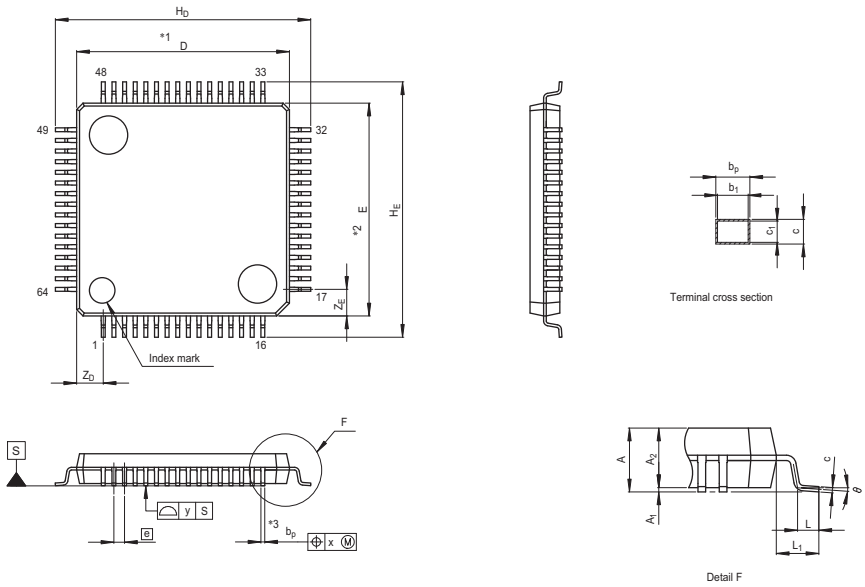
Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	19.9	20.0	20.1
E	19.9	20.0	20.1
A_2	—	1.4	—
H_D	21.8	22.0	22.2
H_E	21.8	22.0	22.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.17	0.22	0.27
b_1	—	0.20	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.10
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.35	0.5	0.65
L_1	—	1.0	—

Figure E 144-pin LQFP (PLQP0144KA-A)

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP64-10x10-0.50	PLQP0064KB-A	64P6Q-A / FP-64K / FP-64KV	0.3g

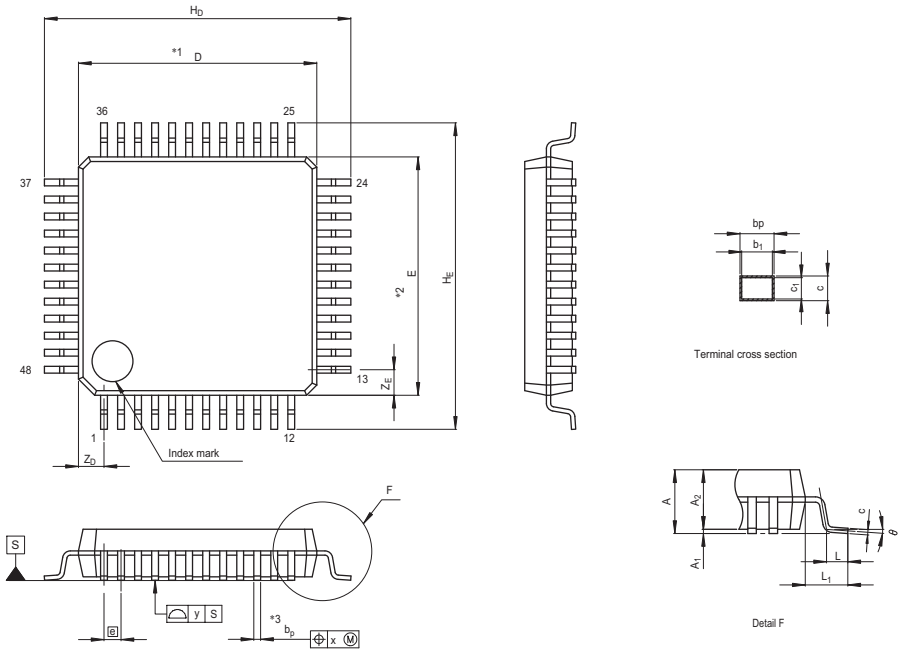


NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A_2	—	1.4	—
H_D	11.8	12.0	12.2
H_E	11.8	12.0	12.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.35	0.5	0.65
L_1	—	1.0	—

Figure I 64-pin LQFP (PLQP0064KB-A)

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP48-7x7-0.50	PLQP0048KB-A	48P6Q-A	0.2g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.9	7.0	7.1
E	6.9	7.0	7.1
A_2	—	1.4	—
H_D	8.8	9.0	9.2
H_E	8.8	9.0	9.2
A	—	—	1.7
A_1	0	0.1	0.2
b_p	0.17	0.22	0.27
b_1	—	0.20	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.10
Z_D	—	0.75	—
Z_E	—	0.75	—
L	0.35	0.5	0.65
L_1	—	1.0	—

Figure J 48-pin LQFP (PLQP0048KB-A)