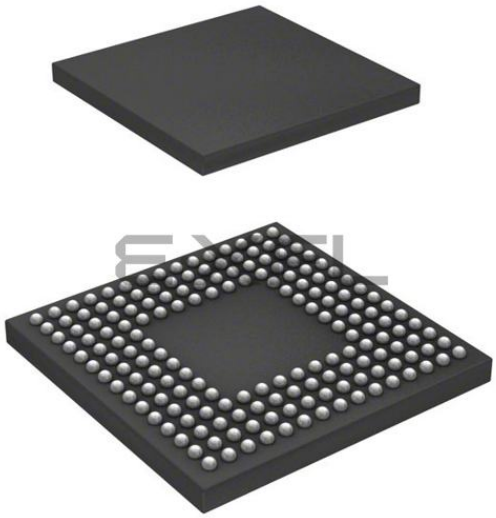
Renesas Electronics America Inc - R5F563NACDBG#U0 Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, LINbus, SCI, SPI, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	133
Program Memory Size	768KB (768K x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b, 21x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LFBGA
Supplier Device Package	176-LFBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f563nacdbg-u0

Table 1.1 Outline of Specifications (5/6)

Classification	Module/Function	Description
Communication function	Ethernet controller (ETHERC)	• Input and output of Ethernet/IEEE 802.3 frames • Transfer at 10 or 100 Mbps • Full- and half-duplex modes • MII (Media Independent Interface) or RMII (Reduced Media Independent Interface) as defined in IEEE 802.3u • Detection of Magic Packets™*1 or output of a "wake-on-LAN" signal (WOL) • Compliance with flow control as defined in IEEE 802.3x standards Note 1. Magic PacketTM is a registered trademark of Advanced Micro Devices, Inc.
	DMA controller for Ethernet controller (EDMAC)	• Alleviation of CPU loads by the descriptor control method • Transmission FIFO: 2 Kbytes; Reception FIFO: 2 Kbytes
	USB 2.0 host/function module (USBa)	• Includes a UDC (USB Device Controller) and transceiver for USB 2.0 • Host/function module: one port, function module: one port • Compliance with the USB 2.0 specification • Transfer rate: Full speed (12 Mbps) • Self-power mode and bus-power mode are selectable • OTG (On the Go) operation is possible • Incorporates 2 Kbytes of RAM as a transfer buffer
	Serial communications interfaces (SCIc, SCId)	• 13 channels (SCIc: 12 channels + SCId: 1 channel) • SCIc Serial communications modes: Asynchronous, clock synchronous, and smart-card interface Multi-processor function On-chip baud rate generator allows selection of the desired bit rate Choice of LSB-first or MSB-first transfer Average transfer rate clock can be input from TMR timers for SCI5, SCI6, and SCI12 Simple I^2C Simple SPI • SCId (The following functions are added to SCIc) Supports the serial communications protocol, which contains the start frame and information frame Supports the LIN format
	I^2C bus interfaces (RIIC)	• 4 channels (one of them is FM+) • Communication formats I^2C bus format/SMBus format Supports the multi-master Max. transfer rate: 1 Mbps (channel 0)
	IEBus (IEB)	• 1 channel • Supports protocol control for the IEBus Half-duplex asynchronous transfer Multi-master operation Broadcast communications function Two selectable modes, differentiated by transfer rate
	CAN module (CAN)	• 3 channels • Compliance with the ISO11898-1 specification (standard frame and extended frame) • 32 mailboxes each
	Serial peripheral interfaces (SPI)	• 3 channels • RSPI transfer facility Using the MOSI (master out, slave in), MISO (master in, slave out), SSL (slave select), and RSPCK (RSPI clock) signals enables serial transfer through SPI operation (four lines) or clock-synchronous operation (three lines) Capable of handling serial transfer as a master or slave • Data formats Switching between MSB first and LSB first The number of bits in each transfer can be changed to any number of bits from 8 to 16, or to 20, 24, or 32 bits. 128-bit buffers for transmission and reception Up to four frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits) • Buffered structure Double buffers for both transmission and reception

Table 1.1 Outline of Specifications (6/6)

Classification	Module/Function	Description
Communication function	Parallel data capture unit (PDC)	• 1 channel • Communicates with an image sensor or other external I/Os and transfer parallel data such as an image output from those devices to internal RAM or external address spaces (CS space and SDRAM space) through DTC or DMAC.
12-bit A/D converter (S12ADa)		• 1 unit (1 unit x 21 channels) • 12-bit resolution • Conversion time: 1.0 μs per channel (in operation with PCLK at 50 MHz) • Operating mode Scan mode (single scan mode or continuous scan mode) • Sample-and-hold function • Reference voltage generation • Three ways to start A/D conversion Conversion can be started by software, a conversion start trigger from a timer (MTU, TPU, or TMR), or an external trigger signal. • A/D conversion of the temperature sensor output
10-bit A/D converter (ADb)		• 1 unit (1 unit x 8 channels) • 10-bit resolution • Conversion time: 1.0 μs per channel (in operation with PCLK at 50 MHz) • Operating mode Scan mode (single scan mode or continuous scan mode) External amplifier connection mode • Sample-and-hold function • Three ways to start A/D conversion Conversion can be started by software, a conversion start trigger from a timer (MTU, TPU, or TMR), or an external trigger signal.
D/A converter (DAa)		• 2 channels • 10-bit resolution • Output voltage: 0 V to VREFH
Temperature sensor		• 1 channel • Precision: ±1ºC • The voltage of the temperature is converted into a digital value by the 12-bit A/D converter.
CRC calculator (CRC)		• CRC code generation for arbitrary amounts of data in 8-bit units • Select any of three generating polynomials: $X^8 + X^2 + X + 1$, $X^{16} + X^{15} + X^2 + 1$, or $X^{16} + X^{12} + X^5 + 1$. • Generation of CRC codes for use with LSB-first or MSB-first communications is selectable
Unique ID		A 16-byte device-specific ID (only for the G version)
Data encryption unit (DEU)*1		• AES encryption and decryption functions • 128/192/256-bit key length • ECB/CBC mode
Operating frequency		Up to 100 MHz
Power supply voltage		VCC = AVCC0 = VREFH = VCC_USB = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0, V_{BATT} = 2.0 V to 3.6 V (for products with 100 or more pins), V_{BATT} = 2.3 V to 3.6 V (for the 64-pin product)
Operating temperature		D version: -40 to +85°C, G version: -40 to +105°C*2
Package		177-pin TFLGA (PTLG0177KA-A) 176-pin LFBGA (PLBG0176GA-A) 176-pin LQFP (PLQP0176KB-A) 145-pin TFLGA (PTLG0145KA-A) 144-pin LQFP (PLQP0144KA-A) 100-pin TFLGA (PTLG0100JA-A) (in the planning stage) 100-pin LQFP (PLQP0100KB-A) 64-pin TFLGA (PTLG0064JA-A) 64-pin LQFP (PLQP0064KB-A) 48-pin LQFP (PLQP0048KB-A)
On-chip debugging system		• E1 emulator (JTAG and FINE interfaces) • E20 emulator (JTAG interface)

Note 1. Please contact our sales office for more information.
Note 2. Please contact us if you are using a G version.

Table 1.3 List of Products (2/8)

Group	Part No.	Package	ROM Capacity	RAM Capacity	E2 Data Flash	Operating Frequency (Max.)	Operating Temp. Range
RX63N (D version)	R5F563NDDDLK	PTLG0145KA-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NBCDLK	PTLG0145KA-A	1 Mbyte	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NBDDLK	PTLG0145KA-A	1 Mbyte	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NACDLK	PTLG0145KA-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NADDLK	PTLG0145KA-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NFHDFB	PLQP0144KA-A	2 Mbytes	256 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NFDDFB	PLQP0144KA-A	2 Mbytes	256 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NKHDFB	PLQP0144KA-A*1	2 Mbytes	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NKDDFB	PLQP0144KA-A	2 Mbytes	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NECDFB	PLQP0144KA-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NEDDFB	PLQP0144KA-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NJHDFB	PLQP0144KA-A*1	1.5 Mbytes	256 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NJDDFB	PLQP0144KA-A*1	1.5 Mbytes	256 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NGHDFB	PLQP0144KA-A*1	1.5 Mbytes	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NGDDFB	PLQP0144KA-A*1	1.5 Mbytes	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NDCDFB	PLQP0144KA-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NDDDFB	PLQP0144KA-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NYHDFB	PLQP0144KA-A	1 Mbyte	256 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NYDDFB	PLQP0144KA-A	1 Mbyte	256 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NWHDFB	PLQP0144KA-A	1 Mbyte	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NWDDFB	PLQP0144KA-A	1 Mbyte	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NBCDFB	PLQP0144KA-A	1 Mbyte	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NBDDFB	PLQP0144KA-A	1 Mbyte	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NACDFB	PLQP0144KA-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NADDFB	PLQP0144KA-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NECDLJ	PTLG0100JA-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NEDDLJ	PTLG0100JA-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NDCDLJ	PTLG0100JA-A*1	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NDDDLJ	PTLG0100JA-A*1	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NBCDLJ	PTLG0100JA-A	1 Mbyte	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NBDDLJ	PTLG0100JA-A	1 Mbyte	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NACDLJ	PTLG0100JA-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NADDLJ	PTLG0100JA-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NFHDFP	PLQP0100KB-A	2 Mbytes	256 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NFDDFP	PLQP0100KB-A	2 Mbytes	256 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NKHDFP	PLQP0100KB-A*1	2 Mbytes	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NKDDFP	PLQP0100KB-A	2 Mbytes	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NECDFP	PLQP0100KB-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NEDDFP	PLQP0100KB-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NJHDFP	PLQP0100KB-A*1	1.5 Mbytes	256 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NJDDFP	PLQP0100KB-A*1	1.5 Mbytes	256 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NGHDFP	PLQP0100KB-A*1	1.5 Mbytes	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NGDDFP	PLQP0100KB-A*1	1.5 Mbytes	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NDCDFP	PLQP0100KB-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NDDDFP	PLQP0100KB-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C

Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (4/5)

Pin Number 177-Pin TFLGA 176-Pin LFBGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SCIc, SCId, RSPI, RIIC, CAN, IEB, USB, and PDC)	Interrupt	S12AD, AD, DA
M2		P26	CS6#	MTIOC2A/TMO1/PO6	TXD1/CTS3#/RTS3# SMOSI1/SS3#/SSDA1/ MOSIB		
M3		P24	CS4#/EDREQ1	MTIOC4A/MTCLKA/ TIOCB4/TMRI1/PO4	SCK3/USB0_VBUSEN/ PIXCLK		
M4		P86		TIOCA0	PIXD1		
M5		P13		MTIOC0B/TIOCA5/TMO3/ PO13	TXD2/SMOSI2/SSDA2/ SDA0[FM+]	IRQ3	ADTRG#
M6		P56	WR2#/BC2#/ EDACK1	MTIOC3C/TIOCA1			
M7		P54	ALE/EDACK0	MTIOC4B/TMCI1	ET_LINKSTA/CTS2#/ RTS2#/SS2#/CTX1		
M8		P53*2	BCLK				
M9		P50	WR0#/WR#		TXD2/SMOSI2/SSDA2/ SSLB1		
M10		PC5	A21/CS2#/ WAIT#	MTIOC3B/MTCLKD/ TIOCD6/TCLKF/TMRI2/ PO29	ET_ETXD2/SCK8/ RSPCKA		
M11		P81	EDACK0	MTIOC3D/PO27	ET_ETXD0/RMII_TXD0/ RXD10/SMISO10/SSCL10		
M12		P77	CS7#	PO23	ET_RX_ER/RMII_RX_ER/ TXD11/SMOSI11/SSDA11		
M13		PB7	A15	MTIOC3B/TIOCB5/PO31	ET_CRS/RMII_CRS_DV/ TXD9/SMOSI9/SSDA9		
M14		PB5	A13	MTIOC2A/MTIOC1B/ TIOCB4/TMRI1/PO29/ POE1#	ET_ETXD0/RMII_TXD0/ SCK9		
M15		PB4	A12	TIOCA4/PO28	ET_TX_EN/ RMII_TXD_EN/CTS9#/ RTS9#/SS9#		
N1	VCC						
N2		P23	EDACK0	MTIOC3D/MTCLKD/ TIOCD3/PO3	TXD3/CTS0#/RTS0#/ SMOSI3/SS0#/SSDA3/ USB0_DPUPE/PIXD7		
N3		P22	EDREQ0	MTIOC3B/MTCLKC/ TIOCC3/TMO0/PO2	SCK0/USB0_DRPD/ PIXD6		
N4		P15		MTIOC0B/MTCLKB/ TIOCB2/TCLKB/TMCI2/ PO13	RXD1/SCK3/SMISO1/ SSCL1/CRX1-DS/ USB1_DPUPE/PIXD0	IRQ5	
N5		P12		MTIC5U/TMCI1	RXD2/SMISO2/SSCL2/ SCL0[FM+]	IRQ2	
N6		P57	WAIT#/WR3#/ BC3#/EDREQ1				
N7		P55	WAIT#/ EDREQ0	MTIOC4D/TMO3	ET_EXOUT/CRX1	IRQ10	
N8	VCC_USB						
N9		P51	WR1#/BC1#/ WAIT#		SCK2/SSLB2		
N10		PC7	A23/CS0#	MTIOC3A/MTCLKB/ TIOCB6/TMO2/PO31	ET_COL/TXD8/SMOSI8/ SSDA8/MISOA	IRQ14	
N11		P82	EDREQ1	MTIOC4A/PO28	ET_ETXD1/RMII_TXD1/ TXD10/SMOSI10/SSDA10		
N12		PC3	A19	MTIOC4D/TCLKB/PO24	ET_TX_ER/TXD5/ SMOSI5/SSDA5/IETXD		
N13		PC0	A16	MTIOC3C/TCLKC/PO17	ET_ERXD3/CTS5#/ RTS5#/SS5#/SSLA1/ SCL3	IRQ14	
N14		P73	CS3#	PO16	ET_WOL		
N15	VSS						

Table 1.7 List of Pins and Pin Functions (145-Pin TFLGA) (3/5)

Pin No. 145-pin TFLGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timers (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SCIc, SCId, RSPI, RIIC, CAN, IEB, USB, and PDC)	Interrupt	S12AD AD DA
H12		PB0	A8	MTIC5W/TIOCA3/PO24	RXD4/RXD6/SMISO4/ SMISO6/SSCL4/SSCL6/ RSPCKA/T_ERXD1/ RMII_RXD1	IRQ12	
H13		PA7	A7	TIOCB2/PO23	MISOA/ET_WOL		
J1	TRST#	P34		MTIOC0A/TMCI3/PO12/ POE2#	SCK6/SCK0/ USB0_DPRPD	IRQ4	
J2		P33		MTIOC0D/TIOCD0/ TMRI3/PO11/POE3#	RXD6/RXD0/SMISO6/ SMISO0/SSCL6/SSCL0/ CRX0/PCKO	IRQ3-DS	
J3		P32		MTIOC0C/TIOCC0/ TMO3/PO10/RTCOUT/ RTCIC2	TXD6/TXD0/SMOSI6/ SMOSI0/SSDA6/SSDA0/ CTX0/USB0_VBUSEN/ VSYNC	IRQ2-DS	
J4	TDI	P30		MTIOC4B/TMRI3/PO8/ RTCIC0/POE8#	RXD1/SMISO1/SSCL1/ MISOB/USB0_DRPD	IRQ0-DS	
J10		PB3	A11	MTIOC0A/MTIOC4A/ TIOCD3/TCLKD/TMO0/ PO27/POE3#	SCK4/SCK6/ET_RX_ER/ RMII_RX_ER		
J11		PB4	A12	TIOCA4/PO28	CTS9#/RTS9#/SS9#/ ET_TX_EN/RMII_TXD_EN		
J12		PB2	A10	TIOCC3/TCLKC/PO26	CTS4#/RTS4#/CTS6#/ RTS6#/SS4#/SS6#/ ET_RX_CLK/REF50CK		
J13		PB1	A9	MTIOC0C/MTIOC4C/ TIOCB3/TMCI0/PO25	TXD4/TXD6/SMOSI4/ SMOSI6/SSDA4/SSDA6/ ET_ERXD0/RMII_RXD0	IRQ4-DS	
K1	TCK/FINEC	P27	CS7#	MTIOC2B/TMCI3/PO7	SCK1/RSPCKB		
K2	TDO	P26	CS6#	MTIOC2A/TMO1/PO6	TXD1/CTS3#/RTS3#/ SMOSI1/SS3#/SSDA1/ MOSIB		
K3	TMS	P31		MTIOC4D/TMCI2/PO9/ RTCIC1	CTS1#/RTS1#/SS1#/ SSLB0/USB0_DPUPE	IRQ1-DS	
K4		P15		MTIOC0B/MTCLKB/ TIOCB2/TCLKB/TMCI2/ PO13	RXD1/SCK3/SMISO1/ SSCL1/CRX1-DS/PIXD0	IRQ5	
K5	TRDATA2	P54	ALE/EDACK0	MTIOC4B/TMCI1	CTS2#/RTS2#/SS2#/ CTX1/ET_LINKSTA		
K6		P53*1	BCLK				
K7		P51	WR1#/BC1#/ WAIT#		SCK2/SSLB2		
K8	VCC						
K9	TRDATA0	P80	EDREQ0	MTIOC3B/PO26	SCK10/ET_TX_EN/ RMII_TXD_EN		
K10		P76	CS6#	PO22	RXD11/SMISO11/SSCL11/ ET_RX_CLK/REF50CK		
K11		PB7	A15	MTIOC3B/TIOCB5/ PO31	TXD9/SMOSI9/SSDA9/ ET_CRS/RMII_CRS_DV		
K12		PB6	A14	MTIOC3D/TIOCA5/ PO30	RXD9/SMISO9/SSCL9/ ET_ETXD1/RMII_TXD1		
K13		PB5	A13	MTIOC2A/MTIOC1B/ TIOCB4/TMRI1/PO29/ POE1#	SCK9/ET_ETXD0/ RMII_TXD0		
L1		P25	CS5#/EDACK1	MTIOC4C/MTCLKB/ TIOCA4/PO5	RXD3/SMISO3/SSCL3/ USB0_DPRPD/HSYNC		ADTRG0#
L2		P23	EDACK0	MTIOC3D/MTCLKD/ TIOCD3/PO3	TXD3/CTS0#/RTS0#/ SMOSI3/SS0#/SSDA3/ USB0_DPUPE/PIXD7		

Table 1.8 List of Pins and Pin Functions (144-Pin LQFP) (4/5)

Pin No. 144-pin LQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timers (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SCIc, SCId, RSPI, RIIC, CAN, IEB, USB, and PDC)	Interrupt	S12AD AD DA
89		PA6	A6	MTIC5V/MTCLKB/ TIOCA2/TMCI3/PO22/ POE2#	CTS5#/RTS5#/SS5# MOSIA/ET_EXOUT		
90		PA5	A5	TIOCB1/PO21	RSPCKA/ET_LINKSTA		
91	VCC						
92		PA4	A4	MTIC5U/MTCLKA/ TIOCA1/TMRI0/PO20	TXD5/SMOSI5/SSDA5/ SSLA0/ET_MDC	IRQ5-DS	
93	VSS						
94		PA3	A3	MTIOC0D/MTCLKD/ TIOCD0/TCLKB/PO19	RXD5/SMISO5/SSCL5/ ET_MDIO	IRQ6-DS	
95		PA2	A2	PO18	RXD5/SMISO5/SSCL5/ SSLA3		
96		PA1	A1	MTIOC0B/MTCLKC/ TIOCB0/PO17	SCK5/SSLA2/ET_WOL	IRQ11	
97		PA0	A0/BC0#	MTIOC4A/TIOCA0/ PO16	SSLA1/ET_TX_EN/ RMII_TXD_EN		
98		P67	CS7#/DQM1		CRX2*2	IRQ15	
99		P66	CS6#/DQM0		CTX2*2		
100		P65	CS5#/CKE				
101		PE7	D15[A15/D15]	TIOCB11	MISOB	IRQ7	AN5
102		PE6	D14[A14/D14]	TIOCA11	MOSIB	IRQ6	AN4
103	VCC						
104	SDCLK	P70					
105	VSS						
106		PE5	D13[A13/D13]	MTIOC4C/MTIOC2B/ TIOCB10	RSPCKB/ET_RX_CLK/ REF50CK	IRQ5	AN3
107		PE4	D12[A12/D12]	MTIOC4D/MTIOC1A/ TIOCA10/PO28	SSLB0/ET_ERXD2		AN2
108		PE3	D11[A11/D11]	MTIOC4B/TIOCB9/ PO26/POE8#	CTS12#/RTS12#/ SS12#/MISOB/ ET_ERXD3		AN1
109		PE2	D10[A10/D10]	MTIOC4A/TIOCA9/ PO23	RXD12/SMISO12/ SSCL12/RXDX12/ SSLB3/MOSIB	IRQ7-DS	AN0
110		PE1	D9[A9/D9]	MTIOC4C/TIOCD9/ PO18	TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12/SSLB2/ RSPCKB		ANEX1
111		PE0	D8[A8/D8]	TIOCC9	SCK12/SSLB1		ANEX0
112		P64	CS4#/WE#				
113		P63	CS3#/CAS#				
114		P62	CS2#/RAS#				
115		P61	CS1#/SDCS#				
116	VSS						
117		P60	CS0#				
118	VCC						
119		PD7	D7[A7/D7]	MTIC5U/POE0#	SSLC3	IRQ7	AN7
120		PD6	D6[A6/D6]	MTIC5V/POE1#	SSLC2	IRQ6	AN6
121		PD5	D5[A5/D5]	MTIC5W/POE2#	SSLC1	IRQ5	AN013
122		PD4	D4[A4/D4]	POE3#	SSLC0	IRQ4	AN012
123		PD3	D3[A3/D3]	TIOCB8/TCLKH/ POE8#	RSPCKC	IRQ3	AN011
124		PD2	D2[A2/D2]	MTIOC4D/TIOCA8	MISOC/CRX0	IRQ2	AN010

Table 1.9 List of Pins and Pin Functions (100-Pin TFLGA) (3/5)

Pin No. 100-pin TFLGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC	Timers (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SCIc, SCId, RSPI, RIIC, CAN, IEB, USB)	Interrupt	S12AD AD DA
F7		PB2	A10	TIOCC3/ TCLKC/PO26	CTS6#/RTS6#/ SS6#/ET_RX_CLK/ REF50CK		
F8		PB0	A8	MTIC5W/ TIOCA3/PO24	RXD6/SMISO6/ SSCL6/RSPCKA/ ET_ERXD1/ RMII_RXD1	IRQ12	
F9		PA7	A7	TIOCB2/PO23	MISOA/ET_WOL		
F10	VSS						
G1		P33		MTIOC0D/ TIOCD0/ TMRI3/PO11/ POE3#	RXD6/RXD0/ SMISO6/SMISO0/ SSCL6/SSCL0/ CRX0*1	IRQ3-DS	
G2	TMS	P31		MTIOC4D/ TMCI2/PO9/ RTCIC1	CTS1#/RTS1#/ SS1#/SSLB0/ USB0_DPUPE	IRQ1-DS	
G3	TDI	P30		MTIOC4B/ TMRI3/PO8/ RTCIC0/POE8#	RXD1/SMISO1/ SSCL1/MISOB/ USB0_DRPD	IRQ0-DS	
G4	TCK/FINEC	P27	CS7#	MTIOC2B/ TMCI3/PO7	SCK1/RSPCKB		
G5	BCLK	P53*2					
G6		P52	RD#		RXD2/SMISO2/ SSCL2/SSLB3		
G7		PB5	A13	MTIOC2A/ MTIOC1B/ TIOCB4/ TMRI1/PO29/ POE1#	SCK9/ET_ETXD0/ RMII_TXD0		
G8		PB4	A12	TIOCA4/PO28	CTS9#/RTS9#/ SS9#/ET_TX_EN/ RMII_TXD_EN		
G9		PB1	A9	MTIOC0C/ MTIOC4C/ TIOCB3/ TMCI0/PO25	TXD6/SMOSI6/ SSDA6/ET_ERXD0/ RMII_RXD0	IRQ4-DS	
G10	VCC						
H1	TDO	P26	CS6#	MTIOC2A/ TMO1/PO6	TXD1/CTS3#/ RTS3#/SMOSI1/ SS3#/SSDA1/ MOSIB		
H2		P25	CS5#/ EDACK1	MTIOC4C/ MTCLKB/ TIOCA4/PO5	RXD3/SMISO3/ SSCL3/ USB0_DPRPD		ADTRG0#
H3		P16		MTIOC3C/ MTIOC3D/ TIOCB1/ TCLKC/TMO2/ PO14/RTCOUT	TXD1/RXD3/ SMOSI1/SMISO3/ SSDA1/SSCL3/ MOSIA/SCL2-DS/ IERXD/ USB0_VBUS/ USB0_VBUSEN/ USB0_OVRCURB	IRQ6	ADTRG0#

Table 1.12 List of Pins and Pin Functions (64-Pin LQFP) (1/3)

Pin Number 64-Pin LQFP	Power Supply Clock System Control	I/O Port	Timer (MTU2a, TPUa, TMR, PPG, RTCa, POE2a)	Timer Communications (SCIc, SCId, RSPI, RIIC, CAN, IEB, USB)	Interrupt	S12ADa, DAa
1	EMLE					
2	VCL					
3	MD/FINED					
4	XCIN					
5	XCOUT					
6	RES#					
7	XTAL	P37				
8	VSS					
9	EXTAL	P36				
10	VCC					
11		P35			NMI	
12	VBATT					
13		P31	MTIOC4D/TMCI2/PO9/ RTCIC1	CTS1#/RTS1#/SS1#/ SSLB0/USB0_DPUPE	IRQ1-DS	
14	TDI	P30	MTIOC4B/TMRI3/PO8/ POE8#/RTCIC0	RXD1/SMISO1/SSCL1/ MISOB/USB0_DRPD	IRQ0-DS	
15	TCK/FINEC	P27	MTIOC2B/TMCI3/PO7	SCK1/RSPCKB		
16	TDO	P26	MTIOC2A/TMO1/PO6	TXD1/SMOSI1/SSDA1/ MOSIB/USB0_VBUSEN		
17	TRST#	P17	MTIOC3A/MTIOC3B/ TIOCB0/TCLKD/TMO1/ PO15/POE8#	SCK1/MISOA/ SDA2-DS/IETXD	IRQ7	
18	TMS	P16	MTIOC3C/MTIOC3D/ TIOCB1/TCLKC/TMO2/ PO14/RTCOUT	TXD1/SMOSI1/SSDA1/ MOSIA/SCL2-DS/IERXD/ USB0_VBUS/ USB0_VBUSEN/ USB0_OVRCURB	IRQ6	ADTRG0#
19		P15	MTIOC0B/MTCLKB/ TIOCB2/TCLKB/TMCI2/ PO13	RXD1/SMISO1/SSCL1/ CRX1-DS	IRQ5	
20		P14	MTIOC3A/MTCLKA/ TIOCB5/TCLKA/TMRI2/ PO15	CTS1#/RTS1#/SS1#/ CTX1/USB0_DPUPE/ USB0_OVRCURA	IRQ4	
21	VCC_USB					
22				USB0_DM		
23				USB0_DP		
24	VSS_USB					
25		P55	MTIOC4D/TMO3	CRX1	IRQ10	
26		P54	MTIOC4B/TMCI1	CTX1		
27		PC7	MTIOC3A/ MTCLKB/TMO2 /PO31	TXD8/SMOSI8/SSDA8/ MISOA	IRQ14	
28		PC6	MTIOC3C/MTCLKA/ TMCI2/PO30	RXD8/SMISO8/SSCL8/ MOSIA/USB0_EXICEN	IRQ13	
29		PC5	MTIOC3B/MTCLKD/ TMRI2/PO29	SCK8/RSPCKA/USB0_ID		
30		PC4	MTIOC3D/MTCLKC/ TMCI1/PO25/POE0#	SCK5/CTS8#/RTS8#/SS8#/ SSLA0/USB0_DPRPD		
31		PC3	MTIOC4D/TCLKB/ PO24	TXD5/SMOSI5/SSDA5/ IETXD		

Table 4.1 List of I/O Registers (Address Order) (4/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 3072h	BSC	CS7 mode register	CS7MOD	16	16	1, 2 BCLK		Buses
0008 3074h	BSC	CS7 wait control register 1	CS7WCR1	32	32	1, 2 BCLK		
0008 3078h	BSC	CS7 wait control register 2	CS7WCR2	32	32	1, 2 BCLK		
0008 3802h	BSC	CS0 control register	CS0CR	16	16	1, 2 BCLK		
0008 380Ah	BSC	CS0 recovery cycle register	CS0REC	16	16	1, 2 BCLK		
0008 3812h	BSC	CS1 control register	CS1CR	16	16	1, 2 BCLK		
0008 381Ah	BSC	CS1 recovery cycle register	CS1REC	16	16	1, 2 BCLK		
0008 3822h	BSC	CS2 control register	CS2CR	16	16	1, 2 BCLK		
0008 382Ah	BSC	CS2 recovery cycle register	CS2REC	16	16	1, 2 BCLK		
0008 3832h	BSC	CS3 control register	CS3CR	16	16	1, 2 BCLK		
0008 383Ah	BSC	CS3 recovery cycle register	CS3REC	16	16	1, 2 BCLK		
0008 3842h	BSC	CS4 control register	CS4CR	16	16	1, 2 BCLK		
0008 384Ah	BSC	CS4 recovery cycle register	CS4REC	16	16	1, 2 BCLK		
0008 3852h	BSC	CS5 control register	CS5CR	16	16	1, 2 BCLK		
0008 385Ah	BSC	CS5 recovery cycle register	CS5REC	16	16	1, 2 BCLK		
0008 3862h	BSC	CS6 control register	CS6CR	16	16	1, 2 BCLK		
0008 386Ah	BSC	CS6 recovery cycle register	CS6REC	16	16	1, 2 BCLK		
0008 3872h	BSC	CS7 control register	CS7CR	16	16	1, 2 BCLK		
0008 387Ah	BSC	CS7 recovery cycle register	CS7REC	16	16	1, 2 BCLK		
0008 3880h	BSC	CS recovery cycle insertion enable register	CSRECEN	16	16	1, 2 BCLK		
0008 3C00h	BSC	SDC control register	SDCCR	8	8	1, 2 BCLK		
0008 3C01h	BSC	SDC mode register	SDCMOD	8	8	1, 2 BCLK		
0008 3C02h	BSC	SDRAM access mode register	SDAMOD	8	8	1, 2 BCLK		
0008 3C10h	BSC	SDRAM self-refresh control register	SDSELF	8	8	1, 2 BCLK		
0008 3C14h	BSC	SDRAM refresh control register	SDRFCR	16	16	1, 2 BCLK		
0008 3C16h	BSC	SDRAM auto-refresh control register	SDRFEN	8	8	1, 2 BCLK		
0008 3C20h	BSC	SDRAM initialization sequence control register	SDICR	8	8	1, 2 BCLK		
0008 3C24h	BSC	SDRAM initialization register	SDIR	16	16	1, 2 BCLK		
0008 3C40h	BSC	SDRAM address register	SDADR	8	8	1, 2 BCLK		
0008 3C44h	BSC	SDRAM timing register	SDTR	32	32	1, 2 BCLK		
0008 3C48h	BSC	SDRAM mode register	SDMOD	16	16	1, 2 BCLK		
0008 3C50h	BSC	SDRAM status register	SDSR	8	8	1, 2 BCLK		
0008 6400h	MPU	Region-0 start page number register	RSPAGE0	32	32	1 ICLK		MPU
0008 6404h	MPU	Region-0 end page number register	REPAGE0	32	32	1 ICLK		
0008 6408h	MPU	Region-1 start page number register	RSPAGE1	32	32	1 ICLK		
0008 640Ch	MPU	Region-1 end page number register	REPAGE1	32	32	1 ICLK		
0008 6410h	MPU	Region-2 start page number register	RSPAGE2	32	32	1 ICLK		
0008 6414h	MPU	Region-2 end page number register	REPAGE2	32	32	1 ICLK		
0008 6418h	MPU	Region-3 start page number register	RSPAGE3	32	32	1 ICLK		
0008 641Ch	MPU	Region-3 end page number register	REPAGE3	32	32	1 ICLK		
0008 6420h	MPU	Region-4 start page number register	RSPAGE4	32	32	1 ICLK		
0008 6424h	MPU	Region-4 end page number register	REPAGE4	32	32	1 ICLK		
0008 6428h	MPU	Region-5 start page number register	RSPAGE5	32	32	1 ICLK		
0008 642Ch	MPU	Region-5 end page number register	REPAGE5	32	32	1 ICLK		
0008 6430h	MPU	Region-6 start page number register	RSPAGE6	32	32	1 ICLK		
0008 6434h	MPU	Region-6 end page number register	REPAGE6	32	32	1 ICLK		
0008 6438h	MPU	Region-7 start page number register	RSPAGE7	32	32	1 ICLK		
0008 643Ch	MPU	Region-7 end page number register	REPAGE7	32	32	1 ICLK		
0008 6500h	MPU	Memory-protection enable register	MPEN	32	32	1 ICLK		
0008 6504h	MPU	Background access control register	MPBAC	32	32	1 ICLK		
0008 6508h	MPU	Memory-protection error status-clearing register	MPECLR	32	32	1 ICLK		

Table 4.1 List of I/O Registers (Address Order) (10/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 719Ch	ICU	DTC activation enable register 156	DTCER156	8	8	2 ICLK		ICUb
0008 719Dh	ICU	DTC activation enable register 157	DTCER157	8	8	2 ICLK		
0008 719Eh	ICU	DTC activation enable register 158	DTCER158	8	8	2 ICLK		
0008 719Fh	ICU	DTC activation enable register 159	DTCER159	8	8	2 ICLK		
0008 71A0h	ICU	DTC activation enable register 160	DTCER160	8	8	2 ICLK		
0008 71A1h	ICU	DTC activation enable register 161	DTCER161	8	8	2 ICLK		
0008 71A2h	ICU	DTC activation enable register 162	DTCER162	8	8	2 ICLK		
0008 71A3h	ICU	DTC activation enable register 163	DTCER163	8	8	2 ICLK		
0008 71A4h	ICU	DTC activation enable register 164	DTCER164	8	8	2 ICLK		
0008 71A5h	ICU	DTC activation enable register 165	DTCER165	8	8	2 ICLK		
0008 71AAh	ICU	DTC activation enable register 170	DTCER170	8	8	2 ICLK		
0008 71ABh	ICU	DTC activation enable register 171	DTCER171	8	8	2 ICLK		
0008 71ADh	ICU	DTC activation enable register 173	DTCER173	8	8	2 ICLK		
0008 71AEh	ICU	DTC activation enable register 174	DTCER174	8	8	2 ICLK		
0008 71B0h	ICU	DTC activation enable register 176	DTCER176	8	8	2 ICLK		
0008 71B1h	ICU	DTC activation enable register 177	DTCER177	8	8	2 ICLK		
0008 71B3h	ICU	DTC activation enable register 179	DTCER179	8	8	2 ICLK		
0008 71B4h	ICU	DTC activation enable register 180	DTCER180	8	8	2 ICLK		
0008 71B7h	ICU	DTC activation enable register 183	DTCER183	8	8	2 ICLK		
0008 71B8h	ICU	DTC activation enable register 184	DTCER184	8	8	2 ICLK		
0008 71BBh	ICU	DTC activation enable register 187	DTCER187	8	8	2 ICLK		
0008 71BCh	ICU	DTC activation enable register 188	DTCER188	8	8	2 ICLK		
0008 71BFh	ICU	DTC activation enable register 191	DTCER191	8	8	2 ICLK		
0008 71C0h	ICU	DTC activation enable register 192	DTCER192	8	8	2 ICLK		
0008 71C3h	ICU	DTC activation enable register 195	DTCER195	8	8	2 ICLK		
0008 71C4h	ICU	DTC activation enable register 196	DTCER196	8	8	2 ICLK		
0008 71C6h	ICU	DTC activation enable register 198	DTCER198	8	8	2 ICLK		
0008 71C7h	ICU	DTC activation enable register 199	DTCER199	8	8	2 ICLK		
0008 71C8h	ICU	DTC activation enable register 200	DTCER200	8	8	2 ICLK		
0008 71C9h	ICU	DTC activation enable register 201	DTCER201	8	8	2 ICLK		
0008 71CAh	ICU	DTC activation enable register 202	DTCER202	8	8	2 ICLK		
0008 71CBh	ICU	DTC activation enable register 203	DTCER203	8	8	2 ICLK		
0008 71CEh	ICU	DTC activation enable register 206	DTCER206	8	8	2 ICLK		
0008 71CFh	ICU	DTC activation enable register 207	DTCER207	8	8	2 ICLK		
0008 71D0h	ICU	DTC activation enable register 208	DTCER208	8	8	2 ICLK		
0008 71D6h	ICU	DTC activation enable register 214	DTCER214	8	8	2 ICLK		
0008 71D7h	ICU	DTC activation enable register 215	DTCER215	8	8	2 ICLK		
0008 71D9h	ICU	DTC activation enable register 217	DTCER217	8	8	2 ICLK		
0008 71DAh	ICU	DTC activation enable register 218	DTCER218	8	8	2 ICLK		
0008 71DCh	ICU	DTC activation enable register 220	DTCER220	8	8	2 ICLK		
0008 71DDh	ICU	DTC activation enable register 221	DTCER221	8	8	2 ICLK		
0008 71DFh	ICU	DTC activation enable register 223	DTCER223	8	8	2 ICLK		
0008 71E0h	ICU	DTC activation enable register 224	DTCER224	8	8	2 ICLK		
0008 71E2h	ICU	DTC activation enable register 226	DTCER226	8	8	2 ICLK		
0008 71E3h	ICU	DTC activation enable register 227	DTCER227	8	8	2 ICLK		
0008 71E5h	ICU	DTC activation enable register 229	DTCER229	8	8	2 ICLK		
0008 71E6h	ICU	DTC activation enable register 230	DTCER230	8	8	2 ICLK		
0008 71E8h	ICU	DTC activation enable register 232	DTCER232	8	8	2 ICLK		
0008 71E9h	ICU	DTC activation enable register 233	DTCER233	8	8	2 ICLK		
0008 71EBh	ICU	DTC activation enable register 235	DTCER235	8	8	2 ICLK		
0008 71ECh	ICU	DTC activation enable register 236	DTCER236	8	8	2 ICLK		

Table 4.1 List of I/O Registers (Address Order) (18/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 8200h	TMR0	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK	TMR
0008 8201h	TMR1	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK	
0008 8202h	TMR0	Timer control/status register	TCSR	8	8	2, 3 PCLKB	2 ICLK	
0008 8203h	TMR1	Timer control/status register	TCSR	8	8	2, 3 PCLKB	2 ICLK	
0008 8204h	TMR0	Time constant register A	TCORA	8	8	2, 3 PCLKB	2 ICLK	
0008 8205h	TMR1	Time constant register A	TCORA	8	8*5	2, 3 PCLKB	2 ICLK	
0008 8206h	TMR0	Time constant register B	TCORB	8	8	2, 3 PCLKB	2 ICLK	
0008 8207h	TMR1	Time constant register B	TCORB	8	8*5	2, 3 PCLKB	2 ICLK	
0008 8208h	TMR0	Timer counter	TCNT	8	8	2, 3 PCLKB	2 ICLK	
0008 8209h	TMR1	Timer counter	TCNT	8	8*5	2, 3 PCLKB	2 ICLK	
0008 820Ah	TMR0	Timer counter control register	TCCR	8	8	2, 3 PCLKB	2 ICLK	
0008 820Bh	TMR1	Timer counter control register	TCCR	8	8*5	2, 3 PCLKB	2 ICLK	
0008 8210h	TMR2	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK	
0008 8211h	TMR3	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK	
0008 8212h	TMR2	Timer control/status register	TCSR	8	8	2, 3 PCLKB	2 ICLK	
0008 8213h	TMR3	Timer control/status register	TCSR	8	8	2, 3 PCLKB	2 ICLK	
0008 8214h	TMR2	Time constant register A	TCORA	8	8	2, 3 PCLKB	2 ICLK	
0008 8215h	TMR3	Time constant register A	TCORA	8	8*5	2, 3 PCLKB	2 ICLK	
0008 8216h	TMR2	Time constant register B	TCORB	8	8	2, 3 PCLKB	2 ICLK	
0008 8217h	TMR3	Time constant register B	TCORB	8	8	2, 3 PCLKB	2 ICLK	
0008 8218h	TMR2	Timer counter	TCNT	8	8	2, 3 PCLKB	2 ICLK	
0008 8219h	TMR3	Timer counter	TCNT	8	8*5	2, 3 PCLKB	2 ICLK	
0008 821Ah	TMR2	Timer counter control register	TCCR	8	8	2, 3 PCLKB	2 ICLK	
0008 821Bh	TMR3	Timer counter control register	TCCR	8	8*5	2, 3 PCLKB	2 ICLK	
0008 8280h	CRC	CRC control register	CRCCR	8	8	2, 3 PCLKB	2 ICLK	CRC
0008 8281h	CRC	CRC data input register	CRCDIR	8	8	2, 3 PCLKB	2 ICLK	
0008 8282h	CRC	CRC data output register	CRCDOR	16	16	2, 3 PCLKB	2 ICLK	
0008 8300h	RIIC0	I^2C bus control register 1	ICCR1	8	8	2, 3 PCLKB	2 ICLK	RIIC
0008 8301h	RIIC0	I^2C bus control register 2	ICCR2	8	8	2, 3 PCLKB	2 ICLK	
0008 8302h	RIIC0	I^2C bus mode register 1	ICMR1	8	8	2, 3 PCLKB	2 ICLK	
0008 8303h	RIIC0	I^2C bus mode register 2	ICMR2	8	8	2, 3 PCLKB	2 ICLK	
0008 8304h	RIIC0	I^2C bus mode register 3	ICMR3	8	8	2, 3 PCLKB	2 ICLK	
0008 8305h	RIIC0	I^2C bus function enable register	ICFER	8	8	2, 3 PCLKB	2 ICLK	
0008 8306h	RIIC0	I^2C bus status enable register	ICSER	8	8	2, 3 PCLKB	2 ICLK	
0008 8307h	RIIC0	I^2C bus interrupt enable register	ICIER	8	8	2, 3 PCLKB	2 ICLK	
0008 8308h	RIIC0	I^2C bus status register 1	ICSR1	8	8	2, 3 PCLKB	2 ICLK	
0008 8309h	RIIC0	I^2C bus status register 2	ICSR2	8	8	2, 3 PCLKB	2 ICLK	
0008 830Ah	RIIC0	Slave address register L0	SARL0	8	8	2, 3 PCLKB	2 ICLK	
0008 830Ah	RIIC0	Timeout Internal Counter L	TMOCNTL	8	8	2, 3 PCLKB	2 ICLK	
0008 830Bh	RIIC0	Slave address register U0	SARU0	8	8	2, 3 PCLKB	2 ICLK	
0008 830Bh	RIIC0	Timeout Internal Counter U	TMOCNTU	8	8	2, 3 PCLKB	2 ICLK	
0008 830Ch	RIIC0	Slave address register L1	SARL1	8	8	2, 3 PCLKB	2 ICLK	
0008 830Dh	RIIC0	Slave address register U1	SARU1	8	8	2, 3 PCLKB	2 ICLK	
0008 830Eh	RIIC0	Slave address register L2	SARL2	8	8	2, 3 PCLKB	2 ICLK	
0008 830Fh	RIIC0	Slave address register U2	SARU2	8	8	2, 3 PCLKB	2 ICLK	
0008 8310h	RIIC0	I^2C bus bit rate low-level register	ICBRL	8	8	2, 3 PCLKB	2 ICLK	
0008 8311h	RIIC0	I^2C bus bit rate high-level register	ICBRH	8	8	2, 3 PCLKB	2 ICLK	
0008 8312h	RIIC0	I^2C bus transmit data register	ICDRT	8	8	2, 3 PCLKB	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (32/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 C114h	MPC	USB0 control register	PFUSB0	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C115h	MPC	USB1 control register	PFUSB1	8	8	2, 3 PCLKB	2 ICLK	
0008 C11Fh	MPC	Write-protect register	PWPR	8	8	2, 3 PCLKB	2 ICLK	
0008 C120h	PORT	Port switching register B	PSRB	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C121h	PORT	Port switching register A	PSRA	8	8	2, 3 PCLKB	2 ICLK	
0008 C140h	MPC	P00 pin function control register	P00PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C141h	MPC	P01 pin function control register	P01PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C142h	MPC	P02 pin function control register	P02PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C143h	MPC	P03 pin function control register	P03PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C145h	MPC	P05 pin function control register	P05PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C147h	MPC	P07 pin function control register	P07PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C148h	MPC	P10 pin function control register	P10PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C149h	MPC	P11 pin function control register	P11PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C14Ah	MPC	P12 pin function control register	P12PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C14Bh	MPC	P13 pin function control register	P13PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C14Ch	MPC	P14 pin function control register	P14PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C14Dh	MPC	P15 pin function control register	P15PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C14Eh	MPC	P16 pin function control register	P16PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C14Fh	MPC	P17 pin function control register	P17PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C150h	MPC	P20 pin function control register	P20PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C151h	MPC	P21 pin function control register	P21PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C152h	MPC	P22 pin function control register	P22PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C153h	MPC	P23 pin function control register	P23PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C154h	MPC	P24 pin function control register	P24PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C155h	MPC	P25 pin function control register	P25PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C156h	MPC	P26 pin function control register	P26PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C157h	MPC	P27 pin function control register	P27PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C158h	MPC	P30 pin function control register	P30PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C159h	MPC	P31 pin function control register	P31PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C15Ah	MPC	P32 pin function control register	P32PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C15Bh	MPC	P33 pin function control register	P33PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C15Ch	MPC	P34 pin function control register	P34PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C160h	MPC	P40 pin function control register	P40PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C161h	MPC	P41 pin function control register	P41PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C162h	MPC	P42 pin function control register	P42PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C163h	MPC	P43 pin function control register	P43PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C164h	MPC	P44 pin function control register	P44PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C165h	MPC	P45 pin function control register	P45PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C166h	MPC	P46 pin function control register	P46PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C167h	MPC	P47 pin function control register	P47PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C168h	MPC	P50 pin function control register	P50PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C169h	MPC	P51 pin function control register	P51PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C16Ah	MPC	P52 pin function control register	P52PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C16Ch	MPC	P54 pin function control register	P54PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C16Dh	MPC	P55 pin function control register	P55PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C16Eh	MPC	P56 pin function control register	P56PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C16Fh	MPC	P57 pin function control register	P57PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C170h	MPC	P60 pin function control register	P60PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C171h	MPC	P61 pin function control register	P61PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C176h	MPC	P66 pin function control register	P66PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C177h	MPC	P67 pin function control register	P67PFS	8	8	2, 3 PCLKB	2 ICLK	

5.2 DC Characteristics

Table 5.2 DC Characteristics (1)

Conditions: VCC = AVCC0 = VREFH = VCC_USB = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0,
VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V, $T_a = T_{opr}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	IRQ input pin*1 MTU input pin*1 TMR input pin*1 SCI input pin*1 ADTRG# input pin*1 RES#, NMI	V_{IH}	VCC × 0.8	—	VCC + 0.3	V	
		V_{IL}	–0.3	—	VCC × 0.2		
		ΔV_T	VCC × 0.06	—	—		
	RIIC input pin (except for SMBus)	V_{IH}	VCC × 0.7	—	5.8		
		V_{IL}	–0.3	—	VCC × 0.3		
		ΔV_T	VCC × 0.05	—	—		
	Ports for 5 V tolerant*2	V_{IH}	VCC × 0.8	—	5.8		
		V_{IL}	–0.3	—	VCC × 0.2		
	Other input pins excluding ports for 5 V tolerant*3	V_{IH}	VCC × 0.8	—	VCC + 0.3		
		V_{IL}	–0.3	—	VCC × 0.2		
Input high voltage (except for Schmitt trigger input pin)	MD pin, EMLE	V_{IH}	VCC × 0.9	—	VCC + 0.3	V	
	EXTAL, RSPI, EXDMAC, WAIT#, TCK		VCC × 0.8	—	VCC + 0.3		
	ETHERC		2.3	—	VCC + 0.3		
	XCIN		—	—	VCC + 0.3		
	D0 to D31		VCC × 0.7	—	VCC + 0.3		
	RIIC (SMBus)		2.1	—	VCC + 0.3		
Input low voltage (except for Schmitt trigger input pin)	MD pin, EMLE	V_{IL}	–0.3	—	VCC × 0.1	V	
	EXTAL, RSPI, ETHERC, EXDMAC, WAIT#, TCK		–0.3	—	VCC × 0.2		
	XCIN		–0.3	—	—		
	D0 to D31		–0.3	—	VCC × 0.3		
	RIIC (SMBus)		–0.3	—	0.8		

Note 1. V_{IH} characteristics of the pins which are multiplexed with pin functions having 5-V tolerance are those of the pin functions for 5-V tolerance.
Note 2. Ports 07, 12 to 17, 20, 21, 30 to 33, 67, and C0 to C3 are 5 V tolerant.
Note 3. For P32, P31, P30, input as follows when the V_{BATT} power supply is selected.
V_{IH} Min. = V_{BATT} × 0.8, V_{IH} Max. = V_{BATT} + 0.3, V_{IL} Min. = –0.3, V_{IL} Max. = V_{BATT} × 0.2

Table 5.4 DC Characteristics (3) (for D and G Versions (-40 ≤ Ta ≤ +85°C))

Conditions: VCC = AVCC0 = VREFH = VCC_USB = V_{BATT} = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0,
VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V, $T_a = T_{opr}$

Item				Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Supply current*1	High-speed operating mode	Max.*2		I_{CC}*3	—	—	100	mA	ICLK = 100 MHz PCLKA = 100MHz PCLKB = 50 MHz FCLK = 50 MHz BCLK = 100MHz
		Normal *4	Peripheral function: clock signal supplied*4		—	52	—		
			Peripheral function: clock signal stopped*4		—	40	—		
		Sleep mode			—	25	65		
		All-module-clock-stop mode (reference value)			—	20	38		
		Increased by BGO operation*5			—	15	—		
	Low-speed operating mode 1*6				—	4	—		ICLK = 1 MHz
	Low-speed operating mode 2				—	1	—		ICLK = 32.768 kHz
	Software standby mode				—	0.2	6		
	Deep software standby mode	Power supplied to RAM and USB resume detecting unit			—	22	200	μA	
		Power not supplied to RAM and USB resume detecting unit	Power-on reset circuit and low-power consumption function disabled		—	21	60		
			Power-on reset circuit and low-power		—	6.2	28		
	Increase when the RTC is operating		When a crystal oscillator for low clock loads is in use		—	1.0	—		
			When a crystal oscillator for standard clock loads is in use		—	3.0	—		
	RTC operating while VCC is off (with the battery backup function, only the RTC and sub-clock oscillator operate)		When a crystal oscillator for low clock loads is in use		—	0.9	—		V_{BATT} = 2.0 V, VCC = 0V
					—	1.6	—		V_{BATT} = 3.3 V, VCC = 0V
			When a crystal oscillator for standard clock loads is in use		—	1.7	—		V_{BATT} = 2.0 V(for products with 100 pins or more), VBATT = 2.3 V (for the 64-pin product), VCC = 0V
					—	3.3	—		V_{BATT} = 3.3 V, VCC = 0V
Analog power supply current*7	During 12-bit A/D conversion (including temperature sensor)			I_{AVCC0}	—	2.3	3.2	mA	
	During 10-bit A/D conversion			I_{VREFH}*9	—	1.0	1.65	mA	
	During D/A conversion (per unit)				—	0.7	1.0	mA	
	Waiting for A/D, D/A conversion (all units)*10			—	—	25	35	μA	
	A/D, D/A converter in standby mode (all units)*10				—	0.1	4.0	μA	
Reference power supply current	During 12-bit A/D conversion			I_{VREFH0}	—	0.6	0.7	mA	
	Waiting for 12-bit A/D conversion (per unit)				—	0.5	0.6	mA	
	12-bit A/D converter in standby mode (per unit)				—	0.1	2.0	μA	

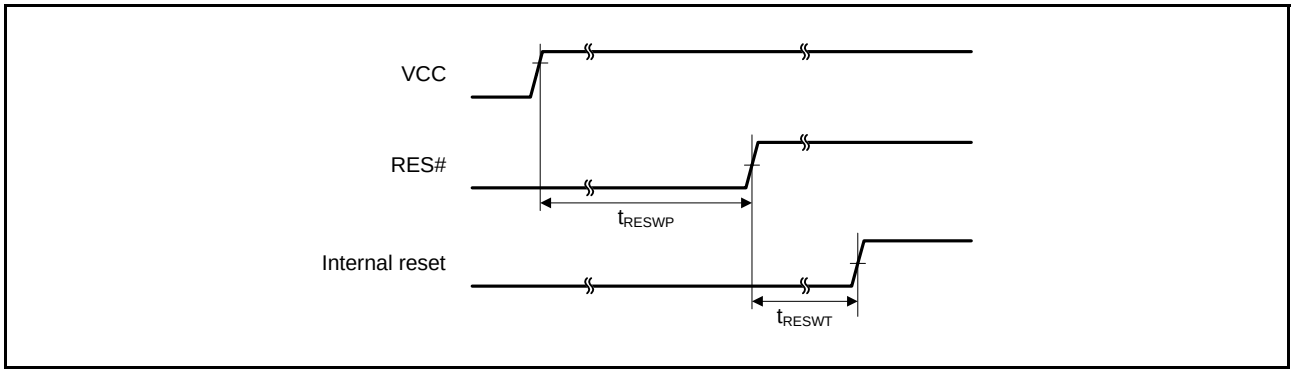


Figure 5.1 Reset Input Timing at Power-On

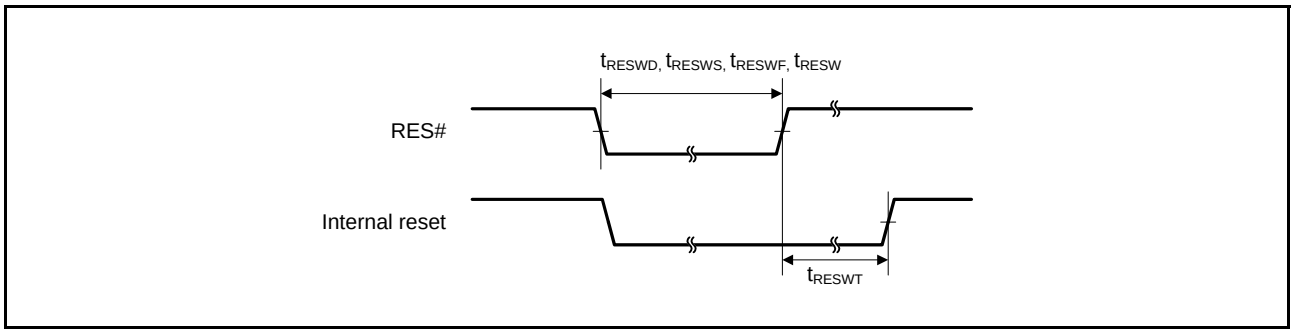


Figure 5.2 Reset Input Timing

Table 5.13 Clock Timing (Sub-Clock Related)

Conditions: VCC = AVCC0 = VREFH = VCC_USB = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0, V_{BATT} = 2.0 to 3.6 V (for products with 100 pins or more), V_{BATT} = 2.3 to 3.6 V (for the 64-pin product),
VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V, $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Sub-clock frequency	f_{SUB}	—	32.768	—	kHz	
Sub-clock oscillator start-up time	t_{SUBOSC}	—	—	*1		Figure 5.12
Sub-clock oscillation stabilization wait offset time*3	$t_{SUBOSCWT0}$	1.8	—	2.6	s	
Sub-clock oscillation stabilization wait time	$t_{SUBOSCWT}$	—	—	*2	s	

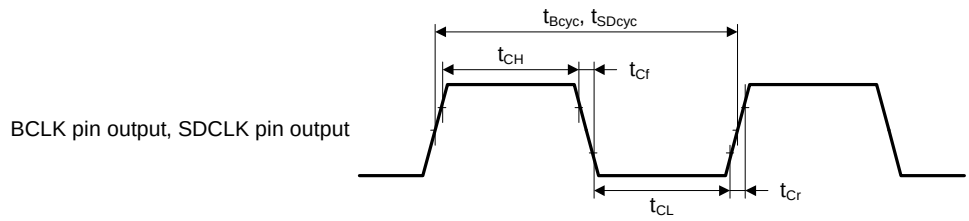
Note 1. When using a sub-clock, ask the manufacturer of the oscillator to evaluate its oscillation. Refer to the results of evaluation provided by the manufacturer for the oscillation stabilization time.

Note 2. The number of cycles n selected by the value of the SOSCWTCR.SSTS[4:0] bits determines the sub-clock oscillation stabilization waiting time in accord with the formula below.

$$t_{SUBOSCWT} = \max\left(t_{SUBOSC}, t_{SUBOSCWT0}\right) + \frac{n}{f_{SUB}}$$

The notation “max (t_{SUBOSC}, $t_{SUBOSCWT0}$)“ indicates whichever is higher of t_{SUBOSC} and $t_{SUBOSCWT0}$.

Note 3. The minimum value and maximum value of the sub-clock oscillation stabilization wait offset time (tSUBOSCWT0) is the references only for 100-pin or more products. For 64-pin products, consider the value of tSUBOSCWT0 to be 0.



Test conditions: VOH = VCC × 0.7, VOL = VCC × 0.3, IOH = –1.0 mA, IOL = 1.0 mA, C = 30 pF

Figure 5.3 BCLK Pin Output, SDCLK Pin Output Timing

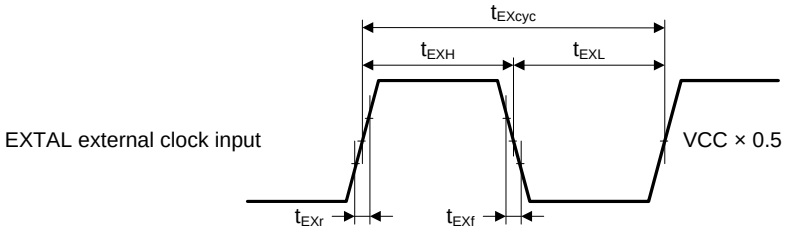
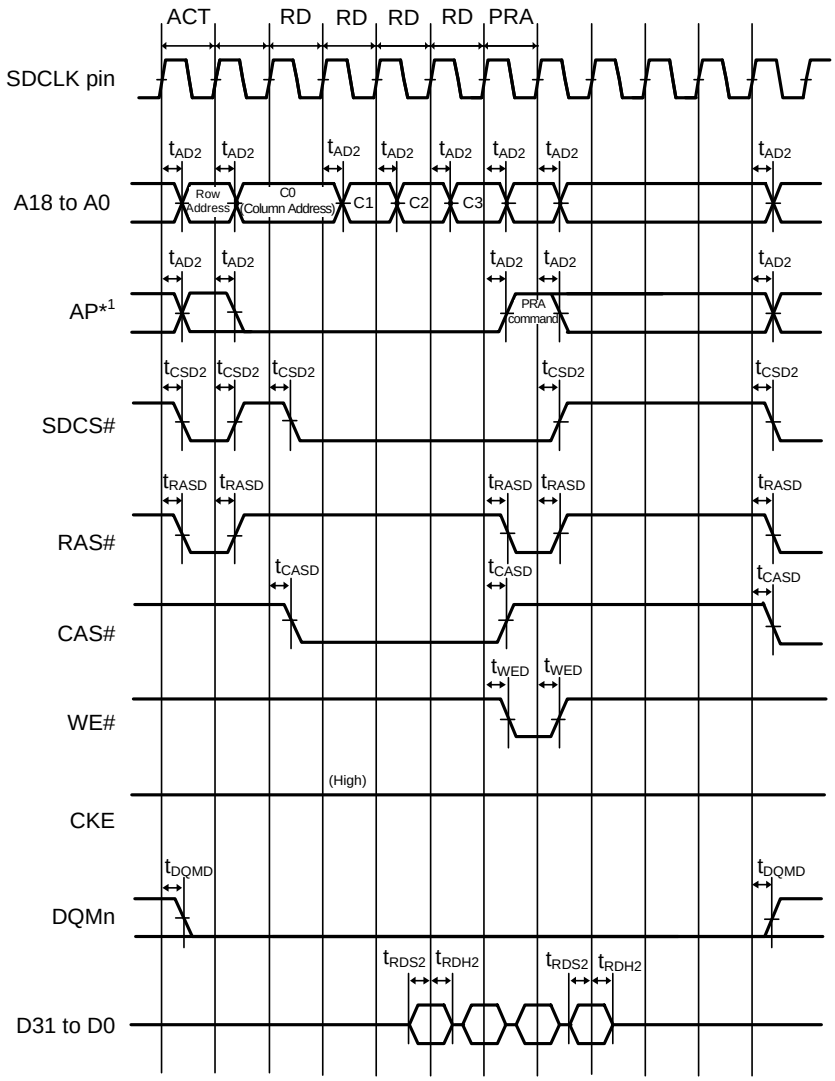
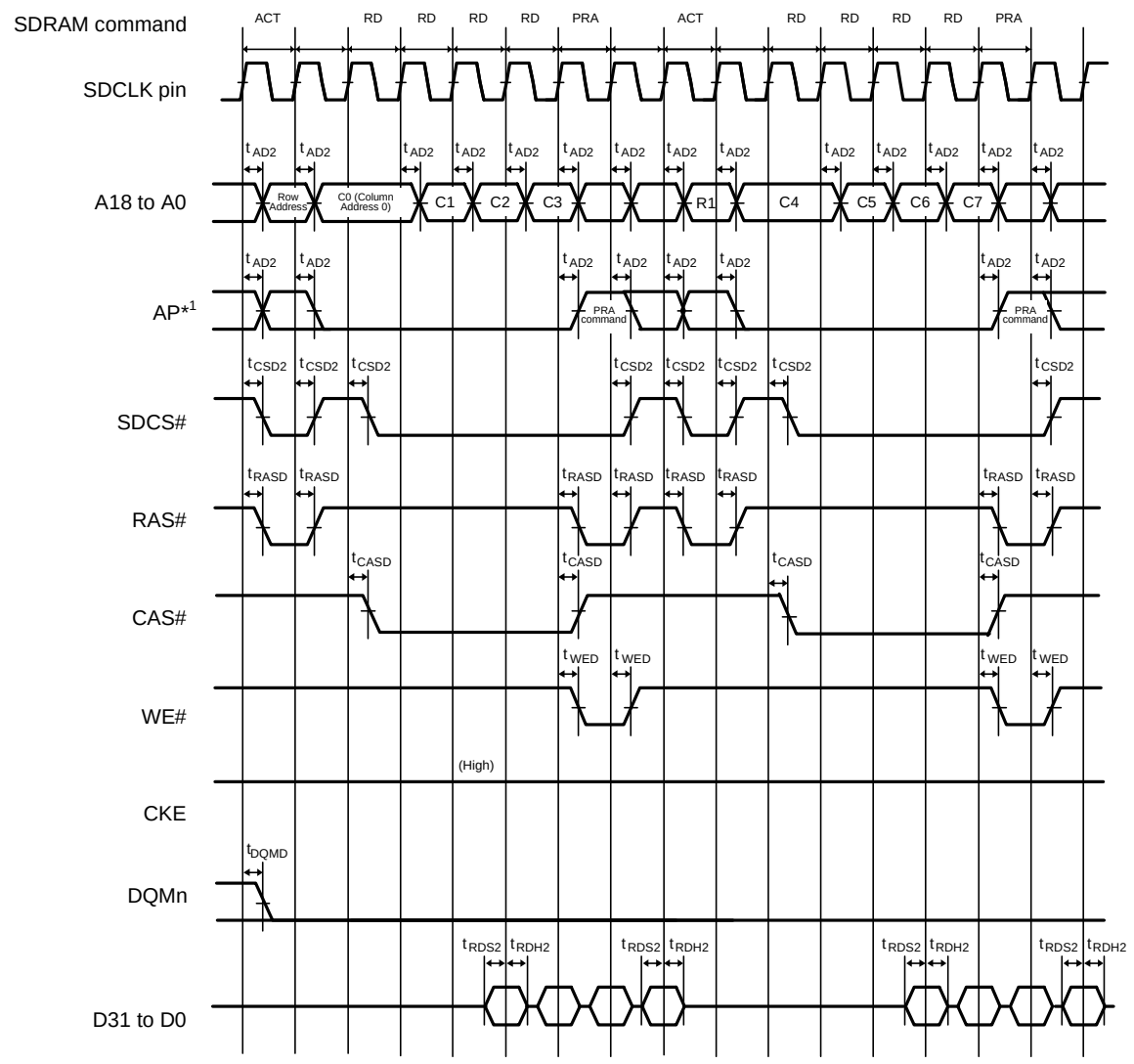


Figure 5.4 EXTAL External Clock Input Timing



Note 1: Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

Figure 5.26 SDRAM Space Multiple Read Bus Timing



Note 1: Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

Figure 5.28 SDRAM Space Multiple Read Line Stride Bus Timing

5.8 Power-on Reset Circuit and Voltage Detection Circuit Characteristics

Table 5.33 Power-on Reset Circuit and Voltage Detection Circuit Characteristics

Conditions: VCC = AVCC0 = VREFH = VCC_USB = V_{BATT} = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0
VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V
$T_a = T_{opr}$

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage detection level	Power-on reset (POR)	Low power consumption function disabled	V_{POR}	2.5	2.6	2.7	V	Figure 5.63
		Low power consumption function enabled		2.0	2.35	2.7		
	Voltage detection circuit (LVD0)		V_{det0}	2.7	2.80	2.9		Figure 5.64
	Voltage detection circuit (LVD1)		V_{det1_A}	2.75	2.95	3.15		Figure 5.65
	Voltage detection circuit (LVD2)		V_{det2_A}	2.75	2.95	3.15		Figure 5.66
Internal reset time	Power-on reset time		t_{POR}	—	4.6	—	ms	Figure 5.63
	LVD0 reset time		t_{LVD0}	—	4.6	—		Figure 5.64
	LVD1 reset time		t_{LVD1}	—	0.9	—		Figure 5.65
	LVD2 reset time		t_{LVD2}	—	0.9	—		Figure 5.66
Minimum VCC down time			t_{VOFF}	200	—	—	µs	Figure 5.63 and Figure 5.64
Response delay time			t_{det}	—	—	200	µs	Figure 5.63 to Figure 5.66
LVD operation stabilization time (after LVD is enabled)			$Td_{(E-A)}$	—	—	3	µs	Figure 5.65 and Figure 5.66
Hysteresis width (LVD1 and LVD2)			V_{LVH}	—	80	—	mV	

Note: The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR}, V_{det1}, and V_{det2} for the POR/ LVD.

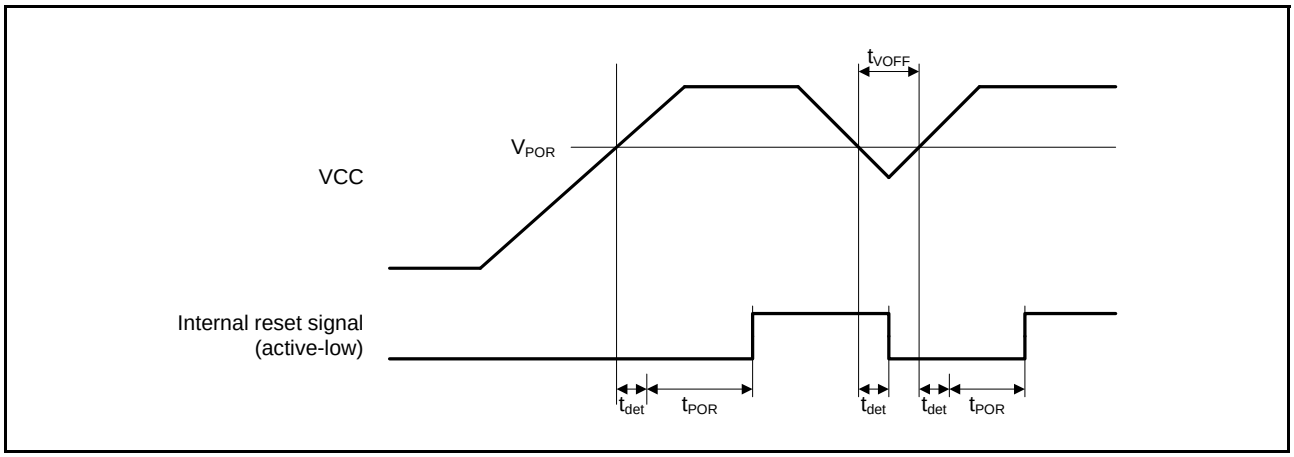


Figure 5.63 Power-on Reset Timing

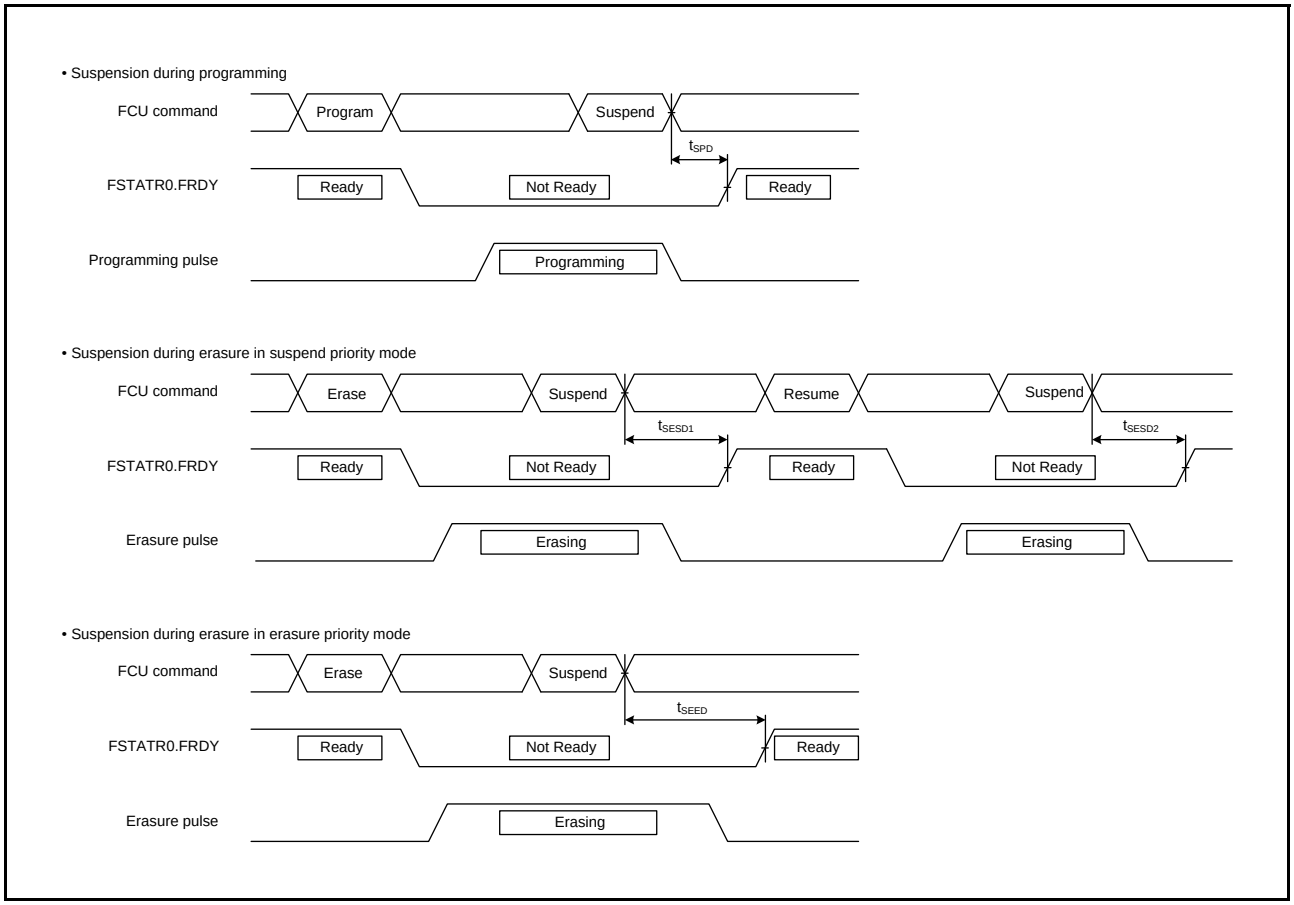


Figure 5.69 Flash Memory Program/Erase Suspend Timing