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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, LINbus, SCI, SPI, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	133
Program Memory Size	768KB (768K x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b, 21x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	177-TFLGA
Supplier Device Package	177-TFLGA (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f563nacdlc-u0

Table 1.3 List of Products (5/8)

Group	Part No.	Package	ROM Capacity	RAM Capacity	E2 Data Flash	Operating Frequency (Max.)	Operating Temp. Range
RX631 (D version)	R5F5631ADDFC	PLQP0176KB-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56318CDFC	PLQP0176KB-A	512 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56318DDFC	PLQP0176KB-A	512 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56317CDFC	PLQP0176KB-A	384 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56317DDFC	PLQP0176KB-A	384 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56316CDFC	PLQP0176KB-A	256 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56316DDFC	PLQP0176KB-A	256 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631ECDLK	PTLG0145KA-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631EDDLK	PTLG0145KA-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631DCDLK	PTLG0145KA-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631DDDLK	PTLG0145KA-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631BCDLK	PTLG0145KA-A	1 Mbyte	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631BDDLK	PTLG0145KA-A	1 Mbyte	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631ACDLK	PTLG0145KA-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631ADDLK	PTLG0145KA-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56318CDLK	PTLG0145KA-A	512 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56318DDLK	PTLG0145KA-A	512 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56317CDLK	PTLG0145KA-A	384 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56317DDLK	PTLG0145KA-A	384 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56316CDLK	PTLG0145KA-A	256 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56316DDLK	PTLG0145KA-A	256 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631FHDFB	PLQP0144KA-A	2 Mbytes	256 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631FDDFB	PLQP0144KA-A	2 Mbytes	256 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631KHDFB	PLQP0144KA-A*1	2 Mbytes	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631KDDFB	PLQP0144KA-A	2 Mbytes	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631ECDFB	PLQP0144KA-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631EDDFB	PLQP0144KA-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631JHDFB	PLQP0144KA-A*1	1.5 Mbytes	256 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631JDDFB	PLQP0144KA-A	1.5 Mbytes	256 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631GHDFB	PLQP0144KA-A*1	1.5 Mbytes	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631GDDFB	PLQP0144KA-A	1.5 Mbytes	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631DCDFB	PLQP0144KA-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631DDDFB	PLQP0144KA-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631YHDFB	PLQP0144KA-A	1 Mbyte	256 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631YDDFB	PLQP0144KA-A	1 Mbyte	256 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631WHDFB	PLQP0144KA-A	1 Mbyte	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631WDDFB	PLQP0144KA-A	1 Mbyte	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631BCDFB	PLQP0144KA-A	1 Mbyte	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631BDDFB	PLQP0144KA-A	1 Mbyte	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631ACDFB	PLQP0144KA-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631ADDFB	PLQP0144KA-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56318CDFB	PLQP0144KA-A	512 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56318DDFB	PLQP0144KA-A	512 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56316CDFB	PLQP0144KA-A	256 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F56316DDFB	PLQP0144KA-A	256 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C

Table 1.3 List of Products (8/8)

Group	Part No.	Package	ROM Capacity	RAM Capacity	E2 Data Flash	Operating Frequency (Max.)	Operating Temp. Range
RX631 (G version) *2	R5F5631GDGFB	PLQP0144KA-A	1.5 Mbytes	192 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631DDGFB	PLQP0144KA-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631YDGFB	PLQP0144KA-A	1 Mbyte	256 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631WDGFB	PLQP0144KA-A	1 Mbyte	192 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631BDGFB	PLQP0144KA-A	1 Mbyte	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631ADGFB	PLQP0144KA-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F56318SGFB	PLQP0144KA-A	512 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F56318DGFB	PLQP0144KA-A	512 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F56317SGFB	PLQP0144KA-A	384 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F56317DGFB	PLQP0144KA-A	384 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F56316SGFB	PLQP0144KA-A	256 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F56316DGFB	PLQP0144KA-A	256 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631FDGFP	PLQP0100KB-A	2 Mbytes	256 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631KDGFP	PLQP0100KB-A	2 Mbytes	192 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631EDGFP	PLQP0100KB-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631JDGFP	PLQP0100KB-A	1.5 Mbytes	256 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631GDGFP	PLQP0100KB-A	1.5 Mbytes	192 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631DDGFP	PLQP0100KB-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631YDGFP	PLQP0100KB-A	1 Mbyte	256 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631WDGFP	PLQP0100KB-A	1 Mbyte	192 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631BDGFP	PLQP0100KB-A	1 Mbyte	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631ADGFP	PLQP0100KB-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F56318DGFP	PLQP0100KB-A	512 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F56317DGFP	PLQP0100KB-A	384 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F56316DGFP	PLQP0100KB-A	256 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631PDGFM	PLQP0064KB-A	512 Kbytes	64 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631NDGFM	PLQP0064KB-A	384 Kbytes	64 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631MDGFM	PLQP0064KB-A	256 Kbytes	64 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631PDGFL	PLQP0048KB-A	512 Kbytes	64 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631NDGFL	PLQP0048KB-A	384 Kbytes	64 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F5631MDGFL	PLQP0048KB-A	256 Kbytes	64 Kbytes	32 Kbytes	100 MHz	-40 to +105°C

Note 1. In the planning stage

Note 2. The specifications of the temperature sensor calibration and unique ID for G-version products differ from those for other products. For details, see section 45.2.2, Temperature Sensor Calibration Data Registers (TSCDRH, TSCDRL), section 45.3, Using the Temperature Sensor, and section 47.2.22, Unique ID Registers n (UIDRn) (n = 0 to 15) in the User's manual: Hardware.

Table 1.4 Pin Functions (2/6)

Classifications	Pin Name	I/O	Description
Bus control	RD#	Output	Strobe signal which indicates that reading from the external bus interface space is in progress.
	WR#	Output	Strobe signal which indicates that writing to the external bus interface space is in progress, in 1-write strobe mode.
	WR0# to WR3#	Output	Strobe signals which indicate that either group of data bus pins (D7 to D0, D15 to D8, D23 to D16, and D31 to D24) is valid in writing to the external bus interface space, in byte strobe mode.
	BC0# to BC3#	Output	Strobe signals which indicate that either group of data bus pins (D7 to D0, D15 to D8, D23 to D16, and D31 to D24) is valid in access to the external bus interface space, in 1-write strobe mode.
	ALE	Output	Address latch signal when address/data multiplexed bus is selected.
	CKE	Output	Output pin for SDRAM clock enable signals.
	SDCS#	Output	Output pin for SDRAM chip select signals.
	RAS#	Output	Output pin for SDRAM row address strobe signals.
	CAS#	Output	Output pin for SDRAM column address strobe signals.
	WE#	Output	Output pin for SDRAM write enable signals.
	DQM0 to DQM3	Output	Output pins for SDRAM I/O data mask enable signals.
	CS0# to CS7#	Output	Select signals for CS area.
	WAIT#	Input	Input pins for wait request signals in access to the external space.
EXDMA controller	EDREQ0, EDREQ1		Input pins for external DMA transfer requests.
	EDACK0, EDACK1		Output pins for single address transfer acknowledge signals.
Interrupt	NMI	Input	Non-maskable interrupt request signal.
	IRQ0 to IRQ15	Input	Maskable interrupt request signals.
Multi-function timer pulse unit 2	MTIOC0A, MTIOC0B MTIOC0C, MTIOC0D	I/O	The TGRA0 to TGRD0 input capture input/output compare output/PWM output pins.
	MTIOC1A, MTIOC1B	I/O	The TGRA1 and TGRB1 input capture input/output compare output/PWM output pins.
	MTIOC2A, MTIOC2B	I/O	The TGRA2 and TGRB2 input capture input/output compare output/PWM output pins.
	MTIOC3A, MTIOC3B MTIOC3C, MTIOC3D	I/O	The TGRA3 to TGRD3 input capture input/output compare output/PWM output pins.
	MTIOC4A, MTIOC4B MTIOC4C, MTIOC4D	I/O	The TGRA4 to TGRD4 input capture input/output compare output/PWM output pins.
	MTIC5U, MTIC5V MTIC5W	Input	The TGRU5, TGRV5, and TGRW5 input capture input/dead time compensation input pins.
	MTCLKA, MTCLKB MTCLKC, MTCLKD	Input	Input pins for external clock signals.
Port output enable 2	POE0# to POE3# POE8#	Input	Input pins for request signals to place the MTU large-current pins in the high impedance state.

Table 1.6 List of Pin and Pin Functions (176-Pin LQFP) (5/5)

Pin Number 176-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SCId, SCId, RSPI, RIIC, CAN, IEB, USB, and PDC)	Interrupt	S12AD, AD, DA
136		P64	CS4#/WE#				
137		P63	CS3#/CAS#				
138		P62	CS2#/RAS#				
139		P61	CS1#/SDCS#				
140	VSS						
141		P60	CS0#				
142	VCC						
143		PD7	D7[A7/D7]	MTIC5U/POE0#	SSLC3	IRQ7	AN7
144		PG1	D25				
145		PD6	D6[A6/D6]	MTIC5V/POE1#	SSLC2	IRQ6	AN6
146		PG0	D24				
147		PD5	D5[A5/D5]	MTIC5W/POE2#	SSLC1	IRQ5	AN013
148		PD4	D4[A4/D4]	POE3#	SSLC0	IRQ4	AN012
149		P97	A23/D23				
150		PD3	D3[A3/D3]	TIOCB8/TCLKH/POE8#	RSPCKC	IRQ3	AN011
151	VSS						
152		P96	A22/D22				
153	VCC						
154		PD2	D2[A2/D2]	MTIOC4D/TIOCA8	MISOC/CRX0	IRQ2	AN010
155		P95	A21/D21				
156		PD1	D1[A1/D1]	MTIOC4B/TIOCB7/ TCLKG	MOSIC/CTX0	IRQ1	AN009
157		P94	A20/D20				
158		PD0	D0[A0/D0]	TIOCA7		IRQ0	AN008
159		P93	A19/D19		CTS7#/RTS7#/SS7#		AN017
160		P92	A18/D18		RXD7/SMISO7/SSCL7		AN016
161		P91	A17/D17		SCK7		AN015
162	VSS						
163		P90	A16/D16		TXD7/SMOSI7/SSDA7		AN014
164	VCC						
165		P47				IRQ15-DS	AN007
166		P46				IRQ14-DS	AN006
167		P45				IRQ13-DS	AN005
168		P44				IRQ12-DS	AN004
169		P43				IRQ11-DS	AN003
170		P42				IRQ10-DS	AN002
171		P41				IRQ9-DS	AN001
172	VREFL0						
173		P40				IRQ8-DS	AN000
174	VREFH0						
175	AVCC0						
176		P07				IRQ15	ADTRG0#

Note 1. The BCLK function is multiplexed with the I/O port function for pin P53, so the port function is not available if the external bus is enabled.

Note 2. Enabled only for the ROM capacity: 2 Mbytes/1.5 Mbytes

Table 1.9 List of Pins and Pin Functions (100-Pin TFLGA) (1/5)

Pin No. 100-pin TFLGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC	Timers (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SC1c, SC1d, RSPI, RIIC, CAN, IEB, USB)	Interrupt	S12AD AD DA
A1		P05				IRQ13	DA1
A2	VREFH						
A3		P07				IRQ15	ADTRG0#
A4	VREFL0						
A5		P43				IRQ11-DS	AN003
A6		PD0	D0[A0/D0]			IRQ0	AN008
A7		PD4	D4[A4/D4]	POE3#		IRQ4	AN012
A8		PE0	D8[A8/D8]		SCK12/SSLB1		ANEX0
A9		PE1	D9[A9/D9]	MTIOC4C/ PO18	TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12/SSLB2/ RSPCKB		ANEX1
A10		PE2	D10[A10/D10]	MTIOC4A/ PO23	RXD12/SMISO12/ SSCL12/RXDX12/ SSLB3/MOSIB	IRQ7-DS	AN0
B1	EMLE						
B2	AVSS0						
B3	AVCC0						
B4		P40				IRQ8-DS	AN000
B5		P44				IRQ12-DS	AN004
B6		PD1	D1[A1/D1]	MTIOC4B	CTX0*1	IRQ1	AN009
B7		PD3	D3[A3/D3]	POE8#		IRQ3	AN011
B8		PD6	D6[A6/D6]	MTIC5V/ POE1#		IRQ6	AN6
B9		PD7	D7[A7/D7]	MTIC5U/ POE0#		IRQ7	AN7
B10		PE3	D11[A11/D11]	MTIOC4B/ PO26/POE8#	CTS12#/RTS12#/ SS12#/MISOB/ ET_ERXD3		AN1
C1	VCL						
C2	VREFL						
C3		PJ3		MTIOC3C	CTS6#/RTS6#/ CTS0#/RTS0#/ SS6#/SS0#		
C4	VREFH0						
C5		P42				IRQ10-DS	AN002
C6		P47				IRQ15-DS	AN007
C7		PD2	D2[A2/D2]	MTIOC4D	CRX0*1	IRQ2	AN010
C8		PD5	D5[A5/D5]	MTIC5W/ POE2#		IRQ5	AN013
C9		PE5	D13[A13/D13]	MTIOC4C/ MTIOC2B	RSPCKB/ ET_RX_CLK/ REF50CK	IRQ5	AN3
C10		PE4	D12[A12/D12]	MTIOC4D/ MTIOC1A/ PO28	SSLB0/ET_ERXD2		AN2
D1	XCIN						

Table 1.10 List of Pins and Pin Functions (100-Pin LQFP) (3/4)

Pin No.	Power Supply Clock System Control	I/O Port	Bus EXDMAC	Timers (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SCIC, SCID, RSPI, RIIC, CAN, IEB, USB)	Interrupt	S12AD AD DA
59		PB1	A9	MTIOC0C/MTIOC4C/ TIOCB3/TMC10/PO25	TXD6/SMOSI6/SSDA6/ ET_ERXD0/ RMII_RXD0	IRQ4-DS	
60	VCC						
61		PB0	A8	MTIC5W/TIOCA3/PO24	RXD6/SMISO6/SSCL6/ RSPCKA/ET_ERXD1/ RMII_RXD1	IRQ12	
62	VSS						
63		PA7	A7	TIOCB2/PO23	MISOA/ET_WOL		
64		PA6	A6	MTIC5V/MTCLKB/ TIOCA2/TMC13/PO22/ POE2#	CTS5#/RTS5#/SS5#/ MOSIA/ET_EXOUT		
65		PA5	A5	TIOCB1/PO21	RSPCKA/ET_LINKSTA		
66		PA4	A4	MTIC5U/MTCLKA/ TIOCA1/TMRI0/PO20	TXD5/SMOSI5/SSDA5/ SSLA0/ET_MDC	IRQ5-DS	
67		PA3	A3	MTIOC0D/MTCLKD/ TIOC0D/TCLKB/PO19	RXD5/SMISO5/SSCL5/ ET_MDIO	IRQ6-DS	
68		PA2	A2	PO18	RXD5/SMISO5/SSCL5/ SSLA3		
69		PA1	A1	MTIOC0B/MTCLKC/ TIOCB0/PO17	SCK5/SSLA2/ET_WOL	IRQ11	
70		PA0	A0/BC0#	MTIOC4A/TIOCA0/ PO16	SSLA1/ET_TX_EN/ RMII_TXD_EN		
71		PE7	D15[A15/D15]		MISOB	IRQ7	AN5
72		PE6	D14[A14/D14]		MOSIB	IRQ6	AN4
73		PE5	D13[A13/D13]	MTIOC4C/MTIOC2B	RSPCKB/ET_RX_CLK/ REF50CK	IRQ5	AN3
74		PE4	D12[A12/D12]	MTIOC4D/MTIOC1A/ PO28	SSLB0/ET_ERXD2		AN2
75		PE3	D11[A11/D11]	MTIOC4B/PO26/POE8#	CTS12#/RTS12#/ SS12#/MISOB/ ET_ERXD3		AN1
76		PE2	D10[A10/D10]	MTIOC4A/PO23	RXD12/SMISO12/ SSCL12/RXD12/ SSLB3/MOSIB	IRQ7-DS	AN0
77		PE1	D9[A9/D9]	MTIOC4C/PO18	TXD12/SMOSI12/ SSDA12/TXD12/ SIOX12/SSLB2/ RSPCKB		ANEX1
78		PE0	D8[A8/D8]		SCK12/SSLB1		ANEX0
79		PD7	D7[A7/D7]	MTIC5U/POE0#		IRQ7	AN7
80		PD6	D6[A6/D6]	MTIC5V/POE1#		IRQ6	AN6
81		PD5	D5[A5/D5]	MTIC5W/POE2#		IRQ5	AN013
82		PD4	D4[A4/D4]	POE3#		IRQ4	AN012
83		PD3	D3[A3/D3]	POE8#		IRQ3	AN011
84		PD2	D2[A2/D2]	MTIOC4D	CRX0*1	IRQ2	AN010
85		PD1	D1[A1/D1]	MTIOC4B	CTX0*1	IRQ1	AN009
86		PD0	D0[A0/D0]			IRQ0	AN008
87		P47				IRQ15-DS	AN007
88		P46				IRQ14-DS	AN006
89		P45				IRQ13-DS	AN005
90		P44				IRQ12-DS	AN004
91		P43				IRQ11-DS	AN003
92		P42				IRQ10-DS	AN002
93		P41				IRQ9-DS	AN001

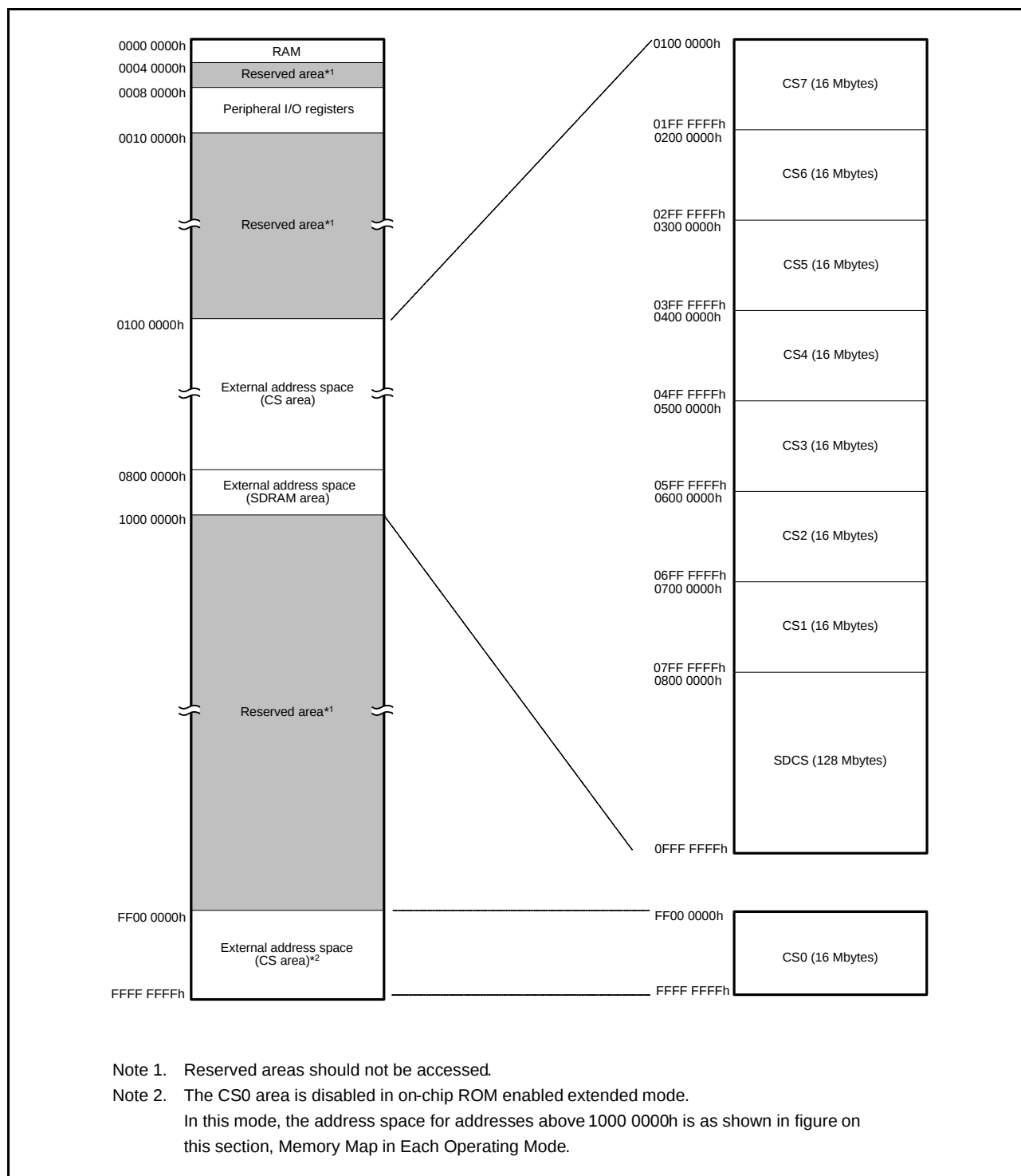
Table 1.13 List of Pins and Pin Functions (48-Pin LQFP) (2/2)

Pin Number 48-Pin LQFP	Power Supply Clock System Control	I/O Port	Timer (MTU2a, TPUa, TMR, PPG, POE2a)	Communications (SC1c, SC1d, RSPI, RIIC, CAN, IEB, USB)	Interrupt	S12ADa, DAa
29		PB0/ PC0	MTIC5W/TIOCA3/PO24	RXD6/SMISO6/SSCL6/ RSPCKA	IRQ12	
30	VSS					
31		PA6	MTIC5V/MTCLKB/TIOCA2/ TMC13/PO22/POE2#	CTS5#/RTS5#/SS5#/ MOSIA		
32		PA4	MTIC5U/MTCLKA/ TIOCA1/TMRI0/PO20	TXD5/SMOSI5/SSDA5/ SSLA0	IRQ5-DS	
33		PA3	MTIOC0D/MTCLKD/ TIOC0D/TCLKB/PO19	RXD5/SMISO5/SSCL5	IRQ6-DS	
34		PA1	MTIOC0B/MTCLKC/ TIOCB0/PO17	SCK5/SSLA2	IRQ11	
35		PE4	MTIOC4D/MTIOC1A/ PO28	SSLB0		AN012
36		PE3	MTIOC4B/PO26/POE8#	CTS12#/RTS12#/SS12#/ MISOB		AN011
37		PE2	MTIOC4A/PO23	RXD12/SMISO12/SSCL12/ RXDX12/ SSLB3/MOSIB	IRQ7-DS	AN010
38		PE1	MTIOC4C/PO18	TXD12/SMISO12/SSDA12/ TXDX12/SIOX12/SSLB2/ RSPCKB		AN009
39	VREFL					
40		P46			IRQ14-DS	AN006
41	VREFH					
42		P42			IRQ10-DS	AN002
43		P41			IRQ9-DS	AN001
44	VREFL0					
45		P40			IRQ8-DS	AN000
46	VREFH0					
47	AVCC0					
48	AVSS0					

3.2 External Address Space

The external address space is classified into CS areas (CS0 to CS7) and SDRAM area (SDCS). CS areas can be divided into up to eight areas (CS0 to CS7) corresponding to the CSn# signal to be output from the CSn# pin.

Figure 3.2 shows the address ranges corresponding to the individual CS areas (CS0 to CS7) and SDRAM area (SDCS) in on-chip ROM disabled extended mode.



**Figure 3.2 Correspondence between External Address Spaces and CS Areas
(In On-Chip ROM Disabled Extended Mode)**

Table 4.1 List of I/O Registers (Address Order) (23/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 8800h	MTU2	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK	MTU2a
0008 8801h	MTU2	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK	
0008 8802h	MTU2	Timer I/O control register	TIOR	8	8	2, 3 PCLKB	2 ICLK	
0008 8804h	MTU2	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK	
0008 8805h	MTU2	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK	
0008 8806h	MTU2	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	
0008 8808h	MTU2	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	
0008 880Ah	MTU2	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	
0008 8880h	MTU5	Timer counter U	TCNTU	16	16	2, 3 PCLKB	2 ICLK	
0008 8882h	MTU5	Timer general register U	TGRU	16	16	2, 3 PCLKB	2 ICLK	
0008 8884h	MTU5	Timer control register U	TCRU	8	8	2, 3 PCLKB	2 ICLK	
0008 8886h	MTU5	Timer I/O control register U	TIORU	8	8	2, 3 PCLKB	2 ICLK	
0008 8890h	MTU5	Timer counter V	TCNTV	16	16	2, 3 PCLKB	2 ICLK	
0008 8892h	MTU5	Timer general register V	TGRV	16	16	2, 3 PCLKB	2 ICLK	
0008 8894h	MTU5	Timer control register V	TCRV	8	8	2, 3 PCLKB	2 ICLK	
0008 8896h	MTU5	Timer I/O control register V	TIORV	8	8	2, 3 PCLKB	2 ICLK	
0008 88A0h	MTU5	Timer counter W	TCNTW	16	16	2, 3 PCLKB	2 ICLK	
0008 88A2h	MTU5	Timer general register W	TGRW	16	16	2, 3 PCLKB	2 ICLK	
0008 88A4h	MTU5	Timer control register W	TCRW	8	8	2, 3 PCLKB	2 ICLK	
0008 88A6h	MTU5	Timer I/O control register W	TIORW	8	8	2, 3 PCLKB	2 ICLK	
0008 88B2h	MTU5	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK	
0008 88B4h	MTU5	Timer start register	TSTR	8	8	2, 3 PCLKB	2 ICLK	
0008 88B6h	MTU5	Timer compare match clear register	TCNTCMPCLR	8	8	2, 3 PCLKB	2 ICLK	
0008 8900h	POE	Input level control/status register 1	ICSR1	16	16	2, 3 PCLKB	2 ICLK	POE2a
0008 8902h	POE	Output level control/status register 1	OCSR1	16	16	2, 3 PCLKB	2 ICLK	
0008 8908h	POE	Input level control/status register 2	ICSR2	16	16	2, 3 PCLKB	2 ICLK	
0008 890Ah	POE	Software port output enable register	SPOER	8	8	2, 3 PCLKB	2 ICLK	
0008 890Bh	POE	Port output enable control register 1	POECR1	8	8	2, 3 PCLKB	2 ICLK	
0008 890Ch	POE	Port output enable control register 2	POECR2	8	8	2, 3 PCLKB	2 ICLK	
0008 890Eh	POE	Input level control/status register 3	ICSR3	16	16	2, 3 PCLKB	2 ICLK	
0008 9000h	S12AD	A/D control register	ADCSR	8	8	2, 3 PCLKB	2 ICLK	S12ADa
0008 9004h	S12AD	A/D channel select register 0	ADANS0	16	16	2, 3 PCLKB	2 ICLK	
0008 9006h	S12AD	A/D channel select register 1	ADANS1	16	16	2, 3 PCLKB	2 ICLK	
0008 9008h	S12AD	A/D-converted value addition mode select register 0	ADADS0	16	16	2, 3 PCLKB	2 ICLK	
0008 900Ah	S12AD	A/D-converted value addition mode select register 1	ADADS1	16	16	2, 3 PCLKB	2 ICLK	
0008 900Ch	S12AD	A/D-converted value addition count select register	ADADC	8	8	2, 3 PCLKB	2 ICLK	
0008 900Eh	S12AD	A/D control extended register	ADCER	16	16	2, 3 PCLKB	2 ICLK	
0008 9010h	S12AD	A/D start trigger select register	ADSTRGR	8	8	2, 3 PCLKB	2 ICLK	
0008 9012h	S12AD	A/D conversion extended input control register	ADEXICR	16	16	2, 3 PCLKB	2 ICLK	
0008 901Ah	S12AD	A/D temperature sensor data register	ADTSDR	16	16	2, 3 PCLKB	2 ICLK	
0008 901Ch	S12AD	A/D internal reference voltage data register	ADOCDR	16	16	2, 3 PCLKB	2 ICLK	
0008 9020h	S12AD	A/D data register 0	ADDR0	16	16	2, 3 PCLKB	2 ICLK	
0008 9022h	S12AD	A/D data register 1	ADDR1	16	16	2, 3 PCLKB	2 ICLK	
0008 9024h	S12AD	A/D data register 2	ADDR2	16	16	2, 3 PCLKB	2 ICLK	
0008 9026h	S12AD	A/D data register 3	ADDR3	16	16	2, 3 PCLKB	2 ICLK	
0008 9028h	S12AD	A/D data register 4	ADDR4	16	16	2, 3 PCLKB	2 ICLK	
0008 902Ah	S12AD	A/D data register 5	ADDR5	16	16	2, 3 PCLKB	2 ICLK	
0008 902Ch	S12AD	A/D data register 6	ADDR6	16	16	2, 3 PCLKB	2 ICLK	
0008 902Eh	S12AD	A/D data register 7	ADDR7	16	16	2, 3 PCLKB	2 ICLK	
0008 9030h	S12AD	A/D data register 8	ADDR8	16	16	2, 3 PCLKB	2 ICLK	
0008 9032h	S12AD	A/D data register 9	ADDR9	16	16	2, 3 PCLKB	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (30/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 C046h	PORT6	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C047h	PORT7	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C048h	PORT8	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C049h	PORT9	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C04Ah	PORTA	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C04Bh	PORTB	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C04Ch	PORTC	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C04Dh	PORTD	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C04Eh	PORTE	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C04Fh	PORTF	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C050h	PORTG	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C052h	PORTJ	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C060h	PORT0	Port input data register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C061h	PORT1	Port input data register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C062h	PORT2	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C063h	PORT3	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C064h	PORT4	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C065h	PORT5	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C066h	PORT6	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C067h	PORT7	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C068h	PORT8	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C069h	PORT9	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C06Ah	PORTA	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C06Bh	PORTB	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C06Ch	PORTC	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C06Dh	PORTD	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C06Eh	PORTE	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C06Fh	PORTF	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C070h	PORTG	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C072h	PORTJ	Port mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 C080h	PORT0	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C081h	PORT0	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C082h	PORT1	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C083h	PORT1	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C084h	PORT2	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C085h	PORT2	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C086h	PORT3	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C087h	PORT3	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C088h	PORT4	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C089h	PORT4	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C08Ah	PORT5	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C08Bh	PORT5	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C08Ch	PORT6	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C08Dh	PORT6	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C08Eh	PORT7	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C08Fh	PORT7	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C090h	PORT8	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C091h	PORT8	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C092h	PORT9	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C093h	PORT9	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C094h	PORTA	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (31/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 C095h	PORTA	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C096h	PORTB	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C097h	PORTB	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C098h	PORTC	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C099h	PORTC	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C09Ah	PORTD	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C09Bh	PORTD	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C09Ch	PORTE	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C09Dh	PORTE	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C09Eh	PORTF	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C09Fh	PORTF	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C0A0h	PORTG	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C0A1h	PORTG	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C0A4h	PORTJ	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C0A5h	PORTJ	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C0C0h	PORT0	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0C1h	PORT1	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0C2h	PORT2	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0C3h	PORT3	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0C4h	PORT4	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0C5h	PORT5	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0C6h	PORT6	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0C7h	PORT7	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0C8h	PORT8	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0C9h	PORT9	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0CAh	PORTA	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0CBh	PORTB	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0CCh	PORTC	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0CDh	PORTD	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0CEh	PORTE	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0CFh	PORTF	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0D0h	PORTG	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0D2h	PORTJ	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0E0h	PORT0	Drive ability control register	DSCR	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C0E2h	PORT2	Drive ability control register	DSCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0E5h	PORT5	Drive ability control register	DSCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0E9h	PORT9	Drive ability control register	DSCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0EAh	PORTA	Drive ability control register	DSCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0EBh	PORTB	Drive ability control register	DSCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0ECh	PORTC	Drive ability control register	DSCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0EDh	PORTD	Drive ability control register	DSCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0EEh	PORTE	Drive ability control register	DSCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0F0h	PORTG	Drive ability control register	DSCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C100h	MPC	CS output enable register	PFCSE	8	8	2, 3 PCLKB	2 ICLK	
0008 C102h	MPC	CS output pin select register 0	PFCSS0	8	8	2, 3 PCLKB	2 ICLK	
0008 C103h	MPC	CS output pin select register 1	PFCSS1	8	8	2, 3 PCLKB	2 ICLK	
0008 C104h	MPC	Address output enable register 0	PFAOE0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C105h	MPC	Address output enable register 1	PFAOE1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C106h	MPC	External bus control register 0	PFBCR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C107h	MPC	External bus control register 1	PFBCR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C10Eh	MPC	Ethernet control register 1	PFENET	8	8	2, 3 PCLKB	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (34/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 C1B1h	MPC	PE1 pin function control register	PE1PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1B2h	MPC	PE2 pin function control register	PE2PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1B3h	MPC	PE3 pin function control register	PE3PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1B4h	MPC	PE4 pin function control register	PE4PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1B5h	MPC	PE5 pin function control register	PE5PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1B6h	MPC	PE6 pin function control register	PE6PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1B7h	MPC	PE7 pin function control register	PE7PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1B8h	MPC	PF0 pin function control register	PF0PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1B9h	MPC	PF1 pin function control register	PF1PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1BAh	MPC	PF2 pin function control register	PF2PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1BDh	MPC	PF5 pin function control register	PF5PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1D3h	MPC	PJ3 pin function control register	PJ3PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C280h	SYSTEM	Deep standby control register	DPSBYCR	8	8	4, 5 PCLKB	2, 3 ICLK	Low Power Consumption
0008 C282h	SYSTEM	Deep standby interrupt enable register 0	DPSIER0	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C283h	SYSTEM	Deep standby interrupt enable register 1	DPSIER1	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C284h	SYSTEM	Deep standby interrupt enable register 2	DPSIER2	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C285h	SYSTEM	Deep standby interrupt enable register 3	DPSIER3	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C286h	SYSTEM	Deep standby interrupt flag register 0	DPSIFR0	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C287h	SYSTEM	Deep standby interrupt flag register 1	DPSIFR1	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C288h	SYSTEM	Deep standby interrupt flag register 2	DPSIFR2	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C289h	SYSTEM	Deep standby interrupt flag register 3	DPSIFR3	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C28Ah	SYSTEM	Deep standby interrupt edge register 0	DPSIEGR0	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C28Bh	SYSTEM	Deep standby interrupt edge register 1	DPSIEGR1	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C28Ch	SYSTEM	Deep standby interrupt edge register 2	DPSIEGR2	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C28Dh	SYSTEM	Deep standby interrupt edge register 3	DPSIEGR3	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C290h	SYSTEM	Reset status register 0	RSTSR0	8	8	4, 5 PCLKB	2, 3 ICLK	Resets
0008 C291h	SYSTEM	Reset status register 1	RSTSR1	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C293h	SYSTEM	Main clock oscillator forced oscillation control register	MOFCR	8	8	4, 5 PCLKB	2, 3 ICLK	Clock Generation Circuit
0008 C294h	SYSTEM	High-speed on-chip oscillator power supply control register	HOCOPCR	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C296h	FLASH	Flash write erase protection register	FWEPROR	8	8	4, 5 PCLKB	2, 3 ICLK	ROM
0008 C297h	SYSTEM	Voltage monitoring circuit control register	LVCMPCR	8	8	4, 5 PCLKB	2, 3 ICLK	LVDA
0008 C298h	SYSTEM	Voltage detection level select register	LVDLVL	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C29Ah	SYSTEM	Voltage monitoring 1 circuit control register 0	LVD1CR0	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C29Bh	SYSTEM	Voltage monitoring 2 circuit control register 0	LVD2CR0	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C2A0h to 0008 C2BFh	SYSTEM	Deep standby backup register 0 to 31	DPSBKR0 to 31	8	8	4, 5 PCLKB	2, 3 ICLK	Low Power Consumption
0008 C300h	ICU	Group 0 interrupt source register	GRP00	32	32	1 to 2PCLKB	2 ICLK	ICUb
0008 C304h	ICU	Group 1 interrupt source register	GRP01	32	32	1 to 2PCLKB	2 ICLK	
0008 C308h	ICU	Group 2 interrupt source register	GRP02	32	32	1 to 2PCLKB	2 ICLK	
0008 C30Ch	ICU	Group 3 interrupt source register	GRP03	32	32	1 to 2PCLKB	2 ICLK	
0008 C310h	ICU	Group 4 interrupt source register	GRP04	32	32	1 to 2PCLKB	2 ICLK	
0008 C314h	ICU	Group 5 interrupt source register	GRP05	32	32	1 to 2PCLKB	2 ICLK	
0008 C318h	ICU	Group 6 interrupt source register	GRP06	32	32	1 to 2PCLKB	2 ICLK	
0008 C330h	ICU	Group 12 interrupt source register	GRP12	32	32	1 to 2PCLKB	2 ICLK	
0008 C340h	ICU	Group 0 interrupt enable register	GEN00	32	32	1 to 2PCLKB	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (45/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK $\geq$ PCLK	ICLK<PCLK	
000A 024Eh	USB1	Device state changing register	DVCHGR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 0250h	USB1	USB address register	USBADDR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 0254h	USB1	USB request type register	USBREQ	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 0256h	USB1	USB request value register	USBVAL	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 0258h	USB1	USB request index register	USBINDX	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 025Ah	USB1	USB request length register	USBLENG	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	USBa
000A 025Ch	USB1	DCP configuration register	DCPCFG	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 025Eh	USB1	DCP maximum packet size register	DCPMAXP	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 0260h	USB1	DCP control register	DCPCTR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 0264h	USB1	Pipe window select register	PIPESEL	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	

Table 5.3 DC Characteristics (2)

Conditions: $V_{CC} = AV_{CC0} = V_{REFH} = V_{CC_USB} = 2.7$ to 3.6 V, $V_{REFH0} = 2.7$ V to AV_{CC0} ,
 $V_{SS} = AV_{SS0} = V_{REFL}/V_{REFL0} = V_{SS_USB} = 0$ V, $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Output high voltage	All output pins	V_{OH}	$V_{CC} - 0.5$	—	V	$I_{OH} = -1$ mA
Output low voltage	All output pins (except for RIIC pins, and ETHERC)	V_{OL}	—	0.5	V	$I_{OL} = 1.0$ mA
	RIIC pins	—	—	0.4	V	$I_{OL} = 3.0$ mA
		—	—	0.6		$I_{OL} = 6.0$ mA
	RIIC pins (only P12 and P13 in channel 0)	V_{OL}	—	0.4	V	$I_{OL} = 15.0$ mA (ICFER.FMPE = 1)
		—	0.4	—		$I_{OL} = 20.0$ mA (ICFER.FMPE = 1)
	ETHERC	V_{OL}	—	0.4	V	$I_{OL} = 1.0$ mA
Input leakage current	RES#, MD pin, EMLE*1, NMI	$ I_{in} $	—	1.0	μ A	$V_{in} = 0$ V $V_{in} = V_{CC}$
Three-state leakage current (off state)	Other than ports for 5 V tolerant	$ I_{TSI} $	—	1.0	μ A	$V_{in} = 0$ V $V_{in} = V_{CC}$
	Ports for 5 V tolerant		—	5.0		$V_{in} = 0$ V $V_{in} = 5.5$ V
Input pull-up MOS current	Ports 0 to 2, 30 to 34, 36, 37, 4 to G, J3, J5	I_p	-10	—	-300	μ A $V_{CC} = 2.7$ to 3.6 V $V_{in} = 0$ V
Input capacitance	All input pins (except for ports 12, 13, 16, 17, 20, 21, 4, C0, C1, and EMLE)	C_{in}	—	—	15	pF $V_{in} = 0$ V $f = 1$ MHz $T_a = 25^\circ\text{C}$
	Ports 12, 13, 16, 17, 20, 21, 4, C0, C1, EMLE		—	—	30	
Input pull-down MOS current	EMLE, BSCANP	I_p	10	—	300	μ A $V_{in} = V_{CC}$

Note 1. The input leakage current value at the EMLE pin is only when $V_{in} = 0$ V.

Table 5.17 Bus Timing (packages with 100 pins or less)

Conditions: $V_{CC} = AVCC0 = VREFH = VCC_USB = 2.7$ to 3.6 V, $VREFH0 = 2.7$ V to $AVCC0$,

$VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0$ V,

$ICLK = 8$ to 100 MHz, $BCLK$ pin = 8 to 50 MHz, $T_a = T_{opr}$

Output load conditions: $V_{OH} = VCC \times 0.5$, $V_{OL} = VCC \times 0.5$, $I_{OH} = -1.0$ mA, $I_{OL} = 1.0$ mA, $C = 30$ pF

High drive output is selected by the drive capacity control register.

Item	Symbol	Min.	Max.	Unit	Test Conditions
Address delay time	t_{AD}	—	20	ns	Figure 5.17 to Figure 5.22
Byte control delay time	t_{BCD}	—	20	ns	
CS# delay time	t_{CSD}	—	20	ns	
ALE delay time	t_{ALED}	—	20	ns	
RD# delay time	t_{RSD}	—	20	ns	
Read data setup time	t_{RDS}	15	—	ns	
Read data hold time	t_{RDH}	0	—	ns	
WR# delay time	t_{WRD}	—	20	ns	
Write data delay time	t_{WDD}	—	20	ns	
Write data hold time	t_{WDH}	0	—	ns	
WAIT# setup time	t_{WTS}	15	—	ns	Figure 5.23
WAIT# hold time	t_{WTH}	0	—	ns	

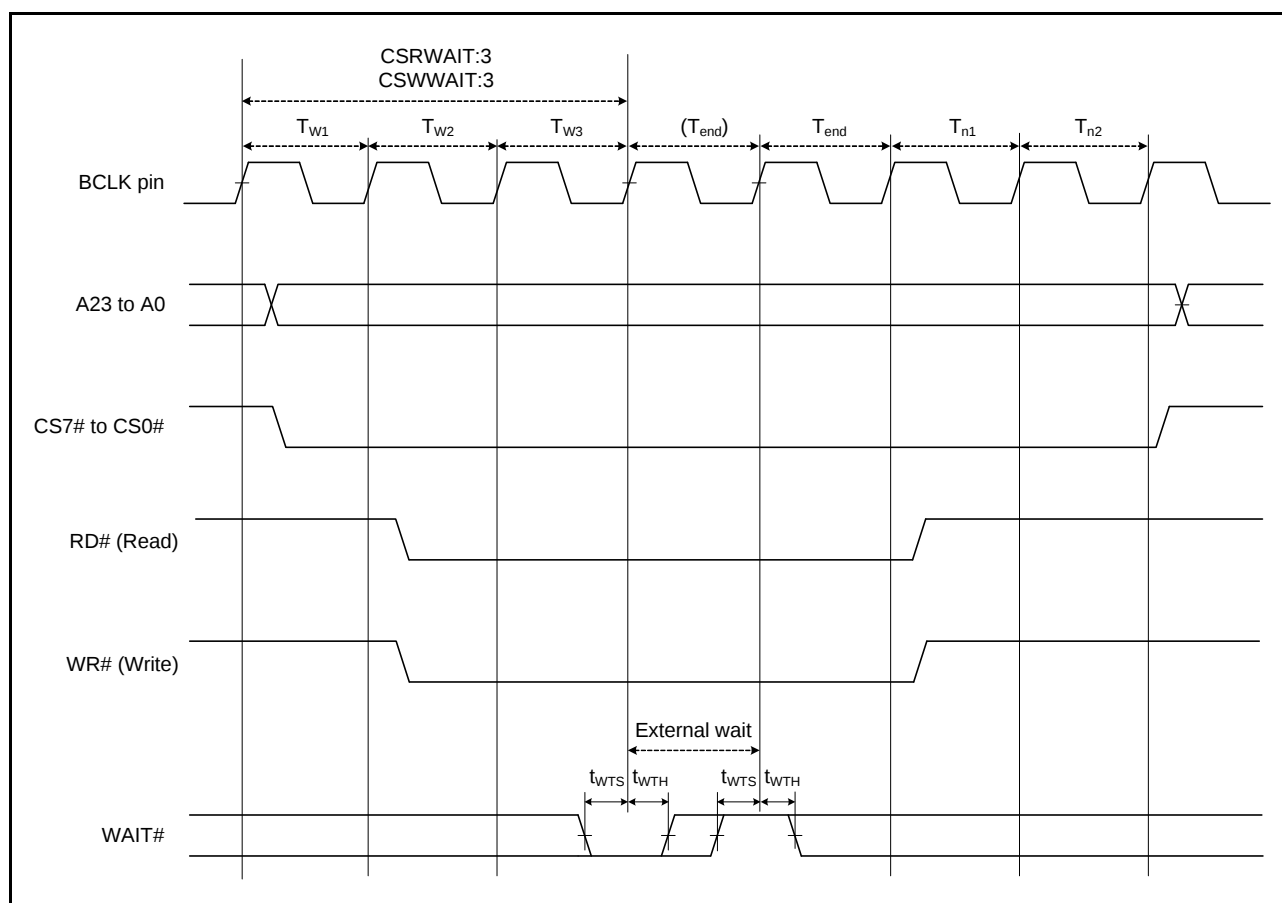


Figure 5.23 External Bus Timing/External Wait Control

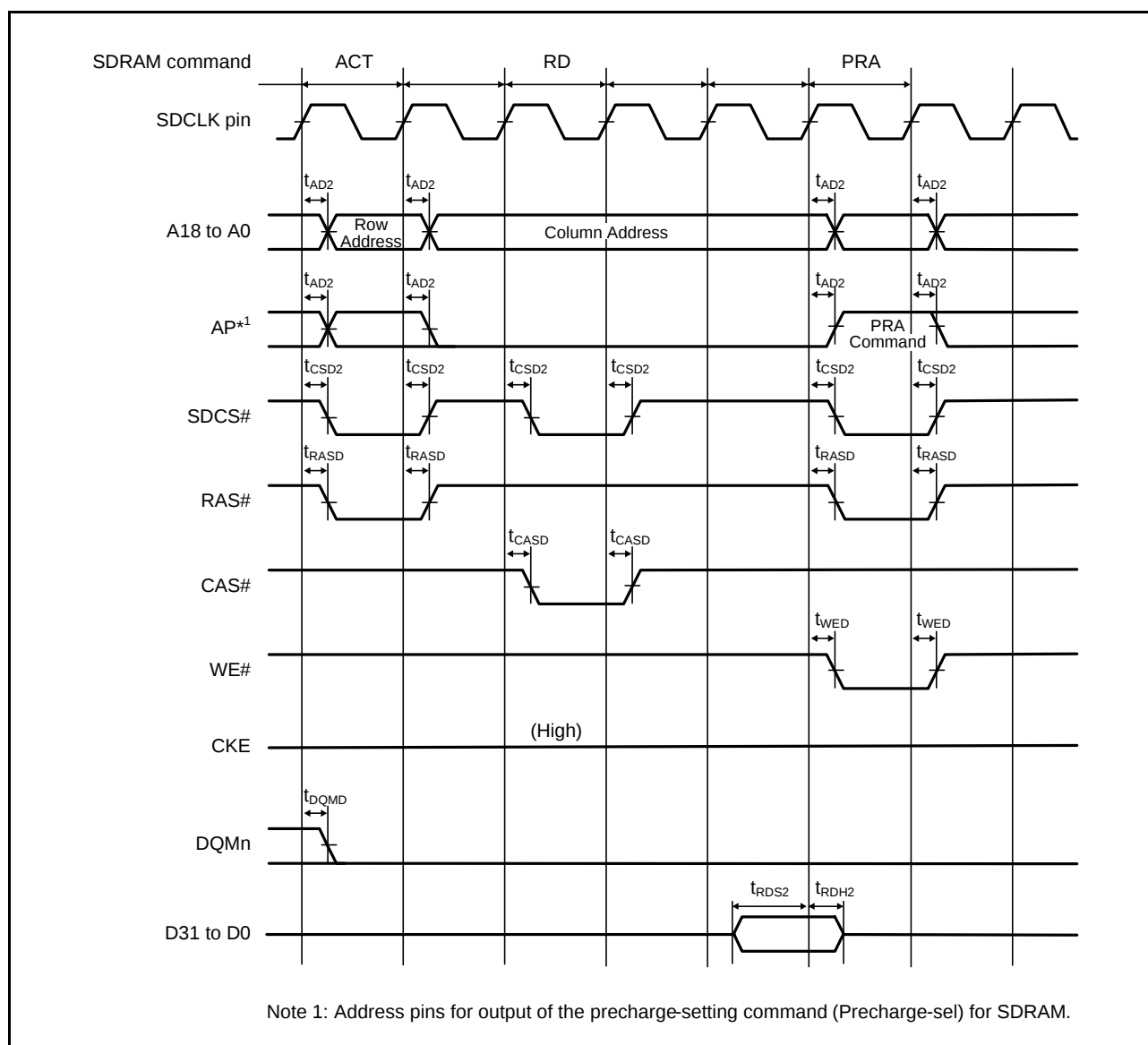


Figure 5.24 SDRAM Space Single Read Bus Timing

5.11 ROM (Flash Memory for Code Storage) Characteristics

Table 5.36 ROM (Flash Memory for Code Storage) Characteristics (1)

Conditions: VCC = AVCC0 = VREFH = VCC_USB = 2.7 to 3.6V, VREFH0 = 2.7V to AVCC0
VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0V
Temperature range for the programming/erasure operation: T_a = T_{opr}

Item	Symbol	min	typ	max	Unit	Condition
Reprogram/erasure cycle*1	N _{PEC}	1000	—	—	Times	
Data hold time	t _{DRP}	30*2	—	—	Year	T _a = +85°C

Note 1. Definition of reprogram/erase cycle:

The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 1000), erasing can be performed n times for each block. For instance, when 256-byte programming is performed 16 times for different addresses in 4-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).

Note 2. The result obtained from the reliability test.

Table 5.37 ROM (Flash Memory for Code Storage) Characteristics (2)

Conditions: VCC = AVCC0 = VREFH = VCC_USB = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0
VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V
Temperature range for the programming/erasure operation: T_a = T_{opr}

Item		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 50 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time N _{PEC} ≤ 100 times	128 bytes	t _{P128}	—	2.8	28	—	1	10	ms
	4 Kbytes	t _{P4K}	—	63	140	—	23	50	ms
	16 Kbytes	t _{P16K}	—	252	560	—	90	200	ms
Programming time N _{PEC} > 100 times	128 bytes	t _{P128}	—	3.4	33.6	—	1.2	12	ms
	4 Kbytes	t _{P4K}	—	75.6	168	—	27.6	60	ms
	16 Kbytes	t _{P16K}	—	302.4	672	—	108	240	ms
Erasure time N _{PEC} ≤ 100 times	4 Kbytes	t _{E4K}	—	50	120	—	25	60	ms
	16 Kbytes	t _{E16K}	—	200	480	—	100	240	ms
Erasure time N _{PEC} > 100 times	4 Kbytes	t _{E4K}	—	60	144	—	30	72	ms
	16 Kbytes	t _{E16K}	—	240	576	—	120	288	ms
Suspend delay time during programming		t _{SPD}	—	—	400	—	—	120	μs
First suspend delay time during erasure (in suspend priority mode)		t _{SESD1}	—	—	300	—	—	120	μs
Second suspend delay time during erasure (in suspend priority mode)		t _{SESD2}	—	—	1.7	—	—	1.7	ms
Suspend delay time during erasure (in erasure priority mode)		t _{SEED}	—	—	1.7	—	—	1.7	ms
FCU reset time		t _{FCUR}	35	—	—	35	—	—	μs

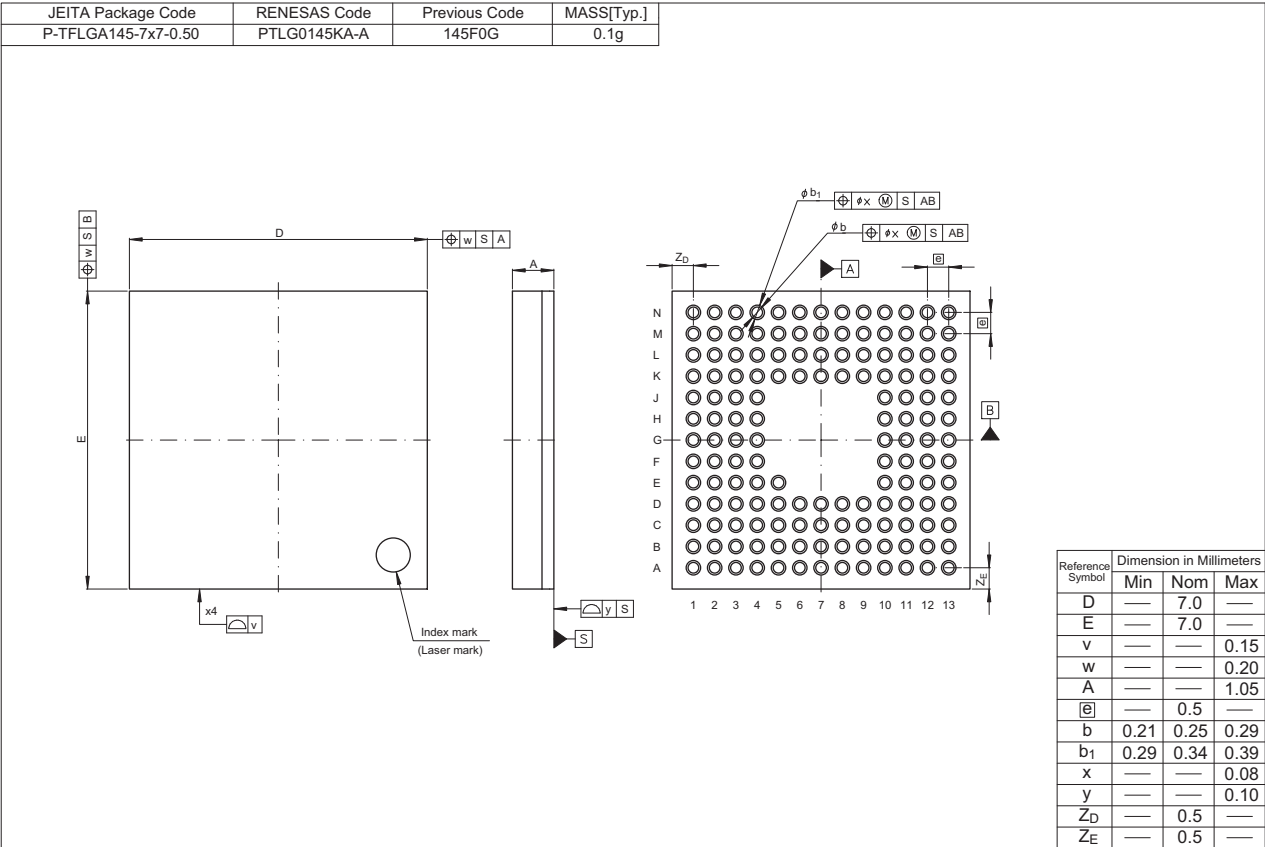


Figure D 145-pin TFLGA (PTLG0145KA-A)

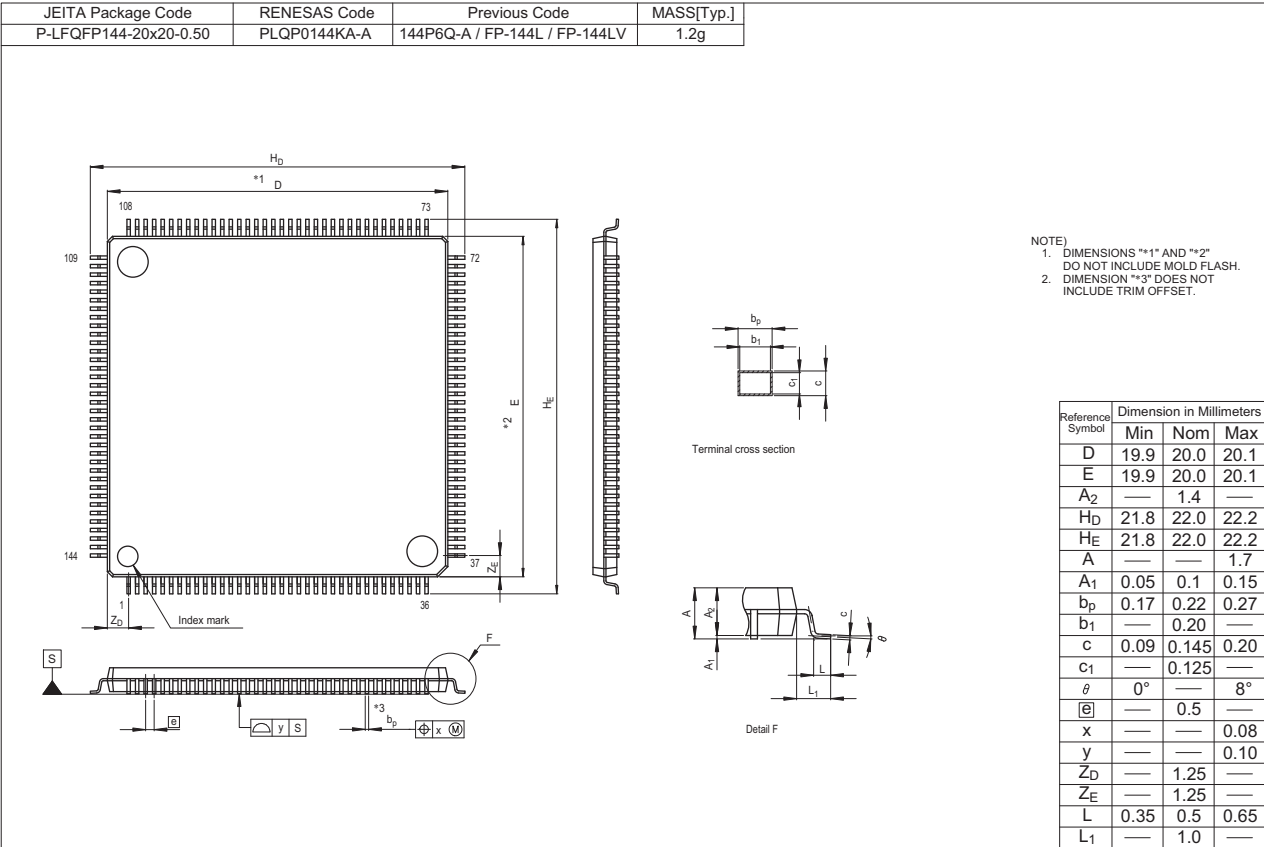


Figure E 144-pin LQFP (PLQP0144KA-A)