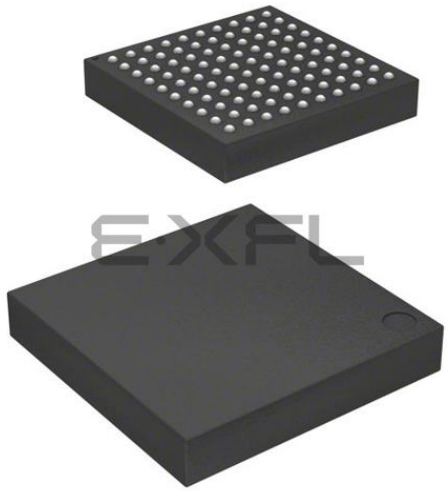
Renesas Electronics America Inc - R5F563NACDLJ#U0 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, LINbus, SCI, SPI, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	78
Program Memory Size	768KB (768K x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b, 14x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TFLGA
Supplier Device Package	100-TFLGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f563nacdlj-u0

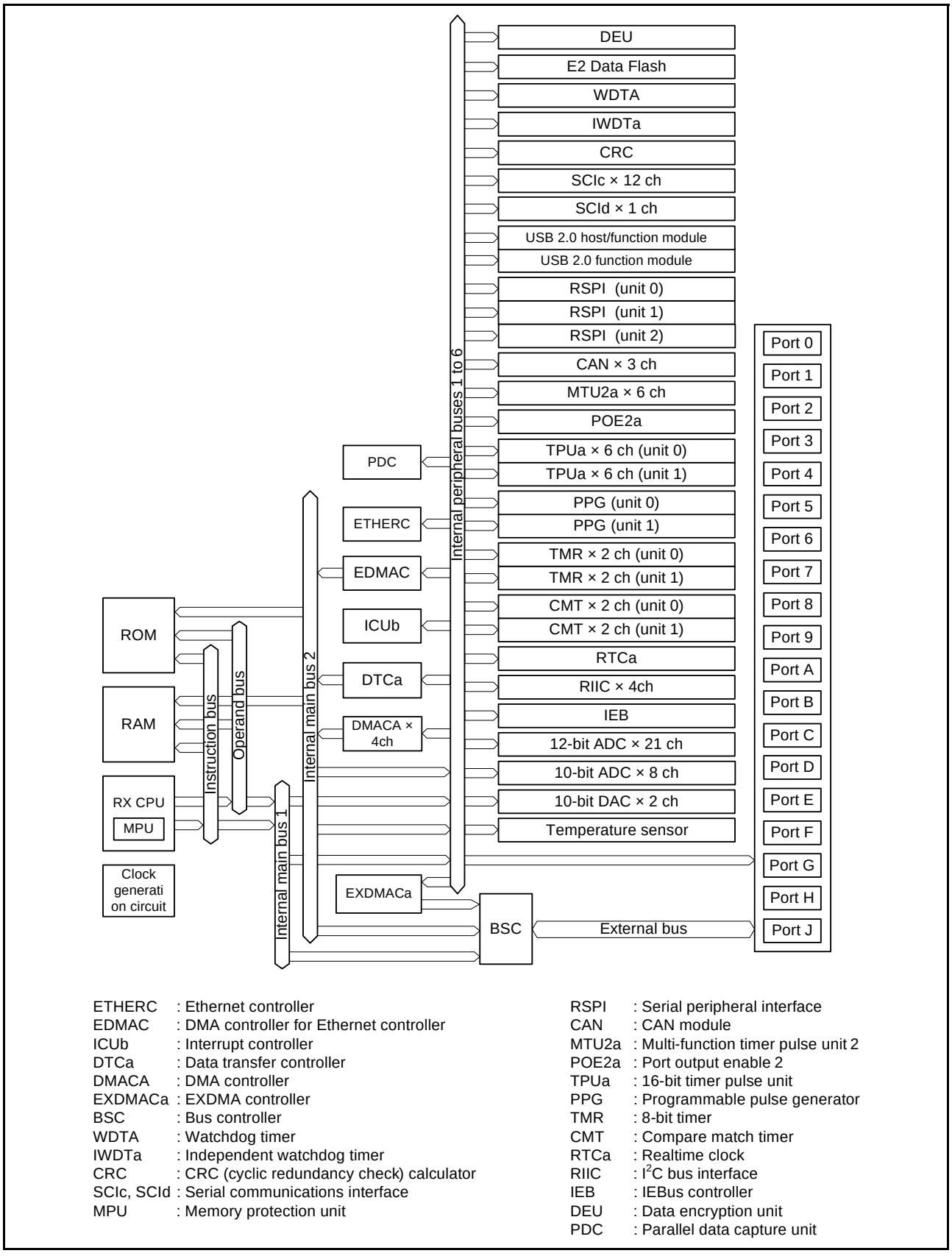
Table 1.1 Outline of Specifications (6/6)

Classification	Module/Function	Description
Communication function	Parallel data capture unit (PDC)	• 1 channel • Communicates with an image sensor or other external I/Os and transfer parallel data such as an image output from those devices to internal RAM or external address spaces (CS space and SDRAM space) through DTC or DMAC.
12-bit A/D converter (S12ADa)		• 1 unit (1 unit x 21 channels) • 12-bit resolution • Conversion time: 1.0 μs per channel (in operation with PCLK at 50 MHz) • Operating mode Scan mode (single scan mode or continuous scan mode) • Sample-and-hold function • Reference voltage generation • Three ways to start A/D conversion Conversion can be started by software, a conversion start trigger from a timer (MTU, TPU, or TMR), or an external trigger signal. • A/D conversion of the temperature sensor output
10-bit A/D converter (ADb)		• 1 unit (1 unit x 8 channels) • 10-bit resolution • Conversion time: 1.0 μs per channel (in operation with PCLK at 50 MHz) • Operating mode Scan mode (single scan mode or continuous scan mode) External amplifier connection mode • Sample-and-hold function • Three ways to start A/D conversion Conversion can be started by software, a conversion start trigger from a timer (MTU, TPU, or TMR), or an external trigger signal.
D/A converter (DAa)		• 2 channels • 10-bit resolution • Output voltage: 0 V to VREFH
Temperature sensor		• 1 channel • Precision: ±1ºC • The voltage of the temperature is converted into a digital value by the 12-bit A/D converter.
CRC calculator (CRC)		• CRC code generation for arbitrary amounts of data in 8-bit units • Select any of three generating polynomials: $X^8 + X^2 + X + 1$, $X^{16} + X^{15} + X^2 + 1$, or $X^{16} + X^{12} + X^5 + 1$. • Generation of CRC codes for use with LSB-first or MSB-first communications is selectable
Unique ID		A 16-byte device-specific ID (only for the G version)
Data encryption unit (DEU)*1		• AES encryption and decryption functions • 128/192/256-bit key length • ECB/CBC mode
Operating frequency		Up to 100 MHz
Power supply voltage		VCC = AVCC0 = VREFH = VCC_USB = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0, V_{BATT} = 2.0 V to 3.6 V (for products with 100 or more pins), V_{BATT} = 2.3 V to 3.6 V (for the 64-pin product)
Operating temperature		D version: -40 to +85°C, G version: -40 to +105°C*2
Package		177-pin TFLGA (PTLG0177KA-A) 176-pin LFBGA (PLBG0176GA-A) 176-pin LQFP (PLQP0176KB-A) 145-pin TFLGA (PTLG0145KA-A) 144-pin LQFP (PLQP0144KA-A) 100-pin TFLGA (PTLG0100JA-A) (in the planning stage) 100-pin LQFP (PLQP0100KB-A) 64-pin TFLGA (PTLG0064JA-A) 64-pin LQFP (PLQP0064KB-A) 48-pin LQFP (PLQP0048KB-A)
On-chip debugging system		• E1 emulator (JTAG and FINE interfaces) • E20 emulator (JTAG interface)

Note 1. Please contact our sales office for more information.
Note 2. Please contact us if you are using a G version.

1.3 Block Diagram

Figure 1.2 shows a block diagram.



ETHERC : Ethernet controller
EDMAC : DMA controller for Ethernet controller
ICUb : Interrupt controller
DTCa : Data transfer controller
DMACA : DMA controller
EXDMACa : EXDMA controller
BSC : Bus controller
WDTA : Watchdog timer
IWDTa : Independent watchdog timer
CRC : CRC (cyclic redundancy check) calculator
SCIc, SCId : Serial communications interface
MPU : Memory protection unit

RSPI : Serial peripheral interface
CAN : CAN module
MTU2a : Multi-function timer pulse unit 2
POE2a : Port output enable 2
TPUa : 16-bit timer pulse unit
PPG : Programmable pulse generator
TMR : 8-bit timer
CMT : Compare match timer
RTCa : Realtime clock
RIIC : I^2C bus interface
IEB : IEBus controller
DEU : Data encryption unit
PDC : Parallel data capture unit

Figure 1.2 Block Diagram

RX63N Group, RX631 Group
PTLG0100JA-A (100-pin TFLGA)
(Top view)

	A	B	C	D	E	F	G	H	J	K	
10	PE2	PE3	PE4	PA0	PA3	VSS	VCC	PB7	PC1	PC2	10
9	PE1	PD7	PE5	PA1	PA5	PA7	PB1	PB6	PC0	PC3	9
8	PE0	PD6	PD5	PE7	PA4	PB0	PB4	PC6	PC4	PC5	8
7	PD4	PD3	PD2	PE6	PA6	PB2	PB5	PC7	P50	P51	7
6	PD0	PD1	P47	P46	PA2	PB3	P52	P54	VCC_ USB	USB0_ DP	6
5	P43	P44	P42	P45	P41	P12	P53	P55	VSS_ USB	USB0_ DM	5
4	VREFL0	P40	VREFH0	VBATT	P34	P32	P27	P15	P13	P14	4
3	P07	AVCC0	PJ3	MD/ FINED	RES#	P35	P30	P16	P17	P20	3
2	VREFH	AVSS0	VREFL	XCOUT	VSS	VCC	P31	P25	P21	P22	2
1	P05	EMLE	VCL	XCIN	XTAL	EXTAL	P33	P26	P24	P23	1
	A	B	C	D	E	F	G	H	J	K	

Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.10, List of Pins and Pin Functions (100-Pin LQFP).

Figure 1.8 Pin Assignment (100-Pin TFLGA)

Table 1.9 List of Pins and Pin Functions (100-Pin TFLGA) (2/5)

Pin No. 100-pin TFLGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC	Timers (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SCIc, SCId, RSPI, RIIC, CAN, IEB, USB)	Interrupt	S12AD AD DA
D2	XCOUT						
D3	MD/FINED						
D4	VBATT						
D5		P45				IRQ13-DS	AN005
D6		P46				IRQ14-DS	AN006
D7		PE6	D14[A14/D14]		MOSIB	IRQ6	AN4
D8		PE7	D15[A15/D15]		MISOB	IRQ7	AN5
D9		PA1	A1	MTIOC0B/ MTCLKC/ TIOCB0/PO17	SCK5/SSLA2/ ET_WOL	IRQ11	
D10		PA0	A0/BC0#	MTIOC4A/ TIOCA0/PO16	SSLA1/ET_TX_EN/ RMII_TXD_EN		
E1	XTAL	P37					
E2	VSS						
E3	RES#						
E4	TRST#	P34		MTIOC0A/ TMCI3/PO12/ POE2#	SCK6/SCK0/ USB0_DPRPD	IRQ4	
E5		P41				IRQ9-DS	AN001
E6		PA2	A2	PO18	RXD5/SMISO5/ SSCL5/SSLA3		
E7		PA6	A6	MTIC5V/ MTCLKB/ TIOCA2/ TMCI3/PO22/ POE2#	CTS5#/RTS5#/ SS5#/MOSIA/ ET_EXOUT		
E8		PA4	A4	MTIC5U/ MTCLKA/ TIOCA1/ TMRI0/PO20	TXD5/SMOSI5/ SSDA5/SSLA0/ ET_MDC	IRQ5-DS	
E9		PA5	A5	TIOCB1/PO21	RSPCKA/ ET_LINKSTA		
E10		PA3	A3	MTIOC0D/ MTCLKD/ TIOCD0/ TCLKB/PO19	RXD5/SMISO5/ SSCL5/ET_MDIO	IRQ6-DS	
F1	EXTAL	P36					
F2	VCC						
F3		P35				NMI	
F4		P32		MTIOC0C/ TIOCC0/TMO3/ PO10/ RTCOUT/ RTCIC2	TXD6/TXD0/ SMOSI6/SMOSI0/ SSDA6/SSDA0/ CTX0*1/ USB0_VBUSEN	IRQ2-DS	
F5		P12		TMCI1	RXD2/SMISO2/ SSCL2/SCL0[FM+]	IRQ2	
F6		PB3	A11	MTIOC0A/ MTIOC4A/ TIOCD3/ TCLKD/TMO0/ PO27/POE3#	SCK6/ET_RX_ER/ RMII_RX_ER		

Table 1.9 List of Pins and Pin Functions (100-Pin TFLGA) (4/5)

Pin No. 100-pin TFLGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC	Timers (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SCIc, SCId, RSPI, RIIC, CAN, IEB, USB)	Interrupt	S12AD AD DA
H4		P15		MTIOC0B/ MTCLKB/ TIOCB2/ TCLKB/TMCI2/ PO13	RXD1/SCK3/ SMISO1/SSCL1/ CRX1-DS	IRQ5	
H5		P55	WAIT#/ EDREQ0	MTIOC4D/ TMO3	CRX1/ET_EXOUT	IRQ10	
H6		P54	ALE/EDACK0	MTIOC4B/ TMCI1	CTS2#/RTS2#/ SS2#/CTX1/ ET_LINKSTA		
H7		PC7	A23/CS0#	MTIOC3A/ MTCLKB/ TMO2/PO31	TXD8/SMOSI8/ SSDA8/MISOA/ ET_COL	IRQ14	
H8		PC6	A22/CS1#	MTIOC3C/ MTCLKA/ TMCI2/PO30	RXD8/SMISO8/ SSCL8/MOSIA/ ET_ETXD3	IRQ13	
H9		PB6	A14	MTIOC3D/ TIOCA5/PO30	RXD9/SMISO9/ SSCL9/ET_ETXD1/ RMII_TXD1		
H10		PB7	A15	MTIOC3B/ TIOCB5/PO31	TXD9/SMOSI9/ SSDA9/ET_CRS/ RMII_CRS_DV		
J1		P24	CS4#/ EDREQ1	MTIOC4A/ MTCLKA/ TIOCB4/ TMRI1/PO4	SCK3/ USB0_VBUSEN		
J2		P21		MTIOC1B/ TIOCA3/ TMCI0/PO1	RXD0/SMISO0/ SSCL0/ USB0_EXICEN	IRQ9	
J3		P17		MTIOC3A/ MTIOC3B/ TIOCB0/ TCLKD/TMO1/ PO15/POE8#	SCK1/TXD3/ SMOSI3/SSDA3/ MISOA/SDA2-DS/ IETXD	IRQ7	ADTRG#
J4		P13		MTIOC0B/ TIOCA5/TMO3/ PO13	TXD2/SMOSI2/ SSDA2/SDA0[FM+]	IRQ3	ADTRG#
J5	VSS_USB						
J6	VCC_USB						
J7		P50	WR0#/WR#		TXD2/SMOSI2/ SSDA2/SSLB1		
J8		PC4	A20/CS3#	MTIOC3D/ MTCLKC/ TMCI1/PO25/ POE0#	SCK5/CTS8#/ RTS8#/SS8#/ SSLA0/ET_TX_CLK		
J9		PC0	A16	MTIOC3C/ TCLKC/PO17	CTS5#/RTS5#/ SS5#/SSLA1/ ET_ERXD3	IRQ14	
J10		PC1	A17	MTIOC3A/ TCLKD/PO18	SCK5/SSLA2/ ET_ERXD2	IRQ12	
K1		P23	EDACK0	MTIOC3D/ MTCLKD/ TIOCD3/PO3	TXD3/CTS0#/ RTS0#/SMOSI3/ SS0#/SSDA3/ USB0_DPUPE		

Table 1.10 List of Pins and Pin Functions (100-Pin LQFP) (2/4)

Pin No. 100-pin LQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC	Timers (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SCIc, SCId, RSPI, RIIC, CAN, IEB, USB)	Interrupt	S12AD AD DA
31		P15		MTIOC0B/MTCLKB/ TIOCB2/TCLKB/TMCI2/ PO13	RXD1/SCK3/SMISO1/ SSCL1/CRX1-DS	IRQ5	
32		P14		MTIOC3A/MTCLKA/ TIOCB5/TCLKA/TMRI2/ PO15	CTS1#/RTS1#/SS1#/ CTX1/USB0_DPUPE/ USB0_OVRCURA	IRQ4	
33		P13		MTIOC0B/TIOCA5/ TMO3/PO13	TXD2/SMOSI2/SSDA2/ SDA0[FM+]	IRQ3	ADTRG#
34		P12		TMCI1	RXD2/SMISO2/SSCL2/ SCL0[FM+]	IRQ2	
35	VCC_USB						
36					USB0_DM		
37					USB0_DP		
38	VSS_USB						
39		P55	WAIT#/ EDREQ0	MTIOC4D/TMO3	CRX1/ET_EXOUT	IRQ10	
40		P54	ALE/EDACK0	MTIOC4B/TMCI1	CTS2#/RTS2#/SS2#/ CTX1/ET_LINKSTA		
41		P53*2	BCLK				
42		P52	RD#		RXD2/SMISO2/SSCL2/ SSLB3		
43		P51	WR1#/BC1#/ WAIT#		SCK2/SSLB2		
44		P50	WR0#/WR#		TXD2/SMOSI2/SSDA2/ SSLB1		
45		PC7	A23/CS0#	MTIOC3A/MTCLKB/ TMO2/PO31	TXD8/SMOSI8/SSDA8/ MISOA/ET_COL	IRQ14	
46		PC6	A22/CS1#	MTIOC3C/MTCLKA/ TMCI2/PO30	RXD8/SMISO8/SSCL8/ MOSIA/ET_ETXD3	IRQ13	
47		PC5	A21/CS2#/ WAIT#	MTIOC3B/MTCLKD/ TMRI2/PO29	SCK8/RSPCKA/ ET_ETXD2		
48		PC4	A20/CS3#	MTIOC3D/MTCLKC/ TMCI1/PO25/POE0#	SCK5/CTS8#/RTS8#/ SS8#/SSLA0/ ET_TX_CLK		
49		PC3	A19	MTIOC4D/TCLKB/ PO24	TXD5/SMOSI5/SSDA5/ IETXD/ET_TX_ER		
50		PC2	A18	MTIOC4B/TCLKA/PO21	RXD5/SMISO5/SSCL5/ SSLA3/IERXD/ ET_RX_DV		
51		PC1	A17	MTIOC3A/TCLKD/ PO18	SCK5/SSLA2/ ET_ERXD2	IRQ12	
52		PC0	A16	MTIOC3C/TCLKC/ PO17	CTS5#/RTS5#/SS5#/ SSLA1/ET_ERXD3	IRQ14	
53		PB7	A15	MTIOC3B/TIOCB5/ PO31	TXD9/SMOSI9/SSDA9/ ET_CRS/ RMII_CRS_DV		
54		PB6	A14	MTIOC3D/TIOCA5/ PO30	RXD9/SMISO9/SSCL9/ ET_ETXD1/RMII_TXD1		
55		PB5	A13	MTIOC2A/MTIOC1B/ TIOCB4/TMRI1/PO29/ POE1#	SCK9/ET_ETXD0/ RMII_TXD0		
56		PB4	A12	TIOCA4/PO28	CTS9#/RTS9#/SS9#/ ET_TX_EN/ RMII_TXD_EN		
57		PB3	A11	MTIOC0A/MTIOC4A/ TIOCD3/TCLKD/TMO0/ PO27/POE3#	SCK6/ET_RX_ER/ RMII_RX_ER		
58		PB2	A10	TIOCC3/TCLKC/PO26	CTS6#/RTS6#/SS6#/ ET_RX_CLK/REF50CK		

3. Address Space

3.1 Address Space

This LSI has a 4-Gbyte address space, consisting of the range of addresses from 0000 0000h to FFFF FFFFh. That is, linear access to an address space of up to 4 Gbytes is possible, and this contains both program and data areas.
Figure 3.1 shows the memory maps in the respective operating modes. Accessible areas will differ according to the operating mode and states of control bits.

Table 4.1 List of I/O Registers (Address Order) (17/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 81A8h	TPU8	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 81AAh	TPU8	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	
0008 81B0h	TPU9	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK	
0008 81B1h	TPU9	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK	
0008 81B2h	TPU9	Timer I/O control register H	TIORH	8	8	2, 3 PCLKB	2 ICLK	
0008 81B3h	TPU9	Timer I/O control register L	TIORL	8	8	2, 3 PCLKB	2 ICLK	
0008 81B4h	TPU9	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK	
0008 81B5h	TPU9	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK	
0008 81B6h	TPU9	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	
0008 81B8h	TPU9	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	
0008 81BAh	TPU9	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	
0008 81BCh	TPU9	Timer general register C	TGRC	16	16	2, 3 PCLKB	2 ICLK	
0008 81BEh	TPU9	Timer general register D	TGRD	16	16	2, 3 PCLKB	2 ICLK	
0008 81C0h	TPU10	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK	
0008 81C1h	TPU10	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK	
0008 81C2h	TPU10	Timer I/O control register	TIOR	8	8	2, 3 PCLKB	2 ICLK	
0008 81C4h	TPU10	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK	
0008 81C5h	TPU10	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK	
0008 81C6h	TPU10	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	
0008 81C8h	TPU10	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	
0008 81CAh	TPU10	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	
0008 81D0h	TPU11	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK	
0008 81D1h	TPU11	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK	
0008 81D2h	TPU11	Timer I/O control register	TIOR	8	8	2, 3 PCLKB	2 ICLK	
0008 81D4h	TPU11	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK	
0008 81D5h	TPU11	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK	
0008 81D6h	TPU11	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	
0008 81D8h	TPU11	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	
0008 81DAh	TPU11	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	
0008 81E6h	PPG0	PPG output control register	PCR	8	8	2, 3 PCLKB	2 ICLK	PPG
0008 81E7h	PPG0	PPG output mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 81E8h	PPG0	Next data enable register H	NDERH	8	8	2, 3 PCLKB	2 ICLK	
0008 81E9h	PPG0	Next data enable register L	NDERL	8	8	2, 3 PCLKB	2 ICLK	
0008 81EAh	PPG0	Output data register H	PODRH	8	8	2, 3 PCLKB	2 ICLK	
0008 81EBh	PPG0	Output data register L	PODRL	8	8	2, 3 PCLKB	2 ICLK	
0008 81ECh*1	PPG0	Next data register H	NDRH	8	8	2, 3 PCLKB	2 ICLK	
0008 81EDh*2	PPG0	Next data register L	NDRL	8	8	2, 3 PCLKB	2 ICLK	
0008 81EEh*1	PPG0	Next data register H	NDRH2	8	8	2, 3 PCLKB	2 ICLK	
0008 81EFh*2	PPG0	Next data register L	NDRL2	8	8	2, 3 PCLKB	2 ICLK	
0008 81F0h	PPG1	PPG trigger select register	PTRSLR	8	8	2, 3 PCLKB	2 ICLK	
0008 81F6h	PPG1	PPG output control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 81F7h	PPG1	PPG output mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 81F8h	PPG1	Next data enable register H	NDERH	8	8	2, 3 PCLKB	2 ICLK	
0008 81F9h	PPG1	Next data enable register L	NDERL	8	8	2, 3 PCLKB	2 ICLK	
0008 81FAh	PPG1	Output data register H	PODRH	8	8	2, 3 PCLKB	2 ICLK	
0008 81FBh	PPG1	Output data register L	PODRL	8	8	2, 3 PCLKB	2 ICLK	
0008 81FCh*3	PPG1	Next data register H	NDRH	8	8	2, 3 PCLKB	2 ICLK	
0008 81FDh*4	PPG1	Next data register L	NDRL	8	8	2, 3 PCLKB	2 ICLK	
0008 81FEh*3	PPG1	Next data register H	NDRH2	8	8	2, 3 PCLKB	2 ICLK	PPG
0008 81FFh*4	PPG1	Next data register L	NDRL2	8	8	2, 3 PCLKB	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (34/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 C1B1h	MPC	PE1 pin function control register	PE1PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1B2h	MPC	PE2 pin function control register	PE2PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1B3h	MPC	PE3 pin function control register	PE3PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1B4h	MPC	PE4 pin function control register	PE4PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1B5h	MPC	PE5 pin function control register	PE5PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1B6h	MPC	PE6 pin function control register	PE6PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1B7h	MPC	PE7 pin function control register	PE7PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1B8h	MPC	PF0 pin function control register	PF0PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1B9h	MPC	PF1 pin function control register	PF1PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1BAh	MPC	PF2 pin function control register	PF2PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1BDh	MPC	PF5 pin function control register	PF5PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1D3h	MPC	PJ3 pin function control register	PJ3PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C280h	SYSTEM	Deep standby control register	DPSBYCR	8	8	4, 5 PCLKB	2, 3 ICLK	Low Power Consumption
0008 C282h	SYSTEM	Deep standby interrupt enable register 0	DPSIER0	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C283h	SYSTEM	Deep standby interrupt enable register 1	DPSIER1	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C284h	SYSTEM	Deep standby interrupt enable register 2	DPSIER2	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C285h	SYSTEM	Deep standby interrupt enable register 3	DPSIER3	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C286h	SYSTEM	Deep standby interrupt flag register 0	DPSIFR0	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C287h	SYSTEM	Deep standby interrupt flag register 1	DPSIFR1	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C288h	SYSTEM	Deep standby interrupt flag register 2	DPSIFR2	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C289h	SYSTEM	Deep standby interrupt flag register 3	DPSIFR3	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C28Ah	SYSTEM	Deep standby interrupt edge register 0	DPSIEGR0	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C28Bh	SYSTEM	Deep standby interrupt edge register 1	DPSIEGR1	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C28Ch	SYSTEM	Deep standby interrupt edge register 2	DPSIEGR2	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C28Dh	SYSTEM	Deep standby interrupt edge register 3	DPSIEGR3	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C290h	SYSTEM	Reset status register 0	RSTSR0	8	8	4, 5 PCLKB	2, 3 ICLK	Resets
0008 C291h	SYSTEM	Reset status register 1	RSTSR1	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C293h	SYSTEM	Main clock oscillator forced oscillation control register	MOFCR	8	8	4, 5 PCLKB	2, 3 ICLK	Clock Generation Circuit
0008 C294h	SYSTEM	High-speed on-chip oscillator power supply control register	HOCOPCR	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C296h	FLASH	Flash write erase protection register	FWEPROR	8	8	4, 5 PCLKB	2, 3 ICLK	ROM
0008 C297h	SYSTEM	Voltage monitoring circuit control register	LVCMPCR	8	8	4, 5 PCLKB	2, 3 ICLK	LVDA
0008 C298h	SYSTEM	Voltage detection level select register	LVDLVLR	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C29Ah	SYSTEM	Voltage monitoring 1 circuit control register 0	LVD1CR0	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C29Bh	SYSTEM	Voltage monitoring 2 circuit control register 0	LVD2CR0	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C2A0h to 0008 C2BFh	SYSTEM	Deep standby backup register 0 to 31	DPSBKR0 to 31	8	8	4, 5 PCLKB	2, 3 ICLK	Low Power Consumption
0008 C300h	ICU	Group 0 interrupt source register	GRP00	32	32	1 to 2PCLKB	2 ICLK	ICUb
0008 C304h	ICU	Group 1 interrupt source register	GRP01	32	32	1 to 2PCLKB	2 ICLK	
0008 C308h	ICU	Group 2 interrupt source register	GRP02	32	32	1 to 2PCLKB	2 ICLK	
0008 C30Ch	ICU	Group 3 interrupt source register	GRP03	32	32	1 to 2PCLKB	2 ICLK	
0008 C310h	ICU	Group 4 interrupt source register	GRP04	32	32	1 to 2PCLKB	2 ICLK	
0008 C314h	ICU	Group 5 interrupt source register	GRP05	32	32	1 to 2PCLKB	2 ICLK	
0008 C318h	ICU	Group 6 interrupt source register	GRP06	32	32	1 to 2PCLKB	2 ICLK	
0008 C330h	ICU	Group 12 interrupt source register	GRP12	32	32	1 to 2PCLKB	2 ICLK	
0008 C340h	ICU	Group 0 interrupt enable register	GEN00	32	32	1 to 2PCLKB	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (39/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
000A 003Ah	USB0	BEMP interrupt enable register	BEMPENB	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	USBa
000A 003Ch	USB0	SOF output configuration register	SOFCFG	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	
000A 0040h	USB0	Interrupt status register 0	INTSTS0	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	
000A 0042h	USB0	Interrupt status register 1	INTSTS1	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	
000A 0046h	USB0	BRDY interrupt status register	BRDYSTS	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	
000A 0048h	USB0	NRDY interrupt status register	NRDYSTS	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	
000A 004Ah	USB0	BEMP interrupt status register	BEMPSTS	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	
000A 004Ch	USB0	Frame number register	FRMNUM	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	
000A 004Eh	USB0	Device state changing register	DVCHGR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	USBa
000A 0050h	USB0	USB address register	USBADDR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6	

Table 4.1 List of I/O Registers (Address Order) (50/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
007F C402h	FLASH	Flash mode register	FMODR	8	8	2 to 4 FCLK	2, 3 ICLK	Flash Memory
007F C410h	FLASH	Flash access status register	FASTAT	8	8	2 to 4 FCLK	2, 3 ICLK	
007F C411h	FLASH	Flash access error interrupt enable register	FAEINT	8	8	2 to 4 FCLK	2, 3 ICLK	
007F C412h	FLASH	Flash ready interrupt enable register	FRDYIE	8	8	2 to 4 FCLK	2, 3 ICLK	
007F C440h	FLASH	E2 DataFlash read enable register 0	DFLRE0	16	16	2 to 4 FCLK	2, 3 ICLK	
007F C442h	FLASH	E2 DataFlash read enable register 1	DFLRE1	16	16	2 to 4 FCLK	2, 3 ICLK	
007F C450h	FLASH	E2 DataFlash P/E enable register 0	DFLWE0	16	16	2 to 4 FCLK	2, 3 ICLK	
007F C452h	FLASH	E2 DataFlash P/E enable register 1	DFLWE1	16	16	2 to 4 FCLK	2, 3 ICLK	
007F C454h	FLASH	FCU RAM enable register	FCURAME	16	16	2 to 4 FCLK	2, 3 ICLK	
007F FFB0h	FLASH	Flash status register 0	FSTATR0	8	8	2 to 4 FCLK	2, 3 ICLK	
007F FFB1h	FLASH	Flash status register 1	FSTATR1	8	8	2 to 4 FCLK	2, 3 ICLK	
007F FFB2h	FLASH	Flash P/E mode entry register	FENTRYR	16	16	2 to 4 FCLK	2, 3 ICLK	
007F FFB4h	FLASH	Flash protection register	FPROTR	16	16	2 to 4 FCLK	2, 3 ICLK	
007F FFB6h	FLASH	Flash reset register	FRESETR	16	16	2 to 4 FCLK	2, 3 ICLK	
007F FFBAh	FLASH	FCU command register	FCMDR	16	16	2 to 4 FCLK	2, 3 ICLK	
007F FFC8h	FLASH	FCU processing switching register	FCPSR	16	16	2 to 4 FCLK	2, 3 ICLK	
007F FFCAh	FLASH	E2 data flash blank check control register	DFLBCCNT	16	16	2 to 4 FCLK	2, 3 ICLK	
007F FFCCh	FLASH	Flash P/E status register	FPESTAT	16	16	2 to 4 FCLK	2, 3 ICLK	
007F FFCEh	FLASH	E2 DataFlash blank check status register	DFLBCSTAT	16	16	2 to 4 FCLK	2, 3 ICLK	
007F FFE8h	FLASH	Peripheral clock notification register	PCKAR	16	16	2 to 4 FCLK	2, 3 ICLK	
FEFF FAC0h	FLASH	Unique ID register 0*8	UIDR0	8	8	1 ICLK	1 ICLK	
FEFF FAC1h	FLASH	Unique ID register 1*8	UIDR1	8	8	1 ICLK	1 ICLK	
FEFF FAC2h	FLASH	Unique ID register 2*8	UIDR2	8	8	1 ICLK	1 ICLK	
FEFF FAC3h	FLASH	Unique ID register 3*8	UIDR3	8	8	1 ICLK	1 ICLK	
FEFF FAC4h	FLASH	Unique ID register 4*8	UIDR4	8	8	1 ICLK	1 ICLK	
FEFF FAC5h	FLASH	Unique ID register 5*8	UIDR5	8	8	1 ICLK	1 ICLK	
FEFF FAC6h	FLASH	Unique ID register 6*8	UIDR6	8	8	1 ICLK	1 ICLK	
FEFF FAC7h	FLASH	Unique ID register 7*8	UIDR7	8	8	1 ICLK	1 ICLK	
FEFF FAC8h	FLASH	Unique ID register 8*8	UIDR8	8	8	1 ICLK	1 ICLK	
FEFF FAC9h	FLASH	Unique ID register 9*8	UIDR9	8	8	1 ICLK	1 ICLK	
FEFF FACAh	FLASH	Unique ID register 10*8	UIDR10	8	8	1 ICLK	1 ICLK	
FEFF FACBh	FLASH	Unique ID register 11*8	UIDR11	8	8	1 ICLK	1 ICLK	
FEFF FACCh	FLASH	Unique ID register 12*8	UIDR12	8	8	1 ICLK	1 ICLK	
FEFF FACDh	FLASH	Unique ID register 13*8	UIDR13	8	8	1 ICLK	1 ICLK	
FEFF FACEh	FLASH	Unique ID register 14*8	UIDR14	8	8	1 ICLK	1 ICLK	
FEFF FACFh	FLASH	Unique ID register 15*8	UIDR15	8	8	1 ICLK	1 ICLK	
FEFF FAD2h	TEMPS	Temperature sensor calibration data register*8	TSCDRL	8	8	1 ICLK	1 ICLK	Temperature sensor
FEFF FAD3h	TEMPS	Temperature sensor calibration data register*8	TSCDRH	8	8	1 ICLK	1 ICLK	

Note 1. When the same output trigger is specified for pulse output groups 2 and 3 by the PPG0.PCR setting, the PPG0.NDRH address is 000881ECh. When different output triggers are specified, the PPG0.NDRH addresses for pulse output groups 2 and 3 are 000881EEh and 000881ECh, respectively.

Note 2. When the same output trigger is specified for pulse output groups 0 and 1 by the PPG0.PCR setting, the PPG0.NDRL address is 000881EDh. When different output triggers are specified, the PPG0.NDRL addresses for pulse output groups 0 and 1 are 000881EFh and 000881EDh, respectively.

Note 3. When the same output trigger is specified for pulse output groups 6 and 7 by the PPG1.PCR setting, the PPG1.NDRH address is 000881FCh. When different output triggers are specified, the PPG1.NDRH addresses for pulse output groups 6 and 7 are 000881FEh and 000881FCh, respectively.

Note 4. When the same output trigger is specified for pulse output groups 4 and 5 by the PPG1.PCR setting, the PPG1.NDRL address is 000881FDh. When different output triggers are specified, the PPG1.NDRL addresses for pulse output groups 4 and 5 are 000881FFh and 000881FDh, respectively.

Note 5. Odd addresses should not be accessed in 16-bit units. When accessing a register in 16-bit units, access the address of the TMR0 or TMR2 register. Table 27.4 lists register allocation for 16-bit access in the User's manual: Hardware.

Note 6. When the register is accessed while the USB is operating, a delay may be generated in accessing.

Note 7. The addresses with odd number cannot be accessed in 16-bit units. 16-bit access to a register should be made to the addresses of the TMOCNTL register. Allocation of registers to be accessed in 16-bit units is described in the Table 36.6, Allocation of Registers to be Accessed in 16-bit Units in the User's manual: Hardware.

Note 8. These registers are only present in the G version.

5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Table 5.1 Absolute Maximum Ratings

Conditions: VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V

Item		Symbol	Value	Unit
Power supply voltage		VCC, VCC_USB	–0.3 to +4.6	V
V_{BATT} power supply voltage		V_{BATT}	–0.3 to +4.6	V
Input voltage (except for ports for 5 V tolerant*1)		V_{in}	–0.3 to VCC + 0.3	V
Input voltage (ports for 5 V tolerant*1)		V_{in}	–0.3 to +5.8	V
Reference power supply voltage		VREFH	–0.3 to VCC + 0.3	V
Analog power supply voltage		AVCC*2	–0.3 to +4.6	V
Analog input voltage		V_{AN}	–0.3 to VCC + 0.3	V
Operating temperature	D version	T_{opr}	–40 to +85	°C
	G version		–40 to +105	°C
Storage temperature		T_{stg}	–55 to +125	°C

Caution: Permanent damage to the LSI may result if absolute maximum ratings are exceeded.

Note 1. Ports 07, 12 to 17, 20, 21, 30 to 33, 67, and C0 to C3 are 5 V tolerant.

Note 2. Connect AVCC0 to VCC. When neither the A/D converter nor the D/A converter is in use, do not leave the AVCC0, VREFH/VREFH0, AVSS0, and VREFL/VREFL0 pins open. Connect the AVCC0 and VREFH/VREFH0 pins to VCC, and the AVSS0 and VREFL/VREFL0 pins to VSS, respectively.

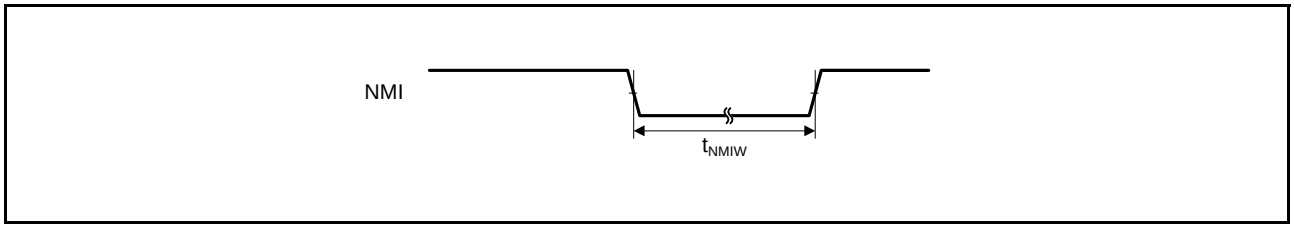


Figure 5.15 NMI Interrupt Input Timing

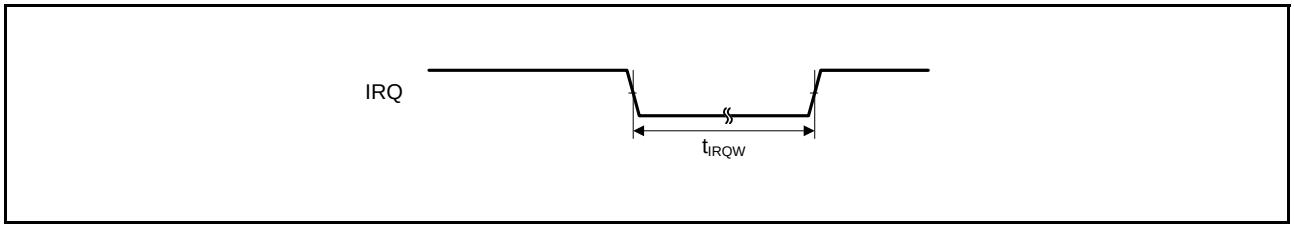
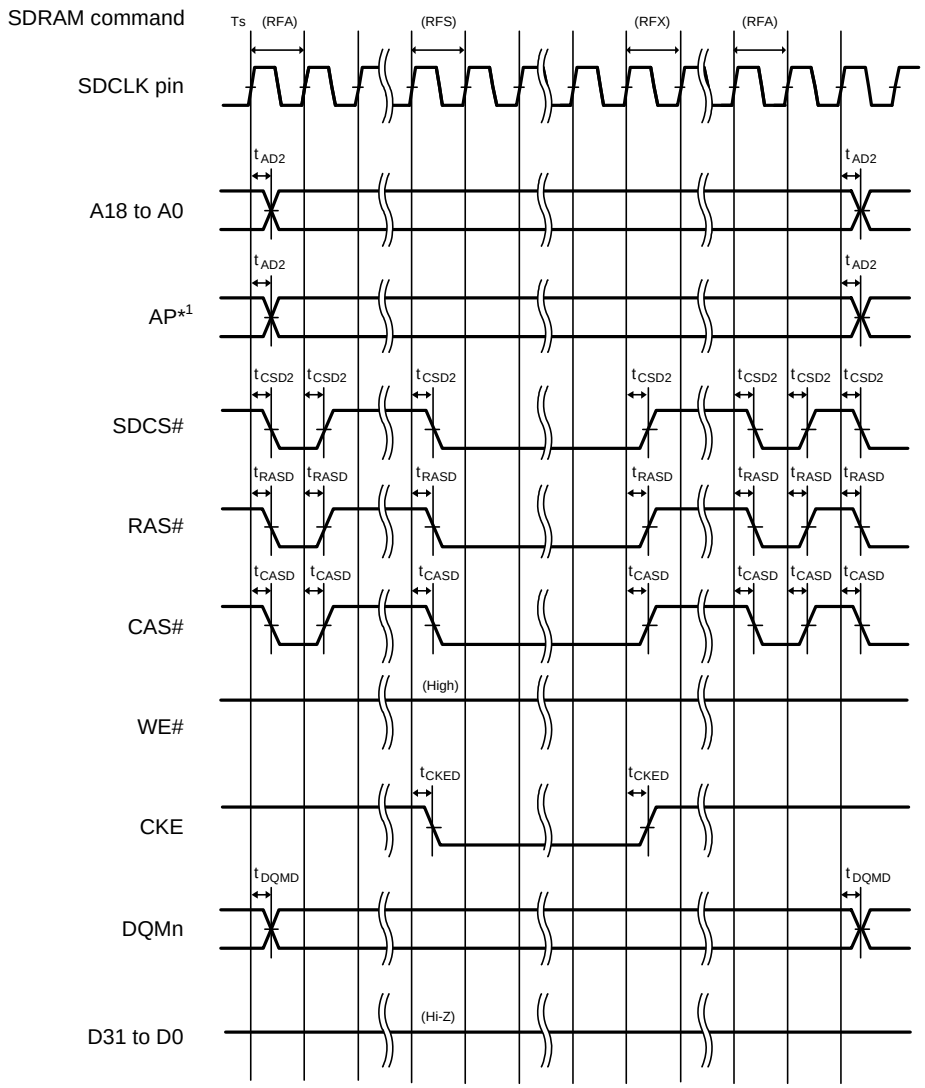


Figure 5.16 IRQ Interrupt Input Timing



Note 1: Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

Figure 5.30 SDRAM Space Self-Refresh Bus Timing

5.3.7 Timing of On-Chip Peripheral Modules

Table 5.19 Timing of On-Chip Peripheral Modules (1)

Conditions: VCC = AVCC0 = VREFH = VCC_USB = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0,
VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V
PCLK = 8 to 50 MHz
$T_a = T_{opr}$
High drive output is selected by the drive capacity control register.

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
I/O ports	Input data pulse width		t_{PRW}	1.5	—	t_{Pcyc}	Figure 5.34
MTU/TPU	Input capture input pulse width	Single-edge setting	t_{TICW}	1.5	—	t_{Pcyc}	Figure 5.35
		Both-edge setting		2.5	—		
	Timer clock pulse width	Single-edge setting	t_{TCKWH}, t_{TCKWL}	1.5	—	t_{Pcyc}	Figure 5.36
		Both-edge setting		2.5	—		
		Phase counting mode		2.5	—		
POE	POE# input pulse width		t_{POEW}	1.5	—	t_{Pcyc}	Figure 5.37
8-bit timer	Timer clock pulse width	Single-edge setting	t_{TMCWH}, t_{TMCWL}	1.5	—	t_{Pcyc}	Figure 5.38
		Both-edge setting		2.5	—		
SCI	Input clock cycle	Asynchronous	t_{Scyc}	4	—	t_{Pcyc}	Figure 5.39
		Clock synchronous		6	—		
	Input clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
	Input clock rise time		t_{SCKr}	—	20	ns	
	Input clock fall time		t_{SCKf}	—	20	ns	
	Output clock cycle	Asynchronous	t_{Scyc}	16	—	t_{Pcyc}	
		Clock synchronous		4	—		
	Output clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
	Output clock rise time		t_{SCKr}	—	20	ns	
	Output clock fall time		t_{SCKf}	—	20	ns	
	Transmit data delay time	Clock synchronous	t_{TXD}	—	40	ns	Figure 5.40
	Receive data setup time	Clock synchronous	t_{RXS}	40	—	ns	
	Receive data hold time	Clock synchronous	t_{RXH}	40	—	ns	
A/D converter	10-bit A/D converter trigger input pulse width		t_{TRGW}	1.5	—	t_{Pcyc}	Figure 5.41
	12-bit A/D converter trigger input pulse width			1.5	—		

Note 1. t_{Pcyc}: PCLK cycle

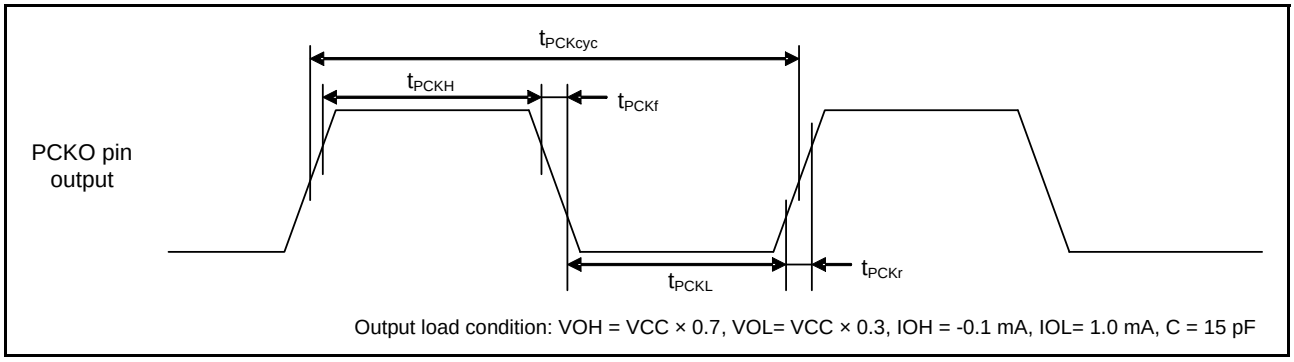


Figure 5.60 PDC Output Clock Characteristic

5.5 A/D Conversion Characteristics

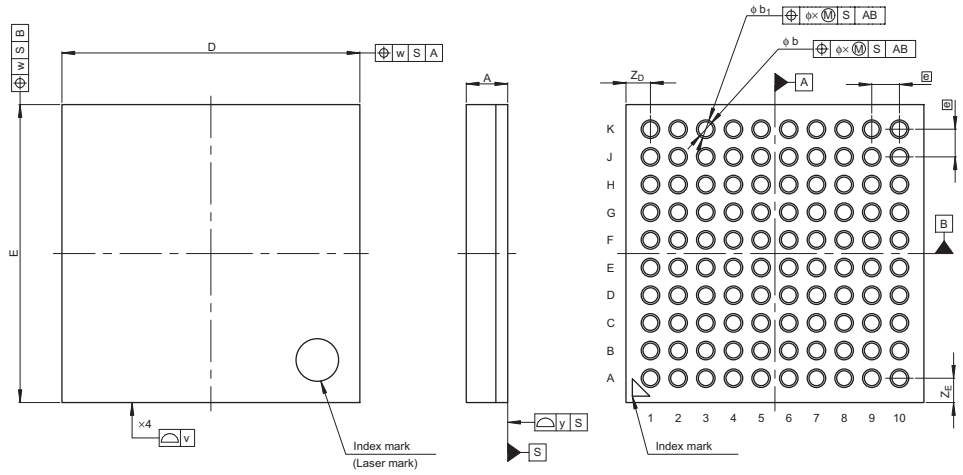
Table 5.28 10-Bit A/D Conversion Characteristics

Conditions: VCC = AVCC0 = VREFH = VCC_USB = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0
VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V
PCLK = 8 to 50 MHz
$T_a = T_{opr}$

Item			Min.	Typ.	Max.	Unit	Test Conditions
Resolution			—	—	10	Bit	
Conversion time*1 (Operation at PCLK = 50 MHz)	With 0.1-µF external capacitor	When the capacitor is charged enough*2	3.0 (2.5)*3	—	—	µs	Sampling in 125 states
	Without 0.1-µF external capacitor	Permissible signal source impedance (max.) = 1.0 kΩ, VCC ≥ 3.0 V	1.5 (1.0)*3	—	—		Sampling in 50 states
		Permissible signal source impedance (max.) = 1.0 kΩ, VCC ≥ 2.7 V	3.5 (3.0)*3	—	—		Sampling in 150 states
		Permissible signal source impedance (max.) = 5.0 kΩ, VCC ≥ 3.0 V	2.0 (1.5)*3	—	—		Sampling in 75 states
		Permissible signal source impedance (max.) = 5.0 kΩ, VCC ≥ 2.7 V	4.0 (3.5)*3	—	—		Sampling in 175 states
Analog input capacitance			—	—	6.0	pF	
Offset error			—	±1.5	±3.0	LSB	
Full-scale error			—	±1.5	±3.0	LSB	
Quantization error			—	±0.5	—	LSB	
Absolute accuracy			—	±1.5	±3.0	LSB	
DNL differential nonlinearity error			—	±0.5	±1.0	LSB	
INL integral nonlinearity error			—	±1.5	±3.0	LSB	

Note: The above specification values apply when there is no access to the external bus during A/D conversion. If access proceeds during A/D conversion, values may not fall within the above ranges.
Note 1. The conversion time includes the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.
Note 2. The scanning is not supported.
Note 3. The value in parentheses indicates the sampling time.

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-TFLGA100-7x7-0.65	PTLG0100JA-A	100F0G	0.1g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	7.0	—
E	—	7.0	—
v	—	—	0.15
w	—	—	0.20
A	—	—	1.05
e	—	0.65	—
b	0.31	0.35	0.39
b_1	0.385	0.435	0.485
x	—	—	0.08
y	—	—	0.10
Z_D	—	0.575	—
Z_E	—	0.575	—

Figure F 100-pin TFLGA (PTLG0100JA-A)

Rev.	Date	Description	
		Page	Summary
1.60	Mar 13. 2013	Feature	
		1	Changed
		1. Overview	
		2 to 7	Table 1.1 Outline of Specifications: changed, note added
		8	Table1.2 Comparison of Functions for Different Packages in the RX63N/RX631 Group, changed
		9 to 15	Table 1.3 List of Products, changed
		16	Figure 1.1 How to Read the Product Part No., changed
		17	Figure 1.2 Block Diagram, changed
		24 to 32	Figure 1.3 to Figure 1.11 Pin Assignment: note, added
		53 to 57	Table 1.9 List of Pins and Pin Functions (100-Pin TFLGA), added
		62 to 64	Table 1.11 List of Pins and Pin Functions (64-Pin LQFP), added
		65, 66	Table 1.12 List of Pins and Pin Functions (48-Pin LQFP), added
		3. Address Space	
		71	Figure 3.1 Memory Map in Each Operating Mode, changed
		4. I/O Registers	
		75 to 120	Table 4.1 List of I/O Registers (Address Order), changed
		5. Electrical Characteristics	
		All	Characteristics and timing conditions in the tables, changed
		124, 125	Table 5.4 DC Characteristics (3), changed
		126	Table 5.5 DC Characteristics (4), changed
		127	5.3 AC Characteristics, changed
		130, 131	Table 5.11, Clock Timing (Except for Sub-Clock Related): Condition and the table, changed, note, added
		132	Table 5.12 Clock Timing (Sub-Clock Related): Condition and the table, changed, note, added
		176	Table 5.33 Battery Backup Function Characteristics: Condition, changed
		Appendix 1.Package Dimensions	
		189	Figure H 64-pin LQFP (PLQP0064KB-A), added
		190	Figure I 48-pin LQFP (PLQP0048KB-A), added
1.70	Oct 08. 2013	Features	
		1	changed
		1. Overview	
		2 to 7	Table 1.1 Outline of Specifications, General I/O ports, Packages, changed, Parallel data capture unit (PDC), added.
		8	Table 1.2 Comparison of Functions for Different Packages in the RX63N/RX631 Group, 64-pin LQFP, changed, 64-pin TFLGA, Parallel data capture unit (PDC), added.
		9 to 16	Table 1.3 List of Products, changed.
		17	Figure 1.1 How to Read the Product Part No., changed
		18	Figure 1.2 Block Diagram, changed
		19 to 24	Table 1.4 Pin Functions,changed, Parallel data capture unit (PDC), added
		32	Figure 1.10 Pin Assignment (64-Pin TFLGA), added
		35 to 40	Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA), changed
		41 to 45	Table 1.6 List of Pin and Pin Functions (176-Pin LQFP), changed
		46 to 50	Table 1.7 List of Pins and Pin Functions (145-Pin TFLGA), changed
		51 to 55	Table 1.8 List of Pins and Pin Functions (144-Pin LQFP), changed
		65 to 66	Table 1.11 List of Pins and Pin Functions (64-Pin TFLGA), added
		3. Address Space	
		76	Figure 3.1 Memory Map in Each Operating Mode, changed
		4. I/O Registers	
		79	(4) Restrictions in Relation to RMPA and String-Manipulation Instructions, added

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.