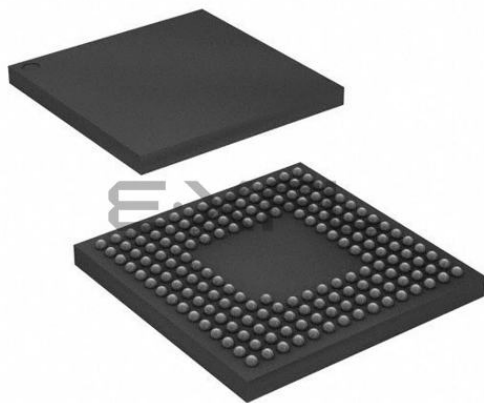




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Details

Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, LINbus, SCI, SPI, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	133
Program Memory Size	768KB (768K x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b, 21x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	177-TFLGA
Supplier Device Package	177-TFLGA (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f563naddlc-u0

	A	B	C	D	E	F	G	H	J	K	L	M	N	
13	PE3	PE4	VSS	PE6	P67	PA2	PA4	PA7	PB1	PB5	VSS	VCC	P74	13
12	PE1	PE2	P70	PE5	P65	PA1	VCC	PB0	PB2	PB6	P73	PC1	P75	12
11	P62	P61	PE0	VCC	P66	VSS	PA6	P71	PB4	PB7	PC2	PC0	PC3	11
10	VSS	VCC	P63	PE7	PA0	PA3	PA5	P72	PB3	P76	PC4	P77	P82	10
9	PD6	PD4	PD7	P64	RX63N Group RX631 Group PTLG0145KA-A (145-pin TFLGA) (Top perspective view)					P80	PC5	P81	PC7	9
8	PD2	PD0	PD3	P60						VCC	P83	PC6	VSS	8
7	P92	P91	PD1	PD5						P51	P52	P50	P55	7
6	P90	P47	VSS	P93						P53	P56	VSS_ USB	USB0_ DP	6
5	P45	P43	P46	VCC	P44					P54	P13	VCC_ USB	USB0_ DM	5
4	P42	VREFL0	P41	P01	EMLE	VBATT	BSCANP	P35	P30	P15	P24	P12	P14	4
3	P40	P05	VREFH0	P03	PJ5	PJ3	MD/ FINED	VSS	P32	P31	P16	P86	P87	3
2	P07	AVCC0	P02	PF5	VCL	XCOUT	RES#	VCC	P33	P26	P23	P17	P20	2
1	AVSS0	VREFH	VREFL	P00	VSS	XCIN	XTAL	EXTAL	P34	P27	P25	P22	P21	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	

Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.7, List of Pins and Pin Functions (145-Pin TFLGA).

Figure 1.6 Pin Assignment (145-Pin TFLGA)

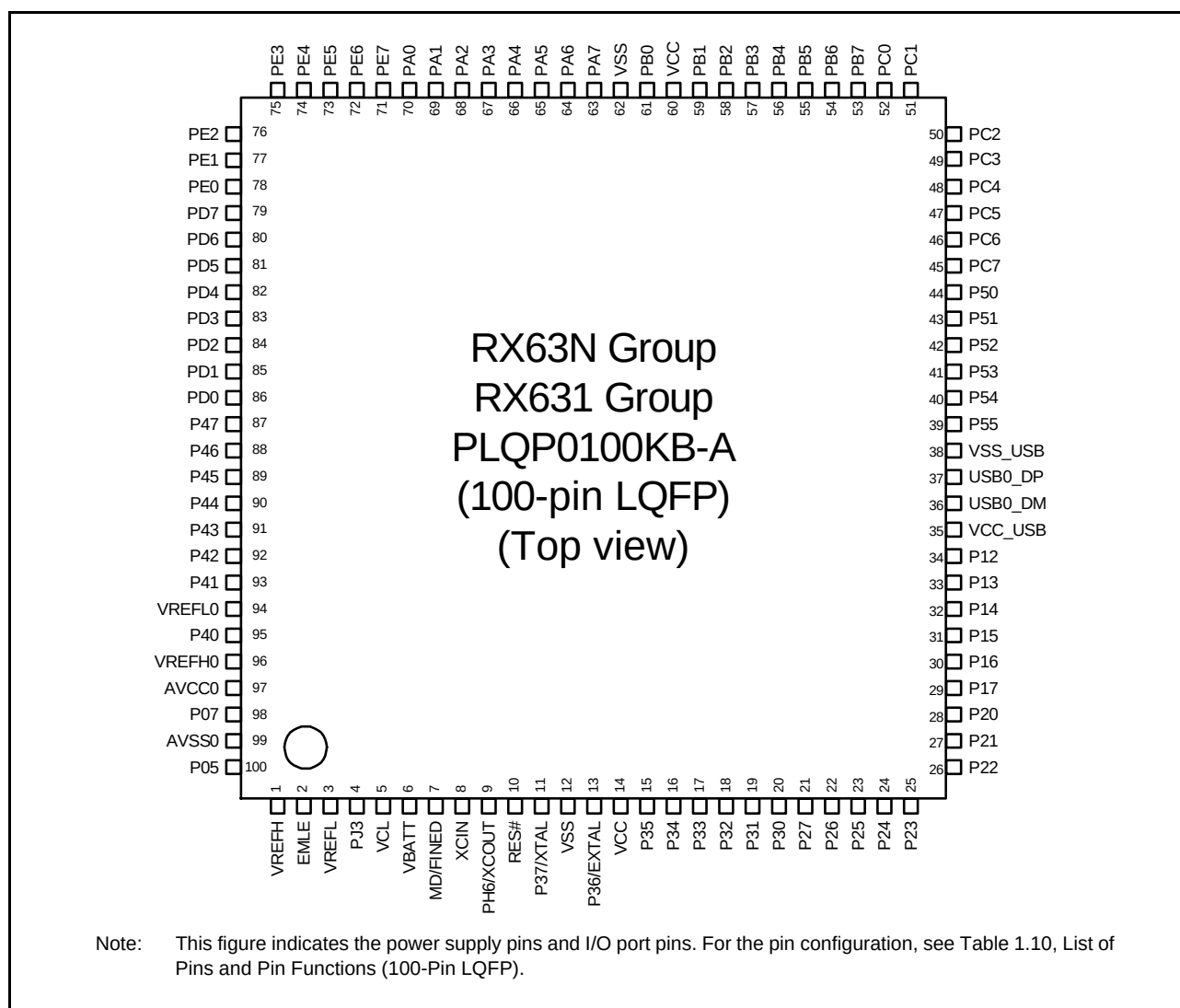
**Figure 1.9 Pin Assignment (100-Pin LQFP)**

Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (4/5)

Pin Number 177-Pin TFLGA 176-Pin LFBGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SCIC, SCID, RSPI, RIIC, CAN, IEB, USB, and PDC)	Interrupt	S12AD, AD, DA
M2		P26	CS6#	MTIOC2A/TMO1/PO6	TXD1/CTS3#/RTS3#/ SMOSI1/SS3#/SSDA1/ MOSIB		
M3		P24	CS4#/EDREQ1	MTIOC4A/MTCLKA/ TIOCB4/TMRI1/PO4	SCK3/USB0_VBUSEN/ PIXCLK		
M4		P86		TIOCA0	PIXD1		
M5		P13		MTIOC0B/TIOCA5/TMO3/ PO13	TXD2/SMOSI2/SSDA2/ SDA0[FM+]	IRQ3	ADTRG#
M6		P56	WR2#/BC2#/ EDACK1	MTIOC3C/TIOCA1			
M7		P54	ALE/EDACK0	MTIOC4B/TMCI1	ET_LINKSTA/CTS2#/ RTS2#/SS2#/CTX1		
M8		P53*2	BCLK				
M9		P50	WR0#/WR#		TXD2/SMOSI2/SSDA2/ SSLB1		
M10		PC5	A21/CS2#/ WAIT#	MTIOC3B/MTCLKD/ TIOCD6/TCLKF/TMRI2/ PO29	ET_ETXD2/SCK8/ RSPCKA		
M11		P81	EDACK0	MTIOC3D/PO27	ET_ETXD0/RMII_TXD0/ RXD10/SMISO10/SSCL10		
M12		P77	CS7#	PO23	ET_RX_ER/RMII_RX_ER/ TXD11/SMOSI11/SSDA11		
M13		PB7	A15	MTIOC3B/TIOCB5/PO31	ET_CRS/RMII_CRS_DV/ TXD9/SMOSI9/SSDA9		
M14		PB5	A13	MTIOC2A/MTIOC1B/ TIOCB4/TMRI1/PO29/ POE1#	ET_ETXD0/RMII_TXD0/ SCK9		
M15		PB4	A12	TIOCA4/PO28	ET_TX_EN/ RMII_TXD_EN/CTS9#/ RTS9#/SS9#		
N1	VCC						
N2		P23	EDACK0	MTIOC3D/MTCLKD/ TIOCD3/PO3	TXD3/CTS0#/RTS0#/ SMOSI3/SS0#/SSDA3/ USB0_DPUPE/PIXD7		
N3		P22	EDREQ0	MTIOC3B/MTCLKC/ TIOCC3/TMO0/PO2	SCK0/USB0_DRPD/ PIXD6		
N4		P15		MTIOC0B/MTCLKB/ TIOCB2/TCLKB/TMCI2/ PO13	RXD1/SCK3/SMISO1/ SSCL1/CRX1-DS/ USB1_DPUPE/PIXD0	IRQ5	
N5		P12		MTIC5U/TMCI1	RXD2/SMISO2/SSCL2/ SCL0[FM+]	IRQ2	
N6		P57	WAIT#/WR3#/ BC3#/EDREQ1				
N7		P55	WAIT#/ EDREQ0	MTIOC4D/TMO3	ET_EXOUT/CRX1	IRQ10	
N8	VCC_USB						
N9		P51	WR1#/BC1#/ WAIT#		SCK2/SSLB2		
N10		PC7	A23/CS0#	MTIOC3A/MTCLKB/ TIOCB6/TMO2/PO31	ET_COL/TXD8/SMOSI8/ SSDA8/MISOA	IRQ14	
N11		P82	EDREQ1	MTIOC4A/PO28	ET_ETXD1/RMII_TXD1/ TXD10/SMOSI10/SSDA10		
N12		PC3	A19	MTIOC4D/TCLKB/PO24	ET_TX_ER/TXD5/ SMOSI5/SSDA5/IETXD		
N13		PC0	A16	MTIOC3C/TCLKC/PO17	ET_ERXD3/CTS5#/ RTS5#/SS5#/SSLA1/ SCL3	IRQ14	
N14		P73	CS3#	PO16	ET_WOL		
N15	VSS						

Table 4.1 List of I/O Registers (Address Order) (7/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 7096h	ICU	Interrupt request register 150	IR150	8	8	2	ICLK	ICUb
0008 7097h	ICU	Interrupt request register 151	IR151	8	8	2	ICLK	
0008 7098h	ICU	Interrupt request register 152	IR152	8	8	2	ICLK	
0008 7099h	ICU	Interrupt request register 153	IR153	8	8	2	ICLK	
0008 709Ah	ICU	Interrupt request register 154	IR154	8	8	2	ICLK	
0008 709Bh	ICU	Interrupt request register 155	IR155	8	8	2	ICLK	
0008 709Ch	ICU	Interrupt request register 156	IR156	8	8	2	ICLK	
0008 709Dh	ICU	Interrupt request register 157	IR157	8	8	2	ICLK	
0008 709Eh	ICU	Interrupt request register 158	IR158	8	8	2	ICLK	
0008 709Fh	ICU	Interrupt request register 159	IR159	8	8	2	ICLK	
0008 70A0h	ICU	Interrupt request register 160	IR160	8	8	2	ICLK	
0008 70A1h	ICU	Interrupt request register 161	IR161	8	8	2	ICLK	
0008 70A2h	ICU	Interrupt request register 162	IR162	8	8	2	ICLK	
0008 70A3h	ICU	Interrupt request register 163	IR163	8	8	2	ICLK	
0008 70A4h	ICU	Interrupt request register 164	IR164	8	8	2	ICLK	
0008 70A5h	ICU	Interrupt request register 165	IR165	8	8	2	ICLK	
0008 70A6h	ICU	Interrupt request register 166	IR166	8	8	2	ICLK	
0008 70A7h	ICU	Interrupt request register 167	IR167	8	8	2	ICLK	
0008 70AAh	ICU	Interrupt request register 170	IR170	8	8	2	ICLK	
0008 70ABh	ICU	Interrupt request register 171	IR171	8	8	2	ICLK	
0008 70ACh	ICU	Interrupt request register 172	IR172	8	8	2	ICLK	
0008 70ADh	ICU	Interrupt request register 173	IR173	8	8	2	ICLK	
0008 70AEh	ICU	Interrupt request register 174	IR174	8	8	2	ICLK	
0008 70AFh	ICU	Interrupt request register 175	IR175	8	8	2	ICLK	
0008 70B0h	ICU	Interrupt request register 176	IR176	8	8	2	ICLK	
0008 70B1h	ICU	Interrupt request register 177	IR177	8	8	2	ICLK	
0008 70B2h	ICU	Interrupt request register 178	IR178	8	8	2	ICLK	
0008 70B3h	ICU	Interrupt request register 179	IR179	8	8	2	ICLK	
0008 70B4h	ICU	Interrupt request register 180	IR180	8	8	2	ICLK	
0008 70B5h	ICU	Interrupt request register 181	IR181	8	8	2	ICLK	
0008 70B6h	ICU	Interrupt request register 182	IR182	8	8	2	ICLK	
0008 70B7h	ICU	Interrupt request register 183	IR183	8	8	2	ICLK	
0008 70B8h	ICU	Interrupt request register 184	IR184	8	8	2	ICLK	
0008 70B9h	ICU	Interrupt request register 185	IR185	8	8	2	ICLK	
0008 70BAh	ICU	Interrupt request register 186	IR186	8	8	2	ICLK	
0008 70BBh	ICU	Interrupt request register 187	IR187	8	8	2	ICLK	
0008 70BCh	ICU	Interrupt request register 188	IR188	8	8	2	ICLK	
0008 70BDh	ICU	Interrupt request register 189	IR189	8	8	2	ICLK	
0008 70BEh	ICU	Interrupt request register 190	IR190	8	8	2	ICLK	
0008 70BFh	ICU	Interrupt request register 191	IR191	8	8	2	ICLK	
0008 70C0h	ICU	Interrupt request register 192	IR192	8	8	2	ICLK	
0008 70C1h	ICU	Interrupt request register 193	IR193	8	8	2	ICLK	
0008 70C2h	ICU	Interrupt request register 194	IR194	8	8	2	ICLK	
0008 70C3h	ICU	Interrupt request register 195	IR195	8	8	2	ICLK	
0008 70C4h	ICU	Interrupt request register 196	IR196	8	8	2	ICLK	
0008 70C5h	ICU	Interrupt request register 197	IR197	8	8	2	ICLK	
0008 70C6h	ICU	Interrupt request register 198	IR198	8	8	2	ICLK	
0008 70C7h	ICU	Interrupt request register 199	IR199	8	8	2	ICLK	
0008 70C8h	ICU	Interrupt request register 200	IR200	8	8	2	ICLK	
0008 70C9h	ICU	Interrupt request register 201	IR201	8	8	2	ICLK	
0008 70CAh	ICU	Interrupt request register 202	IR202	8	8	2	ICLK	

Table 4.1 List of I/O Registers (Address Order) (17/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 81A8h	TPU8	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	TPUa
0008 81AAh	TPU8	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	
0008 81B0h	TPU9	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK	
0008 81B1h	TPU9	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK	
0008 81B2h	TPU9	Timer I/O control register H	TIORH	8	8	2, 3 PCLKB	2 ICLK	
0008 81B3h	TPU9	Timer I/O control register L	TIORL	8	8	2, 3 PCLKB	2 ICLK	
0008 81B4h	TPU9	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK	
0008 81B5h	TPU9	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK	
0008 81B6h	TPU9	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	
0008 81B8h	TPU9	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	
0008 81BAh	TPU9	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	
0008 81BCh	TPU9	Timer general register C	TGRC	16	16	2, 3 PCLKB	2 ICLK	
0008 81BEh	TPU9	Timer general register D	TGRD	16	16	2, 3 PCLKB	2 ICLK	
0008 81C0h	TPU10	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK	
0008 81C1h	TPU10	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK	
0008 81C2h	TPU10	Timer I/O control register	TIOR	8	8	2, 3 PCLKB	2 ICLK	
0008 81C4h	TPU10	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK	
0008 81C5h	TPU10	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK	
0008 81C6h	TPU10	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	
0008 81C8h	TPU10	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	
0008 81CAh	TPU10	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	
0008 81D0h	TPU11	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK	
0008 81D1h	TPU11	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK	
0008 81D2h	TPU11	Timer I/O control register	TIOR	8	8	2, 3 PCLKB	2 ICLK	
0008 81D4h	TPU11	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK	
0008 81D5h	TPU11	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK	
0008 81D6h	TPU11	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	
0008 81D8h	TPU11	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	
0008 81DAh	TPU11	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	
0008 81E6h	PPG0	PPG output control register	PCR	8	8	2, 3 PCLKB	2 ICLK	PPG
0008 81E7h	PPG0	PPG output mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 81E8h	PPG0	Next data enable register H	NDERH	8	8	2, 3 PCLKB	2 ICLK	
0008 81E9h	PPG0	Next data enable register L	NDERL	8	8	2, 3 PCLKB	2 ICLK	
0008 81EAh	PPG0	Output data register H	PODRH	8	8	2, 3 PCLKB	2 ICLK	
0008 81EBh	PPG0	Output data register L	PODRL	8	8	2, 3 PCLKB	2 ICLK	
0008 81ECh ^{*1}	PPG0	Next data register H	NDRH	8	8	2, 3 PCLKB	2 ICLK	
0008 81EDh ^{*2}	PPG0	Next data register L	NDRL	8	8	2, 3 PCLKB	2 ICLK	
0008 81EEh ^{*1}	PPG0	Next data register H	NDRH2	8	8	2, 3 PCLKB	2 ICLK	
0008 81EFh ^{*2}	PPG0	Next data register L	NDRL2	8	8	2, 3 PCLKB	2 ICLK	
0008 81F0h	PPG1	PPG trigger select register	PTRSLR	8	8	2, 3 PCLKB	2 ICLK	
0008 81F6h	PPG1	PPG output control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 81F7h	PPG1	PPG output mode register	PMR	8	8	2, 3 PCLKB	2 ICLK	
0008 81F8h	PPG1	Next data enable register H	NDERH	8	8	2, 3 PCLKB	2 ICLK	
0008 81F9h	PPG1	Next data enable register L	NDERL	8	8	2, 3 PCLKB	2 ICLK	
0008 81FAh	PPG1	Output data register H	PODRH	8	8	2, 3 PCLKB	2 ICLK	
0008 81FBh	PPG1	Output data register L	PODRL	8	8	2, 3 PCLKB	2 ICLK	
0008 81FCh ^{*3}	PPG1	Next data register H	NDRH	8	8	2, 3 PCLKB	2 ICLK	PPG
0008 81FDh ^{*4}	PPG1	Next data register L	NDRL	8	8	2, 3 PCLKB	2 ICLK	
0008 81FEh ^{*3}	PPG1	Next data register H	NDRH2	8	8	2, 3 PCLKB	2 ICLK	
0008 81FFh ^{*4}	PPG1	Next data register L	NDRL2	8	8	2, 3 PCLKB	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (22/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 862Ah	MTU4	Timer general register D	TGRD	16	16	2, 3 PCLKB	2 ICLK	MTU2a
0008 862Ch	MTU3	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK	
0008 862Dh	MTU4	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK	
0008 8630h	MTU	Timer interrupt skipping set register	TITCR	8	8	2, 3 PCLKB	2 ICLK	
0008 8631h	MTU	Timer interrupt skipping counter	TITCNT	8	8	2, 3 PCLKB	2 ICLK	
0008 8632h	MTU	Timer buffer transfer set register	TBTER	8	8	2, 3 PCLKB	2 ICLK	
0008 8634h	MTU	Timer dead time enable register	TDER	8	8	2, 3 PCLKB	2 ICLK	
0008 8636h	MTU	Timer output level buffer register	TOLBR	8	8	2, 3 PCLKB	2 ICLK	
0008 8638h	MTU3	Timer buffer operation transfer mode register	TBTM	8	8	2, 3 PCLKB	2 ICLK	
0008 8639h	MTU4	Timer buffer operation transfer mode register	TBTM	8	8	2, 3 PCLKB	2 ICLK	
0008 8640h	MTU4	Timer A/D converter start request control register	TADCR	16	16	2, 3 PCLKB	2 ICLK	
0008 8644h	MTU4	Timer A/D converter start request cycle set register A	TADCORA	16	16	2, 3 PCLKB	2 ICLK	
0008 8646h	MTU4	Timer A/D converter start request cycle set register B	TADCORB	16	16	2, 3 PCLKB	2 ICLK	
0008 8648h	MTU4	Timer A/D converter start request cycle set buffer register A	TADCOBRA	16	16	2, 3 PCLKB	2 ICLK	
0008 864Ah	MTU4	Timer A/D converter start request cycle set buffer register B	TADCOBRB	16	16	2, 3 PCLKB	2 ICLK	
0008 8660h	MTU	Timer waveform control register	TWCR	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 8680h	MTU	Timer start register	TSTR	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 8681h	MTU	Timer synchronous register	TSYR	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 8684h	MTU	Timer read/write enable register	TRWER	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 8690h	MTU0	Noise filter control register	NFCR	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 8691h	MTU1	Noise filter control register	NFCR	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 8692h	MTU2	Noise filter control register	NFCR	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 8693h	MTU3	Noise filter control register	NFCR	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 8694h	MTU4	Noise filter control register	NFCR	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 8695h	MTU5	Noise filter control register	NFCR	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 8700h	MTU0	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK	
0008 8701h	MTU0	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK	
0008 8702h	MTU0	Timer I/O control register H	TIORH	8	8	2, 3 PCLKB	2 ICLK	
0008 8703h	MTU0	Timer I/O control register L	TIORL	8	8	2, 3 PCLKB	2 ICLK	
0008 8704h	MTU0	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK	
0008 8705h	MTU0	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK	
0008 8706h	MTU0	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	
0008 8708h	MTU0	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	
0008 870Ah	MTU0	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	
0008 870Ch	MTU0	Timer general register C	TGRC	16	16	2, 3 PCLKB	2 ICLK	
0008 870Eh	MTU0	Timer general register D	TGRD	16	16	2, 3 PCLKB	2 ICLK	
0008 8720h	MTU0	Timer general register E	TGRE	16	16	2, 3 PCLKB	2 ICLK	
0008 8722h	MTU0	Timer general register F	TGRF	16	16	2, 3 PCLKB	2 ICLK	
0008 8724h	MTU0	Timer interrupt enable register2	TIER2	8	8	2, 3 PCLKB	2 ICLK	
0008 8726h	MTU0	Timer buffer operation transfer mode register	TBTM	8	8	2, 3 PCLKB	2 ICLK	
0008 8780h	MTU1	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK	
0008 8781h	MTU1	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK	
0008 8782h	MTU1	Timer I/O control register	TIOR	8	8	2, 3 PCLKB	2 ICLK	
0008 8784h	MTU1	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK	
0008 8785h	MTU1	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK	
0008 8786h	MTU1	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	
0008 8788h	MTU1	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	
0008 878Ah	MTU1	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	
0008 8790h	MTU1	Timer input capture control register	TICCR	8	8	2, 3 PCLKB	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (26/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 A0A6h	SCI5	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK	SCIc, SCId
0008 A0A7h	SCI5	Serial extended mode register	SEMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0A8h	SCI5	Noise filter setting register	SNFR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0A9h	SCI5	I ² C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK	
0008 A0AAh	SCI5	I ² C mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK	
0008 A0ABh	SCI5	I ² C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK	
0008 A0ACh	SCI5	I ² C status register	SISR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0ADh	SCI5	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0C0h	SCI6	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0C1h	SCI6	Bit rate register	BRR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0C2h	SCI6	Serial control register	SCR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0C3h	SCI6	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0C4h	SCI6	Serial status register	SSR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0C5h	SCI6	Receive data register	RDR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0C6h	SCI6	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0C7h	SCI6	Serial extended mode register	SEMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0C8h	SCI6	Noise filter setting register	SNFR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0C9h	SCI6	I ² C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK	
0008 A0CAh	SCI6	I ² C mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK	
0008 A0CBh	SCI6	I ² C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK	
0008 A0CCh	SCI6	I ² C status register	SISR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0CDh	SCI6	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0E0h	SCI7	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0E1h	SCI7	Bit rate register	BRR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0E2h	SCI7	Serial control register	SCR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0E3h	SCI7	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0E4h	SCI7	Serial status register	SSR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0E5h	SCI7	Receive data register	RDR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0E6h	SCI7	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0E7h	SCI7	Serial extended mode register	SEMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0E8h	SCI7	Noise filter setting register	SNFR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0E9h	SCI7	I ² C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK	
0008 A0EAh	SCI7	I ² C mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK	
0008 A0EBh	SCI7	I ² C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK	
0008 A0ECh	SCI7	I ² C status register	SISR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0EDh	SCI7	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A100h	SCI8	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A101h	SCI8	Bit rate register	BRR	8	8	2, 3 PCLKB	2 ICLK	
0008 A102h	SCI8	Serial control register	SCR	8	8	2, 3 PCLKB	2 ICLK	
0008 A103h	SCI8	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK	
0008 A104h	SCI8	Serial status register	SSR	8	8	2, 3 PCLKB	2 ICLK	
0008 A105h	SCI8	Receive data register	RDR	8	8	2, 3 PCLKB	2 ICLK	
0008 A106h	SCI8	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A107h	SCI8	Serial extended mode register	SEMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A108h	SCI8	Noise filter setting register	SNFR	8	8	2, 3 PCLKB	2 ICLK	
0008 A109h	SCI8	I ² C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK	
0008 A10Ah	SCI8	I ² C mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK	
0008 A10Bh	SCI8	I ² C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK	
0008 A10Ch	SCI8	I ² C status register	SISR	8	8	2, 3 PCLKB	2 ICLK	
0008 A10Dh	SCI8	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A120h	SCI9	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (31/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 C095h	PORTA	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C096h	PORTB	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C097h	PORTB	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C098h	PORTC	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C099h	PORTC	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C09Ah	PORTD	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C09Bh	PORTD	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C09Ch	PORTE	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C09Dh	PORTE	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C09Eh	PORTF	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C09Fh	PORTF	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C0A0h	PORTG	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C0A1h	PORTG	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C0A4h	PORTJ	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C0A5h	PORTJ	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C0C0h	PORT0	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0C1h	PORT1	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0C2h	PORT2	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0C3h	PORT3	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0C4h	PORT4	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0C5h	PORT5	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0C6h	PORT6	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0C7h	PORT7	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0C8h	PORT8	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0C9h	PORT9	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0CAh	PORTA	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0CBh	PORTB	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0CCh	PORTC	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0CDh	PORTD	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0CEh	PORTE	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0CFh	PORTF	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0D0h	PORTG	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0D2h	PORTJ	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0E0h	PORT0	Drive ability control register	DSCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0E2h	PORT2	Drive ability control register	DSCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0E5h	PORT5	Drive ability control register	DSCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0E9h	PORT9	Drive ability control register	DSCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0EAh	PORTA	Drive ability control register	DSCR	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C0EBh	PORTB	Drive ability control register	DSCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0ECh	PORTC	Drive ability control register	DSCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0EDh	PORTD	Drive ability control register	DSCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0EEh	PORTE	Drive ability control register	DSCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0F0h	PORTG	Drive ability control register	DSCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C100h	MPC	CS output enable register	PFCSE	8	8	2, 3 PCLKB	2 ICLK	
0008 C102h	MPC	CS output pin select register 0	PFCSS0	8	8	2, 3 PCLKB	2 ICLK	
0008 C103h	MPC	CS output pin select register 1	PFCSS1	8	8	2, 3 PCLKB	2 ICLK	
0008 C104h	MPC	Address output enable register 0	PFAOE0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C105h	MPC	Address output enable register 1	PFAOE1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C106h	MPC	External bus control register 0	PFBCR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C107h	MPC	External bus control register 1	PFBCR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C10Eh	MPC	Ethernet control register 1	PFENET	8	8	2, 3 PCLKB	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (34/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 C1B1h	MPC	PE1 pin function control register	PE1PFS	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C1B2h	MPC	PE2 pin function control register	PE2PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1B3h	MPC	PE3 pin function control register	PE3PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1B4h	MPC	PE4 pin function control register	PE4PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1B5h	MPC	PE5 pin function control register	PE5PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1B6h	MPC	PE6 pin function control register	PE6PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1B7h	MPC	PE7 pin function control register	PE7PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1B8h	MPC	PF0 pin function control register	PF0PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1B9h	MPC	PF1 pin function control register	PF1PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1BAh	MPC	PF2 pin function control register	PF2PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1BDh	MPC	PF5 pin function control register	PF5PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C1D3h	MPC	PJ3 pin function control register	PJ3PFS	8	8	2, 3 PCLKB	2 ICLK	
0008 C280h	SYSTEM	Deep standby control register	DPSBYCR	8	8	4, 5 PCLKB	2, 3 ICLK	Low Power Consumption
0008 C282h	SYSTEM	Deep standby interrupt enable register 0	DPSIER0	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C283h	SYSTEM	Deep standby interrupt enable register 1	DPSIER1	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C284h	SYSTEM	Deep standby interrupt enable register 2	DPSIER2	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C285h	SYSTEM	Deep standby interrupt enable register 3	DPSIER3	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C286h	SYSTEM	Deep standby interrupt flag register 0	DPSIFR0	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C287h	SYSTEM	Deep standby interrupt flag register 1	DPSIFR1	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C288h	SYSTEM	Deep standby interrupt flag register 2	DPSIFR2	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C289h	SYSTEM	Deep standby interrupt flag register 3	DPSIFR3	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C28Ah	SYSTEM	Deep standby interrupt edge register 0	DPSIEGR0	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C28Bh	SYSTEM	Deep standby interrupt edge register 1	DPSIEGR1	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C28Ch	SYSTEM	Deep standby interrupt edge register 2	DPSIEGR2	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C28Dh	SYSTEM	Deep standby interrupt edge register 3	DPSIEGR3	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C290h	SYSTEM	Reset status register 0	RSTSR0	8	8	4, 5 PCLKB	2, 3 ICLK	Resets
0008 C291h	SYSTEM	Reset status register 1	RSTSR1	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C293h	SYSTEM	Main clock oscillator forced oscillation control register	MOFCR	8	8	4, 5 PCLKB	2, 3 ICLK	Clock Generation Circuit
0008 C294h	SYSTEM	High-speed on-chip oscillator power supply control register	HOCOPCR	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C296h	FLASH	Flash write erase protection register	FWEPROR	8	8	4, 5 PCLKB	2, 3 ICLK	ROM
0008 C297h	SYSTEM	Voltage monitoring circuit control register	LVCMPCR	8	8	4, 5 PCLKB	2, 3 ICLK	LVDA
0008 C298h	SYSTEM	Voltage detection level select register	LVDLVL	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C29Ah	SYSTEM	Voltage monitoring 1 circuit control register 0	LVD1CR0	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C29Bh	SYSTEM	Voltage monitoring 2 circuit control register 0	LVD2CR0	8	8	4, 5 PCLKB	2, 3 ICLK	
0008 C2A0h to 0008 C2BFh	SYSTEM	Deep standby backup register 0 to 31	DPSBKR0 to 31	8	8	4, 5 PCLKB	2, 3 ICLK	Low Power Consumption
0008 C300h	ICU	Group 0 interrupt source register	GRP00	32	32	1 to 2PCLKB	2 ICLK	ICUb
0008 C304h	ICU	Group 1 interrupt source register	GRP01	32	32	1 to 2PCLKB	2 ICLK	
0008 C308h	ICU	Group 2 interrupt source register	GRP02	32	32	1 to 2PCLKB	2 ICLK	
0008 C30Ch	ICU	Group 3 interrupt source register	GRP03	32	32	1 to 2PCLKB	2 ICLK	
0008 C310h	ICU	Group 4 interrupt source register	GRP04	32	32	1 to 2PCLKB	2 ICLK	
0008 C314h	ICU	Group 5 interrupt source register	GRP05	32	32	1 to 2PCLKB	2 ICLK	
0008 C318h	ICU	Group 6 interrupt source register	GRP06	32	32	1 to 2PCLKB	2 ICLK	
0008 C330h	ICU	Group 12 interrupt source register	GRP12	32	32	1 to 2PCLKB	2 ICLK	
0008 C340h	ICU	Group 0 interrupt enable register	GEN00	32	32	1 to 2PCLKB	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (44/50)

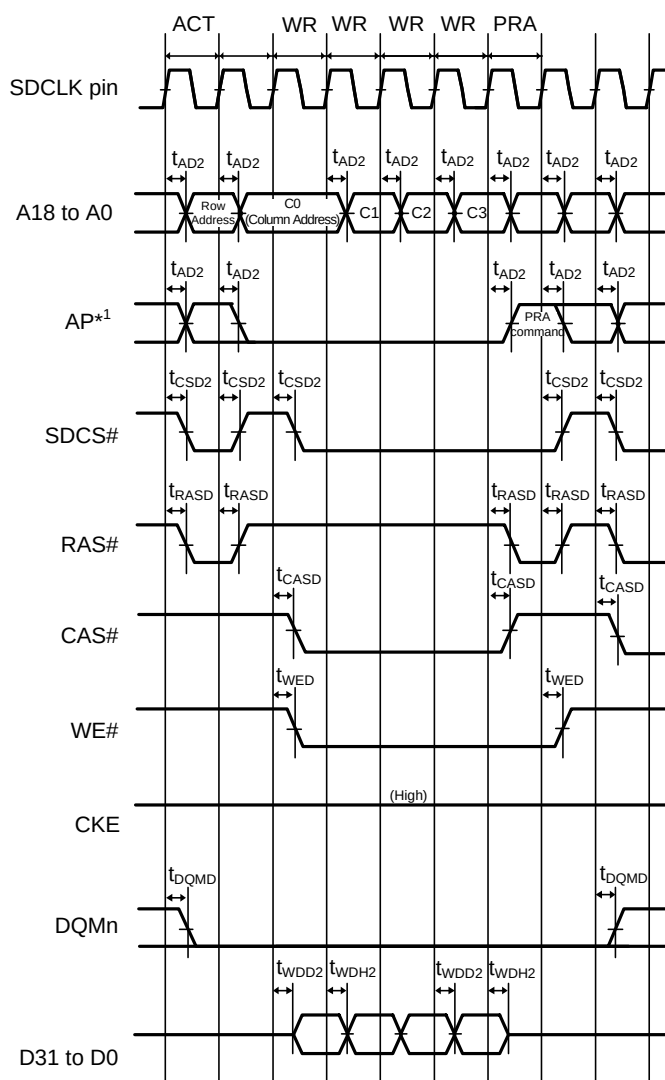
Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK $\geq$ PCLK	ICLK<PCLK	
000A 0230h	USB1	Interrupt enable register 0	INTENB0	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 0236h	USB1	BRDY interrupt enable register	BRDYENB	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 0238h	USB1	NRDY interrupt enable register	NRDYENB	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 023Ah	USB1	BEMP interrupt enable register	BEMPENB	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 023Ch	USB1	SOF output configuration register	SOFCFG	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 0240h	USB1	Interrupt status register 0	INTSTS0	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 0246h	USB1	BRDY interrupt status register	BRDYSTS	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 0248h	USB1	NRDY interrupt status register	NRDYSTS	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	USBa
000A 024Ah	USB1	BEMP interrupt status register	BEMPSTS	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 024Ch	USB1	Frame number register	FRMNUM	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	

5.3.5 Bus Timing

Table 5.16 Bus Timing (packages with 177 to 144 pins)

Conditions: $V_{CC} = AVCC0 = VREFH = VCC_USB = 2.7$ to 3.6 V, $VREFH0 = 2.7$ V to $AVCC0$,
 $VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0$ V,
 $ICLK = 8$ to 100 MHz, $BCLK$ pin = 8 to 50 MHz, $SDCLK$ pin = 8 to 50 MHz, $T_a = T_{opr}$
 Output load conditions: $V_{OH} = VCC \times 0.5$, $V_{OL} = VCC \times 0.5$, $I_{OH} = -1.0$ mA, $I_{OL} = 1.0$ mA, $C = 30$ pF
 High drive output is selected by the drive capacity control register.

Item	Symbol	Min.	Max.	Unit	Test Conditions
Address delay time	t_{AD}	—	15	ns	Figure 5.17 to Figure 5.22
Byte control delay time	t_{BCD}	—	15	ns	
CS# delay time	t_{CSD}	—	15	ns	
ALE delay time	t_{ALED}	—	20	ns	
RD# delay time	t_{RSD}	—	15	ns	
Read data setup time	t_{RDS}	15	—	ns	
Read data hold time	t_{RDH}	0	—	ns	
WR# delay time	t_{WRD}	—	15	ns	
Write data delay time	t_{WDD}	—	15	ns	
Write data hold time	t_{WDH}	0	—	ns	
WAIT# setup time	t_{WTS}	15	—	ns	Figure 5.23
WAIT# hold time	t_{WTH}	0	—	ns	
Address delay time 2 (SDRAM)	t_{AD2}	1	15	ns	Figure 5.24 to Figure 5.30
CS# delay time 2 (SDRAM)	t_{CSD2}	1	15	ns	
DQM delay time (SDRAM)	t_{DQMD}	1	15	ns	
CKE delay time (SDRAM)	t_{CKED}	1	15	ns	
Read data setup time 2 (SDRAM)	t_{RDS2}	12	—	ns	
Read data hold time 2 (SDRAM)	t_{RDH2}	0	—	ns	
Write data delay time 2 (SDRAM)	t_{WDD2}	—	15	ns	
Write data hold time 2 (SDRAM)	t_{WDH2}	1	—	ns	
WE# delay time (SDRAM)	t_{WED}	1	15	ns	
RAS# delay time (SDRAM)	t_{RASD}	1	15	ns	
CAS# delay time (SDRAM)	t_{CASD}	1	15	ns	



Note 1: Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

Figure 5.27 SDRAM Space Multiple Write Bus Timing

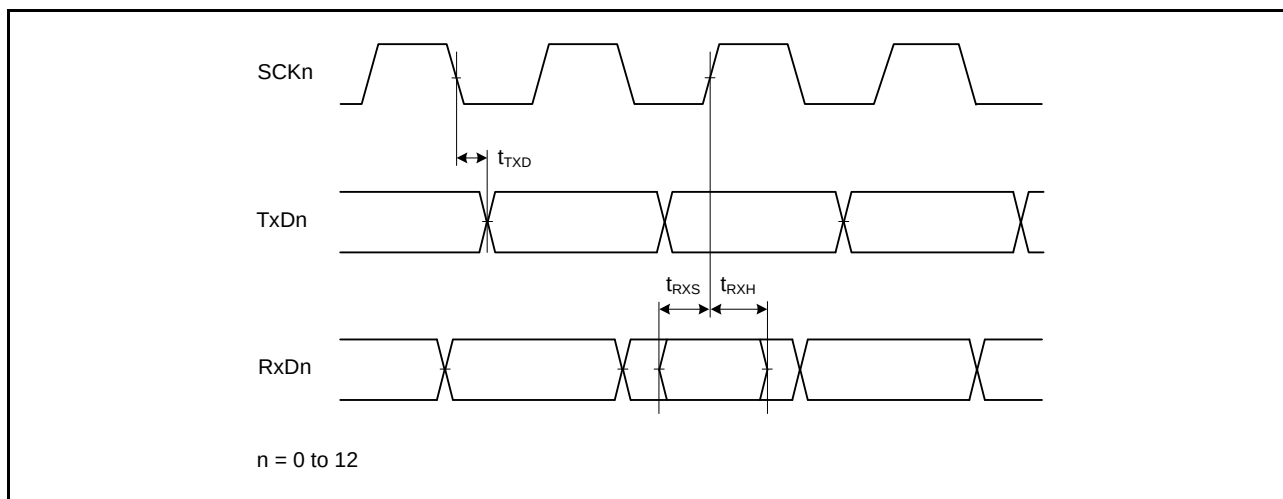


Figure 5.40 SCI Input/Output Timing: Clock Synchronous Mode

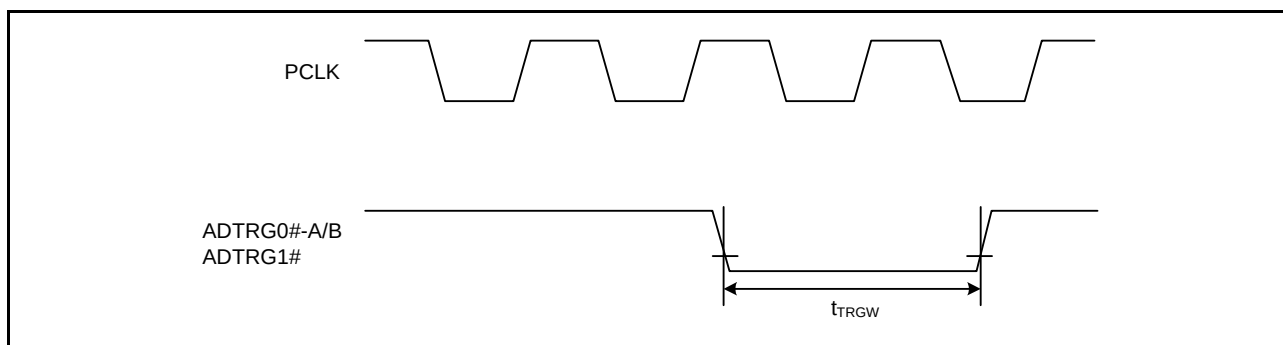


Figure 5.41 A/D Converter External Trigger Input Timing

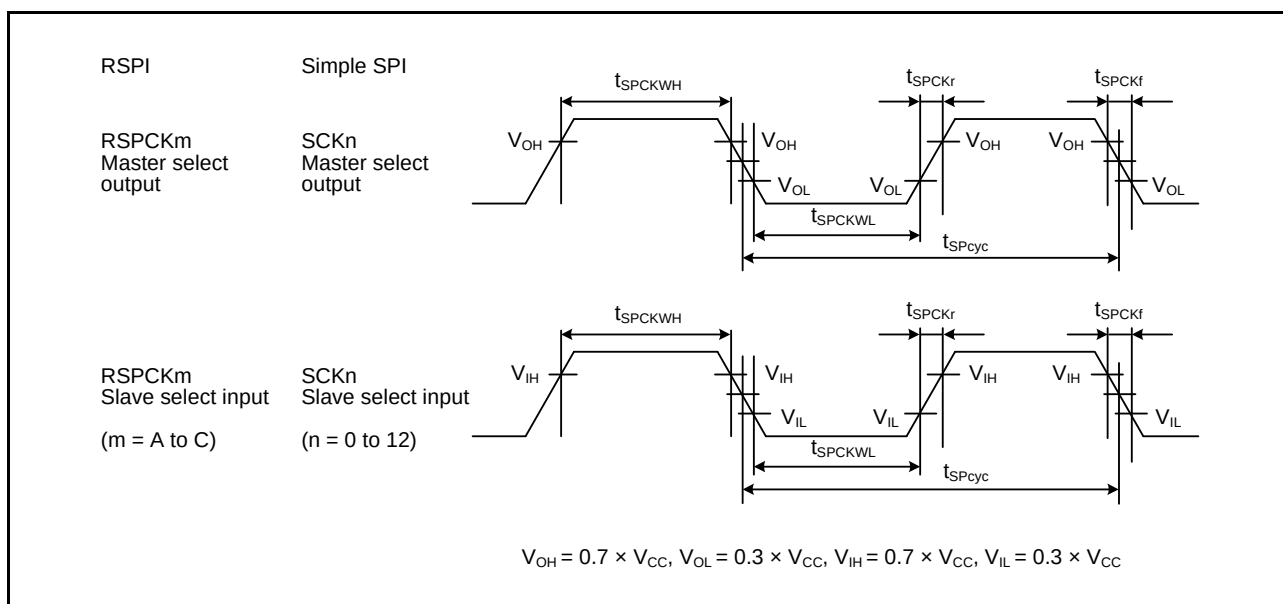


Figure 5.42 RSPI Clock Timing and Simple SPI Clock Timing

5.6 D/A Conversion Characteristics

Table 5.31 D/A Conversion Characteristics

Conditions: $VCC = AVCC0 = VREFH = VCC_USB = 2.7$ to 3.6 V, $VREFH0 = 2.7$ V to VCC
 $VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0$ V
 $T_a = T_{opr}$

Item	Min.	Typ.	Max.	Unit	Test Conditions
Resolution	10	10	10	Bit	
Conversion time	—	—	3.0	μs	20-pF capacitive load
Absolute accuracy	—	±2.0	±4.0	LSB	2-MΩ resistive load
	—	—	±3.0	LSB	4-MΩ resistive load
	—	—	±2.0	LSB	10-MΩ resistive load
RO output resistance	—	3.6	—	kΩ	

5.7 Temperature Sensor Characteristics

Table 5.32 Temperature Sensor Characteristics

Conditions: $VCC = AVCC0 = VREFH = VCC_USB = 2.7$ to 3.6 V, $VREFH0 = 2.7$ V to VCC
 $VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0$ V
 $T_a = T_{opr}$

Item	Min.	Typ.	Max.	Unit	Test Conditions
Relative accuracy	—	±1	—	°C	
Temperature slope	—	4.1	—	mV/°C	
Output voltage (@25°C)	—	1.26	—	V	
Temperature sensor start time	—	—	30	μs	
Sampling time	—	—	5	μs	

5.11 ROM (Flash Memory for Code Storage) Characteristics

Table 5.36 ROM (Flash Memory for Code Storage) Characteristics (1)

Conditions: VCC = AVCC0 = VREFH = VCC_USB = 2.7 to 3.6V, VREFH0 = 2.7V to AVCC0

VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0V

Temperature range for the programming/erasure operation: T_a = T_{opr}

Item	Symbol	min	typ	max	Unit	Condition
Reprogram/erase cycle*1	N _{PEC}	1000	—	—	Times	
Data hold time	t _{DRP}	30*2	—	—	Year	T _a = +85°C

Note 1. Definition of reprogram/erase cycle:

The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 1000), erasing can be performed n times for each block. For instance, when 256-byte programming is performed 16 times for different addresses in 4-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).

Note 2. The result obtained from the reliability test.

Table 5.37 ROM (Flash Memory for Code Storage) Characteristics (2)

Conditions: VCC = AVCC0 = VREFH = VCC_USB = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0

VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V

Temperature range for the programming/erasure operation: T_a = T_{opr}

Item		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 50 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time N _{PEC} ≤ 100 times	128 bytes	t _{P128}	—	2.8	28	—	1	10	ms
	4 Kbytes	t _{P4K}	—	63	140	—	23	50	ms
	16 Kbytes	t _{P16K}	—	252	560	—	90	200	ms
Programming time N _{PEC} > 100 times	128 bytes	t _{P128}	—	3.4	33.6	—	1.2	12	ms
	4 Kbytes	t _{P4K}	—	75.6	168	—	27.6	60	ms
	16 Kbytes	t _{P16K}	—	302.4	672	—	108	240	ms
Erasure time N _{PEC} ≤ 100 times	4 Kbytes	t _{E4K}	—	50	120	—	25	60	ms
	16 Kbytes	t _{E16K}	—	200	480	—	100	240	ms
Erasure time N _{PEC} > 100 times	4 Kbytes	t _{E4K}	—	60	144	—	30	72	ms
	16 Kbytes	t _{E16K}	—	240	576	—	120	288	ms
Suspend delay time during programming		t _{SPD}	—	—	400	—	—	120	μs
First suspend delay time during erasure (in suspend priority mode)		t _{SESD1}	—	—	300	—	—	120	μs
Second suspend delay time during erasure (in suspend priority mode)		t _{SESD2}	—	—	1.7	—	—	1.7	ms
Suspend delay time during erasure (in erasure priority mode)		t _{SEED}	—	—	1.7	—	—	1.7	ms
FCU reset time		t _{FCUR}	35	—	—	35	—	—	μs

Appendix 1. Package Dimensions

Information on the latest version of the package dimensions or mountings has been displayed in “Packages” on Renesas Electronics Corporation website.

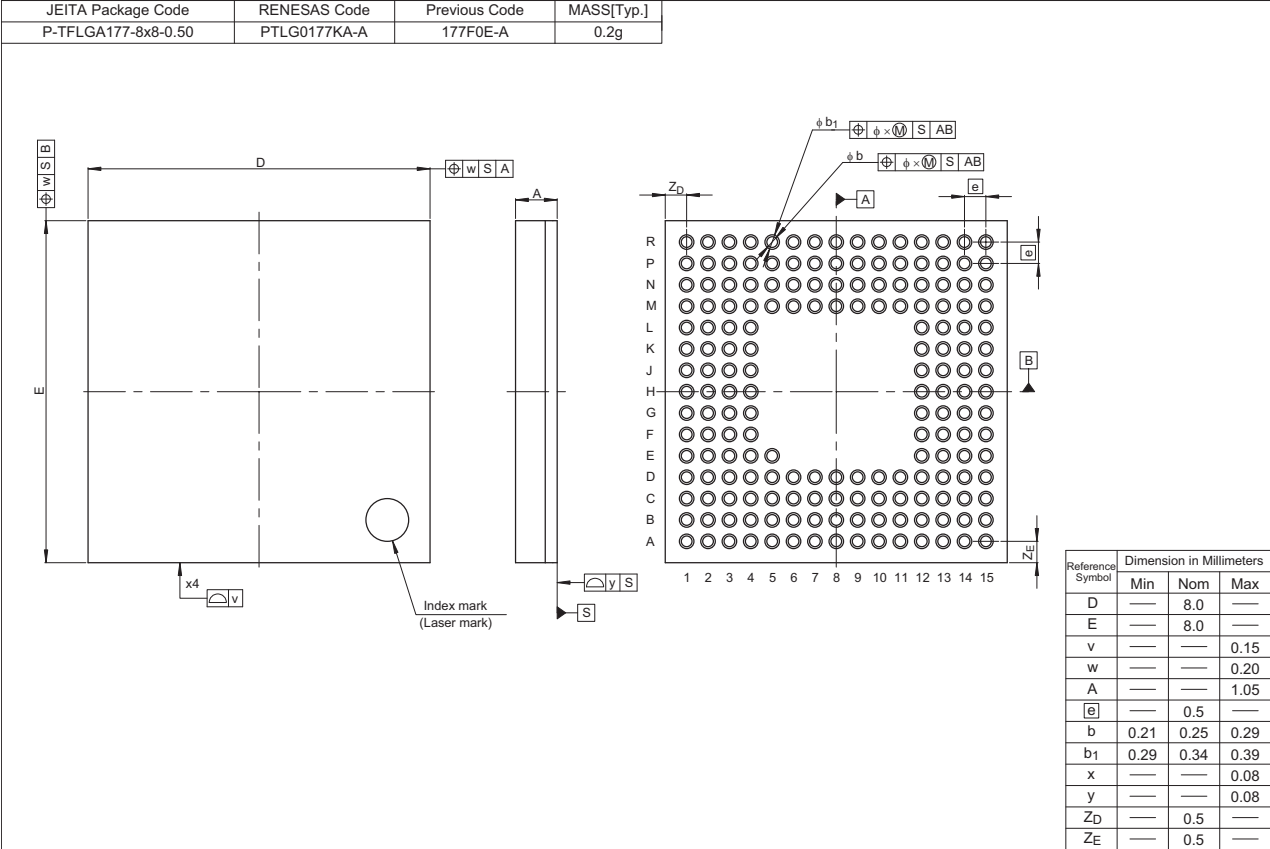


Figure A 177-pin TFLGA (PTLG0177KA-A)

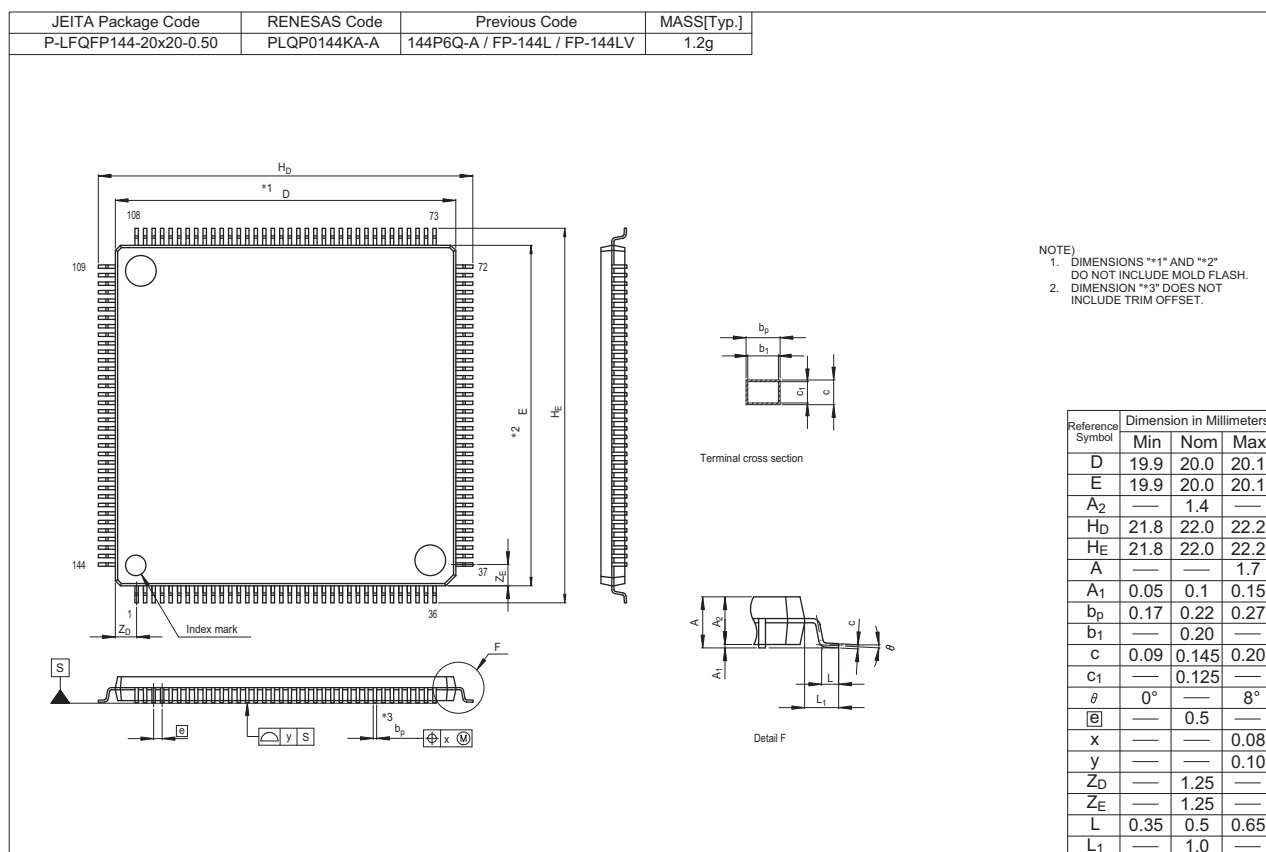


Figure E 144-pin LQFP (PLQP0144KA-A)

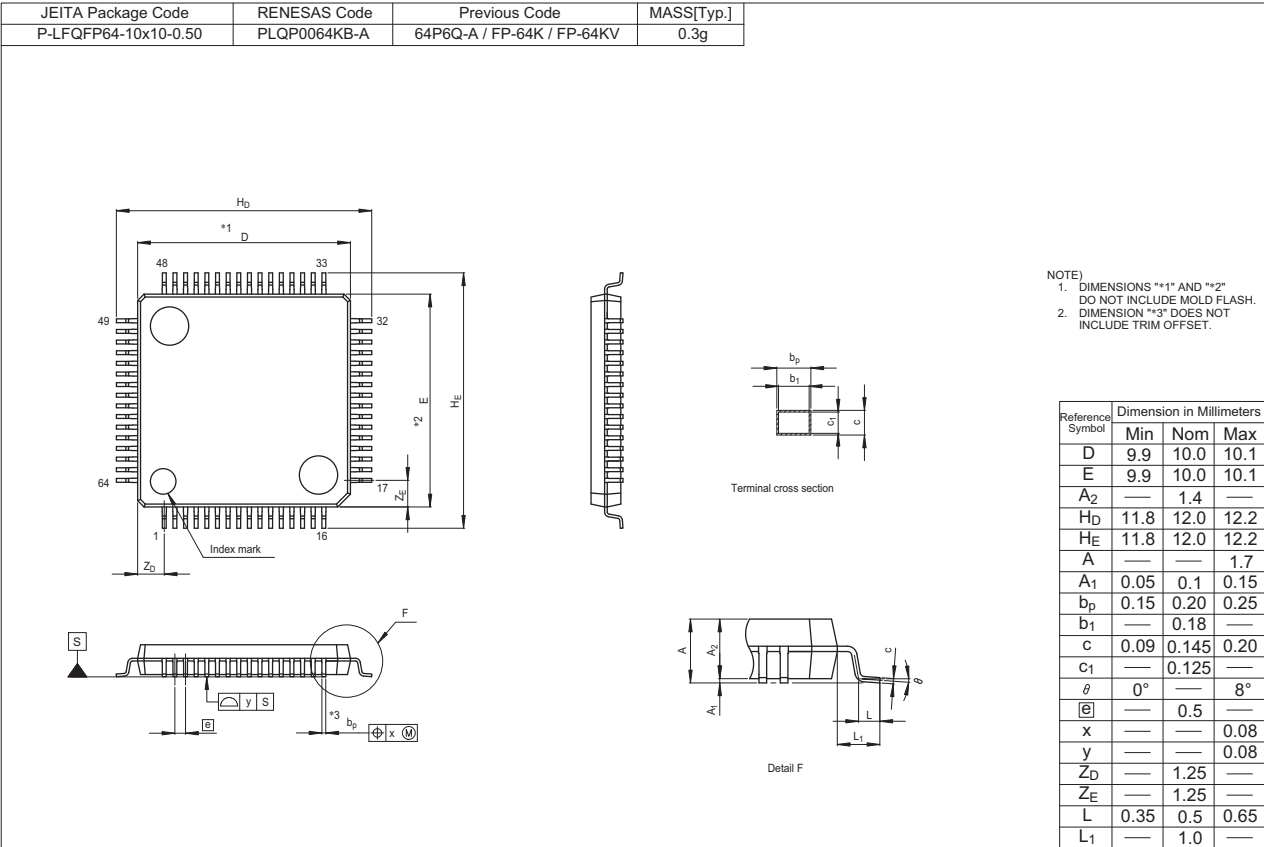


Figure I 64-pin LQFP (PLQP0064KB-A)

REVISION HISTORY	RX63N Group, RX631 Group Datasheet
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Rev.	Date	Description	
		Page	Summary
0.50	May 13, 2011	—	First Edition issued
0.90	Dec 27, 2011	All	— Package added (177-pin TFLGA, 176-pin LFBGA, 145-pin TFLGA), module name changed — Interrupt Controller (ICUb) module name changed 1. Overview 2 to 6 Table 1.1 Outline of Specifications, Reset, Realtime clock, Temperature sensor, Power supply voltage, changed 8 to 10 Table 1.3 List of Products, changed 10 Figure 1.1 How to Read the Product Part No., changed 12 to 17 Table 1.4 Pin Functions, BSCANP pin added 18 Figure 1.3 Pin Assignment (176-Pin TFLGA), added 19 Figure 1.4 Pin Assignment (176-Pin LFBGA), added 20 Figure 1.5 Pin Assignment (176-Pin LQFP), pin 18 changed 21 Figure 1.6 Pin Assignment (144-Pin TFLGA), added 22 Figure 1.7 Pin Assignment (144-Pin LQFP), pin 16 changed 23 Figure 1.8 Pin Assignment (100-Pin LQFP), pin 7 changed 24 to 28 Table 1.5 List of Pins and Pin Functions (177-pin TFLGA, 176-pin LFBGA), added 34 to 38 Table 1.7 List of Pins and Pin Functions (145-Pin TFLGA), added 4. I/O Registers 56 to 99 Table 5.1 List of I/O Registers, changed Appendix 2. Package Dimensions 100 Figure A. 177-pin TFLGA (PTLG0177KA-A), added 101 Figure B. 176-pin LFBGA (PLBG0176GA-A), added 103 Figure D. 145-pin TFLGA (PTLG0145KA-A), added 105 Figure F. 100-pin TFLGA (PTLG0100KA-A), added
1.00	Jun 06, 2012	1. Overview	2 to 6 Table 1.1 Outline of Specifications: CPU, ROM, RAM, E2 DataFlash, clock generation circuit, temperature sensor, power supply voltage, changed. Low power consumption, deleted 8 to 10 Table 1.3 List of Products, changed 11 Figure 1.2 Block Diagram, changed 12 Table 1.4 Pin Functions, description of VCC, changed 24 to 28 Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA): SDRAMC, added to table header; BCLK in pin number line M8, moved to Power Supply Clock System Control column 29 to 33 Table 1.6 List of Pin and Pin Functions (176-Pin LQFP): SDRAMC, added to table header; BCLK in pin number line 68, moved to Power Supply Clock System Control column 34 to 38 Table 1.7 List of Pin and Pin Functions (145-Pin TFLGA): SDRAMC, added to table header; MOSIB, added to pin number line D13; T_ERXD1 in pin number line H12, changed to ET_ERXD1; PO8, added to pin number line J4; BCLK in pin number line K6, moved to Power Supply Clock System Control column 39 to 43 Table 1.8 List of Pins and Pin Functions (144-Pin LQFP): SDRAMC, added to table header; PO8, added to pin number line 29; BCLK in pin number line 53, moved to Power Supply Clock System Control column; T_ERXD1 in pin number 87, changed to ET_ERXD1; MOSIB, added to pin number line 102 44 to 47 Table 1.9 List of Pins and Pin Functions (100-Pin LQFP): BCLK in pin number line 41, moved to Power Supply Clock System Control column 4. I/O Registers 57, 58 Table 4.1, MPU registers, added 5. Electrical Characteristics 105 to 163 Added

Classifications

- Items with Technical Update document number: Changes according to the corresponding issued Technical Update
- Items without Technical Update document number: Minor changes that do not require Technical Update to be issued

Rev.	Date	Description		Classification
		Page	Summary	
1.80	May 13. 2014	Features		TN-RX*-A092A/J
		1	Operating temp. range chaged, Unique ID added	
		1. Overview		
		2 to 7	Table 1.1 Outline of Specifications: Operating temperature changed, Unique ID and Note 2, added	
		8	Table 1.2 Comparison of Functions for Different Packages: Unique ID, added	
		9 to 16	Table 1.3 List of Products, changed and Note 2, added	
		17	Figure 1.1 How to Read the Product Part Number: Operating temperature range, changed	
		19, 23	Table 1.4 Pin Functions: VBATT and USB power pins, changed	
		3. Address Space		
		76	Figure 3.1 Memory Map in Each Operating Mode, changed	
		77	Figure 3.2 Correspondence between External Address Spaces and CS Areas (In On-Chip ROM Disabled Extended Mode), changed	
		5. Electrical Characteristics		
		130	Table 5.1 Absolute Maximum Ratings: Operating temperature, changed	
		131	Table 5.2 DC Characteristics (1): Note 1, chaged	
		133 to 134	Table 5.4 DC Characteristics (3) (for D and G Versions (-40 ≤ Ta ≤ +85°C)): Title	
		135 to 136	Table 5.5 DC Characteristics (4) (for G Version (-85 < Ta ≤ +105°C)), added	
		1921	Table 5.12 Clock Timing (Except for Sub-Clock Related): LOCO changed to LOCO and IWDTCCLKB	
		144	Figure 5.6 LOCO, IWDTCCLK Clock Oscillation Start Timing, added	
		189	Figure 5.68 Battery Backup Function Characteristics changed	

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