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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

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Details

Product Status	Discontinued at Digi-Key
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, LINbus, SCI, SPI, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	78
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b, 14x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f563nbcdfp-v0

Table 1.1 Outline of Specifications (2/6)

Classification	Module/Function	Description
Low power consumption	Low power consumption facilities	• Module stop function • Four low power consumption modes Sleep mode, all-module clock stop mode, software standby mode, and deep software standby mode • Battery backup function
Interrupt	Interrupt controller (ICUb)	• Peripheral function interrupts: 187 sources • External interrupts: 16 (pins IRQ0 to IRQ15) • Software interrupts: One source • Non-maskable interrupts: 6 sources • Sixteen levels specifiable for the order of priority
External bus extension		• The external address space can be divided into nine areas (CS0 to CS7, SDCS), each with independent control of access settings. Capacity of each area: 16 Mbytes (CS0 to CS7), 128 Mbytes (SDCS) A chip-select signal (CS0# to CS7#, SDCS#) can be output for each area. Each area is specifiable as an 8-, 16-, or 32-bit bus space. The data arrangement in each area is selectable as little or big endian (only for data). • SDRAM interface connectable • Bus format: Separate bus, multiplex bus • Wait control • Write buffer facility
DMA	DMA controller (DMAC)	• 4 channels • Three transfer modes: Normal transfer, repeat transfer, and block transfer • Activation sources: Software trigger, external interrupts, and interrupt requests from peripheral functions
	EXDMA controller (EXDMACa)	• 2 channels • Four transfer modes: Normal transfer, repeat transfer, block transfer, and cluster transfer • Single-address transfer enabled with the EDAKn signal • Capable of direct data transfer to TFT LCD panels • Activation sources: Software trigger, external DMA requests (EDREQn), and interrupt requests from peripheral functions
	Data transfer controller (DTCa)	• Three transfer modes: Normal transfer, repeat transfer, and block transfer • Activation sources: External interrupts and interrupt requests from peripheral functions

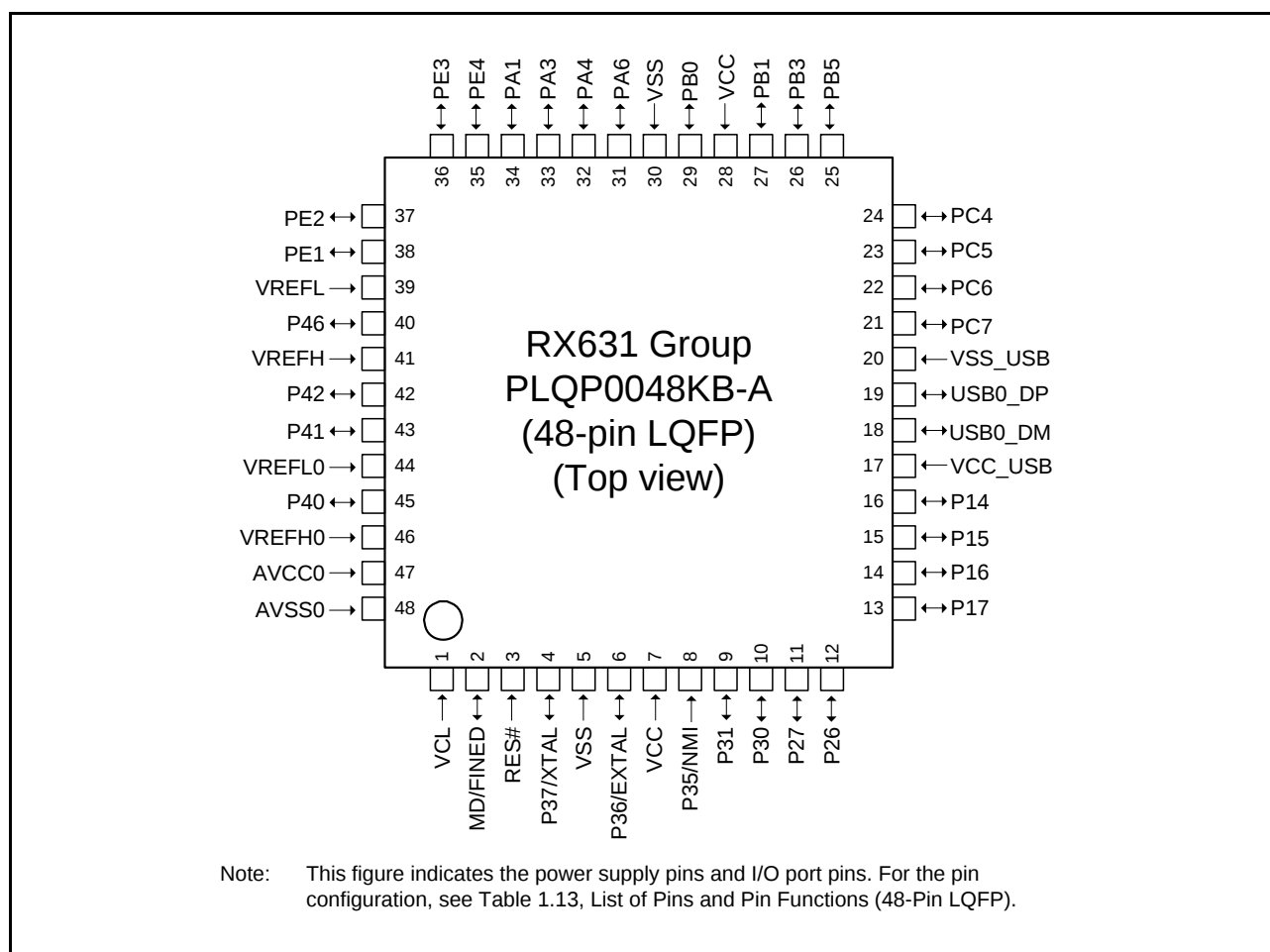


Figure 1.12 Pin Assignment (48-Pin LQFP)

Table 1.6 List of Pin and Pin Functions (176-Pin LQFP) (5/5)

Pin Number 176-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SCId, SCId, RSPI, RIIC, CAN, IEB, USB, and PDC)	Interrupt	S12AD, AD, DA
136		P64	CS4#/WE#				
137		P63	CS3#/CAS#				
138		P62	CS2#/RAS#				
139		P61	CS1#/SDCS#				
140	VSS						
141		P60	CS0#				
142	VCC						
143		PD7	D7[A7/D7]	MTIC5U/POE0#	SSLC3	IRQ7	AN7
144		PG1	D25				
145		PD6	D6[A6/D6]	MTIC5V/POE1#	SSLC2	IRQ6	AN6
146		PG0	D24				
147		PD5	D5[A5/D5]	MTIC5W/POE2#	SSLC1	IRQ5	AN013
148		PD4	D4[A4/D4]	POE3#	SSLC0	IRQ4	AN012
149		P97	A23/D23				
150		PD3	D3[A3/D3]	TIOCB8/TCLKH/POE8#	RSPCKC	IRQ3	AN011
151	VSS						
152		P96	A22/D22				
153	VCC						
154		PD2	D2[A2/D2]	MTIOC4D/TIOCA8	MISOC/CRX0	IRQ2	AN010
155		P95	A21/D21				
156		PD1	D1[A1/D1]	MTIOC4B/TIOCB7/ TCLKG	MOSIC/CTX0	IRQ1	AN009
157		P94	A20/D20				
158		PD0	D0[A0/D0]	TIOCA7		IRQ0	AN008
159		P93	A19/D19		CTST7#/RTST7#/SS7#		AN017
160		P92	A18/D18		RXD7/SMISO7/SSCL7		AN016
161		P91	A17/D17		SCK7		AN015
162	VSS						
163		P90	A16/D16		TXD7/SMOSI7/SSDA7		AN014
164	VCC						
165		P47				IRQ15-DS	AN007
166		P46				IRQ14-DS	AN006
167		P45				IRQ13-DS	AN005
168		P44				IRQ12-DS	AN004
169		P43				IRQ11-DS	AN003
170		P42				IRQ10-DS	AN002
171		P41				IRQ9-DS	AN001
172	VREFL0						
173		P40				IRQ8-DS	AN000
174	VREFH0						
175	AVCC0						
176		P07				IRQ15	ADTRG0#

Note 1. The BCLK function is multiplexed with the I/O port function for pin P53, so the port function is not available if the external bus is enabled.

Note 2. Enabled only for the ROM capacity: 2 Mbytes/1.5 Mbytes

Table 1.9 List of Pins and Pin Functions (100-Pin TFLGA) (1/5)

Pin No. 100-pin TFLGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC	Timers (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SC1c, SC1d, RSPI, RIIC, CAN, IEB, USB)	Interrupt	S12AD AD DA
A1		P05				IRQ13	DA1
A2	VREFH						
A3		P07				IRQ15	ADTRG0#
A4	VREFL0						
A5		P43				IRQ11-DS	AN003
A6		PD0	D0[A0/D0]			IRQ0	AN008
A7		PD4	D4[A4/D4]	POE3#		IRQ4	AN012
A8		PE0	D8[A8/D8]		SCK12/SSLB1		ANEX0
A9		PE1	D9[A9/D9]	MTIOC4C/ PO18	TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12/SSLB2/ RSPCKB		ANEX1
A10		PE2	D10[A10/D10]	MTIOC4A/ PO23	RXD12/SMISO12/ SSCL12/RXDX12/ SSLB3/MOSIB	IRQ7-DS	AN0
B1	EMLE						
B2	AVSS0						
B3	AVCC0						
B4		P40				IRQ8-DS	AN000
B5		P44				IRQ12-DS	AN004
B6		PD1	D1[A1/D1]	MTIOC4B	CTX0*1	IRQ1	AN009
B7		PD3	D3[A3/D3]	POE8#		IRQ3	AN011
B8		PD6	D6[A6/D6]	MTIC5V/ POE1#		IRQ6	AN6
B9		PD7	D7[A7/D7]	MTIC5U/ POE0#		IRQ7	AN7
B10		PE3	D11[A11/D11]	MTIOC4B/ PO26/POE8#	CTS12#/RTS12#/ SS12#/MISOB/ ET_ERXD3		AN1
C1	VCL						
C2	VREFL						
C3		PJ3		MTIOC3C	CTS6#/RTS6#/ CTS0#/RTS0#/ SS6#/SS0#		
C4	VREFH0						
C5		P42				IRQ10-DS	AN002
C6		P47				IRQ15-DS	AN007
C7		PD2	D2[A2/D2]	MTIOC4D	CRX0*1	IRQ2	AN010
C8		PD5	D5[A5/D5]	MTIC5W/ POE2#		IRQ5	AN013
C9		PE5	D13[A13/D13]	MTIOC4C/ MTIOC2B	RSPCKB/ ET_RX_CLK/ REF50CK	IRQ5	AN3
C10		PE4	D12[A12/D12]	MTIOC4D/ MTIOC1A/ PO28	SSLB0/ET_ERXD2		AN2
D1	XCIN						

Table 1.11 List of Pins and Pin Functions (64-Pin TFLGA) (2/2)

Pin No. 64-pin TFLGA	Power Supply Clock System Control	I/O Port	Timers (MTU2a, TPUa, TMR, PPG, RTCa, POE2a)	Communications (SClC, SClD, RSPI, RIIC, CAN, IEB, USB)	Interrupt	S12ADa, DAa
E4	TMS	P16	MTIOC3C/MTIOC3D/ TIOCB1/TCLKC/TMO2/ RTCOUT	TXD1/SMOSI1/SSDA1/ MOSIA/SCL2-DS/IERXD/ USB0_VBUS/ USB0_VBUSEN/ USB0_OVRCURB	IRQ6	ADTRG0#
E5		PC4	MTIOC3D/MTCLKC/TMC1/ PO25/POE0#	SCK5/SSLA0/ USB0_DPRPD		
E6	VCC					
E7	VSS					
E8		PB0	MTIC5W/TIOCA3/PO24	RXD6/SMISO6/SSCL6/ RSPCKA	IRQ12	
F1	VCC					
F2		P35			NMI	
F3		P31	MTIOC4D/TMC12/RTCIC1	CTS1#/RTS1#/SS1#/ SSLB0/USB0_DPUPE	IRQ1-DS	
F4		PC5	MTIOC3B/MTCLKD/TMR12/ PO29	RSPCKA/USB0_ID		
F5		P15	MTIOC0B/MTCLKB/ TIOCB2/TCLKB/TMC12	RXD1/SMISO1/SSCL1/ CRX1-DS/USB1_DPUPE	IRQ5	
F6		PB1	MTIOC0C/MTIOC4C/ TIOCB3/TMC10/PO25	TXD6/SMOSI6/SSDA6	IRQ4-DS	
F7		PB5	MTIOC2A/MTIOC1B/ TIOCB4/TMR11/PO29/ POE1#	SCK9		
F8		PB3	MTIOC0A/MTIOC4A/ TIOC3D/TCLKD/TMO0/ PO27/POE3#	SCK6		
G1	EXTAL	P36				
G2	TDO	P26	MTIOC2A/TMO1	TXD1/SMOSI1/SSDA1/ MOSIB/USB0_VBUSEN		
G3	VCC_USB					
G4	VSS_USB					
G5	VCC_USB					
G6		PC6	MTIOC3C/MTCLKA/TMC12/ PO30	MOSIA/USB0_EXICEN	IRQ13	
G7		PC3	MTIOC4D/TCLKB/PO24	TXD5/SMOSI5/SSDA5/ SDA2/IETXD		
G8		PB6	MTIOC3D/TIOCA5/PO30	RXD9/SMISO9/SSCL9		
H1	XTAL	P37				
H2	TRST#	P17	MTIOC3A/MTIOC3B/ TIOCB0/TCLKD/TMO1/ POE8#	SCK1/MISOA/SDA2-DS/ IETXD/USB1_VBUS	IRQ7	
H3				USB0_DM		
H4				USB0_DP		
H5				USB1_DM		
H6				USB1_DP		
H7		PC2	MTIOC4B/TCLKA/PO21	RXD5/SMISO5/SSCL5/ SSLA3/SCL2/IERXD		
H8		PB7	MTIOC3B/TIOCB5/PO31	TXD9/SMOSI9/SSDA9		

2.3 Register Associated with DSP Instructions

(1) Accumulator (ACC)

The accumulator (ACC) is a 64-bit register used for DSP instructions. The accumulator is also used for the multiply and multiply-and-accumulate instructions; EMUL, EMULU, FMUL, MUL, and RMPA, in which case the prior value in the accumulator is modified by execution of the instruction.

Use the MVTACHI and MVTACLO instructions for writing to the accumulator. The MVTACHI and MVTACLO instructions write data to the higher-order 32 bits (bits 63 to 32) and the lower-order 32 bits (bits 31 to 0), respectively. Use the MVFACHI and MVFACMI instructions for reading data from the accumulator. The MVFACHI and MVFACMI instructions read data from the higher-order 32 bits (bits 63 to 32) and the middle 32 bits (bits 47 to 16), respectively.

Table 4.1 List of I/O Registers (Address Order) (11/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 71EEh	ICU	DTC activation enable register 238	DTCER238	8	8	2	ICLK	ICUb
0008 71EFh	ICU	DTC activation enable register 239	DTCER239	8	8	2	ICLK	
0008 71F1h	ICU	DTC activation enable register 241	DTCER241	8	8	2	ICLK	
0008 71F2h	ICU	DTC activation enable register 242	DTCER242	8	8	2	ICLK	
0008 71F4h	ICU	DTC activation enable register 244	DTCER244	8	8	2	ICLK	
0008 71F5h	ICU	DTC activation enable register 245	DTCER245	8	8	2	ICLK	
0008 71F7h	ICU	DTC activation enable register 247	DTCER247	8	8	2	ICLK	
0008 71F8h	ICU	DTC activation enable register 248	DTCER248	8	8	2	ICLK	
0008 71FAh	ICU	DTC activation enable register 250	DTCER250	8	8	2	ICLK	
0008 71FBh	ICU	DTC activation enable register 251	DTCER251	8	8	2	ICLK	
0008 7202h	ICU	Interrupt request enable register 02	IER02	8	8	2	ICLK	
0008 7203h	ICU	Interrupt request enable register 03	IER03	8	8	2	ICLK	
0008 7204h	ICU	Interrupt request enable register 04	IER04	8	8	2	ICLK	
0008 7205h	ICU	Interrupt request enable register 05	IER05	8	8	2	ICLK	
0008 7206h	ICU	Interrupt request enable register 06	IER06	8	8	2	ICLK	
0008 7207h	ICU	Interrupt request enable register 07	IER07	8	8	2	ICLK	
0008 7208h	ICU	Interrupt request enable register 08	IER08	8	8	2	ICLK	
0008 7209h	ICU	Interrupt request enable register 09	IER09	8	8	2	ICLK	
0008 720Bh	ICU	Interrupt request enable register 0B	IER0B	8	8	2	ICLK	
0008 720Ch	ICU	Interrupt request enable register 0C	IER0C	8	8	2	ICLK	
0008 720Dh	ICU	Interrupt request enable register 0D	IER0D	8	8	2	ICLK	
0008 720Eh	ICU	Interrupt request enable register 0E	IER0E	8	8	2	ICLK	
0008 720Fh	ICU	Interrupt request enable register 0F	IER0F	8	8	2	ICLK	
0008 7210h	ICU	Interrupt request enable register 10	IER10	8	8	2	ICLK	ICUb
0008 7211h	ICU	Interrupt request enable register 11	IER11	8	8	2	ICLK	
0008 7212h	ICU	Interrupt request enable register 12	IER12	8	8	2	ICLK	
0008 7213h	ICU	Interrupt request enable register 13	IER13	8	8	2	ICLK	
0008 7214h	ICU	Interrupt request enable register 14	IER14	8	8	2	ICLK	
0008 7215h	ICU	Interrupt request enable register 15	IER15	8	8	2	ICLK	
0008 7216h	ICU	Interrupt request enable register 16	IER16	8	8	2	ICLK	
0008 7217h	ICU	Interrupt request enable register 17	IER17	8	8	2	ICLK	
0008 7218h	ICU	Interrupt request enable register 18	IER18	8	8	2	ICLK	
0008 7219h	ICU	Interrupt request enable register 19	IER19	8	8	2	ICLK	
0008 721Ah	ICU	Interrupt request enable register 1A	IER1A	8	8	2	ICLK	
0008 721Bh	ICU	Interrupt request enable register 1B	IER1B	8	8	2	ICLK	
0008 721Ch	ICU	Interrupt request enable register 1C	IER1C	8	8	2	ICLK	
0008 721Dh	ICU	Interrupt request enable register 1D	IER1D	8	8	2	ICLK	
0008 721Eh	ICU	Interrupt request enable register 1E	IER1E	8	8	2	ICLK	
0008 721Fh	ICU	Interrupt request enable register 1F	IER1F	8	8	2	ICLK	
0008 72E0h	ICU	Software interrupt activation register	SWINTR	8	8	2	ICLK	
0008 72F0h	ICU	Fast interrupt set register	FIR	16	16	2	ICLK	
0008 7300h	ICU	Interrupt source priority register 000	IPR000	8	8	2	ICLK	ICUb
0008 7301h	ICU	Interrupt source priority register 001	IPR001	8	8	2	ICLK	
0008 7302h	ICU	Interrupt source priority register 002	IPR002	8	8	2	ICLK	
0008 7303h	ICU	Interrupt source priority register 003	IPR003	8	8	2	ICLK	
0008 7304h	ICU	Interrupt source priority register 004	IPR004	8	8	2	ICLK	
0008 7305h	ICU	Interrupt source priority register 005	IPR005	8	8	2	ICLK	
0008 7306h	ICU	Interrupt source priority register 006	IPR006	8	8	2	ICLK	
0008 7307h	ICU	Interrupt source priority register 007	IPR007	8	8	2	ICLK	
0008 7320h	ICU	Interrupt source priority register 032	IPR032	8	8	2	ICLK	
0008 7321h	ICU	Interrupt source priority register 033	IPR033	8	8	2	ICLK	

Table 4.1 List of I/O Registers (Address Order) (12/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 7322h	ICU	Interrupt source priority register 034	IPR034	8	8	2	ICLK	ICUb
0008 7323h	ICU	Interrupt source priority register 035	IPR035	8	8	2	ICLK	
0008 7324h	ICU	Interrupt source priority register 036	IPR036	8	8	2	ICLK	
0008 7325h	ICU	Interrupt source priority register 037	IPR037	8	8	2	ICLK	
0008 7326h	ICU	Interrupt source priority register 038	IPR038	8	8	2	ICLK	
0008 7327h	ICU	Interrupt source priority register 039	IPR039	8	8	2	ICLK	
0008 732Ah	ICU	Interrupt source priority register 042	IPR042	8	8	2	ICLK	
0008 732Dh	ICU	Interrupt source priority register 045	IPR045	8	8	2	ICLK	
0008 7330h	ICU	Interrupt source priority register 048	IPR048	8	8	2	ICLK	
0008 7334h	ICU	Interrupt source priority register 052	IPR052	8	8	2	ICLK	
0008 7338h	ICU	Interrupt source priority register 056	IPR056	8	8	2	ICLK	
0008 733Eh	ICU	Interrupt source priority register 062	IPR062	8	8	2	ICLK	
0008 7340h	ICU	Interrupt source priority register 064	IPR064	8	8	2	ICLK	
0008 7341h	ICU	Interrupt source priority register 065	IPR065	8	8	2	ICLK	
0008 7342h	ICU	Interrupt source priority register 066	IPR066	8	8	2	ICLK	
0008 7343h	ICU	Interrupt source priority register 067	IPR067	8	8	2	ICLK	
0008 7344h	ICU	Interrupt source priority register 068	IPR068	8	8	2	ICLK	
0008 7345h	ICU	Interrupt source priority register 069	IPR069	8	8	2	ICLK	
0008 7346h	ICU	Interrupt source priority register 070	IPR070	8	8	2	ICLK	
0008 7347h	ICU	Interrupt source priority register 071	IPR071	8	8	2	ICLK	
0008 7348h	ICU	Interrupt source priority register 072	IPR072	8	8	2	ICLK	
0008 7349h	ICU	Interrupt source priority register 073	IPR073	8	8	2	ICLK	
0008 734Ah	ICU	Interrupt source priority register 074	IPR074	8	8	2	ICLK	
0008 734Bh	ICU	Interrupt source priority register 075	IPR075	8	8	2	ICLK	
0008 734Ch	ICU	Interrupt source priority register 076	IPR076	8	8	2	ICLK	
0008 734Dh	ICU	Interrupt source priority register 077	IPR077	8	8	2	ICLK	
0008 734Eh	ICU	Interrupt source priority register 078	IPR078	8	8	2	ICLK	
0008 734Fh	ICU	Interrupt source priority register 079	IPR079	8	8	2	ICLK	
0008 735Ah	ICU	Interrupt source priority register 090	IPR090	8	8	2	ICLK	
0008 735Bh	ICU	Interrupt source priority register 091	IPR091	8	8	2	ICLK	
0008 735Ch	ICU	Interrupt source priority register 092	IPR092	8	8	2	ICLK	
0008 735Dh	ICU	Interrupt source priority register 093	IPR093	8	8	2	ICLK	
0008 7362h	ICU	Interrupt source priority register 098	IPR098	8	8	2	ICLK	
0008 7366h	ICU	Interrupt source priority register 102	IPR102	8	8	2	ICLK	
0008 736Ah	ICU	Interrupt source priority register 106	IPR106	8	8	2	ICLK	
0008 736Bh	ICU	Interrupt source priority register 107	IPR107	8	8	2	ICLK	
0008 736Ch	ICU	Interrupt source priority register 108	IPR108	8	8	2	ICLK	
0008 736Dh	ICU	Interrupt source priority register 109	IPR109	8	8	2	ICLK	
0008 736Eh	ICU	Interrupt source priority register 110	IPR110	8	8	2	ICLK	
0008 736Fh	ICU	Interrupt source priority register 111	IPR111	8	8	2	ICLK	
0008 7370h	ICU	Interrupt source priority register 112	IPR112	8	8	2	ICLK	
0008 7372h	ICU	Interrupt source priority register 114	IPR114	8	8	2	ICLK	
0008 737Ah	ICU	Interrupt source priority register 122	IPR122	8	8	2	ICLK	
0008 737Eh	ICU	Interrupt source priority register 126	IPR126	8	8	2	ICLK	
0008 7382h	ICU	Interrupt source priority register 130	IPR130	8	8	2	ICLK	
0008 7384h	ICU	Interrupt source priority register 132	IPR132	8	8	2	ICLK	
0008 7386h	ICU	Interrupt source priority register 134	IPR134	8	8	2	ICLK	
0008 738Ah	ICU	Interrupt source priority register 138	IPR138	8	8	2	ICLK	
0008 738Ch	ICU	Interrupt source priority register 140	IPR140	8	8	2	ICLK	
0008 738Eh	ICU	Interrupt source priority register 142	IPR142	8	8	2	ICLK	
0008 7392h	ICU	Interrupt source priority register 146	IPR146	8	8	2	ICLK	

Table 4.1 List of I/O Registers (Address Order) (39/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
000A 003Ah	USB0	BEMP interrupt enable register	BEMPENB	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	USBa
000A 003Ch	USB0	SOF output configuration register	SOFCFG	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 0040h	USB0	Interrupt status register 0	INTSTS0	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 0042h	USB0	Interrupt status register 1	INTSTS1	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 0046h	USB0	BRDY interrupt status register	BRDYSTS	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 0048h	USB0	NRDY interrupt status register	NRDYSTS	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 004Ah	USB0	BEMP interrupt status register	BEMPSTS	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 004Ch	USB0	Frame number register	FRMNUM	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	USBa
000A 004Eh	USB0	Device state changing register	DVCHGR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 0050h	USB0	USB address register	USBADDR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	

Table 4.1 List of I/O Registers (Address Order) (49/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
000C 0100h	ETHERC	ETHERC mode register	ECMR	32	32	5, 6 PCLKA	—	ETHERC
000C 0108h	ETHERC	Receive frame length register	RFLR	32	32	5, 6 PCLKA	—	
000C 0110h	ETHERC	ETHERC status register	ECSR	32	32	5, 6 PCLKA	—	
000C 0118h	ETHERC	ETHERC interrupt permission register	ECSIPR	32	32	5, 6 PCLKA	—	
000C 0120h	ETHERC	PHY interface register	PIR	32	32	5, 6 PCLKA	—	
000C 0128h	ETHERC	PHY status register	PSR	32	32	5, 6 PCLKA	—	
000C 0140h	ETHERC	Random number generation counter upper limit setting register	RDMLR	32	32	5, 6 PCLKA	—	
000C 0150h	ETHERC	IPG register	IPGR	32	32	5, 6 PCLKA	—	
000C 0154h	ETHERC	Automatic PAUSE frame register	APR	32	32	5, 6 PCLKA	—	
000C 0158h	ETHERC	Manual PAUSE frame register	MPR	32	32	5, 6 PCLKA	—	
000C 0160h	ETHERC	PAUSE Frame receive counter register	RFCF	32	32	5, 6 PCLKA	—	
000C 0164h	ETHERC	Automatic PAUSE frame retransmit count register	TPAUSER	32	32	5, 6 PCLKA	—	
000C 0168h	ETHERC	PAUSE frame retransmit counter register	TPAUSECR	32	32	5, 6 PCLKA	—	
000C 016Ch	ETHERC	Broadcast frame receive count setting register	BCFR	32	32	5, 6 PCLKA	—	
000C 01C0h	ETHERC	MAC address high register	MAHR	32	32	5, 6 PCLKA	—	
000C 01C8h	ETHERC	MAC address low register	MALR	32	32	5, 6 PCLKA	—	
000C 01D0h	ETHERC	Transmit retry over counter register	TROCR	32	32	5, 6 PCLKA	—	
000C 01D4h	ETHERC	Delayed collision detect counter register	CDCR	32	32	5, 6 PCLKA	—	
000C 01D8h	ETHERC	Lost carrier counter register	LCCR	32	32	5, 6 PCLKA	—	
000C 01DCh	ETHERC	Carrier not detect counter register	CNDCR	32	32	5, 6 PCLKA	—	
000C 01E4h	ETHERC	CRC error frame receive counter register	CEFCR	32	32	5, 6 PCLKA	—	
000C 01E8h	ETHERC	Frame receive error counter register	FRECR	32	32	5, 6 PCLKA	—	
000C 01ECh	ETHERC	Too-short frame receive counter register	TSFRCR	32	32	5, 6 PCLKA	—	
000C 01F0h	ETHERC	Too-long frame receive counter register	TLFRCR	32	32	5, 6 PCLKA	—	
000C 01F4h	ETHERC	Residual-bit frame receive counter register	RFCR	32	32	5, 6 PCLKA	—	
000C 01F8h	ETHERC	Multicast address frame receive counter register	MAFCR	32	32	5, 6 PCLKA	—	

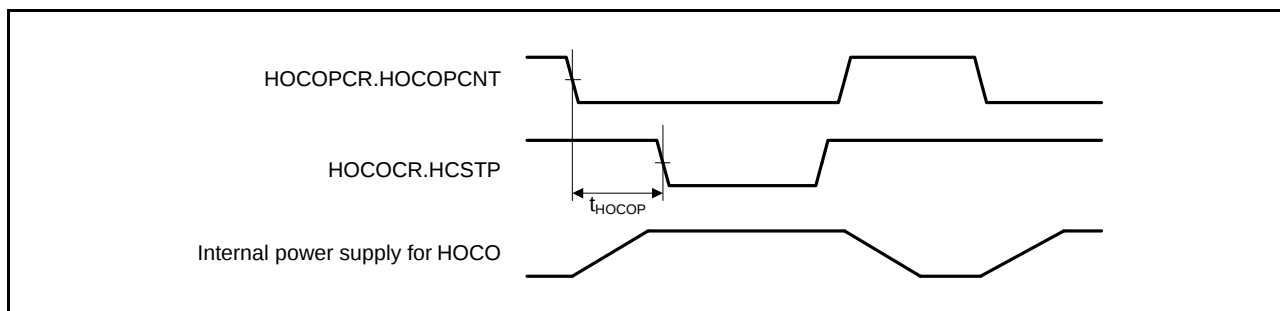


Figure 5.9 HOCO Power Supply Control Timing

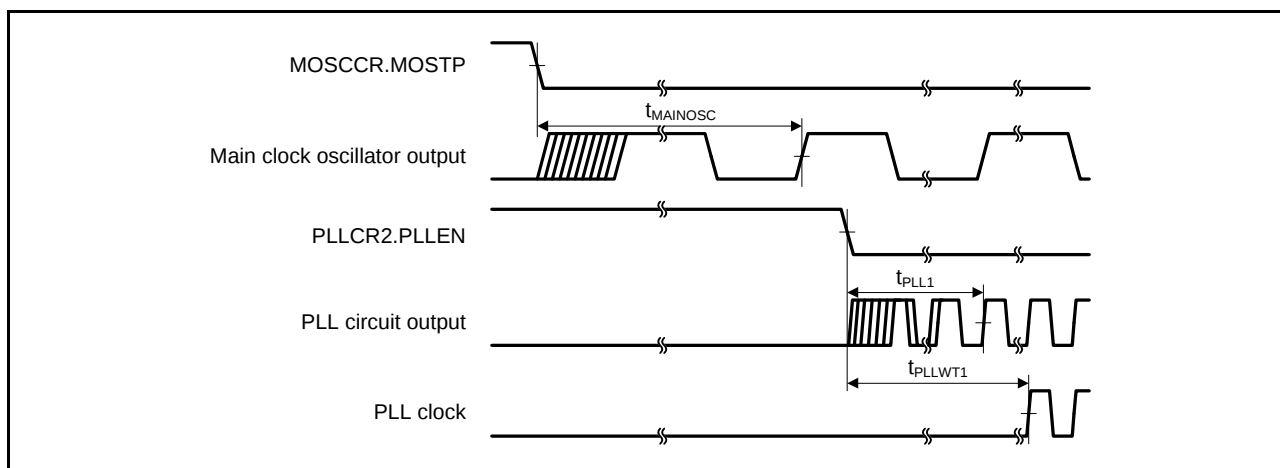


Figure 5.10 PLL Clock Oscillation Start Timing (PLL is Operated after Main Clock Oscillation Has Settled)

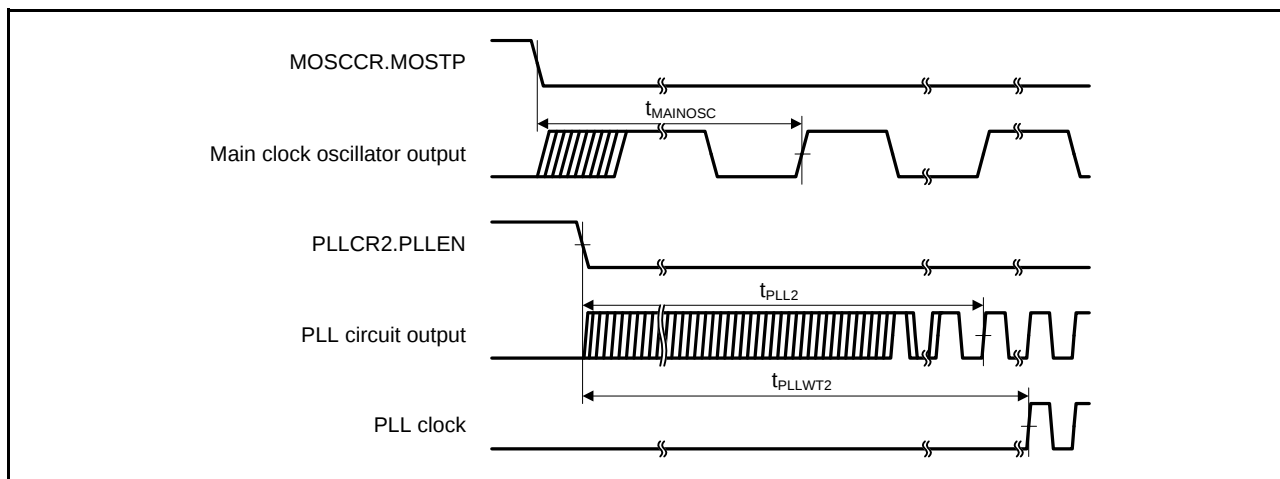


Figure 5.11 PLL Clock Oscillation Start Timing (PLL is Operated before Main Clock Oscillation Has Settled)

5.3.5 Bus Timing

Table 5.16 Bus Timing (packages with 177 to 144 pins)

Conditions: $V_{CC} = AVCC0 = VREFH = VCC_USB = 2.7$ to 3.6 V, $VREFH0 = 2.7$ V to $AVCC0$,
 $VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0$ V,
 $ICLK = 8$ to 100 MHz, $BCLK$ pin = 8 to 50 MHz, $SDCLK$ pin = 8 to 50 MHz, $T_a = T_{opr}$
 Output load conditions: $V_{OH} = VCC \times 0.5$, $V_{OL} = VCC \times 0.5$, $I_{OH} = -1.0$ mA, $I_{OL} = 1.0$ mA, $C = 30$ pF
 High drive output is selected by the drive capacity control register.

Item	Symbol	Min.	Max.	Unit	Test Conditions
Address delay time	t_{AD}	—	15	ns	Figure 5.17 to Figure 5.22
Byte control delay time	t_{BCD}	—	15	ns	
CS# delay time	t_{CSD}	—	15	ns	
ALE delay time	t_{ALED}	—	20	ns	
RD# delay time	t_{RSD}	—	15	ns	
Read data setup time	t_{RDS}	15	—	ns	
Read data hold time	t_{RDH}	0	—	ns	
WR# delay time	t_{WRD}	—	15	ns	
Write data delay time	t_{WDD}	—	15	ns	
Write data hold time	t_{WDH}	0	—	ns	
WAIT# setup time	t_{WTS}	15	—	ns	Figure 5.23
WAIT# hold time	t_{WTH}	0	—	ns	
Address delay time 2 (SDRAM)	t_{AD2}	1	15	ns	Figure 5.24 to Figure 5.30
CS# delay time 2 (SDRAM)	t_{CSD2}	1	15	ns	
DQM delay time (SDRAM)	t_{DQMD}	1	15	ns	
CKE delay time (SDRAM)	t_{CKED}	1	15	ns	
Read data setup time 2 (SDRAM)	t_{RDS2}	12	—	ns	
Read data hold time 2 (SDRAM)	t_{RDH2}	0	—	ns	
Write data delay time 2 (SDRAM)	t_{WDD2}	—	15	ns	
Write data hold time 2 (SDRAM)	t_{WDH2}	1	—	ns	
WE# delay time (SDRAM)	t_{WED}	1	15	ns	
RAS# delay time (SDRAM)	t_{RASD}	1	15	ns	
CAS# delay time (SDRAM)	t_{CASD}	1	15	ns	

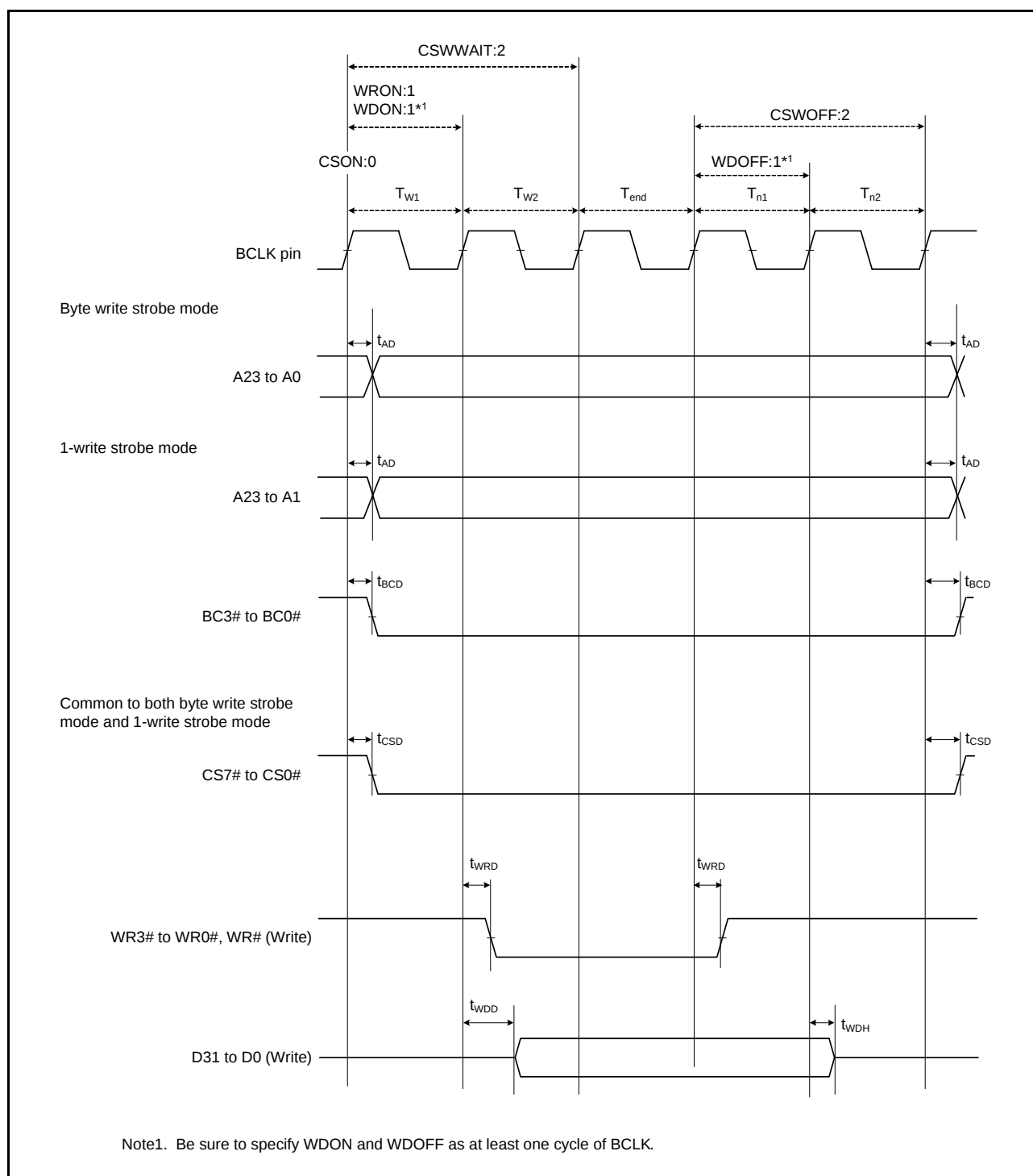


Figure 5.20 External Bus Timing/Normal Write Cycle (Bus Clock Synchronized)

5.3.6 EXDMAC Timing

Table 5.18 EXDMAC Timing

Conditions: $V_{CC} = AV_{CC0} = V_{REFH} = V_{CC_USB} = 2.7$ to 3.6 V, $V_{REFH0} = 2.7$ V to AV_{CC0} ,

$V_{SS} = AV_{SS0} = V_{REFL}/V_{REFL0} = V_{SS_USB} = 0$ V

$ICLK = 8$ to 100 MHz, $PCLK = 8$ to 50 MHz, $BCLK$ pin = 8 to 100 MHz, $SDCLK$ pin = 8 to 50 MHz, $T_a = T_{opr}$

High drive output is selected by the drive capacity control register

	Item	Symbol	Min.	Max.	Unit	Test Conditions
EXDMAC	EDREQ setup time	t_{EDRQS}	20	—	ns	Figure 5.31
	EDREQ hold time	t_{EDRQH}	5	—	ns	Figure 5.32 and Figure 5.33
	EDACK delay time	t_{EDACD}	—	15	ns	Figure 5.33

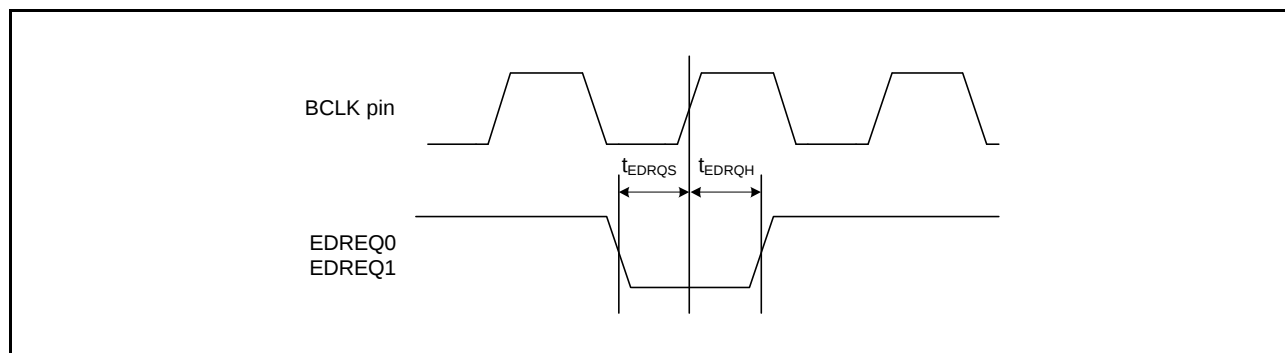
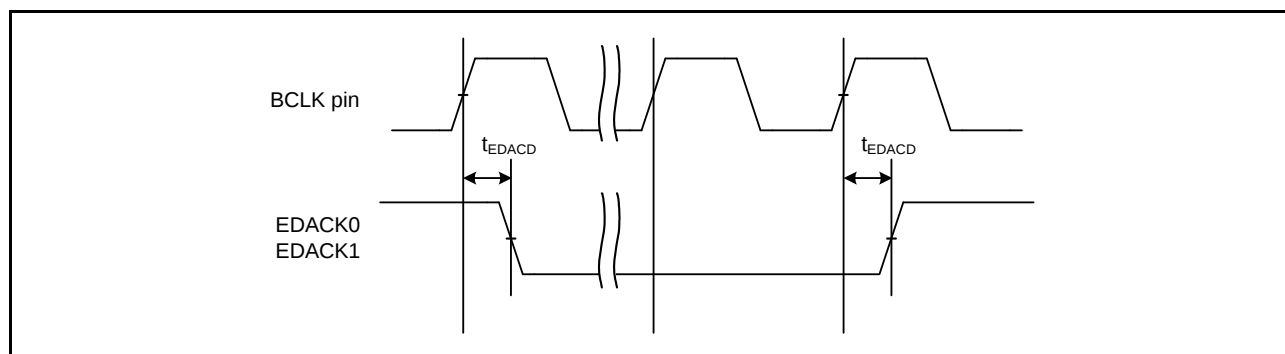
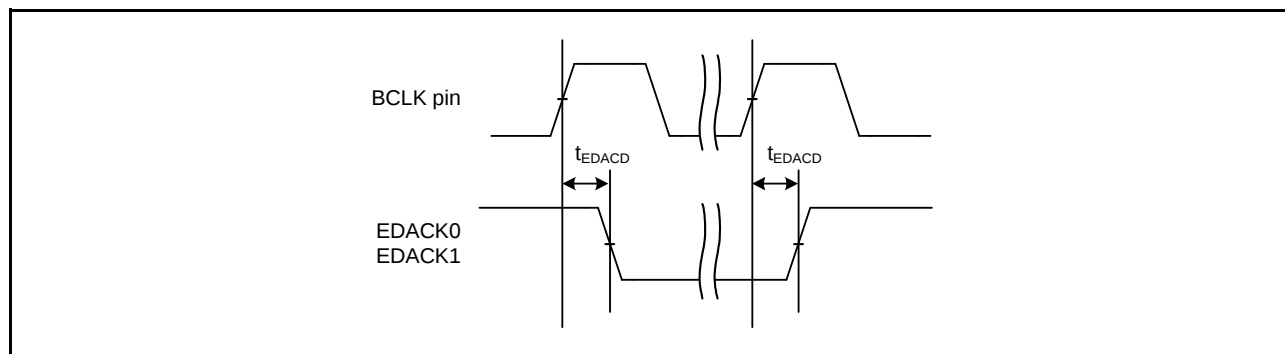
**Figure 5.31 EDREQ0 and EDREQ1 Input Timing****Figure 5.32 EDACK0 and EDACK1 Single-Address Transfer Timing (for a CS Area)****Figure 5.33 EDACK0 and EDACK1 Single-Address Transfer Timing (for SDRAM)**

Table 5.21 Timing of On-Chip Peripheral Modules (3)

Conditions: $V_{CC} = AVCC0 = VREFH = VCC_USB = 2.7$ to 3.6 V^{*1} , $VREFH0 = 2.7\text{ V}$ to $AVCC0^{*1}$,
 $VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0\text{ V}$,
 $PCLK = 8$ to 50 MHz ,
 $T_a = T_{opr}$
 High drive output is selected by the drive capacity control register.

Item				Symbol	Min.	Max.	Unit*2	Test Conditions
RSPI	Data output delay time	Master	Packages with 177 to 144 pins	t_{OD}	—	18	ns	Figure 5.43 to Figure 5.46 C = 30pF
			Packages with 100 pins or less		—	30		
		Slave	Packages with 177 to 144 pins		—	$3 \times t_{Pcyc} + 40$		
			Packages with 100 pins or less		—	$3 \times t_{Pcyc} + 50$		
	Data output hold time	Master		t_{OH}	0	—	ns	
		Slave			0	—		
	Successive transmission delay time	Master		t_{TD}	$t_{SPcyc} + 2 \times t_{Pcyc}$	$8 \times t_{SPcyc} + 2 \times t_{Pcyc}$	ns	
		Slave			$4 \times t_{Pcyc}$	—		
	MOSI and MISO rise/fall time	Output	Packages with 177 to 144 pins	t_{Dr}, t_{Df}	—	5	ns	
			Packages with 100 pins or less		—	10		
		Input			—	1	μs	
	SSL rise/fall time	Output	Packages with 177 to 144 pins	t_{SSLr}, t_{SSLf}	—	5	ns	
			Packages with 100 pins or less		—	10		
		Input			—	1	μs	
Slave access time				t_{SA}	—	4	t_{Pcyc}	Figure 5.45 and Figure 5.46 C = 30pF
Slave output release time				t_{REL}	—	3	t_{Pcyc}	

Note 1. When operation at 3.0 V or a lower voltage is needed, please contact a Renesas sales office.

Note 2. t_{Pcyc} : PCLK cycle

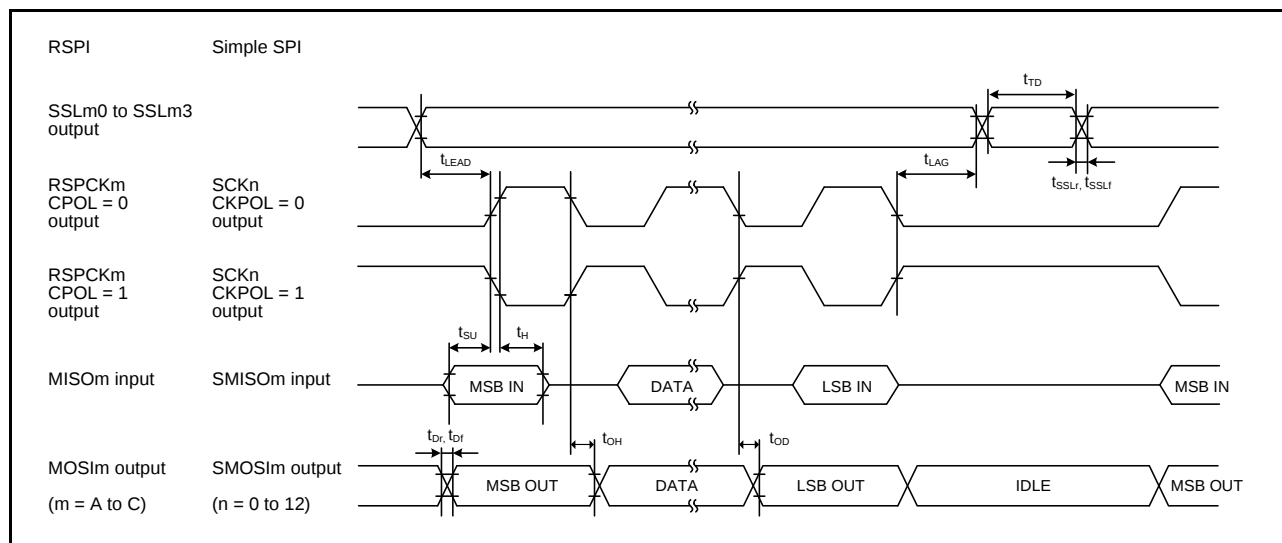


Figure 5.43 RSPI Timing (Master, CPHA = 0) and Simple SPI Timing (Master, CKPH = 1)

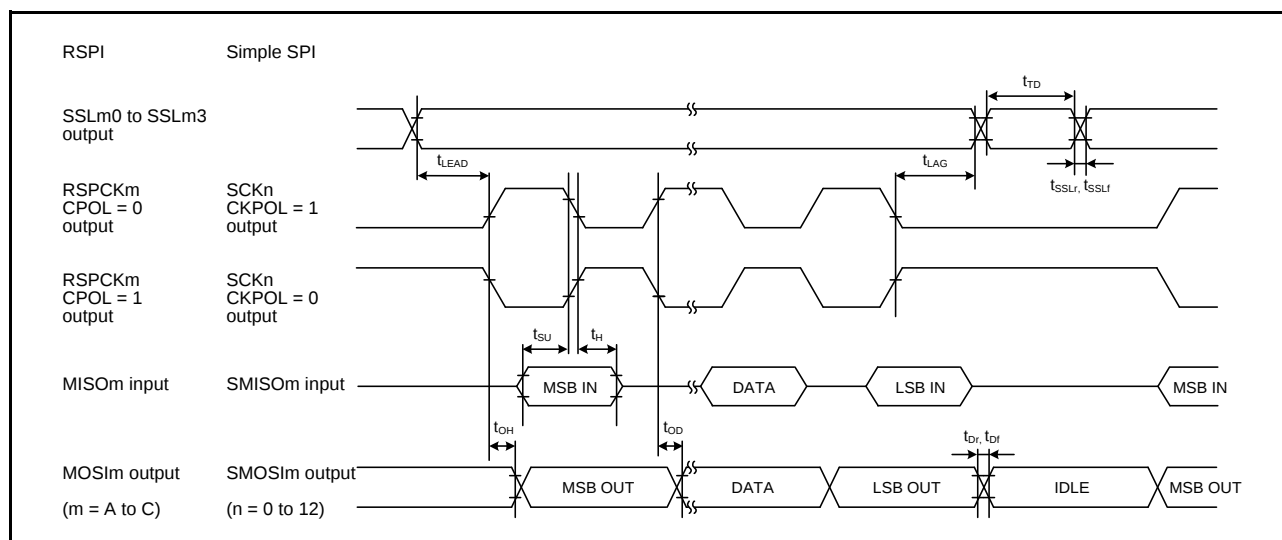


Figure 5.44 RSPI Timing (Master, CPHA = 1) and Simple SPI Timing (Master, CKPH = 0)

5.4 USB Characteristics

Table 5.27 On-Chip USB Full-Speed Characteristics (DP and DM Pin Characteristics)Conditions: $V_{CC} = AV_{CC0} = V_{REFH} = V_{CC_USB} = 3.0$ to 3.6 V, $V_{REFH0} = 3.0$ V to AV_{CC0} $V_{SS} = AV_{SS0} = V_{REFL}/V_{REFL0} = V_{SS_USB} = 0$ V $PCLK = 24$ to 50 MHz $T_a = T_{opr}$

High drive output is selected by the drive capacity control register.

Item		Symbol	Min.	Max.	Unit	Test Conditions	
Input characteristics	Input high level voltage	V_{IH}	2.0	—	V		
	Input low level voltage	V_{IL}	—	0.8	V		
	Differential input sensitivity	V_{DI}	0.2	—	V	DP – DM	
	Differential common mode range	V_{CM}	0.8	2.5	V		
Output characteristics	Output high level voltage	V_{OH}	2.8	3.6	V	$I_{OH} = -200 \mu A$	
	Output low level voltage	V_{OL}	0.0	0.3	V	$I_{OL} = 2$ mA	
	Cross-over voltage	V_{CRS}	1.3	2.0	V		Figure 5.61
	Rise time	t_{Lr}	4	20	ns		
	Fall time	t_{Lf}	4	20	ns		
	Rise/fall time ratio	t_{Lr} / t_{Lf}	90	111.11	%	t_{Lr} / t_{Lf}	
	Output resistance	Z_{DRV}	28	44	Ω	$R_s = 22 \Omega$ included	

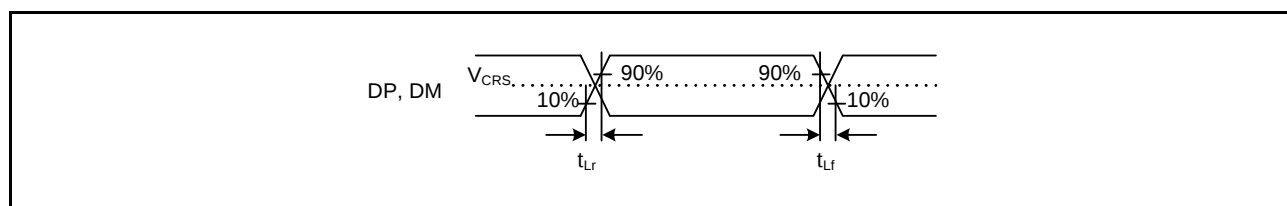
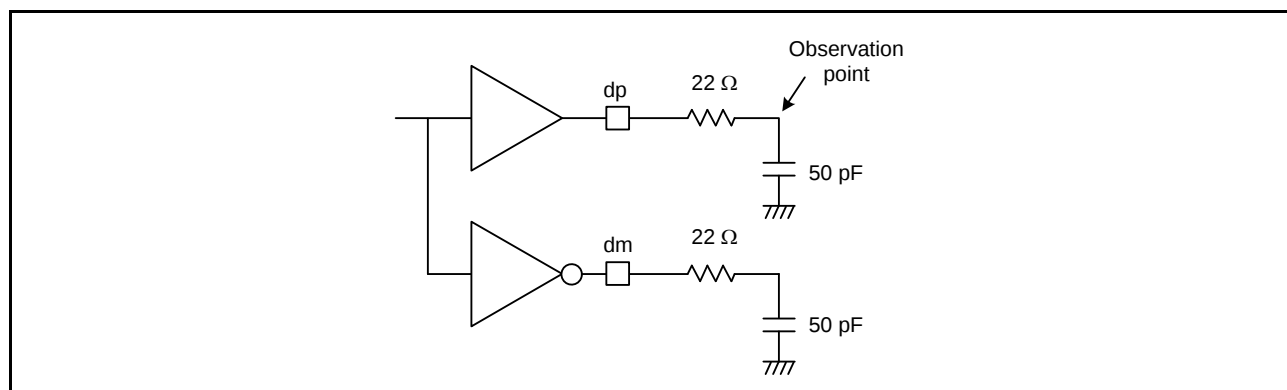
**Figure 5.61 DP and DM Output Timing (Full-Speed)****Figure 5.62 Test Circuit (Full-Speed)**

Table 5.29 12-Bit A/D Conversion CharacteristicsConditions: $V_{CC} = AVCC0 = VREFH = VCC_USB = 2.7$ to 3.6 V, $VREFH0 = 2.7$ V to $AVCC0$ $VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0$ V $PCLK = 8$ to 50 MHz $T_a = T_{opr}$

Item			Min.	Typ.	Max.	Unit	Test Conditions
Resolution			—	—	12	Bit	
Conversion time*1 (Operation at PCLK = 50 MHz)	AN0 to AN7	Permissible signal source impedance (max.) = 1.0 kΩ	1.0 (0.4)*2	—	—	μs	Sampling in 20 states
	Other channels	Permissible signal source impedance (max.) = 1.0 kΩ, AVCC ≥ 3.0 V	2.0 (1.4)*2	—	—	μs	Sampling in 70 states
		Permissible signal source impedance (max.) = 1.0 kΩ, AVCC ≥ 2.7 V	5.6 (5.0)*2	—	—	μs	Sampling in 250 states
Analog input capacitance			—	—	30	pF	
Offset error			—	±2.0	±7.5	LSB	
Full-scale error			—	±2.0	±7.5	LSB	
Quantization error			—	±0.5	—	LSB	
Absolute accuracy			—	±2.5	±8.0	LSB	
DNL differential nonlinearity error			—	±2.0	±4.0	LSB	
INL integral nonlinearity error			—	±2.0	±4.0	LSB	

Note: The above specification values apply when there is no access to the external bus during A/D conversion. If access proceeds during A/D conversion, values may not fall within the above ranges.

Note 1. The conversion time includes the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Note 2. The value in parentheses indicates the sampling time.

Table 5.30 A/D Internal Reference Voltage CharacteristicsConditions: $V_{CC} = AVCC0 = VREFH = VCC_USB = 2.7$ to 3.6 V, $VREFH0 = 2.7$ V to $AVCC0$ $VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0$ V $PCLK = 8$ to 50 MHz $T_a = T_{opr}$

Item	Min.	Typ.	Max.	Unit	Test Conditions
A/D Internal reference voltage	1.45	1.50	1.55	V	

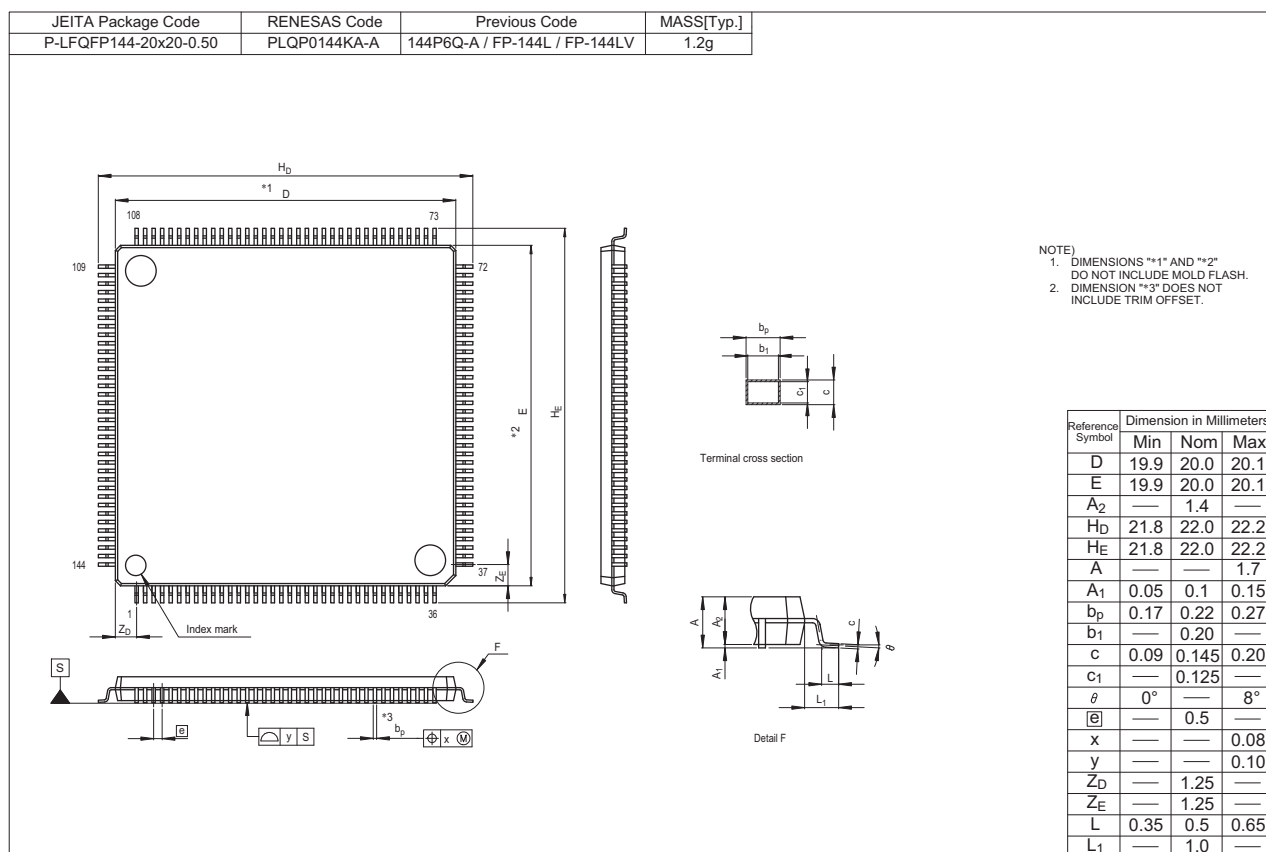


Figure E 144-pin LQFP (PLQP0144KA-A)

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