Renesas Electronics America Inc - R5F563NECDFB#V0 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, LINbus, SCI, SPI, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	111
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b, 21x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LFQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f563necdfb-v0

1. Overview

1.1 Outline of Specifications

Table 1.1 lists the specifications in outline, and table 1.2 gives a comparison of the functions of products in different packages.
Table 1.1 is for products with the greatest number of functions, so numbers of peripheral modules and channels will differ in accord with the package. For details, see Table 1.2, Comparison of Functions for Different Packages in the RX63N/RX631 Group.

Table 1.1 Outline of Specifications (1/6)

Classification	Module/Function	Description
CPU	CPU	• Maximum operating frequency: 100 MHz • 32-bit RX CPU • Minimum instruction execution time: One instruction per state (cycle of the system clock) • Address space: 4-Gbyte linear • Register set of the CPU General purpose: Sixteen 32-bit registers Control: Nine 32-bit registers Accumulator: One 64-bit register • Basic instructions: 73 • Floating-point instructions: 8 • DSP instructions: 9 • Addressing modes: 10 • Data arrangement Instructions: Little endian Data: Selectable as little endian or big endian • On-chip 32-bit multiplier: 32 x 32 → 64 bits • On-chip divider: 32 / 32 → 32 bits • Barrel shifter: 32 bits • Memory protection unit (MPU)
	FPU	• Single precision (32-bit) floating point • Data types and floating-point exceptions in conformance with the IEEE754 standard
Memory	ROM	• Capacity: ROMless, 256 Kbytes, 384 Kbytes, 512 Kbytes, 768 Kbytes, 1 Mbyte, 1.5 Mbytes, 2 Mbytes • 100 MHz, no-wait access • On-board programming: Four types • Off-board programming (parallel programmer mode) (for products with 100 pins or more)
	RAM	• Capacity: 64 Kbytes, 128 Kbytes, 192 Kbytes, 256 Kbytes • 100 MHz, no-wait access
	E2 data flash	Capacity: 32 Kbytes Programming/erasing: 100,000 times
MCU operating modes		Single-chip mode, on-chip ROM enabled expansion mode, and on-chip ROM disabled expansion mode (software switching)
Clock	Clock generation circuit	• Main clock oscillator, subclock oscillator, low-speed/high-speed on-chip oscillator, PLL frequency synthesizer, and IWDT-dedicated on-chip oscillator • Main-clock oscillation stoppage detection • Separate frequency-division and multiplication settings for the system clock (ICLK), peripheral module clock (PCLK), FlashIF clock (FCLK) and external bus clock (BCLK) The CPU and other bus masters run in synchronization with the system clock (ICLK): Up to 100 MHz Peripheral modules run in synchronization with the peripheral module clock (PCLK): Up to 50 MHz Flash IF run in synchronization with the flashIF clock (FCLK): Up to 50 MHz Devices connected to the external bus run in synchronization with the external bus clock (BCLK): Up to 50 MHz
Reset		RES# pin reset, power-on reset, voltage-monitoring reset, independent watchdog timer reset, watchdog timer reset, deep software standby reset, and software reset
Voltage detection circuit		When the voltage on VCC passes the voltage detection level (Vdet), an internal reset or internal interrupt is generated.

Table 1.1 Outline of Specifications (4/6)

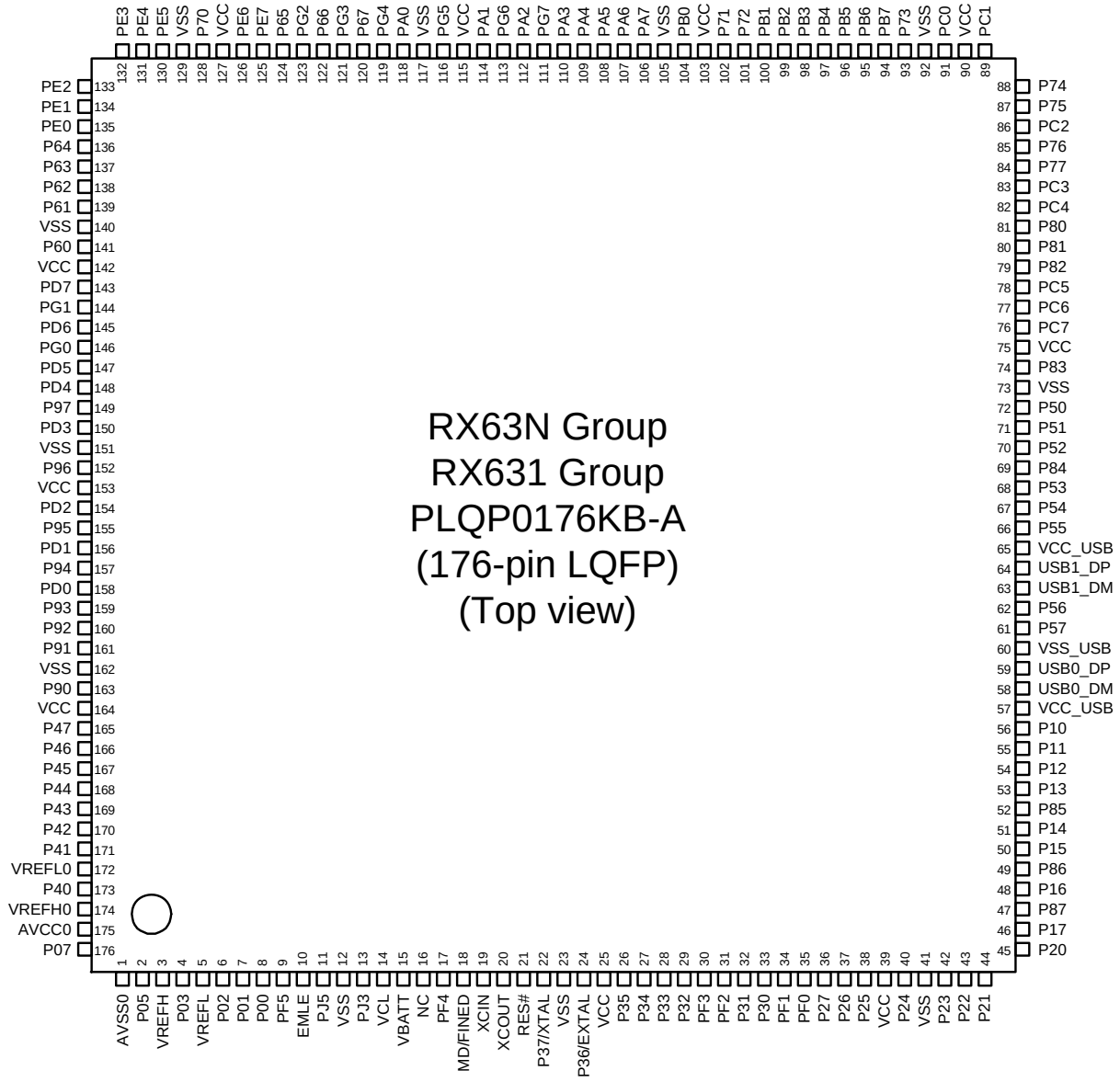
Classification	Module/Function	Description
Timers	16-bit timer pulse unit (TPUa)	• (16 bits x 6 channels) x 2 unit • Maximum of 16 pulse-input/output possible • Select from among seven or eight counter-input clock signals for each channel • Input capture/output compare function • Output of PWM waveforms in up to 15 phases in PWM mode • Buffered operation and phase-counting mode (two phase encoder input) depending on the channel • Support for cascade-connected operation (32 bits x 2 channels) • PPG output trigger can be generated • Capable of generating conversion start triggers for the A/D converters • Signals from the input capture pins are input via a digital filter • Clock frequency measuring method
	Multi-function timer pulse unit 2 (MTU2a)	• (16 bits x 6 channels) x 1 unit • Time bases for the 6 × 16-bit timer channels can be provided via up to sixteen pulse-input/output lines and three pulse-input lines • Select from among eight counter-input clock signals for each channel (PCLK/1, PCLK/4, PCLK/16, PCLK/64, MTCLKA, MTCLKB, MTCLKC, MTCLKD) other than channel 5, for which only four signals are available. • Input capture function • 21 output compare/input capture registers • Complementary PWM output mode • Reset synchronous PWM mode • Phase-counting mode • Generation of triggers for A/D converter conversion • Digital filter • Signals from the input capture pins are input via a digital filter • PPG output trigger can be generated • Clock frequency measuring function
	Frequency measuring method (MCK)	The MTU or unit 0 TPU module can be used to monitor the main clock, subclock, HOCO clock, LOCO clock, and PLL clock for abnormal frequencies.
	Port output enable 2 (POE2a)	Controls the high-impedance state of the MTU's waveform output pins
	Programmable pulse generator (PPG)	• (4 bits x 4 groups) x 2 units • Pulse output with the MTU2 or TPU output as a trigger • Maximum of 32 pulse-output possible
	8-bit timers (TMR)	• (8 bits x 2 channels) x 2 units • Select from among seven internal clock signals (PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1024, PCLK/8192) and one external clock signal • Capable of output of pulse trains with desired duty cycles or of PWM signals • The 2 channels of each unit can be cascaded to create a 16-bit timer • Generation of triggers for A/D converter conversion • Capable of generating baud-rate clocks for SCI5, SCI6, and SCI12
	Compare match timer (CMT)	• (16 bits x 2 channels) x 2 units • Select from among four internal clock signals (PCLK/8, PCLK/32, PCLK/128, PCLK/512)
	Realtime clock (RTCa)	• Clock sources: Main clock, subclock • Clock and calendar functions Interrupt sources: Alarm interrupt, periodic interrupt, and carry interrupt • Battery backup operation • Time-capture facility for three values
	Watchdog timer (WDTA)	• 14 bits x 1 channel • Select from among 6 counter-input clock signals (PCLK/4, PCLK/64, PCLK/128, PCLK/512, PCLK/2048, PCLK/8192)
	Independent watchdog timer (IWDTa)	• 14 bits x 1 channel • Counter-input clock: IWDT-dedicated on-chip oscillator • Dedicated clock/1, dedicated clock/16, dedicated clock/32, dedicated clock/64, dedicated clock/128, dedicated clock/256

1.2 List of Products

Table 1.3 is a list of products, and Figure 1.1 shows how to read the product part no.

Table 1.3 List of Products (1/8)

Group	Part No.	Package	ROM Capacity	RAM Capacity	E2 Data Flash	Operating Frequency (Max.)	Operating Temp. Range
RX63N (D version)	R5F563NECDLC	PTLG0177KA-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NEDDLC	PTLG0177KA-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NDCDLC	PTLG0177KA-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NDDDLC	PTLG0177KA-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NBCDLC	PTLG0177KA-A	1 Mbyte	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NBDDLC	PTLG0177KA-A	1 Mbyte	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NACDLC	PTLG0177KA-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NADDLC	PTLG0177KA-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NECDBG	PLBG0176GA-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NEDDBG	PLBG0176GA-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NDCDBG	PLBG0176GA-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NDDDBG	PLBG0176GA-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NBCDBG	PLBG0176GA-A	1 Mbyte	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NBDDBG	PLBG0176GA-A	1 Mbyte	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NACDBG	PLBG0176GA-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NADDBG	PLBG0176GA-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NFHDFC	PLQP0176KB-A	2 Mbytes	256 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NFDDFC	PLQP0176KB-A	2 Mbytes	256 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NKHDFC	PLQP0176KB-A*1	2 Mbytes	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NKDDFC	PLQP0176KB-A	2 Mbytes	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NECDFC	PLQP0176KB-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NEDDFC	PLQP0176KB-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NJHDFC	PLQP0176KB-A*1	1.5 Mbytes	256 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NJDDFC	PLQP0176KB-A*1	1.5 Mbytes	256 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NGHDFC	PLQP0176KB-A*1	1.5 Mbytes	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NGDDFC	PLQP0176KB-A*1	1.5 Mbytes	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NDCDFC	PLQP0176KB-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NDDDFC	PLQP0176KB-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NYHDFC	PLQP0176KB-A	1 Mbyte	256 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NYDDFC	PLQP0176KB-A	1 Mbyte	256 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NWHDFC	PLQP0176KB-A	1 Mbyte	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NWDDFC	PLQP0176KB-A	1 Mbyte	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NWGDFC	PLQP0176KB-A	1 Mbyte	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NWCDFC	PLQP0176KB-A	1 Mbyte	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NBCDFC	PLQP0176KB-A	1 Mbyte	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NBDDFC	PLQP0176KB-A	1 Mbyte	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NACDFC	PLQP0176KB-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NADDFC	PLQP0176KB-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NECDLK	PTLG0145KA-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NEDDLK	PTLG0145KA-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NDCDLK	PTLG0145KA-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C



Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.6, List of Pin and Pin Functions (176-Pin LQFP).

Figure 1.5 Pin Assignment (176-Pin LQFP)

Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (1/5)

Pin Number 177-Pin TFLGA 176-Pin LFBGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SCIc, SCId, RSPI, RIIC, CAN, IEB, USB, and PDC)	Interrupt	S12AD, AD, DA
A1	AVSS0						
A2	AVCC0						
A3	VREFL0						
A4		P42				IRQ10-DS	AN002
A5		P46				IRQ14-DS	AN006
A6	VCC						
A7	VSS						
A8		P94	A20/D20				
A9	VCC						
A10		P97	A23/D23				
A11		PD6	D6[A6/D6]	MTIC5V/POE1#	SSLC2	IRQ6	AN6
A12		P60	CS0#				
A13		P63	CS3#/CAS#				
A14		PE1	D9[A9/D9]	MTIOC4C/TIOCD9/PO18	TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12/SSLB2/RSPCKB		ANEX1
A15		PE2	D10[A10/D10]	MTIOC4A/TIOCA9/PO23	RXD12/SMISO12/ SSCL12/RXDX12/SSLB3/ MOSIB	IRQ7-DS	AN0
B1		P05				IRQ13	DA1
B2		P07				IRQ15	ADTRG0#
B3		P40				IRQ8-DS	AN000
B4		P41				IRQ9-DS	AN001
B5		P47				IRQ15-DS	AN007
B6		P91	A17/D17		SCK7		AN015
B7		P92	A18/D18		RXD7/SMISO7/SSCL7		AN016
B8		PD1	D1[A1/D1]	MTIOC4B/TIOCB7/ TCLKG	MOSIC/CTX0	IRQ1	AN009
B9		P96	A22/D22				
B10		PD4	D4[A4/D4]	POE3#	SSLC0	IRQ4	AN012
B11		PG1	D25				
B12	VSS						
B13		P64	CS4#/WE#				
B14		PE0	D8[A8/D8]	TIOCC9	SCK12/SSLB1		ANEX0
B15		PE3	D11[A11/D11]	MTIOC4B/TIOCB9/PO26/ POE8#	ET_ERXD3/CTS12#/ RTS12#/SS12#/MISOB		AN1
C1	VREFL						
C2	VREFH						
C3	VREFH0						
C4		P43				IRQ11-DS	AN003
C5		P45				IRQ13-DS	AN005
C6		P90	A16/D16		TXD7/SMOSI7/SSDA7		AN014
C7		PD0	D0[A0/D0]	TIOCA7		IRQ0	AN008
C8		PD2	D2[A2/D2]	MTIOC4D/TIOCA8	MISOC/CRX0	IRQ2	AN010
C9		PD3	D3[A3/D3]	TIOCB8/TCLKH/POE8#	RSPCKC	IRQ3	AN011
C10		PG0	D24				
C11	VCC						
C12		P62	CS2#/RAS#				
C13		PE4	D12[A12/D12]	MTIOC4D/MTIOC1A/ TIOCA10/PO28	ET_ERXD2/SSLB0		AN2

Table 1.7 List of Pins and Pin Functions (145-Pin TFLGA) (4/5)

Pin No. 145-pin TFLGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timers (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SCIc, SCId, RSPI, RIIC, CAN, IEB, USB, and PDC)	Interrupt	S12AD AD DA
L3		P16		MTIOC3C/MTIOC3D/ TIOCB1/TCLKC/TMO2/ PO14/RTCOUT	TXD1/RXD3/SMOSI1/ SMISO3/SSDA1/SSCL3/ MOSIA/SCL2-DS/IERXD/ USB0_VBUS/ USB0_VBUSEN/ USB0_OVRCURB	IRQ6	ADTRG0#
L4		P24	CS4#/EDREQ1	MTIOC4A/MTCLKA/ TIOCB4/TMRI1/PO4	SCK3/USB0_VBUSEN/ PIXCLK		
L5		P13		MTIOC0B/TIOCA5/ TMO3/PO13	TXD2/SMOSI2/SSDA2/ SDA0[FM+]	IRQ3	ADTRG#
L6		P56	EDACK1	MTIOC3C/TIOCA1			
L7		P52	RD#		RXD2/SMISO2/SSCL2/ SSLB3		
L8	TRCLK	P83	EDACK1	MTIOC4C	CTS10#/RTS10#/SS10#/ ET_CRS/RMII_CRS_DV		
L9		PC5	A21/CS2#/ WAIT#	MTIOC3B/MTCLKD/ TIOCD6/TCLKF/TMRI2/ PO29	SCK8/RSPCKA/ ET_ETXD2		
L10		PC4	A20/CS3#	MTIOC3D/MTCLKC/ TIOCC6/TCLKE/TMCI1/ PO25/POE0#	SCK5/CTS8#/RTS8#/ SS8#/SSLA0/ET_TX_CLK		
L11		PC2	A18	MTIOC4B/TCLKA/PO21	RXD5/SMISO5/SSCL5/ SSLA3/IERXD/ET_RX_DV		
L12		P73	CS3#	PO16	ET_WOL		
L13	VSS						
M1		P22	EDREQ0	MTIOC3B/MTCLKC/ TIOCC3/TMO0/PO2	SCK0/USB0_DRPD/PIXD6		
M2		P17		MTIOC3A/MTIOC3B/ TIOCB0/TCLKD/TMO1/ PO15/POE8#	SCK1/TXD3/SMOSI3/ SSDA3/MISOA/SDA2-DS/ IETXD/PIXD3	IRQ7	ADTRG#
M3		P86		TIOCA0	PIXD1		
M4		P12		TMCI1	RXD2/SMISO2/SSCL2/ SCL0[FM+]	IRQ2	
M5	VCC_USB						
M6	VSS_USB						
M7		P50	WR0#/WR#		TXD2/SMOSI2/SSDA2/ SSLB1		
M8		PC6	A22/CS1#	MTIOC3C/MTCLKA/ TIOCA6/TMCI2/PO30	RXD8/SMISO8/SSCL8/ MOSIA/ET_ETXD3	IRQ13	
M9	TRDATA1	P81	EDACK0	MTIOC3D/PO27	RXD10/SMISO10/SSCL10/ ET_ETXD0/RMII_TXD0		
M10		P77	CS7#	PO23	TXD11/SMOSI11/SSDA11/ ET_RX_ER/RMII_RX_ER		
M11		PC0	A16	MTIOC3C/TCLKC/PO17	CTS5#/RTS5#/SS5#/ SSLA1/SCL3/ET_ERXD3	IRQ14	
M12		PC1	A17	MTIOC3A/TCLKD/PO18	SCK5/SSLA2/SDA3/ ET_ERXD2	IRQ12	
M13	VCC						
N1		P21		MTIOC1B/TIOCA3/ TMCI0/PO1	RXD0/SMISO0/SSCL0/ SCL1/USB0_EXICEN/ PIXD5	IRQ9	
N2		P20		MTIOC1A/TIOCB3/ TMRI0/PO0	TXD0/SMOSI0/SSDA0/ SDA1/USB0_ID/PIXD4	IRQ8	
N3		P87		TIOCA2	PIXD2		
N4		P14		MTIOC3A/MTCLKA/ TIOCB5/TCLKA/TMRI2/ PO15	CTS1#/RTS1#/SS1#/ CTX1/USB0_DPUPE/ USB0_OVRCURA	IRQ4	
N5					USB0_DM		
N6					USB0_DP		

Table 1.8 List of Pins and Pin Functions (144-Pin LQFP) (5/5)

Pin No. 144-pin LQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timers (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SCIc, SCId, RSPI, RIIC, CAN, IEB, USB, and PDC)	Interrupt	S12AD AD DA
125		PD1	D1[A1/D1]	MTIOC4B/TIOCB7/ TCLKG	MOSIC/CTX0	IRQ1	AN009
126		PD0	D0[A0/D0]	TIOCA7		IRQ0	AN008
127		P93	A19		CTS7#/RTS7#/SS7#		AN017
128		P92	A18		RXD7/SMISO7/SSCL7		AN016
129		P91	A17		SCK7		AN015
130	VSS						
131		P90	A16		TXD7/SMOSI7/SSDA7		AN014
132	VCC						
133		P47				IRQ15-DS	AN007
134		P46				IRQ14-DS	AN006
135		P45				IRQ13-DS	AN005
136		P44				IRQ12-DS	AN004
137		P43				IRQ11-DS	AN003
138		P42				IRQ10-DS	AN002
139		P41				IRQ9-DS	AN001
140	VREFL0						
141		P40				IRQ8-DS	AN000
142	VREFH0						
143	AVCC0						
144		P07				IRQ15	ADTRG0#

Note 1. The BCLK function is multiplexed with the I/O port function for pin P53, so the port function is not available if the external bus is enabled.

Note 2. Enabled only for the ROM capacity: 2 Mbytes/1.5 Mbytes

Table 1.10 List of Pins and Pin Functions (100-Pin LQFP) (3/4)

Pin No. 100-pin LQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC	Timers (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SCIc, SCId, RSPI, RIIC, CAN, IEB, USB)	Interrupt	S12AD AD DA
59		PB1	A9	MTIOC0C/MTIOC4C/ TIOCB3/TMCI0/PO25	TXD6/SMOSI6/SSDA6/ ET_ERXD0/ RMII_RXD0	IRQ4-DS	
60	VCC						
61		PB0	A8	MTIC5W/TIOCA3/PO24	RXD6/SMISO6/SSCL6/ RSPCKA/ET_ERXD1/ RMII_RXD1	IRQ12	
62	VSS						
63		PA7	A7	TIOCB2/PO23	MISOA/ET_WOL		
64		PA6	A6	MTIC5V/MTCLKB/ TIOCA2/TMCI3/PO22/ POE2#	CTS5#/RTS5#/SS5#/ MOSIA/ET_EXOUT		
65		PA5	A5	TIOCB1/PO21	RSPCKA/ET_LINKSTA		
66		PA4	A4	MTIC5U/MTCLKA/ TIOCA1/TMRI0/PO20	TXD5/SMOSI5/SSDA5/ SSLA0/ET_MDC	IRQ5-DS	
67		PA3	A3	MTIOC0D/MTCLKD/ TIOCD0/TCLKB/PO19	RXD5/SMISO5/SSCL5/ ET_MDIO	IRQ6-DS	
68		PA2	A2	PO18	RXD5/SMISO5/SSCL5/ SSLA3		
69		PA1	A1	MTIOC0B/MTCLKC/ TIOCB0/PO17	SCK5/SSLA2/ET_WOL	IRQ11	
70		PA0	A0/BC0#	MTIOC4A/TIOCA0/ PO16	SSLA1/ET_TX_EN/ RMII_TXD_EN		
71		PE7	D15[A15/D15]		MISOB	IRQ7	AN5
72		PE6	D14[A14/D14]		MOSIB	IRQ6	AN4
73		PE5	D13[A13/D13]	MTIOC4C/MTIOC2B	RSPCKB/ET_RX_CLK/ REF50CK	IRQ5	AN3
74		PE4	D12[A12/D12]	MTIOC4D/MTIOC1A/ PO28	SSLB0/ET_ERXD2		AN2
75		PE3	D11[A11/D11]	MTIOC4B/PO26/POE8#	CTS12#/RTS12#/ SS12#/MISOB/ ET_ERXD3		AN1
76		PE2	D10[A10/D10]	MTIOC4A/PO23	RXD12/SMISO12/ SSCL12/RXDX12/ SSLB3/MOSIB	IRQ7-DS	AN0
77		PE1	D9[A9/D9]	MTIOC4C/PO18	TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12/SSLB2/ RSPCKB		ANEX1
78		PE0	D8[A8/D8]		SCK12/SSLB1		ANEX0
79		PD7	D7[A7/D7]	MTIC5U/POE0#		IRQ7	AN7
80		PD6	D6[A6/D6]	MTIC5V/POE1#		IRQ6	AN6
81		PD5	D5[A5/D5]	MTIC5W/POE2#		IRQ5	AN013
82		PD4	D4[A4/D4]	POE3#		IRQ4	AN012
83		PD3	D3[A3/D3]	POE8#		IRQ3	AN011
84		PD2	D2[A2/D2]	MTIOC4D	CRX0*1	IRQ2	AN010
85		PD1	D1[A1/D1]	MTIOC4B	CTX0*1	IRQ1	AN009
86		PD0	D0[A0/D0]			IRQ0	AN008
87		P47				IRQ15-DS	AN007
88		P46				IRQ14-DS	AN006
89		P45				IRQ13-DS	AN005
90		P44				IRQ12-DS	AN004
91		P43				IRQ11-DS	AN003
92		P42				IRQ10-DS	AN002
93		P41				IRQ9-DS	AN001

Table 1.12 List of Pins and Pin Functions (64-Pin LQFP) (3/3)

Pin Number 64-Pin LQFP	Power Supply Clock System Control	I/O Port	Timer (MTU2a, TPUa, TMR, PPG, RTCa, POE2a)	Timer Communications (SCIc, SCId, RSPI, RIIC, CAN, IEB, USB)	Interrupt	S12ADa, DAa
61	VREFH0					
62	AVCC0					
63		P05			IRQ13	DA1
64	AVSS0					

Table 4.1 List of I/O Registers (Address Order) (2/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 201Ch	DMAC0	DMA transfer enable register	DMCNT	8	8	2 ICLK		DMACA
0008 201Dh	DMAC0	DMA software start register	DMREQ	8	8	2 ICLK		DMACA
0008 201Eh	DMAC0	DMA status register	DMSTS	8	8	2 ICLK		
0008 201Fh	DMAC0	DMA activation source flag control register	DMCSL	8	8	2 ICLK		
0008 2040h	DMAC1	DMA source address register	DMSAR	32	32	2 ICLK		
0008 2044h	DMAC1	DMA destination address register	DMDAR	32	32	2 ICLK		
0008 2048h	DMAC1	DMA transfer count register	DMCRA	32	32	2 ICLK		
0008 204Ch	DMAC1	DMA block transfer count register	DMCRB	16	16	2 ICLK		
0008 2050h	DMAC1	DMA transfer mode register	DMTMD	16	16	2 ICLK		
0008 2053h	DMAC1	DMA interrupt setting register	DMINT	8	8	2 ICLK		
0008 2054h	DMAC1	DMA address mode register	DMAMD	16	16	2 ICLK		
0008 205Ch	DMAC1	DMA transfer enable register	DMCNT	8	8	2 ICLK		
0008 205Dh	DMAC1	DMA software start register	DMREQ	8	8	2 ICLK		
0008 205Eh	DMAC1	DMA status register	DMSTS	8	8	2 ICLK		
0008 205Fh	DMAC1	DMA activation source flag control register	DMCSL	8	8	2 ICLK		
0008 2080h	DMAC2	DMA source address register	DMSAR	32	32	2 ICLK		
0008 2084h	DMAC2	DMA destination address register	DMDAR	32	32	2 ICLK		
0008 2088h	DMAC2	DMA transfer count register	DMCRA	32	32	2 ICLK		
0008 208Ch	DMAC2	DMA block transfer count register	DMCRB	16	16	2 ICLK		
0008 2090h	DMAC2	DMA transfer mode register	DMTMD	16	16	2 ICLK		
0008 2093h	DMAC2	DMA interrupt setting register	DMINT	8	8	2 ICLK		
0008 2094h	DMAC2	DMA address mode register	DMAMD	16	16	2 ICLK		
0008 209Ch	DMAC2	DMA transfer enable register	DMCNT	8	8	2 ICLK		
0008 209Dh	DMAC2	DMA software start register	DMREQ	8	8	2 ICLK		
0008 209Eh	DMAC2	DMA status register	DMSTS	8	8	2 ICLK		
0008 209Fh	DMAC2	DMA activation source flag control register	DMCSL	8	8	2 ICLK		
0008 20C0h	DMAC3	DMA source address register	DMSAR	32	32	2 ICLK		
0008 20C4h	DMAC3	DMA destination address register	DMDAR	32	32	2 ICLK		
0008 20C8h	DMAC3	DMA transfer count register	DMCRA	32	32	2 ICLK		
0008 20CCh	DMAC3	DMA block transfer count register	DMCRB	16	16	2 ICLK		
0008 20D0h	DMAC3	DMA transfer mode register	DMTMD	16	16	2 ICLK		
0008 20D3h	DMAC3	DMA interrupt setting register	DMINT	8	8	2 ICLK		
0008 20D4h	DMAC3	DMA address mode register	DMAMD	16	16	2 ICLK		
0008 20DCh	DMAC3	DMA transfer enable register	DMCNT	8	8	2 ICLK		
0008 20DDh	DMAC3	DMA software start register	DMREQ	8	8	2 ICLK		
0008 20DEh	DMAC3	DMA status register	DMSTS	8	8	2 ICLK		
0008 20DFh	DMAC3	DMA activation source flag control register	DMCSL	8	8	2 ICLK		
0008 2200h	DMAC	DMACA module activation register	DMAST	8	8	2 ICLK		
0008 2400h	DTC	DTC control register	DTCCR	8	8	2 ICLK		DTCa
0008 2404h	DTC	DTC vector base register	DTCVBR	32	32	2 ICLK		
0008 2408h	DTC	DTC address mode register	DTCADMOD	8	8	2 ICLK		
0008 240Ch	DTC	DTC module start register	DTCST	8	8	2 ICLK		
0008 240Eh	DTC	DTC status register	DTCSTS	16	16	2 ICLK		
0008 2800h	EXDMAC0	EXDMA source address register	EDMSAR	32	32	1, 2 BCLK		EXDMACa
0008 2804h	EXDMAC0	EXDMA destination address register	EDMDAR	32	32	1, 2 BCLK		
0008 2808h	EXDMAC0	EXDMA transfer count register	EDMCRA	32	32	1, 2 BCLK		
0008 280Ch	EXDMAC0	EXDMA block transfer count register	EDMCRB	16	16	1, 2 BCLK		
0008 2810h	EXDMAC0	EXDMA transfer mode register	EDMTMD	16	16	1, 2 BCLK		
0008 2812h	EXDMAC0	EXDMA output setting register	EDMOMD	8	8	1, 2 BCLK		
0008 2813h	EXDMAC0	EXDMA interrupt setting register	EDMINT	8	8	1, 2 BCLK		
0008 2814h	EXDMAC0	EXDMA address mode register	EDMAMD	32	32	1, 2 BCLK		

Table 4.1 List of I/O Registers (Address Order) (11/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 71EEh	ICU	DTC activation enable register 238	DTCER238	8	8	2 ICLK		ICUb
0008 71EFh	ICU	DTC activation enable register 239	DTCER239	8	8	2 ICLK		
0008 71F1h	ICU	DTC activation enable register 241	DTCER241	8	8	2 ICLK		
0008 71F2h	ICU	DTC activation enable register 242	DTCER242	8	8	2 ICLK		
0008 71F4h	ICU	DTC activation enable register 244	DTCER244	8	8	2 ICLK		
0008 71F5h	ICU	DTC activation enable register 245	DTCER245	8	8	2 ICLK		
0008 71F7h	ICU	DTC activation enable register 247	DTCER247	8	8	2 ICLK		
0008 71F8h	ICU	DTC activation enable register 248	DTCER248	8	8	2 ICLK		
0008 71FAh	ICU	DTC activation enable register 250	DTCER250	8	8	2 ICLK		
0008 71FBh	ICU	DTC activation enable register 251	DTCER251	8	8	2 ICLK		
0008 7202h	ICU	Interrupt request enable register 02	IER02	8	8	2 ICLK		
0008 7203h	ICU	Interrupt request enable register 03	IER03	8	8	2 ICLK		
0008 7204h	ICU	Interrupt request enable register 04	IER04	8	8	2 ICLK		
0008 7205h	ICU	Interrupt request enable register 05	IER05	8	8	2 ICLK		
0008 7206h	ICU	Interrupt request enable register 06	IER06	8	8	2 ICLK		
0008 7207h	ICU	Interrupt request enable register 07	IER07	8	8	2 ICLK		
0008 7208h	ICU	Interrupt request enable register 08	IER08	8	8	2 ICLK		
0008 7209h	ICU	Interrupt request enable register 09	IER09	8	8	2 ICLK		
0008 720Bh	ICU	Interrupt request enable register 0B	IER0B	8	8	2 ICLK		
0008 720Ch	ICU	Interrupt request enable register 0C	IER0C	8	8	2 ICLK		
0008 720Dh	ICU	Interrupt request enable register 0D	IER0D	8	8	2 ICLK		
0008 720Eh	ICU	Interrupt request enable register 0E	IER0E	8	8	2 ICLK		
0008 720Fh	ICU	Interrupt request enable register 0F	IER0F	8	8	2 ICLK		
0008 7210h	ICU	Interrupt request enable register 10	IER10	8	8	2 ICLK		
0008 7211h	ICU	Interrupt request enable register 11	IER11	8	8	2 ICLK		
0008 7212h	ICU	Interrupt request enable register 12	IER12	8	8	2 ICLK		
0008 7213h	ICU	Interrupt request enable register 13	IER13	8	8	2 ICLK		
0008 7214h	ICU	Interrupt request enable register 14	IER14	8	8	2 ICLK		
0008 7215h	ICU	Interrupt request enable register 15	IER15	8	8	2 ICLK		
0008 7216h	ICU	Interrupt request enable register 16	IER16	8	8	2 ICLK		
0008 7217h	ICU	Interrupt request enable register 17	IER17	8	8	2 ICLK		
0008 7218h	ICU	Interrupt request enable register 18	IER18	8	8	2 ICLK		
0008 7219h	ICU	Interrupt request enable register 19	IER19	8	8	2 ICLK		
0008 721Ah	ICU	Interrupt request enable register 1A	IER1A	8	8	2 ICLK		
0008 721Bh	ICU	Interrupt request enable register 1B	IER1B	8	8	2 ICLK		
0008 721Ch	ICU	Interrupt request enable register 1C	IER1C	8	8	2 ICLK		
0008 721Dh	ICU	Interrupt request enable register 1D	IER1D	8	8	2 ICLK		
0008 721Eh	ICU	Interrupt request enable register 1E	IER1E	8	8	2 ICLK		
0008 721Fh	ICU	Interrupt request enable register 1F	IER1F	8	8	2 ICLK		
0008 72E0h	ICU	Software interrupt activation register	SWINTR	8	8	2 ICLK		
0008 72F0h	ICU	Fast interrupt set register	FIR	16	16	2 ICLK		
0008 7300h	ICU	Interrupt source priority register 000	IPR000	8	8	2 ICLK		
0008 7301h	ICU	Interrupt source priority register 001	IPR001	8	8	2 ICLK		
0008 7302h	ICU	Interrupt source priority register 002	IPR002	8	8	2 ICLK		
0008 7303h	ICU	Interrupt source priority register 003	IPR003	8	8	2 ICLK		
0008 7304h	ICU	Interrupt source priority register 004	IPR004	8	8	2 ICLK		
0008 7305h	ICU	Interrupt source priority register 005	IPR005	8	8	2 ICLK		
0008 7306h	ICU	Interrupt source priority register 006	IPR006	8	8	2 ICLK		
0008 7307h	ICU	Interrupt source priority register 007	IPR007	8	8	2 ICLK		
0008 7320h	ICU	Interrupt source priority register 032	IPR032	8	8	2 ICLK		
0008 7321h	ICU	Interrupt source priority register 033	IPR033	8	8	2 ICLK		

Table 4.1 List of I/O Registers (Address Order) (23/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 8800h	MTU2	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK	MTU2a
0008 8801h	MTU2	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK	
0008 8802h	MTU2	Timer I/O control register	TIOR	8	8	2, 3 PCLKB	2 ICLK	
0008 8804h	MTU2	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK	
0008 8805h	MTU2	Timer status register	TSR	8	8	2, 3 PCLKB	2 ICLK	
0008 8806h	MTU2	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	
0008 8808h	MTU2	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	
0008 880Ah	MTU2	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	
0008 8880h	MTU5	Timer counter U	TCNTU	16	16	2, 3 PCLKB	2 ICLK	
0008 8882h	MTU5	Timer general register U	TGRU	16	16	2, 3 PCLKB	2 ICLK	
0008 8884h	MTU5	Timer control register U	TCRU	8	8	2, 3 PCLKB	2 ICLK	
0008 8886h	MTU5	Timer I/O control register U	TIORU	8	8	2, 3 PCLKB	2 ICLK	
0008 8890h	MTU5	Timer counter V	TCNTV	16	16	2, 3 PCLKB	2 ICLK	
0008 8892h	MTU5	Timer general register V	TGRV	16	16	2, 3 PCLKB	2 ICLK	
0008 8894h	MTU5	Timer control register V	TCRV	8	8	2, 3 PCLKB	2 ICLK	
0008 8896h	MTU5	Timer I/O control register V	TIORV	8	8	2, 3 PCLKB	2 ICLK	
0008 88A0h	MTU5	Timer counter W	TCNTW	16	16	2, 3 PCLKB	2 ICLK	
0008 88A2h	MTU5	Timer general register W	TGRW	16	16	2, 3 PCLKB	2 ICLK	
0008 88A4h	MTU5	Timer control register W	TCRW	8	8	2, 3 PCLKB	2 ICLK	
0008 88A6h	MTU5	Timer I/O control register W	TIORW	8	8	2, 3 PCLKB	2 ICLK	
0008 88B2h	MTU5	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK	
0008 88B4h	MTU5	Timer start register	TSTR	8	8	2, 3 PCLKB	2 ICLK	
0008 88B6h	MTU5	Timer compare match clear register	TCNTCMPCLR	8	8	2, 3 PCLKB	2 ICLK	
0008 8900h	POE	Input level control/status register 1	ICSR1	16	16	2, 3 PCLKB	2 ICLK	POE2a
0008 8902h	POE	Output level control/status register 1	OCSR1	16	16	2, 3 PCLKB	2 ICLK	
0008 8908h	POE	Input level control/status register 2	ICSR2	16	16	2, 3 PCLKB	2 ICLK	
0008 890Ah	POE	Software port output enable register	SPOER	8	8	2, 3 PCLKB	2 ICLK	
0008 890Bh	POE	Port output enable control register 1	POECR1	8	8	2, 3 PCLKB	2 ICLK	
0008 890Ch	POE	Port output enable control register 2	POECR2	8	8	2, 3 PCLKB	2 ICLK	
0008 890Eh	POE	Input level control/status register 3	ICSR3	16	16	2, 3 PCLKB	2 ICLK	
0008 9000h	S12AD	A/D control register	ADCSR	8	8	2, 3 PCLKB	2 ICLK	S12ADa
0008 9004h	S12AD	A/D channel select register 0	ADANS0	16	16	2, 3 PCLKB	2 ICLK	
0008 9006h	S12AD	A/D channel select register 1	ADANS1	16	16	2, 3 PCLKB	2 ICLK	
0008 9008h	S12AD	A/D-converted value addition mode select register 0	ADADS0	16	16	2, 3 PCLKB	2 ICLK	
0008 900Ah	S12AD	A/D-converted value addition mode select register 1	ADADS1	16	16	2, 3 PCLKB	2 ICLK	
0008 900Ch	S12AD	A/D-converted value addition count select register	ADADC	8	8	2, 3 PCLKB	2 ICLK	
0008 900Eh	S12AD	A/D control extended register	ADCER	16	16	2, 3 PCLKB	2 ICLK	
0008 9010h	S12AD	A/D start trigger select register	ADSTRGR	8	8	2, 3 PCLKB	2 ICLK	
0008 9012h	S12AD	A/D conversion extended input control register	ADEXICR	16	16	2, 3 PCLKB	2 ICLK	
0008 901Ah	S12AD	A/D temperature sensor data register	ADTSDR	16	16	2, 3 PCLKB	2 ICLK	
0008 901Ch	S12AD	A/D internal reference voltage data register	ADOCDR	16	16	2, 3 PCLKB	2 ICLK	
0008 9020h	S12AD	A/D data register 0	ADDR0	16	16	2, 3 PCLKB	2 ICLK	
0008 9022h	S12AD	A/D data register 1	ADDR1	16	16	2, 3 PCLKB	2 ICLK	
0008 9024h	S12AD	A/D data register 2	ADDR2	16	16	2, 3 PCLKB	2 ICLK	
0008 9026h	S12AD	A/D data register 3	ADDR3	16	16	2, 3 PCLKB	2 ICLK	
0008 9028h	S12AD	A/D data register 4	ADDR4	16	16	2, 3 PCLKB	2 ICLK	
0008 902Ah	S12AD	A/D data register 5	ADDR5	16	16	2, 3 PCLKB	2 ICLK	
0008 902Ch	S12AD	A/D data register 6	ADDR6	16	16	2, 3 PCLKB	2 ICLK	
0008 902Eh	S12AD	A/D data register 7	ADDR7	16	16	2, 3 PCLKB	2 ICLK	
0008 9030h	S12AD	A/D data register 8	ADDR8	16	16	2, 3 PCLKB	2 ICLK	
0008 9032h	S12AD	A/D data register 9	ADDR9	16	16	2, 3 PCLKB	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (25/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 A02Bh	SCI1	I²C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK	SCIc, SCId
0008 A02Ch	SCI1	I²C status register	SISR	8	8	2, 3 PCLKB	2 ICLK	
0008 A02Dh	SCI1	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A040h	SCI2	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A041h	SCI2	Bit rate register	BRR	8	8	2, 3 PCLKB	2 ICLK	
0008 A042h	SCI2	Serial control register	SCR	8	8	2, 3 PCLKB	2 ICLK	
0008 A043h	SCI2	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK	
0008 A044h	SCI2	Serial status register	SSR	8	8	2, 3 PCLKB	2 ICLK	
0008 A045h	SCI2	Receive data register	RDR	8	8	2, 3 PCLKB	2 ICLK	
0008 A046h	SCI2	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A047h	SCI2	Serial extended mode register	SEM	8	8	2, 3 PCLKB	2 ICLK	
0008 A048h	SCI2	Noise filter setting register	SNFR2	8	8	2, 3 PCLKB	2 ICLK	
0008 A049h	SCI2	I²C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK	
0008 A04Ah	SCI2	I²C mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK	
0008 A04Bh	SCI2	I²C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK	
0008 A04Ch	SCI2	I²C status register	SISR	8	8	2, 3 PCLKB	2 ICLK	
0008 A04Dh	SCI2	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A060h	SCI3	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A061h	SCI3	Bit rate register	BRR	8	8	2, 3 PCLKB	2 ICLK	
0008 A062h	SCI3	Serial control register	SCR	8	8	2, 3 PCLKB	2 ICLK	
0008 A063h	SCI3	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK	
0008 A064h	SCI3	Serial status register	SSR	8	8	2, 3 PCLKB	2 ICLK	
0008 A065h	SCI3	Receive data register	RDR	8	8	2, 3 PCLKB	2 ICLK	
0008 A066h	SCI3	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A067h	SCI3	Serial extended mode register	SEMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A068h	SCI3	Noise filter setting register	SNFR	8	8	2, 3 PCLKB	2 ICLK	
0008 A069h	SCI3	I²C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK	
0008 A06Ah	SCI3	I²C mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK	
0008 A06Bh	SCI3	I²C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK	
0008 A06Ch	SCI3	I²C status register	SISR	8	8	2, 3 PCLKB	2 ICLK	
0008 A06Dh	SCI3	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A080h	SCI4	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A081h	SCI4	Bit rate register	BRR	8	8	2, 3 PCLKB	2 ICLK	
0008 A082h	SCI4	Serial control register	SCR	8	8	2, 3 PCLKB	2 ICLK	
0008 A083h	SCI4	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK	
0008 A084h	SCI4	Serial status register	SSR	8	8	2, 3 PCLKB	2 ICLK	
0008 A085h	SCI4	Receive data register	RDR	8	8	2, 3 PCLKB	2 ICLK	
0008 A086h	SCI4	Smart card mode register	SCMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A087h	SCI4	Serial extended mode register	SEMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A088h	SCI4	Noise filter setting register	SNFR	8	8	2, 3 PCLKB	2 ICLK	
0008 A089h	SCI4	I²C mode register 1	SIMR1	8	8	2, 3 PCLKB	2 ICLK	
0008 A08Ah	SCI4	I²C mode register 2	SIMR2	8	8	2, 3 PCLKB	2 ICLK	
0008 A08Bh	SCI4	I²C mode register 3	SIMR3	8	8	2, 3 PCLKB	2 ICLK	
0008 A08Ch	SCI4	I²C status register	SISR	8	8	2, 3 PCLKB	2 ICLK	
0008 A08Dh	SCI4	SPI mode register	SPMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0A0h	SCI5	Serial mode register	SMR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0A1h	SCI5	Bit rate register	BRR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0A2h	SCI5	Serial control register	SCR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0A3h	SCI5	Transmit data register	TDR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0A4h	SCI5	Serial status register	SSR	8	8	2, 3 PCLKB	2 ICLK	
0008 A0A5h	SCI5	Receive data register	RDR	8	8	2, 3 PCLKB	2 ICLK	

Table 5.3 DC Characteristics (2)

Conditions: VCC = AVCC0 = VREFH = VCC_USB = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0,
VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V, $T_a = T_{opr}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Output high voltage	All output pins	V_{OH}	VCC – 0.5	—	—	V	I_{OH} = –1 mA
Output low voltage	All output pins (except for RIIC pins, and ETHERC)	V_{OL}	—	—	0.5	V	I_{OL} = 1.0 mA
	RIIC pins		—	—	0.4	V	I_{OL} = 3.0 mA
			—	—	0.6		I_{OL} = 6.0 mA
	RIIC pins (only P12 and P13 in channel 0)	V_{OL}	—	—	0.4	V	I_{OL} = 15.0 mA (ICFER.FMPE = 1)
			—	0.4	—		I_{OL} = 20.0 mA (ICFER.FMPE = 1)
	ETHERC	V_{OL}	—	—	0.4	V	I_{OL} = 1.0 mA
Input leakage current	RES#, MD pin, EMLE*1, NMI	$\lvert I_{in} \rvert$	—	—	1.0	µA	V_{in} = 0 V V_{in} = VCC
Three-state leakage current (off state)	Other than ports for 5 V tolerant	$\lvert I_{TSI} \rvert$	—	—	1.0	µA	V_{in} = 0 V V_{in} = VCC
	Ports for 5 V tolerant		—	—	5.0		Vin = 0 V Vin = 5.5 V
Input pull-up MOS current	Ports 0 to 2, 30 to 34, 36, 37, 4 to G, J3, J5	I_p	–10	—	–300	µA	VCC= 2.7 to 3.6 V V_{in} = 0 V
Input capacitance	All input pins (except for ports 12, 13, 16, 17, 20, 21, 4, C0, C1, and EMLE)	C_{in}	—	—	15	pF	V_{in} = 0 V f = 1 MHz T_a = 25°C
	Ports 12, 13, 16, 17, 20, 21, 4, C0, C1, EMLE		—	—	30		
Input pull-down MOS current	EMLE, BSCANP	I_p	10	—	300	µA	V_{in} = VCC

Note 1. The input leakage current value at the EMLE pin is only when V_{in} = 0 V.

Table 5.4 DC Characteristics (3) (for D and G Versions (-40 ≤ Ta ≤ +85°C))

Conditions: VCC = AVCC0 = VREFH = VCC_USB = V_{BATT} = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0,
VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V, $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
RAM standby voltage	V_{RAM}	2.7	—	—	V	
VCC rising gradient	SrVCC	8.4	—	20000	µs/V	
VCC falling gradient*8	SfVCC	8.4	—	—	µs/V	

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. Measured with clocks supplied to the peripheral functions. This does not include the BGO operation.
Note 3. I_{CC} depends on f (ICLK) as follows. (ICLK:PCLK:BCLK:BCLK pin = 8:4:4:2)
I_{CC} Max. = 0.87 × f + 13 (max. operation in high-speed operating mode)
I_{CC} Typ. = 0.35 × f + 5 (normal operation in high-speed operating mode)
I_{CC} Typ. = 1.0 × f + 3 (low-speed operating mode 1)
I_{CC} Max. = 0.53 × f + 12 (sleep mode)
Note 4. This does not include the BGO operation.
Note 5. This is the increase for programming or erasure of the ROM or flash memory for data storage during program execution.
Note 6. Supply of the clock signal to peripherals is stopped in this state. This does not include the BGO operation.
Note 7. The reference power supply current is included in the power supply current value for 10-bit A/D conversion and D/A conversion.
Note 8. When V_{BATT} is used
Note 9. The current values for 10-bit A/D converter and 10-bit D/A converter are included in the current from the VREFH pin.
Note 10. The values are the sum of I_{AVCC0} and I_{VREFH}.

Table 5.6 DC Characteristics (4)

Conditions: VCC = AVCC0 = VREFH = VCC_USB = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0,
VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V, $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Permissible total power consumption*1	P_d	—	—	380	mW	*2

Note 1. This is the total power consumption of the chip as a whole (including the power consumed by the output buffers).
Note 2. Contact a Renesas sales office or agent regarding further details of the conditions of measurement.

Table 5.7 Permissible Output Currents

Conditions: VCC = AVCC0 = VREFH = VCC_USB = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0,
VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V, $T_a = T_{opr}$

Item			Symbol	Min.	Typ.	Max.	Unit
Permissible output low current (average value per pin)	All output pins*1	Normal drive	I_{OL}	—	—	2.0	mA
	All output pins*2	High drive	I_{OL}			3.8	mA
Permissible output low current (max. value per pin)	All output pins*1	Normal drive	I_{OL}	—	—	4.0	mA
	All output pins*2	High drive	I_{OL}			7.6	mA
Permissible output low current (total)	Total of all output pins		ΣI_{OL}	—	—	80	mA
Permissible output high current (average value per pin)	All output pins*1	Normal drive	I_{OH}	—	—	–2.0	mA
	USB_DPUPE pin*2	High drive	I_{OH}	—	—	–3.8	mA
Permissible output high current (max. value per pin)	All output pins*1	Normal drive	I_{OH}	—	—	–4.0	mA
	All output pins*2	High drive	I_{OH}	—	—	–7.6	mA
Permissible output high current (total)	Total of all output pins		ΣI_{OH}	—	—	–80	mA

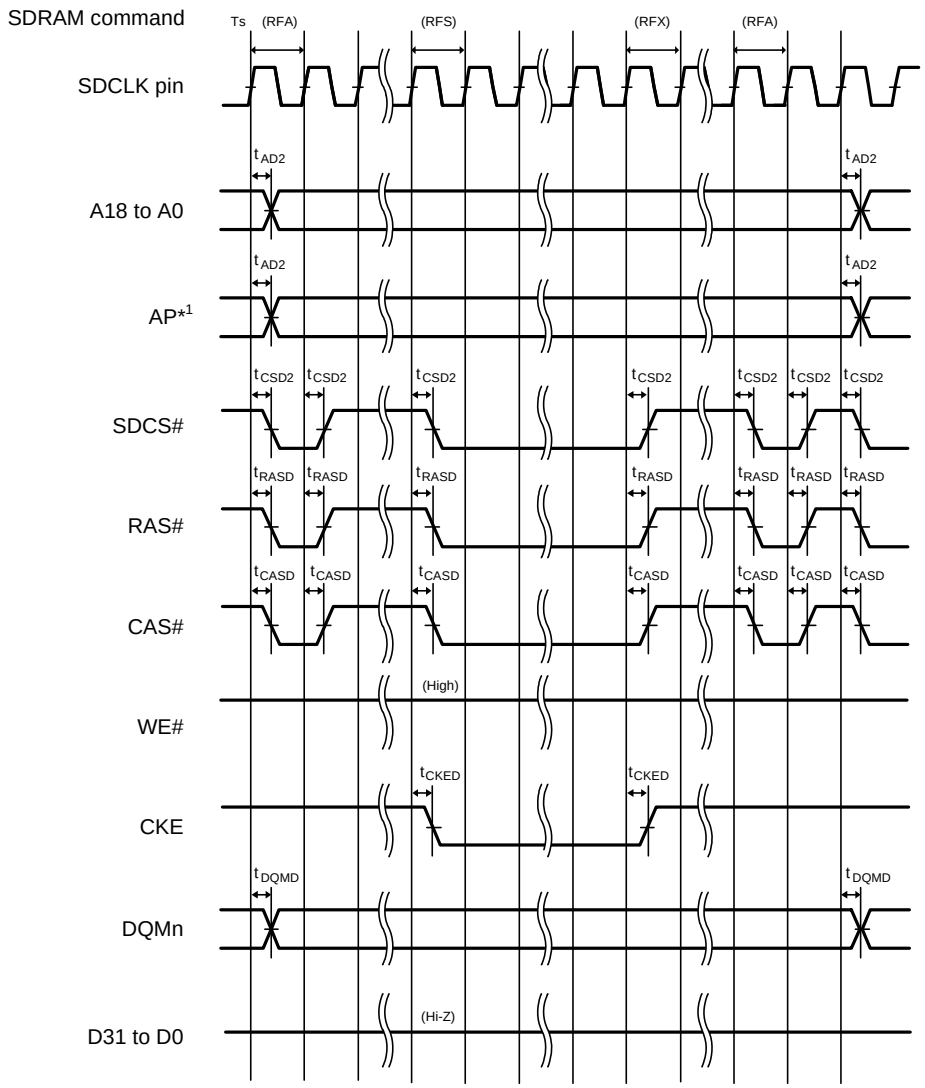
Caution: To protect the LSI's reliability, the output current values should not exceed the values in this table.
Note 1. This is the value when normal driving ability is set with a pin for which normal driving ability is selectable.
Note 2. This is the value when high driving ability is set with a pin for which normal driving ability is selectable or the value of the pin to which high driving ability is fixed.

5.3.5 Bus Timing

Table 5.16 Bus Timing (packages with 177 to 144 pins)

Conditions: VCC = AVCC0 = VREFH = VCC_USB = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0,
VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V,
ICLK = 8 to 100 MHz, BCLK pin = 8 to 50 MHz, SDCLK pin = 8 to 50MHz, $T_a = T_{opr}$
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, I_{OH} = -1.0 mA, I_{OL} = 1.0 mA, C = 30 pF
High drive output is selected by the drive capacity control register.

Item	Symbol	Min.	Max.	Unit	Test Conditions
Address delay time	t_{AD}	—	15	ns	Figure 5.17 to Figure 5.22
Byte control delay time	t_{BCD}	—	15	ns	
CS# delay time	t_{CSD}	—	15	ns	
ALE delay time	t_{ALED}	—	20	ns	
RD# delay time	t_{RSD}	—	15	ns	
Read data setup time	t_{RDS}	15	—	ns	
Read data hold time	t_{RDH}	0	—	ns	
WR# delay time	t_{WRD}	—	15	ns	
Write data delay time	t_{WDD}	—	15	ns	
Write data hold time	t_{WDH}	0	—	ns	
WAIT# setup time	t_{WTS}	15	—	ns	Figure 5.23
WAIT# hold time	t_{WTH}	0	—	ns	
Address delay time 2 (SDRAM)	t_{AD2}	1	15	ns	Figure 5.24 to Figure 5.30
CS# delay time 2 (SDRAM)	t_{CSD2}	1	15	ns	
DQM delay time (SDRAM)	t_{DQMD}	1	15	ns	
CKE delay time (SDRAM)	t_{CKED}	1	15	ns	
Read data setup time 2 (SDRAM)	t_{RDS2}	12	—	ns	
Read data hold time 2 (SDRAM)	t_{RDH2}	0	—	ns	
Write data delay time 2 (SDRAM)	t_{WDD2}	—	15	ns	
Write data hold time 2 (SDRAM)	t_{WDH2}	1	—	ns	
WE# delay time (SDRAM)	t_{WED}	1	15	ns	
RAS# delay time (SDRAM)	t_{RASD}	1	15	ns	
CAS# delay time (SDRAM)	t_{CASD}	1	15	ns	



Note 1: Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

Figure 5.30 SDRAM Space Self-Refresh Bus Timing

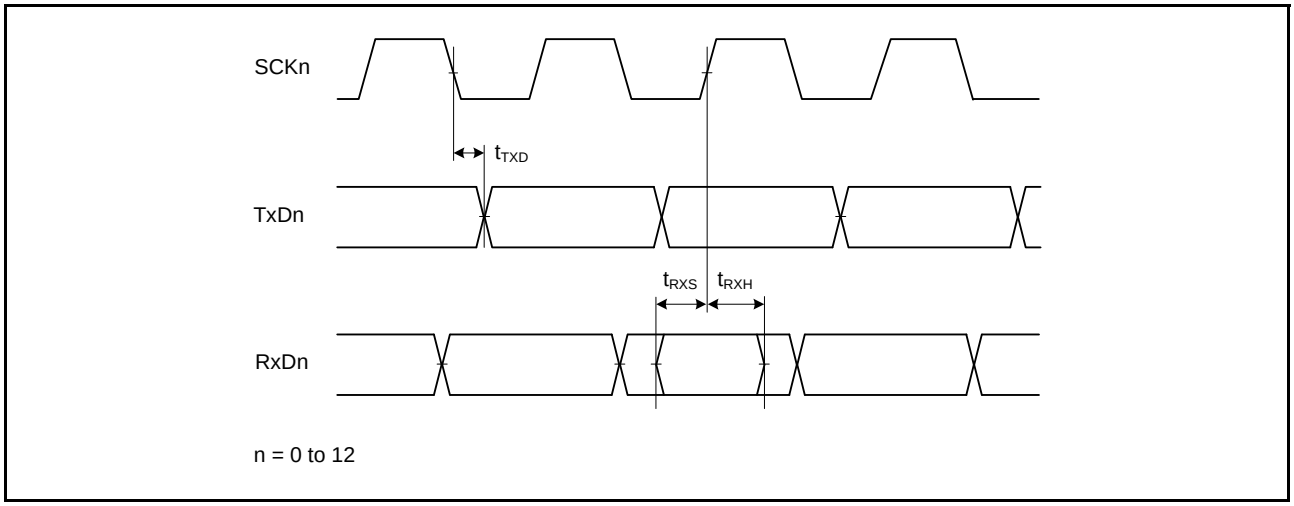


Figure 5.40 SCI Input/Output Timing: Clock Synchronous Mode

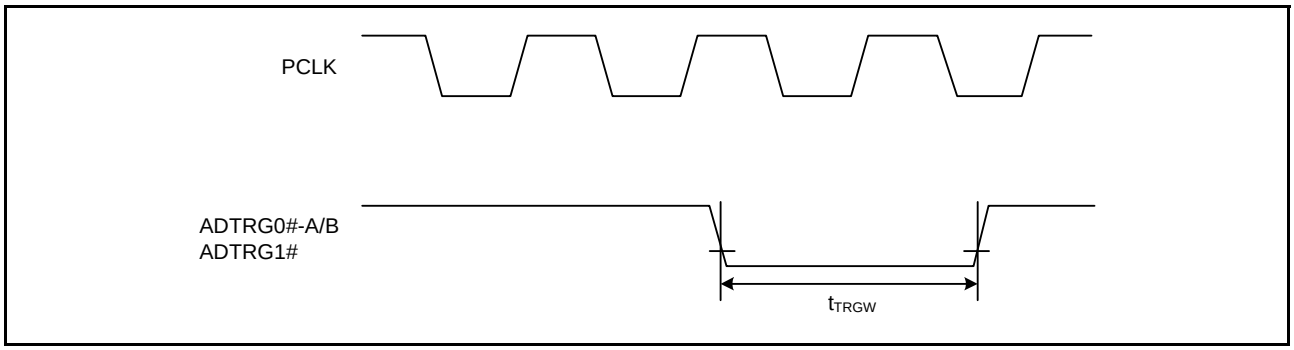


Figure 5.41 A/D Converter External Trigger Input Timing

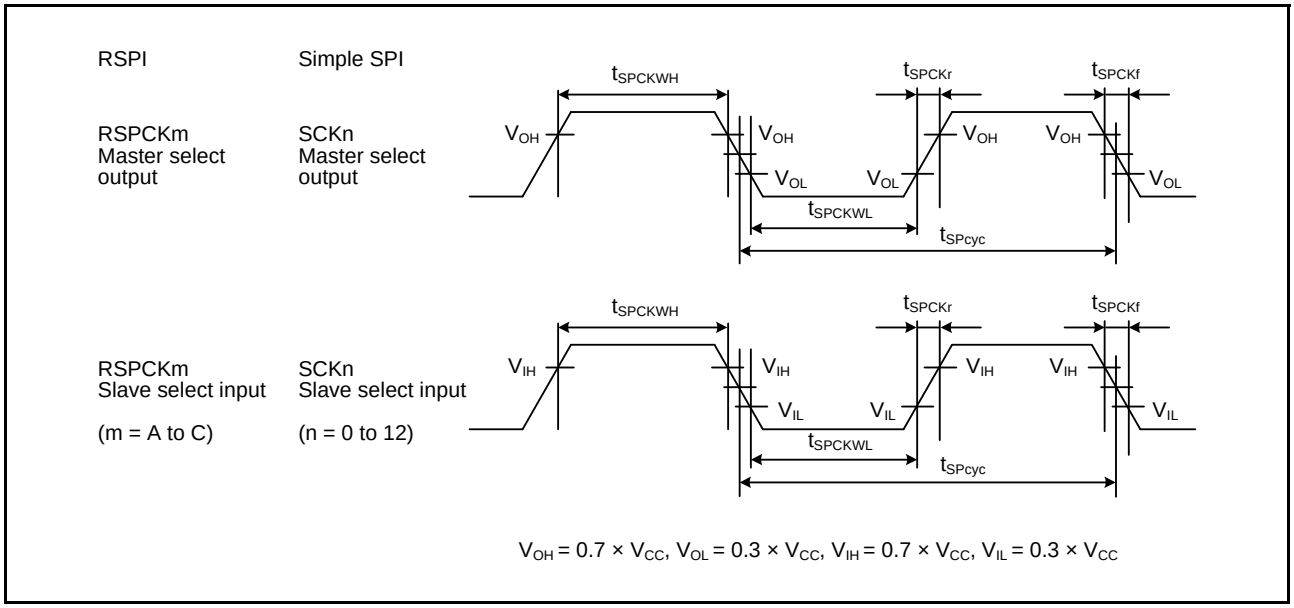
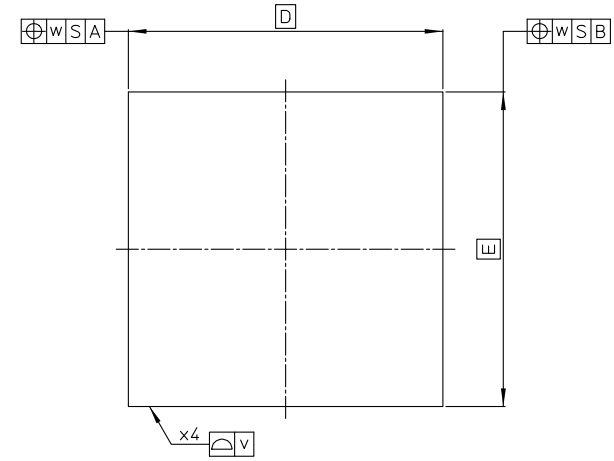
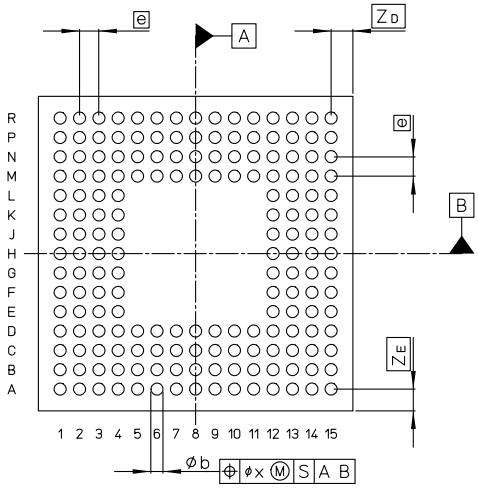


Figure 5.42 RSPI Clock Timing and Simple SPI Clock Timing

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFBGA176-13x13-0.80	PLBG0176GA-A	BP-176/BP-176V	0.45g





Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	13.0	—
E	—	13.0	—
v	—	—	0.15
w	—	—	0.20
A	—	—	1.40
A_1	0.35	0.40	0.45
e	—	0.80	—
b	0.45	0.50	0.55
x	—	—	0.08
y	—	—	0.10
y_1	—	—	0.2
S_D	—	—	—
S_E	—	—	—
Z_D	—	0.90	—
Z_E	—	0.90	—

Figure B 176-pin LFBGA (PLBG0176GA-A)