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Details

Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, LINbus, SCI, SPI, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	133
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b, 21x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LFQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f563nwddfc-v0

Table 1.3 List of Products (3/8)

Group	Part No.	Package	ROM Capacity	RAM Capacity	E2 Data Flash	Operating Frequency (Max.)	Operating Temp. Range
RX63N (D version)	R5F563NYHDFP	PLQP0100KB-A	1 Mbyte	256 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NYDDFP	PLQP0100KB-A	1 Mbyte	256 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NWHDFP	PLQP0100KB-A	1 Mbyte	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NWDDFP	PLQP0100KB-A	1 Mbyte	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NWGDFP	PLQP0100KB-A*1	1 Mbyte	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NWCDFP	PLQP0100KB-A*1	1 Mbyte	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NBCDFP	PLQP0100KB-A	1 Mbyte	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NBDDFP	PLQP0100KB-A	1 Mbyte	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NACDFP	PLQP0100KB-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NADDFP	PLQP0100KB-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
RX63N (G version) *2	R5F563NFHGFC	PLQP0176KB-A	2 Mbytes	256 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NFDGFC	PLQP0176KB-A	2 Mbytes	256 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NKDGFC	PLQP0176KB-A	2 Mbytes	192 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NEDGFC	PLQP0176KB-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NDDGFC	PLQP0176KB-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NYHGFC	PLQP0176KB-A	1 Mbyte	256 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NYDGFC	PLQP0176KB-A	1 Mbyte	256 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NWHGFC	PLQP0176KB-A	1 Mbyte	192 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NWDGFC	PLQP0176KB-A	1 Mbyte	192 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NBDGFC	PLQP0176KB-A	1 Mbyte	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NADGFC	PLQP0176KB-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NFHGF	PLQP0144KA-A	2 Mbytes	256 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NFDGF	PLQP0144KA-A	2 Mbytes	256 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NKDGF	PLQP0144KA-A	2 Mbytes	192 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NEDGF	PLQP0144KA-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NDDGF	PLQP0144KA-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NYHGF	PLQP0144KA-A	1 Mbyte	256 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NYDGF	PLQP0144KA-A	1 Mbyte	256 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NWHGF	PLQP0144KA-A	1 Mbyte	192 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NWDGF	PLQP0144KA-A	1 Mbyte	192 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NBDGF	PLQP0144KA-A	1 Mbyte	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NADGF	PLQP0144KA-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NFHGF	PLQP0100KB-A	2 Mbytes	256 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NFDGF	PLQP0100KB-A	2 Mbytes	256 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NKDGF	PLQP0100KB-A	2 Mbytes	192 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NEDGF	PLQP0100KB-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NDDGF	PLQP0100KB-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NYHGF	PLQP0100KB-A	1 Mbyte	256 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NYDGF	PLQP0100KB-A	1 Mbyte	256 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NWHGF	PLQP0100KB-A	1 Mbyte	192 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NWDGF	PLQP0100KB-A	1 Mbyte	192 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NBDGF	PLQP0100KB-A	1 Mbyte	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NADGF	PLQP0100KB-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
RX631 (D version)	R5F5631ECDLC	PTLG0177KA-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631EDDLC	PTLG0177KA-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C

Table 1.4 Pin Functions (3/6)

Classifications	Pin Name	I/O	Description
16-bit timer pulse unit	TIOCA0, TIOCB0 TIOCC0, TIOCD0	I/O	The TGRA0 to TGRD0 input capture input/output compare output/PWM output pins.
	TIOCA1, TIOCB1	I/O	The TGRA1 and TGRB1 input capture input/output compare output/PWM output pins.
	TIOCA2, TIOCB2	I/O	The TGRA2 and TGRB2 input capture input/output compare output/PWM output pins.
	TIOCA3, TIOCB3 TIOCC3, TIOCD3	I/O	The TGRA3 to TGRD3 input capture input/output compare output/PWM output pins.
	TIOCA4, TIOCB4	I/O	The TGRA4 and TGRB4 input capture input/output compare output/PWM output pins.
	TIOCA5, TIOCB5	I/O	The TGRA5 and TGRB5 input capture input/output compare output/PWM output pins.
	TCLKA, TCLKB TCLKC, TCLKD	Input	Input pins for external clock signals.
	TIOCA6, TIOCB6 TIOCC6, TIOCD6	I/O	The TGRA6 to TGRD6 input capture input/output compare output/PWM output pins.
	TIOCA7, TIOCB7	I/O	The TGRA7 and TGRB7 input capture input/output compare output/PWM output pins.
	TIOCA8, TIOCB8	I/O	The TGRA8 and TGRB8 input capture input/output compare output/PWM output pins.
	TIOCA9, TIOCB9 TIOCC9, TIOCD9	I/O	The TGRA9 to TGRD9 input capture input/output compare output/PWM output pins.
	TIOCA10, TIOCB10	I/O	The TGRA10 and TGRB10 input capture input/output compare output/PWM output pins.
	TIOCA11, TIOCB11	I/O	The TGRA11 and TGRB11 input capture input/output compare output/PWM output pins.
	TCLKE, TCLKF TCLKG, TCLKH	Input	Input pins for external clock signals.
Programmable pulse generator	PO0 to PO31	Output	Output pins for the pulse signals.
8-bit timer	TMO0 to TMO3	Output	Output pins for the compare match signals.
	TMCI0 to TMCI3	Input	Input pins for the external clock signals that drive for the counters.
	TMRI0 to TMRI3	Input	Input pins for the counter-reset signals.
Serial communications interface (SC1c)	• Asynchronous mode/clock synchronous mode		
	SCK0 to SCK11	I/O	Input/output pins for clock signals.
	RXD0 to RXD11	Input	Input pins for data reception.
	TXD0 to TXD11	Output	Output pins for data transmission.
	CTS0# to CTS11#	Input	Transmit/receive start control input pins
	RTS0# to RTS11#	Output	Transmit/receive start control output pins
	• Simple I ² C mode		
	SSCL0 to SSCL11	I/O	Input/output pins for the I ² C clock
	SSDA0 to SSDA11	I/O	Input/output pins for the I ² C data
Serial communications interface (SC1c)	• Simple SPI mode		
	SCK0 to SCK11	I/O	Input/output pins for the clock
	SMISO0 to SMISO11	I/O	Input/output pins for slave transmit data.
	SMOSI0 to SMOSI11	I/O	Input/output pins for master transmit data.
	SS0# to SS11#	Input	Input pins for chip select signals

1.5 Pin Assignments

Figure 1.5 to Figure 1.12 show the pins assignments. Table 1.5 to Table 1.13 show the list of pins and pin functions. Power pins and I/O ports are shown in the pin assignment diagrams.

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	
15	PE2	PE3	P70	P65	P67	VSS	VCC	PG7	PA6	PB0	P72	PB4	VSS	VCC	PC1	15
14	PE1	PE0	VSS	PE7	PG3	PA0	PA1	PA2	PA7	VCC	PB1	PB5	P73	P75	P74	14
13	P63	P64	PE4	VCC	PG2	PG4	PG6	PA3	VSS	P71	PB3	PB7	PC0	PC2	P76	13
12	P60	VSS	P62	PE5	PE6	P66	PG5	PA4	PA5	PB2	PB6	P77	PC3	PC4	P80	12
11	PD6	PG1	VCC	P61	RX63N Group RX631 Group PTLG0177KA-A (177-pin TFLGA) (Top perspective view)							P81	P82	PC6	VCC	11
10	P97	PD4	PG0	PD7								PC5	PC7	P83	VSS	10
9	VCC	P96	PD3	PD5								P50	P51	P52	P84	9
8	P94	PD1	PD2	VSS								P53	VCC_USB	USB1_DP	USB1_DM	8
7	VSS	P92	PD0	P95								P54	P55	VSS_USB	USB0_DP	7
6	VCC	P91	P90	P93	NC							P56	P57	VCC_USB	USB0_DM	6
5	P46	P47	P45	P44								P13	P12	P10	P11	5
4	P42	P41	P43	P00	VSS	BSCANP	PF4	P35	PF3	PF1	P25	P86	P15	P14	P85	4
3	VREFL0	P40	VREFH0	P03	PF5	PJ3	MD/FINED	RES#	P34	PF2	PF0	P24	P22	P87	P16	3
2	AVCC0	P07	VREFH	P02	EMLE	VCL	XCOUT	VSS	VCC	P32	P30	P26	P23	P17	P20	2
1	AVSS0	P05	VREFL	P01	PJ5	VBATT	XCIN	XTAL	EXTAL	P33	P31	P27	VCC	VSS	P21	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	

Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.5, List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA).

Figure 1.3 Pin Assignment (177-Pin TFLGA)

Table 1.9 List of Pins and Pin Functions (100-Pin TFLGA) (1/5)

Pin No. 100-pin TFLGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC	Timers (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SC1c, SC1d, RSPI, RIIC, CAN, IEB, USB)	Interrupt	S12AD AD DA
A1		P05				IRQ13	DA1
A2	VREFH						
A3		P07				IRQ15	ADTRG0#
A4	VREFL0						
A5		P43				IRQ11-DS	AN003
A6		PD0	D0[A0/D0]			IRQ0	AN008
A7		PD4	D4[A4/D4]	POE3#		IRQ4	AN012
A8		PE0	D8[A8/D8]		SCK12/SSLB1		ANEX0
A9		PE1	D9[A9/D9]	MTIOC4C/ PO18	TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12/SSLB2/ RSPCKB		ANEX1
A10		PE2	D10[A10/D10]	MTIOC4A/ PO23	RXD12/SMISO12/ SSCL12/RXDX12/ SSLB3/MOSIB	IRQ7-DS	AN0
B1	EMLE						
B2	AVSS0						
B3	AVCC0						
B4		P40				IRQ8-DS	AN000
B5		P44				IRQ12-DS	AN004
B6		PD1	D1[A1/D1]	MTIOC4B	CTX0*1	IRQ1	AN009
B7		PD3	D3[A3/D3]	POE8#		IRQ3	AN011
B8		PD6	D6[A6/D6]	MTIC5V/ POE1#		IRQ6	AN6
B9		PD7	D7[A7/D7]	MTIC5U/ POE0#		IRQ7	AN7
B10		PE3	D11[A11/D11]	MTIOC4B/ PO26/POE8#	CTS12#/RTS12#/ SS12#/MISOB/ ET_ERXD3		AN1
C1	VCL						
C2	VREFL						
C3		PJ3		MTIOC3C	CTS6#/RTS6#/ CTS0#/RTS0#/ SS6#/SS0#		
C4	VREFH0						
C5		P42				IRQ10-DS	AN002
C6		P47				IRQ15-DS	AN007
C7		PD2	D2[A2/D2]	MTIOC4D	CRX0*1	IRQ2	AN010
C8		PD5	D5[A5/D5]	MTIC5W/ POE2#		IRQ5	AN013
C9		PE5	D13[A13/D13]	MTIOC4C/ MTIOC2B	RSPCKB/ ET_RX_CLK/ REF50CK	IRQ5	AN3
C10		PE4	D12[A12/D12]	MTIOC4D/ MTIOC1A/ PO28	SSLB0/ET_ERXD2		AN2
D1	XCIN						

Table 1.10 List of Pins and Pin Functions (100-Pin LQFP) (2/4)

Pin No. 100-pin LQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC	Timers (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SCIC, SCID, RSPI, RIIC, CAN, IEB, USB)	Interrupt	S12AD AD DA
31		P15		MTIOC0B/MTCLKB/ TIOCB2/TCLKB/TMC12/ PO13	RXD1/SCK3/SMISO1/ SSCL1/CRX1-DS	IRQ5	
32		P14		MTIOC3A/MTCLKA/ TIOCB5/TCLKA/TMR12/ PO15	CTS1#/RTS1#/SS1#/ CTX1/USB0_DPUPE/ USB0_OVRCURA	IRQ4	
33		P13		MTIOC0B/TIOCA5/ TMO3/PO13	TXD2/SMOSI2/SSDA2/ SDA0[FM+]	IRQ3	ADTRG#
34		P12		TMC11	RXD2/SMISO2/SSCL2/ SCL0[FM+]	IRQ2	
35	VCC_USB						
36					USB0_DM		
37					USB0_DP		
38	VSS_USB						
39		P55	WAIT#/ EDREQ0	MTIOC4D/TMO3	CRX1/ET_EXOUT	IRQ10	
40		P54	ALE/EDACK0	MTIOC4B/TMC11	CTS2#/RTS2#/SS2#/ CTX1/ET_LINKSTA		
41		P53*2	BCLK				
42		P52	RD#		RXD2/SMISO2/SSCL2/ SSLB3		
43		P51	WR1#/BC1#/ WAIT#		SCK2/SSLB2		
44		P50	WR0#/WR#		TXD2/SMOSI2/SSDA2/ SSLB1		
45		PC7	A23/CS0#	MTIOC3A/MTCLKB/ TMO2/PO31	TXD8/SMOSI8/SSDA8/ MISOA/ET_COL	IRQ14	
46		PC6	A22/CS1#	MTIOC3C/MTCLKA/ TMC12/PO30	RXD8/SMISO8/SSCL8/ MOSIA/ET_ETXD3	IRQ13	
47		PC5	A21/CS2#/ WAIT#	MTIOC3B/MTCLKD/ TMR12/PO29	SCK8/RSPCKA/ ET_ETXD2		
48		PC4	A20/CS3#	MTIOC3D/MTCLKC/ TMC11/PO25/POE0#	SCK5/CTS8#/RTS8#/ SS8#/SSLA0/ ET_TX_CLK		
49		PC3	A19	MTIOC4D/TCLKB/ PO24	TXD5/SMOSI5/SSDA5/ IETXD/ET_TX_ER		
50		PC2	A18	MTIOC4B/TCLKA/PO21	RXD5/SMISO5/SSCL5/ SSLA3/IERXD/ ET_RX_DV		
51		PC1	A17	MTIOC3A/TCLKD/ PO18	SCK5/SSLA2/ ET_ERXD2	IRQ12	
52		PC0	A16	MTIOC3C/TCLKC/ PO17	CTS5#/RTS5#/SS5#/ SSLA1/ET_ERXD3	IRQ14	
53		PB7	A15	MTIOC3B/TIOCB5/ PO31	TXD9/SMOSI9/SSDA9/ ET_CRS/ RMII_CRS_DV		
54		PB6	A14	MTIOC3D/TIOCA5/ PO30	RXD9/SMISO9/SSCL9/ ET_ETXD1/RMII_TXD1		
55		PB5	A13	MTIOC2A/MTIOC1B/ TIOCB4/TMR11/PO29/ POE1#	SCK9/ET_ETXD0/ RMII_TXD0		
56		PB4	A12	TIOCA4/PO28	CTS9#/RTS9#/SS9#/ ET_TX_EN/ RMII_TXD_EN		
57		PB3	A11	MTIOC0A/MTIOC4A/ TIOC3D/TCLKD/TMO0/ PO27/POE3#	SCK6/ET_RX_ER/ RMII_RX_ER		
58		PB2	A10	TIOCC3/TCLKC/PO26	CTS6#/RTS6#/SS6#/ ET_RX_CLK/REF50CK		

Table 4.1 List of I/O Registers (Address Order) (7/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 7096h	ICU	Interrupt request register 150	IR150	8	8	2	ICLK	ICUb
0008 7097h	ICU	Interrupt request register 151	IR151	8	8	2	ICLK	
0008 7098h	ICU	Interrupt request register 152	IR152	8	8	2	ICLK	
0008 7099h	ICU	Interrupt request register 153	IR153	8	8	2	ICLK	
0008 709Ah	ICU	Interrupt request register 154	IR154	8	8	2	ICLK	
0008 709Bh	ICU	Interrupt request register 155	IR155	8	8	2	ICLK	
0008 709Ch	ICU	Interrupt request register 156	IR156	8	8	2	ICLK	
0008 709Dh	ICU	Interrupt request register 157	IR157	8	8	2	ICLK	
0008 709Eh	ICU	Interrupt request register 158	IR158	8	8	2	ICLK	
0008 709Fh	ICU	Interrupt request register 159	IR159	8	8	2	ICLK	
0008 70A0h	ICU	Interrupt request register 160	IR160	8	8	2	ICLK	
0008 70A1h	ICU	Interrupt request register 161	IR161	8	8	2	ICLK	
0008 70A2h	ICU	Interrupt request register 162	IR162	8	8	2	ICLK	
0008 70A3h	ICU	Interrupt request register 163	IR163	8	8	2	ICLK	
0008 70A4h	ICU	Interrupt request register 164	IR164	8	8	2	ICLK	
0008 70A5h	ICU	Interrupt request register 165	IR165	8	8	2	ICLK	
0008 70A6h	ICU	Interrupt request register 166	IR166	8	8	2	ICLK	
0008 70A7h	ICU	Interrupt request register 167	IR167	8	8	2	ICLK	
0008 70AAh	ICU	Interrupt request register 170	IR170	8	8	2	ICLK	
0008 70ABh	ICU	Interrupt request register 171	IR171	8	8	2	ICLK	
0008 70ACh	ICU	Interrupt request register 172	IR172	8	8	2	ICLK	
0008 70ADh	ICU	Interrupt request register 173	IR173	8	8	2	ICLK	
0008 70AEh	ICU	Interrupt request register 174	IR174	8	8	2	ICLK	
0008 70AFh	ICU	Interrupt request register 175	IR175	8	8	2	ICLK	
0008 70B0h	ICU	Interrupt request register 176	IR176	8	8	2	ICLK	
0008 70B1h	ICU	Interrupt request register 177	IR177	8	8	2	ICLK	
0008 70B2h	ICU	Interrupt request register 178	IR178	8	8	2	ICLK	
0008 70B3h	ICU	Interrupt request register 179	IR179	8	8	2	ICLK	
0008 70B4h	ICU	Interrupt request register 180	IR180	8	8	2	ICLK	
0008 70B5h	ICU	Interrupt request register 181	IR181	8	8	2	ICLK	
0008 70B6h	ICU	Interrupt request register 182	IR182	8	8	2	ICLK	
0008 70B7h	ICU	Interrupt request register 183	IR183	8	8	2	ICLK	
0008 70B8h	ICU	Interrupt request register 184	IR184	8	8	2	ICLK	
0008 70B9h	ICU	Interrupt request register 185	IR185	8	8	2	ICLK	
0008 70BAh	ICU	Interrupt request register 186	IR186	8	8	2	ICLK	
0008 70BBh	ICU	Interrupt request register 187	IR187	8	8	2	ICLK	
0008 70BCh	ICU	Interrupt request register 188	IR188	8	8	2	ICLK	
0008 70BDh	ICU	Interrupt request register 189	IR189	8	8	2	ICLK	
0008 70BEh	ICU	Interrupt request register 190	IR190	8	8	2	ICLK	
0008 70BFh	ICU	Interrupt request register 191	IR191	8	8	2	ICLK	
0008 70C0h	ICU	Interrupt request register 192	IR192	8	8	2	ICLK	
0008 70C1h	ICU	Interrupt request register 193	IR193	8	8	2	ICLK	
0008 70C2h	ICU	Interrupt request register 194	IR194	8	8	2	ICLK	
0008 70C3h	ICU	Interrupt request register 195	IR195	8	8	2	ICLK	
0008 70C4h	ICU	Interrupt request register 196	IR196	8	8	2	ICLK	
0008 70C5h	ICU	Interrupt request register 197	IR197	8	8	2	ICLK	
0008 70C6h	ICU	Interrupt request register 198	IR198	8	8	2	ICLK	
0008 70C7h	ICU	Interrupt request register 199	IR199	8	8	2	ICLK	
0008 70C8h	ICU	Interrupt request register 200	IR200	8	8	2	ICLK	
0008 70C9h	ICU	Interrupt request register 201	IR201	8	8	2	ICLK	
0008 70CAh	ICU	Interrupt request register 202	IR202	8	8	2	ICLK	

Table 4.1 List of I/O Registers (Address Order) (14/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function	
						ICLK≥PCLK	ICLK<PCLK		
0008 7400h	ICU	DMAC activation request select register 0	DMRSR0	8	8	2 ICLK		ICUb	
0008 7404h	ICU	DMAC activation request select register 1	DMRSR1	8	8	2 ICLK			
0008 7408h	ICU	DMAC activation request select register 2	DMRSR2	8	8	2 ICLK			
0008 740Ch	ICU	DMAC activation request select register 3	DMRSR3	8	8	2 ICLK			
0008 7500h	ICU	IRQ control register 0	IRQCR0	8	8	2 ICLK			
0008 7501h	ICU	IRQ control register 1	IRQCR1	8	8	2 ICLK			
0008 7502h	ICU	IRQ control register 2	IRQCR2	8	8	2 ICLK			
0008 7503h	ICU	IRQ control register 3	IRQCR3	8	8	2 ICLK			
0008 7504h	ICU	IRQ control register 4	IRQCR4	8	8	2 ICLK			
0008 7505h	ICU	IRQ control register 5	IRQCR5	8	8	2 ICLK			
0008 7506h	ICU	IRQ control register 6	IRQCR6	8	8	2 ICLK			
0008 7507h	ICU	IRQ control register 7	IRQCR7	8	8	2 ICLK			
0008 7508h	ICU	IRQ control register 8	IRQCR8	8	8	2 ICLK			
0008 7509h	ICU	IRQ control register 9	IRQCR9	8	8	2 ICLK			
0008 750Ah	ICU	IRQ control register 10	IRQCR10	8	8	2 ICLK			
0008 750Bh	ICU	IRQ control register 11	IRQCR11	8	8	2 ICLK			
0008 750Ch	ICU	IRQ control register 12	IRQCR12	8	8	2 ICLK			
0008 750Dh	ICU	IRQ control register 13	IRQCR13	8	8	2 ICLK			
0008 750Eh	ICU	IRQ control register 14	IRQCR14	8	8	2 ICLK			
0008 750Fh	ICU	IRQ control register 15	IRQCR15	8	8	2 ICLK			
0008 7510h	ICU	IRQ pin digital filter enable register 0	IRQFLTE0	8	8	2 ICLK			
0008 7511h	ICU	IRQ pin digital filter enable register 1	IRQFLTE1	8	8	2 ICLK			
0008 7514h	ICU	IRQ pin digital filter setting register 0	IRQFLTC0	16	16	2 ICLK			
0008 7516h	ICU	IRQ pin digital filter setting register 1	IRQFLTC1	16	16	2 ICLK			
0008 7580h	ICU	Non-maskable interrupt status register	NMISR	8	8	2 ICLK			
0008 7581h	ICU	Non-maskable interrupt enable register	NMIER	8	8	2 ICLK			
0008 7582h	ICU	Non-maskable interrupt status clear register	NMICLR	8	8	2 ICLK			
0008 7583h	ICU	NMI pin interrupt control register	NMICR	8	8	2 ICLK			
0008 7590h	ICU	NMI pin digital filter enable register	NMIFLTE	8	8	2 ICLK			
0008 7594h	ICU	NMI pin digital filter setting register	NMIFLTC	16	16	2 ICLK			
0008 8000h	CMT	Compare match timer start register 0	CMSTR0	16	16	2, 3 PCLKB	2 ICLK	CMT	
0008 8002h	CMT0	Compare match timer control register	CMCR	16	16	2, 3 PCLKB	2 ICLK		
0008 8004h	CMT0	Compare match timer counter	CMCNT	16	16	2, 3 PCLKB	2 ICLK		
0008 8006h	CMT0	Compare match timer constant register	CMCOR	16	16	2, 3 PCLKB	2 ICLK		
0008 8008h	CMT1	Compare match timer control register	CMCR	16	16	2, 3 PCLKB	2 ICLK		
0008 800Ah	CMT1	Compare match timer counter	CMCNT	16	16	2, 3 PCLKB	2 ICLK		
0008 800Ch	CMT1	Compare match timer constant register	CMCOR	16	16	2, 3 PCLKB	2 ICLK		
0008 8010h	CMT	Compare match timer start register 1	CMSTR1	16	16	2, 3 PCLKB	2 ICLK		
0008 8012h	CMT2	Compare match timer control register	CMCR	16	16	2, 3 PCLKB	2 ICLK		
0008 8014h	CMT2	Compare match timer counter	CMCNT	16	16	2, 3 PCLKB	2 ICLK		
0008 8016h	CMT2	Compare match timer constant register	CMCOR	16	16	2, 3 PCLKB	2 ICLK		
0008 8018h	CMT3	Compare match timer control register	CMCR	16	16	2, 3 PCLKB	2 ICLK		
0008 801Ah	CMT3	Compare match timer counter	CMCNT	16	16	2, 3 PCLKB	2 ICLK		
0008 801Ch	CMT3	Compare match timer constant register	CMCOR	16	16	2, 3 PCLKB	2 ICLK		
0008 8020h	WDT	WDT refresh register	WDTRR	8	8	2, 3 PCLKB	2 ICLK		WDTA
0008 8022h	WDT	WDT control register	WDTCR	16	16	2, 3 PCLKB	2 ICLK		
0008 8024h	WDT	WDT status register	WDTSR	16	16	2, 3 PCLKB	2 ICLK		
0008 8026h	WDT	WDT reset control register	WDTRCR	8	8	2, 3 PCLKB	2 ICLK		
0008 8030h	IWDT	IWDT refresh register	IWDTRR	8	8	2, 3 PCLKB	2 ICLK		
0008 8032h	IWDT	IWDT control register	IWDTCR	16	16	2, 3 PCLKB	2 ICLK		
0008 8034h	IWDT	IWDT status register	IWDTSR	16	16	2, 3 PCLKB	2 ICLK		

Table 4.1 List of I/O Registers (Address Order) (29/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 C000h	PORT0	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C001h	PORT1	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C002h	PORT2	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C003h	PORT3	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C004h	PORT4	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C005h	PORT5	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C006h	PORT6	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C007h	PORT7	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C008h	PORT8	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C009h	PORT9	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C00Ah	PORTA	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C00Bh	PORTB	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C00Ch	PORTC	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C00Dh	PORTD	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C00Eh	PORTE	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C00Fh	PORTF	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C010h	PORTG	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C012h	PORTJ	Port direction register	PDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C020h	PORT0	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C021h	PORT1	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C022h	PORT2	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C023h	PORT3	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C024h	PORT4	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C025h	PORT5	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C026h	PORT6	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C027h	PORT7	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C028h	PORT8	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C029h	PORT9	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C02Ah	PORTA	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C02Bh	PORTB	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C02Ch	PORTC	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C02Dh	PORTD	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C02Eh	PORTE	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C02Fh	PORTF	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C030h	PORTG	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C032h	PORTJ	Port output data register	PODR	8	8	2, 3 PCLKB	2 ICLK	
0008 C040h	PORT0	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C041h	PORT1	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C042h	PORT2	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C043h	PORT3	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C044h	PORT4	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	
0008 C045h	PORT5	Port input data register	PIDR	8	8	2, 3 PCLKB	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (31/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 C095h	PORTA	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	I/O Ports
0008 C096h	PORTB	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C097h	PORTB	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C098h	PORTC	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C099h	PORTC	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C09Ah	PORTD	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C09Bh	PORTD	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C09Ch	PORTE	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C09Dh	PORTE	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C09Eh	PORTF	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C09Fh	PORTF	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C0A0h	PORTG	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C0A1h	PORTG	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C0A4h	PORTJ	Open drain control register 0	ODR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C0A5h	PORTJ	Open drain control register 1	ODR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C0C0h	PORT0	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0C1h	PORT1	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0C2h	PORT2	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0C3h	PORT3	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0C4h	PORT4	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0C5h	PORT5	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0C6h	PORT6	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0C7h	PORT7	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0C8h	PORT8	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0C9h	PORT9	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0CAh	PORTA	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0CBh	PORTB	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0CCh	PORTC	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0CDh	PORTD	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0CEh	PORTE	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0CFh	PORTF	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0D0h	PORTG	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0D2h	PORTJ	Pull-up control register	PCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0E0h	PORT0	Drive ability control register	DSCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0E2h	PORT2	Drive ability control register	DSCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0E5h	PORT5	Drive ability control register	DSCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0E9h	PORT9	Drive ability control register	DSCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0EAh	PORTA	Drive ability control register	DSCR	8	8	2, 3 PCLKB	2 ICLK	MPC
0008 C0EBh	PORTB	Drive ability control register	DSCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0ECh	PORTC	Drive ability control register	DSCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0EDh	PORTD	Drive ability control register	DSCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0EEh	PORTE	Drive ability control register	DSCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C0F0h	PORTG	Drive ability control register	DSCR	8	8	2, 3 PCLKB	2 ICLK	
0008 C100h	MPC	CS output enable register	PFCSE	8	8	2, 3 PCLKB	2 ICLK	
0008 C102h	MPC	CS output pin select register 0	PFCSS0	8	8	2, 3 PCLKB	2 ICLK	
0008 C103h	MPC	CS output pin select register 1	PFCSS1	8	8	2, 3 PCLKB	2 ICLK	
0008 C104h	MPC	Address output enable register 0	PFAOE0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C105h	MPC	Address output enable register 1	PFAOE1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C106h	MPC	External bus control register 0	PFBCR0	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C107h	MPC	External bus control register 1	PFBCR1	8	8, 16	2, 3 PCLKB	2 ICLK	
0008 C10Eh	MPC	Ethernet control register 1	PFENET	8	8	2, 3 PCLKB	2 ICLK	

5.2 DC Characteristics

Table 5.2 DC Characteristics (1)

Conditions: $V_{CC} = AV_{CC0} = V_{REFH} = V_{CC_USB} = 2.7$ to 3.6 V, $V_{REFH0} = 2.7$ V to AV_{CC0} ,
 $V_{SS} = AV_{SS0} = V_{REFL}/V_{REFL0} = V_{SS_USB} = 0$ V, $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	IRQ input pin*1	V_{IH}	$V_{CC} \times 0.8$	—	$V_{CC} + 0.3$	V
	MTU input pin*1	V_{IL}	-0.3	—	$V_{CC} \times 0.2$	
	TMR input pin*1	ΔV_T	$V_{CC} \times 0.06$	—	—	
	SCI input pin*1					
	ADTRG# input pin*1					
	RES#, NMI					
	RIIC input pin (except for SMBus)	V_{IH}	$V_{CC} \times 0.7$	—	5.8	
		V_{IL}	-0.3	—	$V_{CC} \times 0.3$	
		ΔV_T	$V_{CC} \times 0.05$	—	—	
	Ports for 5 V tolerant*2	V_{IH}	$V_{CC} \times 0.8$	—	5.8	
		V_{IL}	-0.3	—	$V_{CC} \times 0.2$	
Input high voltage (except for Schmitt trigger input pin)	Other input pins excluding ports for 5 V tolerant*3	V_{IH}	$V_{CC} \times 0.8$	—	$V_{CC} + 0.3$	V
		V_{IL}	-0.3	—	$V_{CC} \times 0.2$	
		V_{IH}	$V_{CC} \times 0.9$	—	$V_{CC} + 0.3$	
		V_{IL}	$V_{CC} \times 0.8$	—	$V_{CC} + 0.3$	
		V_{IH}	2.3	—	$V_{CC} + 0.3$	
		V_{IL}	—	—	$V_{CC} + 0.3$	
		V_{IH}	$V_{CC} \times 0.7$	—	$V_{CC} + 0.3$	
Input low voltage (except for Schmitt trigger input pin)	MD pin, EMLE	V_{IL}	2.1	—	$V_{CC} + 0.3$	V
	EXTAL, RSPI, EXDMAC, WAIT#, TCK	V_{IL}	-0.3	—	$V_{CC} \times 0.1$	
	ETHERC	V_{IL}	-0.3	—	$V_{CC} \times 0.2$	
	XCIN	V_{IL}	-0.3	—	—	
	D0 to D31	V_{IL}	-0.3	—	$V_{CC} \times 0.3$	
	RIIC (SMBus)	V_{IL}	-0.3	—	0.8	

Note 1. V_{IH} characteristics of the pins which are multiplexed with pin functions having 5-V tolerance are those of the pin functions for 5-V tolerance.

Note 2. Ports 07, 12 to 17, 20, 21, 30 to 33, 67, and C0 to C3 are 5 V tolerant.

Note 3. For P32, P31, P30, input as follows when the V_{BATT} power supply is selected.

V_{IH} Min. = $V_{BATT} \times 0.8$, V_{IH} Max. = $V_{BATT} + 0.3$, V_{IL} Min. = -0.3, V_{IL} Max. = $V_{BATT} \times 0.2$

Table 5.4 DC Characteristics (3) (for D and G Versions (-40 ≤ Ta ≤ +85°C))

Conditions: VCC = AVCC0 = VREFH = VCC_USB = V_{BATT} = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0,
VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V, T_a = T_{opr}

Item				Symbol	Min.	Typ.	Max.	Unit	Test Conditions		
Supply current*1	High-speed operating mode	Max.*2		I _{CC} *3	—	—	100	mA	ICLK = 100 MHz PCLKA = 100MHz PCLKB = 50 MHz FCLK = 50 MHz BCLK = 100MHz		
		Normal*4	Peripheral function: clock signal supplied*4		—	52	—				
			Peripheral function: clock signal stopped*4		—	40	—				
		Sleep mode			—	25	65				
		All-module-clock-stop mode (reference value)			—	20	38				
		Increased by BGO operation*5			—	15	—				
	Low-speed operating mode 1*6				—	4	—			ICLK = 1 MHz	
	Low-speed operating mode 2				—	1	—				ICLK = 32.768 kHz
	Software standby mode				—	0.2	6				
	Deep software standby mode	Power supplied to RAM and USB resume detecting unit			—	22	200			μA	
		Power not supplied to RAM and USB resume detecting unit	Power-on reset circuit and low-power consumption function disabled	—	21	60					
			Power-on reset circuit and low-power	—	6.2	28					
		Increase when the RTC is operating	When a crystal oscillator for low clock loads is in use	—	1.0	—					
			When a crystal oscillator for standard clock loads is in use	—	3.0	—					
		RTC operating while VCC is off (with the battery backup function, only the RTC and sub-clock oscillator operate)	When a crystal oscillator for low clock loads is in use	—	0.9	—	V _{BATT} = 2.0 V, VCC = 0V				
	When a crystal oscillator for standard clock loads is in use		—	1.6	—	V _{BATT} = 3.3 V, VCC = 0V					
			—	1.7	—	V _{BATT} = 2.0 V(for products with 100 pins or more), VBATT = 2.3 V (for the 64-pin product), VCC = 0V					
			—	3.3	—	V _{BATT} = 3.3 V, VCC = 0V					
	Analog power supply current*7	During 12-bit A/D conversion (including temperature sensor)			I _{AVCC0}	—	2.3	3.2	mA		
		During 10-bit A/D conversion			I _{VREFH} *9	—	1.0	1.65		mA	
During D/A conversion (per unit)			—	0.7		1.0	mA				
Waiting for A/D, D/A conversion (all units)*10			—	—	25	35		μA			
A/D, D/A converter in standby mode (all units)*10				—	0.1	4.0	μA				
Reference power supply current	During 12-bit A/D conversion			I _{VREFH0}	—	0.6		0.7	mA		
	Waiting for 12-bit A/D conversion (per unit)				—	0.5	0.6	mA			
	12-bit A/D converter in standby mode (per unit)				—	0.1	2.0			μA	

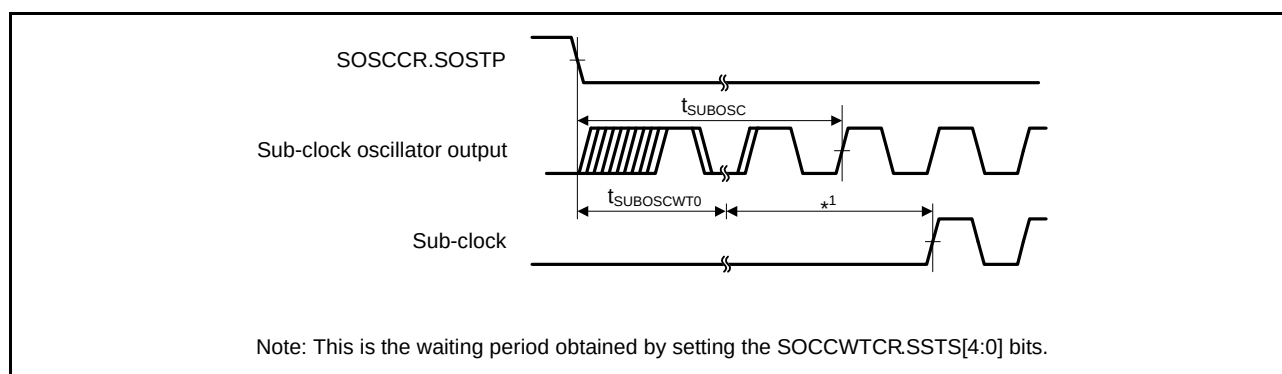


Figure 5.12 Sub-Clock Oscillation Start Timing

5.3.3 Timing of Recovery from Low Power Consumption Modes

Table 5.14 Timing of Recovery from Low Power Consumption Modes

Conditions: $V_{CC} = AV_{CC0} = V_{REFH} = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, $V_{REFH0} = 2.7$ V to AV_{CC0} ,
 $V_{SS} = AV_{SS0} = V_{REFL}/V_{REFL0} = V_{SS_USB} = 0$ V, $T_a = T_{opr}$

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Recovery time after cancellation of software standby mode	Crystal resonator connected to main clock oscillator	Main clock oscillator operating	t _{SBYMC}	10	—	—	ms	Figure 5.13
		Main clock oscillator and PLL circuit operating	t _{SBYPC}	10	—	—	ms	
	External clock input to main clock oscillator	Main clock oscillator operating	t _{SBYEX}	1	—	—	ms	
		Main clock oscillator and PLL circuit operating	t _{SBYPE}	1	—	—	ms	
	Sub-clock oscillator operating		t _{SBYSC}	2	—	—	s	
	High-speed on-chip oscillator operating		t _{SBYHO}	—	—	2	ms	
	Low-speed on-chip oscillator or IWDG-dedicated on-chip oscillator operating		t _{SBYLO}	—	—	800	μs	
Recovery time after cancellation of deep software standby mode			t _{DSBY}	—	—	1.0	ms	Figure 5.14
Wait time after cancellation of deep software standby mode			t _{DSBYWT}	45	—	46	t _{cyc}	

Note: The wait time varies depending on the state in which each oscillator was when the WAIT instruction was executed. The recovery time when multiple oscillators are operating is the same period as that when the oscillator which requires the longest time of all operating oscillators to recover is operating alone.

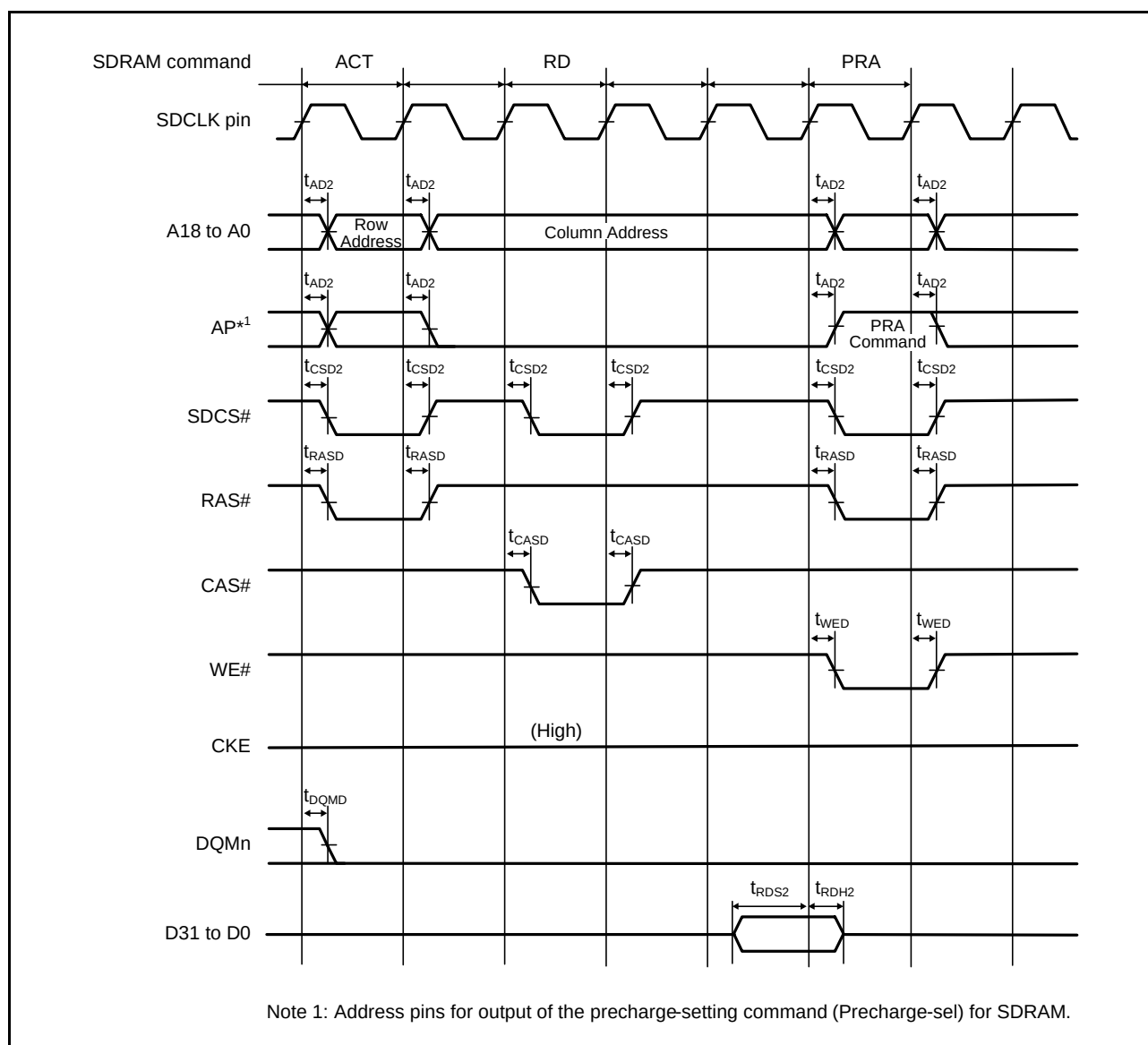


Figure 5.24 SDRAM Space Single Read Bus Timing

Table 5.24 Timing of On-Chip Peripheral Modules (6)

Conditions: VCC = AVCC0 = VREFH = VCC_USB = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0

VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V

PCLK = 8 to 50 MHz

 $T_a = T_{opr}$

High drive output is selected by the drive capacity control register.

Item		Symbol	Min.*1, *2	Max.*1	Unit	Test Conditions
RIIC (Fast-mode+) ICFER.FMPE = 1	SCL input cycle time	t_{SCL}	$6(12) \times t_{IICcyc} + 240$	—	ns	Figure 5.47
	SCL input high pulse width	t_{SCLH}	$3(6) \times t_{IICcyc} + 120$	—	ns	
	SCL input low pulse width	t_{SCLL}	$3(6) \times t_{IICcyc} + 120$	—	ns	
	SCL, SDA input rise time	t_{Sr}	—	120	ns	
	SCL, SDA input fall time	t_{Sf}	—	120	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	$1(4) \times t_{IICcyc}$	ns	
	SDA input bus free time	t_{BUF}	$3(6) \times t_{IICcyc} + 120$	—	ns	
	Start condition input hold time	t_{STAH}	$t_{IICcyc} + 120$	—	ns	
	Restart condition input setup time	t_{STAS}	120	—	ns	
	Stop condition input setup time	t_{STOS}	120	—	ns	
	Data input setup time	t_{SDAS}	$t_{IICcyc} + 120$	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	550	pF	
Simple IIC (Standard-mode)	SDA input rise time	t_{Sr}	—	1000	ns	
	SDA input fall time	t_{Sf}	—	300	ns	
	SDA input spike pulse removal time	t_{SP}	0	$4 \times t_{IICcyc}$	ns	
	Data input setup time	t_{SDAS}	250	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
Simple IIC (Fast-mode)	SCL, SDA input rise time	t_{Sr}	$20 + 0.1C_b$	300	ns	
	SCL, SDA input fall time	t_{Sf}	$20 + 0.1C_b$	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	$4 \times t_{IICcyc}$	ns	
	Data input setup time	t_{SDAS}	100	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

Note: t_{IICcyc} : RIIC internal reference clock (IIC ϕ) Cycle, t_{Pcyc} : PCLK cycle

Note 1. The value in parentheses is used when ICMR3.NF[1:0] are set to 11b while a digital filter is enabled with ICFER.NFE = 1.

Note 2. C_b indicates the total capacity of the bus line.

5.6 D/A Conversion Characteristics

Table 5.31 D/A Conversion Characteristics

Conditions: $V_{CC} = AVCC0 = VREFH = VCC_USB = 2.7$ to 3.6 V, $VREFH0 = 2.7$ V to V_{CC}
 $VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0$ V
 $T_a = T_{opr}$

Item	Min.	Typ.	Max.	Unit	Test Conditions
Resolution	10	10	10	Bit	
Conversion time	—	—	3.0	μs	20-pF capacitive load
Absolute accuracy	—	±2.0	±4.0	LSB	2-MΩ resistive load
	—	—	±3.0	LSB	4-MΩ resistive load
	—	—	±2.0	LSB	10-MΩ resistive load
RO output resistance	—	3.6	—	kΩ	

5.7 Temperature Sensor Characteristics

Table 5.32 Temperature Sensor Characteristics

Conditions: $V_{CC} = AVCC0 = VREFH = VCC_USB = 2.7$ to 3.6 V, $VREFH0 = 2.7$ V to V_{CC}
 $VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0$ V
 $T_a = T_{opr}$

Item	Min.	Typ.	Max.	Unit	Test Conditions
Relative accuracy	—	±1	—	°C	
Temperature slope	—	4.1	—	mV/°C	
Output voltage (@25°C)	—	1.26	—	V	
Temperature sensor start time	—	—	30	μs	
Sampling time	—	—	5	μs	

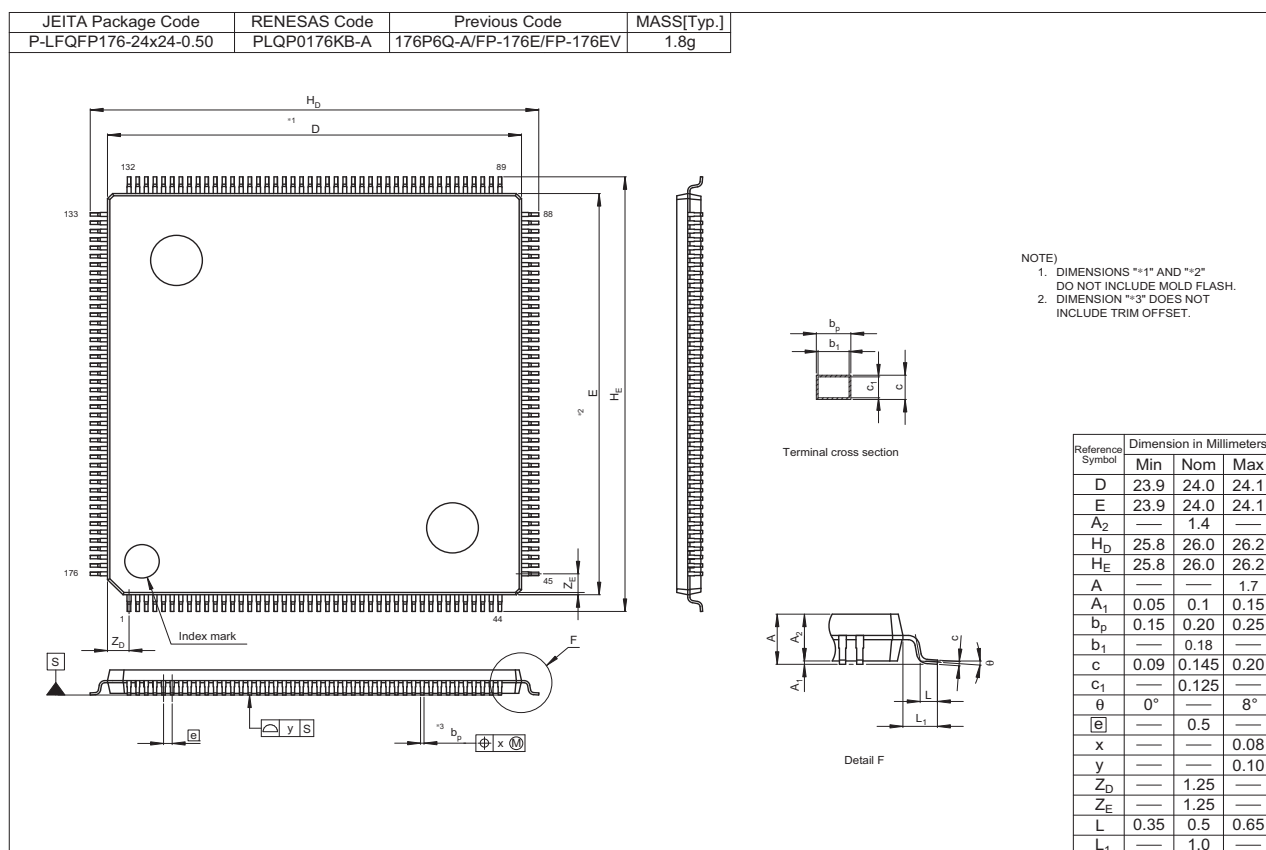


Figure C 176-pin LQFP (PLQP0176KB-A)

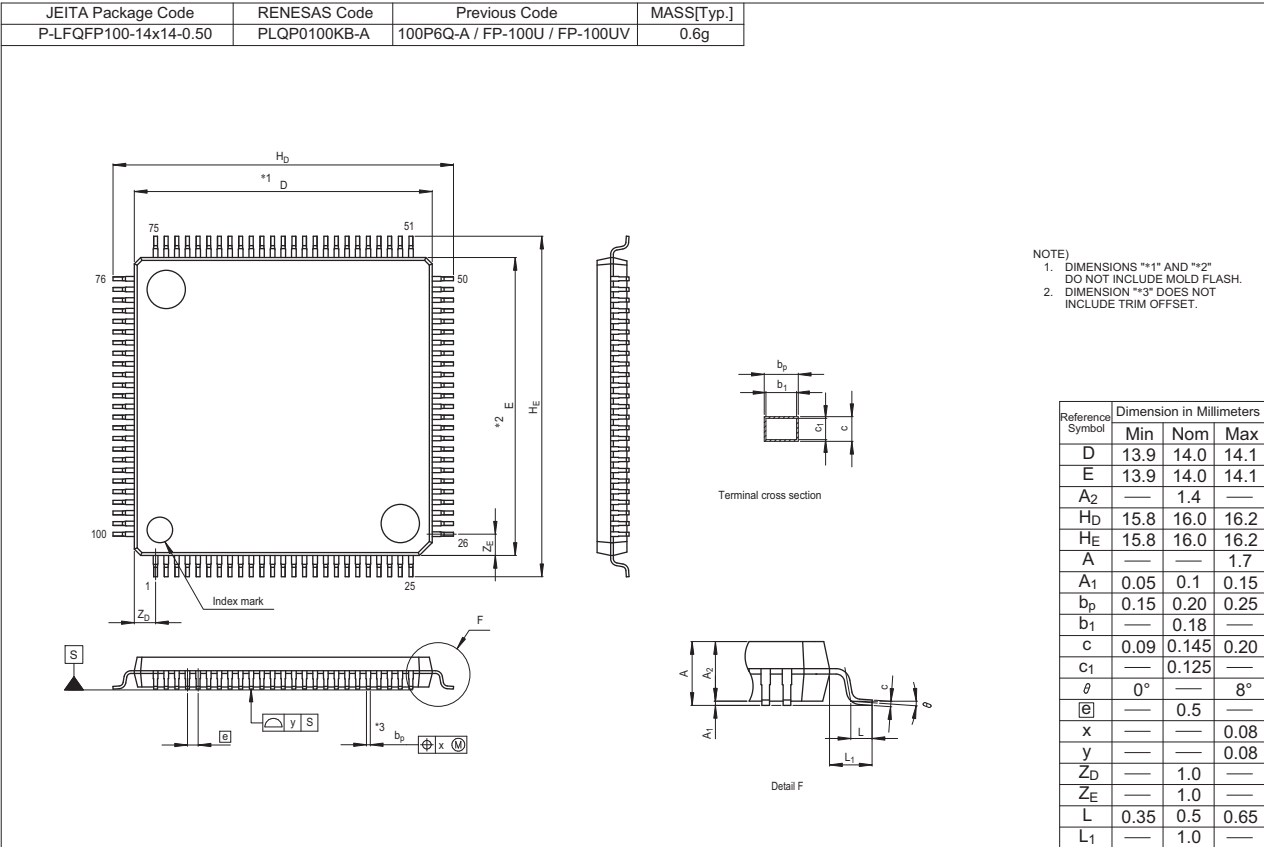


Figure G 100-pin LQFP (PLQP0100KB-A)

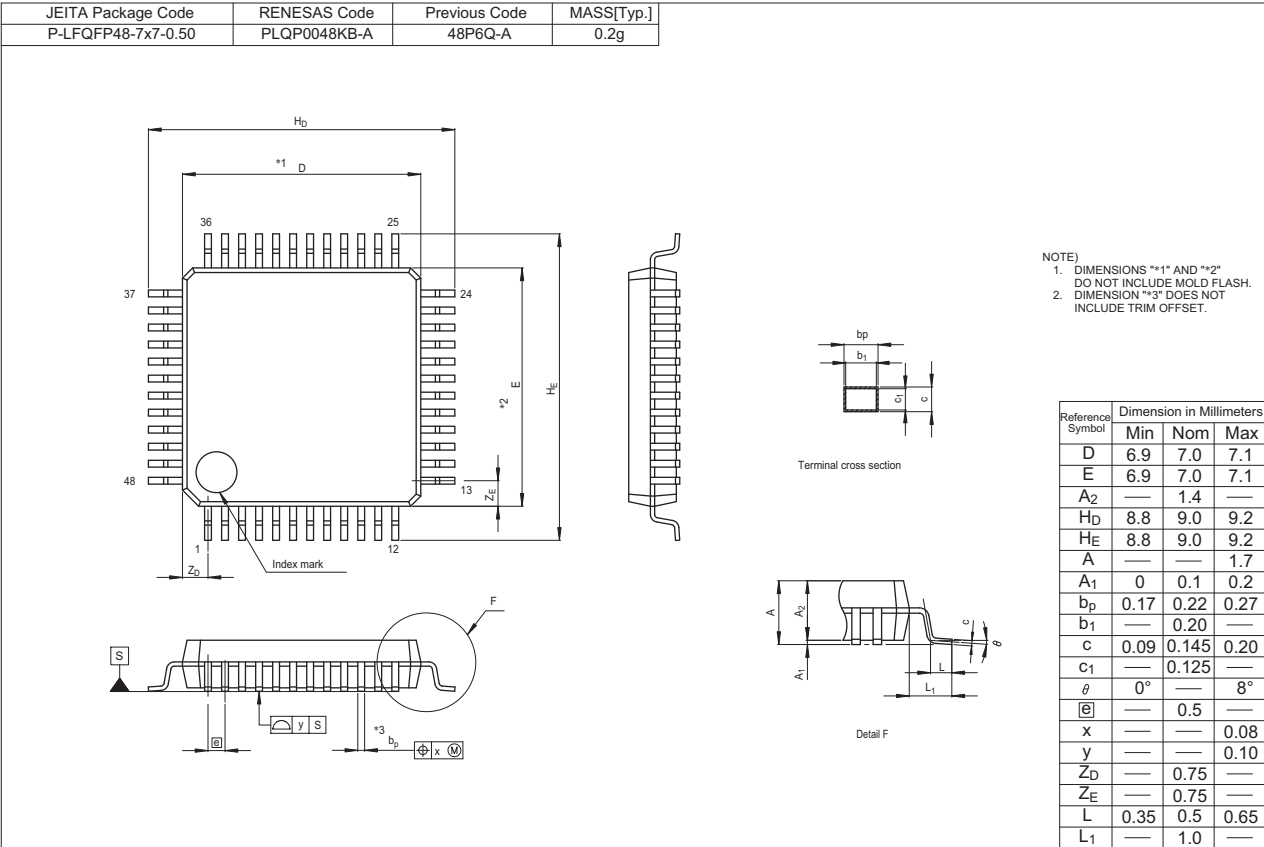


Figure J 48-pin LQFP (PLQP0048KB-A)

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

- The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

- The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

- The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

- When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

- The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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Renesas Electronics Corporation

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Renesas Electronics America Inc.

2801 Scott Boulevard Santa Clara, CA 95050-2549, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited

1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited

Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH

Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.

Room 1709, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100191, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.

Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, P. R. China 200333
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited

Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.

13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.

80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.

Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd.

12F., 234 Teheran-ro, Gangnam-Ku, Seoul, 135-920, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141