# Renesas Electronics America Inc - R5F563NWHDFC#V0 Datasheet

**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | RX |
| Core Size | 32-Bit Single-Core |
| Speed | 100MHz |
| Connectivity | CANbus, EBI/EMI, Ethernet, I²C, LINbus, SCI, SPI, USB |
| Peripherals | DMA, LVD, POR, PWM, WDT |
| Number of I/O | 133 |
| Program Memory Size | 1MB (1M x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 32K x 8 |
| RAM Size | 192K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 3.6V |
| Data Converters | A/D 8x10b, 21x12b; D/A 2x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 176-LQFP |
| Supplier Device Package | 176-LFQFP (24x24) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f563nwhdfc-v0 |

**Table 1.1 Outline of Specifications (5/6)**

| Classification | Module/Function | Description |
|---|---|---|
| Communication function | Ethernet controller (ETHERC) | • Input and output of Ethernet/IEEE 802.3 frames<br>• Transfer at 10 or 100 Mbps<br>• Full- and half-duplex modes<br>• MII (Media Independent Interface) or RMII (Reduced Media Independent Interface) as defined in IEEE 802.3u<br>• Detection of Magic Packets™*1 or output of a "wake-on-LAN" signal (WOL)<br>• Compliance with flow control as defined in IEEE 802.3x standards<br>Note 1. Magic PacketTM is a registered trademark of Advanced Micro Devices, Inc. |
| | DMA controller for Ethernet controller (EDMAC) | • Alleviation of CPU loads by the descriptor control method<br>• Transmission FIFO: 2 Kbytes; Reception FIFO: 2 Kbytes |
| | USB 2.0 host/function module (USBa) | • Includes a UDC (USB Device Controller) and transceiver for USB 2.0<br>• Host/function module: one port, function module: one port<br>• Compliance with the USB 2.0 specification<br>• Transfer rate: Full speed (12 Mbps)<br>• Self-power mode and bus-power mode are selectable<br>• OTG (On the Go) operation is possible<br>• Incorporates 2 Kbytes of RAM as a transfer buffer |
| | Serial communications interfaces (SCIc, SCId) | • 13 channels (SCIc: 12 channels + SCId: 1 channel)<br>• SCIc<br>Serial communications modes: Asynchronous, clock synchronous, and smart-card interface<br>Multi-processor function<br>On-chip baud rate generator allows selection of the desired bit rate<br>Choice of LSB-first or MSB-first transfer<br>Average transfer rate clock can be input from TMR timers for SCI5, SCI6, and SCI12<br>Simple $I^2C$<br>Simple SPI<br>• SCId (The following functions are added to SCIc)<br>Supports the serial communications protocol, which contains the start frame and information frame<br>Supports the LIN format |
| | $I^2C$ bus interfaces (RIIC) | • 4 channels (one of them is FM+)<br>• Communication formats<br>$I^2C$ bus format/SMBus format<br>Supports the multi-master<br>Max. transfer rate: 1 Mbps (channel 0) |
| | IEBus (IEB) | • 1 channel<br>• Supports protocol control for the IEBus<br>Half-duplex asynchronous transfer<br>Multi-master operation<br>Broadcast communications function<br>Two selectable modes, differentiated by transfer rate |
| | CAN module (CAN) | • 3 channels<br>• Compliance with the ISO11898-1 specification (standard frame and extended frame)<br>• 32 mailboxes each |
| | Serial peripheral interfaces (SPI) | • 3 channels<br>• RSPI transfer facility<br>Using the MOSI (master out, slave in), MISO (master in, slave out), SSL (slave select), and RSPCK (RSPI clock) signals enables serial transfer through SPI operation (four lines) or clock-synchronous operation (three lines)<br>Capable of handling serial transfer as a master or slave<br>• Data formats<br>Switching between MSB first and LSB first<br>The number of bits in each transfer can be changed to any number of bits from 8 to 16, or to 20, 24, or 32 bits.<br>128-bit buffers for transmission and reception<br>Up to four frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits)<br>• Buffered structure<br>Double buffers for both transmission and reception |

**Table 1.3 List of Products (8/8)**

| Group | Part No. | Package | ROM Capacity | RAM Capacity | E2 Data Flash | Operating Frequency (Max.) | Operating Temp. Range |
|---|---|---|---|---|---|---|---|
| RX631 (G version) *2 | R5F5631GDGFB | PLQP0144KA-A | 1.5 Mbytes | 192 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F5631DDGFB | PLQP0144KA-A | 1.5 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F5631YDGFB | PLQP0144KA-A | 1 Mbyte | 256 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F5631WDGFB | PLQP0144KA-A | 1 Mbyte | 192 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F5631BDGFB | PLQP0144KA-A | 1 Mbyte | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F5631ADGFB | PLQP0144KA-A | 768 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F56318SGFB | PLQP0144KA-A | 512 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F56318DGFB | PLQP0144KA-A | 512 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F56317SGFB | PLQP0144KA-A | 384 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F56317DGFB | PLQP0144KA-A | 384 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F56316SGFB | PLQP0144KA-A | 256 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F56316DGFB | PLQP0144KA-A | 256 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F5631FDGFP | PLQP0100KB-A | 2 Mbytes | 256 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F5631KDGFP | PLQP0100KB-A | 2 Mbytes | 192 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F5631EDGFP | PLQP0100KB-A | 2 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F5631JDGFP | PLQP0100KB-A | 1.5 Mbytes | 256 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F5631GDGFP | PLQP0100KB-A | 1.5 Mbytes | 192 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F5631DDGFP | PLQP0100KB-A | 1.5 Mbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F5631YDGFP | PLQP0100KB-A | 1 Mbyte | 256 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F5631WDGFP | PLQP0100KB-A | 1 Mbyte | 192 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F5631BDGFP | PLQP0100KB-A | 1 Mbyte | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F5631ADGFP | PLQP0100KB-A | 768 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F56318DGFP | PLQP0100KB-A | 512 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F56317DGFP | PLQP0100KB-A | 384 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F56316DGFP | PLQP0100KB-A | 256 Kbytes | 128 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F5631PDGFM | PLQP0064KB-A | 512 Kbytes | 64 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F5631NDGFM | PLQP0064KB-A | 384 Kbytes | 64 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F5631MDGFM | PLQP0064KB-A | 256 Kbytes | 64 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F5631PDGFL | PLQP0048KB-A | 512 Kbytes | 64 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F5631NDGFL | PLQP0048KB-A | 384 Kbytes | 64 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |
| | R5F5631MDGFL | PLQP0048KB-A | 256 Kbytes | 64 Kbytes | 32 Kbytes | 100 MHz | -40 to +105°C |

Note 1. In the planning stage

Note 2. The specifications of the temperature sensor calibration and unique ID for G-version products differ from those for other products. For details, see section 45.2.2, Temperature Sensor Calibration Data Registers (TSCDRH, TSCDRL), section 45.3, Using the Temperature Sensor, and section 47.2.22, Unique ID Registers n (UIDRn) (n = 0 to 15) in the User's manual: Hardware.

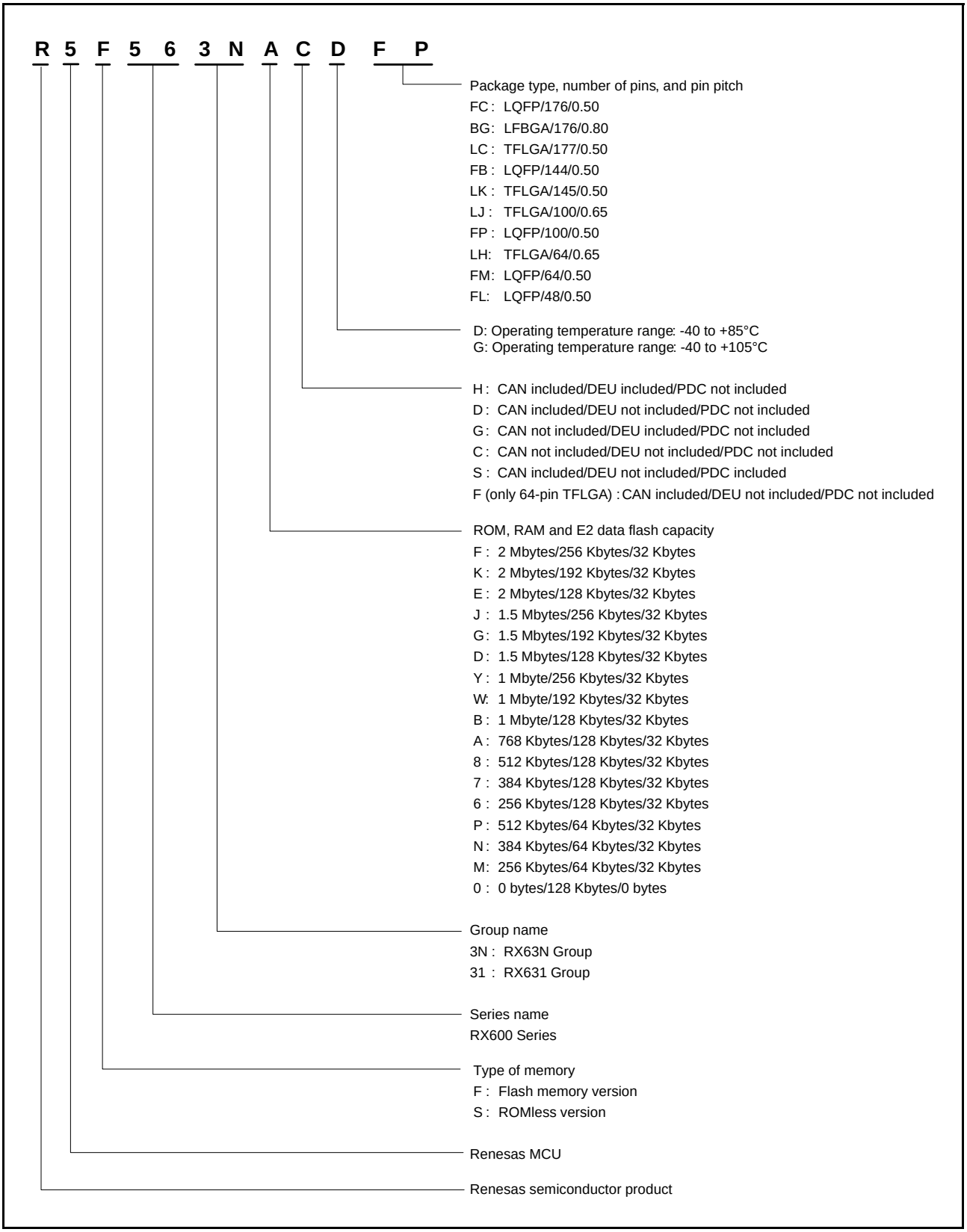



**Figure 1.1 How to Read the Product Part No.**

**Table 1.9 List of Pins and Pin Functions (100-Pin TFLGA) (1/5)**

| Pin No. 100-pin TFLGA | Power Supply Clock System Control | I/O Port | Bus EXDMAC | Timers (MTU, TPU, TMR, PPG, RTC, POE) | Communications (ETHERC, SCIc, SCId, RSPI, RIIC, CAN, IEB, USB) | Interrupt | S12AD AD DA |
|---|---|---|---|---|---|---|---|
| A1 | | P05 | | | | IRQ13 | DA1 |
| A2 | VREFH | | | | | | |
| A3 | | P07 | | | | IRQ15 | ADTRG0# |
| A4 | VREFL0 | | | | | | |
| A5 | | P43 | | | | IRQ11-DS | AN003 |
| A6 | | PD0 | D0[A0/D0] | | | IRQ0 | AN008 |
| A7 | | PD4 | D4[A4/D4] | POE3# | | IRQ4 | AN012 |
| A8 | | PE0 | D8[A8/D8] | | SCK12/SSLB1 | | ANEX0 |
| A9 | | PE1 | D9[A9/D9] | MTIOC4C/ PO18 | TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12/SSLB2/ RSPCKB | | ANEX1 |
| A10 | | PE2 | D10[A10/D10] | MTIOC4A/ PO23 | RXD12/SMISO12/ SSCL12/RXDX12/ SSLB3/MOSIB | IRQ7-DS | AN0 |
| B1 | EMLE | | | | | | |
| B2 | AVSS0 | | | | | | |
| B3 | AVCC0 | | | | | | |
| B4 | | P40 | | | | IRQ8-DS | AN000 |
| B5 | | P44 | | | | IRQ12-DS | AN004 |
| B6 | | PD1 | D1[A1/D1] | MTIOC4B | CTX0*1 | IRQ1 | AN009 |
| B7 | | PD3 | D3[A3/D3] | POE8# | | IRQ3 | AN011 |
| B8 | | PD6 | D6[A6/D6] | MTIC5V/ POE1# | | IRQ6 | AN6 |
| B9 | | PD7 | D7[A7/D7] | MTIC5U/ POE0# | | IRQ7 | AN7 |
| B10 | | PE3 | D11[A11/D11] | MTIOC4B/ PO26/POE8# | CTS12#/RTS12#/ SS12#/MISOB/ ET_ERXD3 | | AN1 |
| C1 | VCL | | | | | | |
| C2 | VREFL | | | | | | |
| C3 | | PJ3 | | MTIOC3C | CTS6#/RTS6#/ CTS0#/RTS0#/ SS6#/SS0# | | |
| C4 | VREFH0 | | | | | | |
| C5 | | P42 | | | | IRQ10-DS | AN002 |
| C6 | | P47 | | | | IRQ15-DS | AN007 |
| C7 | | PD2 | D2[A2/D2] | MTIOC4D | CRX0*1 | IRQ2 | AN010 |
| C8 | | PD5 | D5[A5/D5] | MTIC5W/ POE2# | | IRQ5 | AN013 |
| C9 | | PE5 | D13[A13/D13] | MTIOC4C/ MTIOC2B | RSPCKB/ ET_RX_CLK/ REF50CK | IRQ5 | AN3 |
| C10 | | PE4 | D12[A12/D12] | MTIOC4D/ MTIOC1A/ PO28 | SSLB0/ET_ERXD2 | | AN2 |
| D1 | XCIN | | | | | | |

**Table 1.11 List of Pins and Pin Functions (64-Pin TFLGA) (1/2)**

| Pin No. 64-pin TFLGA | Power Supply Clock System Control | I/O Port | Timers (MTU2a, TPUa, TMR, PPG, RTCa, POE2a) | Communications (SCIc, SCId, RSPI, RIIC, CAN, IEB, USB) | Interrupt | S12ADa, DAa |
|---|---|---|---|---|---|---|
| A1 | | P05 | | | IRQ13 | DA1 |
| A2 | AVCC0 | | | | | |
| A3 | VREFH0 | | | | | |
| A4 | VREFL0 | | | | | |
| A5 | VREFH | | | | | |
| A6 | VREFL | | | | | |
| A7 | | PE2 | MTIOC4A/PO23 | RXD12/SMISO12/SSCL12/ RXDX12/SSLB3/MOSIB | IRQ7-DS | AN010 |
| A8 | | PE3 | MTIOC4B/PO26/POE8# | CTS12#/RTS12#/SS12#/ MISOB | | AN011 |
| B1 | VCL | | | | | |
| B2 | AVSS0 | | | | | |
| B3 | | P40 | | | IRQ8-DS | AN000 |
| B4 | | P42 | | | IRQ10-DS | AN002 |
| B5 | | P44 | | | IRQ12-DS | AN004 |
| B6 | | P46 | | | IRQ14-DS | AN006 |
| B7 | | PE1 | MTIOC4C/PO18 | TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/SSLB2/ RSPCKB | | AN009 |
| B8 | | PE4 | MTIOC4D/MTIOC1A/PO28 | SSLB0 | | AN012 |
| C1 | XCIN | | | | | |
| C2 | MD/FINED | | | | | |
| C3 | EMLE | | | | | |
| C4 | | P41 | | | IRQ9-DS | AN001 |
| C5 | | P43 | | | IRQ11-DS | AN003 |
| C6 | | PE0 | | SCK12/SSLB1 | | AN008 |
| C7 | | PE5 | MTIOC4C/MTIOC2B | RSPCKB | IRQ5 | AN013 |
| C8 | | PA0 | MTIOC4A/TIOCA0/PO16 | SSLA1 | | |
| D1 | XCOUT | | | | | |
| D2 | RES# | | | | | |
| D3 | TCK FINEC | P27 | MTIOC2B/TMCI3 | SCK1/RSPCKB | | |
| D4 | | P14 | MTIOC3A/MTCLKA/ TIOCB5/TCLKA/TMRI2 | CTS1#/RTS1#/SS1#/CTX1/ USB0_DPUPE/ USB0_OVRCURA | IRQ4 | |
| D5 | | PA6 | MTIC5V/MTCLKB/TIOCA2/ TMCI3/PO22/POE2# | CTS5#/RTS5#/SS5#/ MOSIA | | |
| D6 | | PA4 | MTIC5U/MTCLKA/TIOCA1/ TMRI0/PO20 | TXD5/SMOSI5/SSDA5/ SSLA0 | IRQ5-DS | |
| D7 | | PA1 | MTIOC0B/MTCLKC/ TIOCB0/PO17 | SCK5/SSLA2/SCL2 | IRQ11 | |
| D8 | | PA3 | MTIOC0D/MTCLKD/ TIOCD0/TCLKB/PO19 | RXD5/SMISO5/SSCL5/ SDA2 | IRQ6-DS | |
| E1 | VSS | | | | | |
| E2 | VBATT | | | | | |
| E3 | TDI | P30 | MTIOC4B/TMRI3/POE8#/ RTCIC0 | RXD1/SMISO1/SSCL1/ MISOB/USB0_DRPD | IRQ0-DS | |

**Table 1.12 List of Pins and Pin Functions (64-Pin LQFP) (1/3)**

| Pin Number 64-Pin LQFP | Power Supply Clock System Control | I/O Port | Timer (MTU2a, TPUa, TMR, PPG, RTCa, POE2a) | Timer Communications (SCIc, SCId, RSPI, RIIC, CAN, IEB, USB) | Interrupt | S12ADa, DAa |
|---|---|---|---|---|---|---|
| 1 | EMLE | | | | | |
| 2 | VCL | | | | | |
| 3 | MD/FINED | | | | | |
| 4 | XCIN | | | | | |
| 5 | XCOUT | | | | | |
| 6 | RES# | | | | | |
| 7 | XTAL | P37 | | | | |
| 8 | VSS | | | | | |
| 9 | EXTAL | P36 | | | | |
| 10 | VCC | | | | | |
| 11 | | P35 | | | NMI | |
| 12 | VBATT | | | | | |
| 13 | | P31 | MTIOC4D/TMCI2/PO9/ RTCIC1 | CTS1#/RTS1#/SS1#/ SSLB0/USB0_DPUPE | IRQ1-DS | |
| 14 | TDI | P30 | MTIOC4B/TMRI3/PO8/ POE8#/RTCIC0 | RXD1/SMISO1/SSCL1/ MISOB/USB0_DRPD | IRQ0-DS | |
| 15 | TCK/FINEC | P27 | MTIOC2B/TMCI3/PO7 | SCK1/RSPCKB | | |
| 16 | TDO | P26 | MTIOC2A/TMO1/PO6 | TXD1/SMOSI1/SSDA1/ MOSIB/USB0_VBUSEN | | |
| 17 | TRST# | P17 | MTIOC3A/MTIOC3B/ TIOCB0/TCLKD/TMO1/ PO15/POE8# | SCK1/MISOA/ SDA2-DS/IETXD | IRQ7 | |
| 18 | TMS | P16 | MTIOC3C/MTIOC3D/ TIOCB1/TCLKC/TMO2/ PO14/RTCOUT | TXD1/SMOSI1/SSDA1/ MOSIA/SCL2-DS/IERXD/ USB0_VBUS/ USB0_VBUSEN/ USB0_OVRCURB | IRQ6 | ADTRG0# |
| 19 | | P15 | MTIOC0B/MTCLKB/ TIOCB2/TCLKB/TMCI2/ PO13 | RXD1/SMISO1/SSCL1/ CRX1-DS | IRQ5 | |
| 20 | | P14 | MTIOC3A/MTCLKA/ TIOCB5/TCLKA/TMRI2/ PO15 | CTS1#/RTS1#/SS1#/ CTX1/USB0_DPUPE/ USB0_OVRCURA | IRQ4 | |
| 21 | VCC_USB | | | | | |
| 22 | | | | USB0_DM | | |
| 23 | | | | USB0_DP | | |
| 24 | VSS_USB | | | | | |
| 25 | | P55 | MTIOC4D/TMO3 | CRX1 | IRQ10 | |
| 26 | | P54 | MTIOC4B/TMCI1 | CTX1 | | |
| 27 | | PC7 | MTIOC3A/ MTCLKB/TMO2 /PO31 | TXD8/SMOSI8/SSDA8/ MISOA | IRQ14 | |
| 28 | | PC6 | MTIOC3C/MTCLKA/ TMCI2/PO30 | RXD8/SMISO8/SSCL8/ MOSIA/USB0_EXICEN | IRQ13 | |
| 29 | | PC5 | MTIOC3B/MTCLKD/ TMRI2/PO29 | SCK8/RSPCKA/USB0_ID | | |
| 30 | | PC4 | MTIOC3D/MTCLKC/ TMCI1/PO25/POE0# | SCK5/CTS8#/RTS8#/SS8#/ SSLA0/USB0_DPRPD | | |
| 31 | | PC3 | MTIOC4D/TCLKB/ PO24 | TXD5/SMOSI5/SSDA5/ IETXD | | |

**Table 4.1 List of I/O Registers (Address Order) (8/50)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access States | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK≥PCLK | ICLK<PCLK | |
| 0008 70CBh | ICU | Interrupt request register 203 | IR203 | 8 | 8 | 2 ICLK | | ICUb |
| 0008 70D6h | ICU | Interrupt request register 214 | IR214 | 8 | 8 | 2 ICLK | | |
| 0008 70D7h | ICU | Interrupt request register 215 | IR215 | 8 | 8 | 2 ICLK | | |
| 0008 70D8h | ICU | Interrupt request register 216 | IR216 | 8 | 8 | 2 ICLK | | |
| 0008 70D9h | ICU | Interrupt request register 217 | IR217 | 8 | 8 | 2 ICLK | | |
| 0008 70DAh | ICU | Interrupt request register 218 | IR218 | 8 | 8 | 2 ICLK | | |
| 0008 70DBh | ICU | Interrupt request register 219 | IR219 | 8 | 8 | 2 ICLK | | |
| 0008 70DCh | ICU | Interrupt request register 220 | IR220 | 8 | 8 | 2 ICLK | | |
| 0008 70DDh | ICU | Interrupt request register 221 | IR221 | 8 | 8 | 2 ICLK | | |
| 0008 70DEh | ICU | Interrupt request register 222 | IR222 | 8 | 8 | 2 ICLK | | |
| 0008 70DFh | ICU | Interrupt request register 223 | IR223 | 8 | 8 | 2 ICLK | | |
| 0008 70E0h | ICU | Interrupt request register 224 | IR224 | 8 | 8 | 2 ICLK | | |
| 0008 70E1h | ICU | Interrupt request register 225 | IR225 | 8 | 8 | 2 ICLK | | |
| 0008 70E2h | ICU | Interrupt request register 226 | IR226 | 8 | 8 | 2 ICLK | | |
| 0008 70E3h | ICU | Interrupt request register 227 | IR227 | 8 | 8 | 2 ICLK | | |
| 0008 70E4h | ICU | Interrupt request register 228 | IR228 | 8 | 8 | 2 ICLK | | |
| 0008 70E5h | ICU | Interrupt request register 229 | IR229 | 8 | 8 | 2 ICLK | | |
| 0008 70E6h | ICU | Interrupt request register 230 | IR230 | 8 | 8 | 2 ICLK | | |
| 0008 70E7h | ICU | Interrupt request register 231 | IR231 | 8 | 8 | 2 ICLK | | |
| 0008 70E8h | ICU | Interrupt request register 232 | IR232 | 8 | 8 | 2 ICLK | | |
| 0008 70E9h | ICU | Interrupt request register 233 | IR233 | 8 | 8 | 2 ICLK | | |
| 0008 70EAh | ICU | Interrupt request register 234 | IR234 | 8 | 8 | 2 ICLK | | |
| 0008 70EBh | ICU | Interrupt request register 235 | IR235 | 8 | 8 | 2 ICLK | | |
| 0008 70ECh | ICU | Interrupt request register 236 | IR236 | 8 | 8 | 2 ICLK | | |
| 0008 70EDh | ICU | Interrupt request register 237 | IR237 | 8 | 8 | 2 ICLK | | |
| 0008 70EEh | ICU | Interrupt request register 238 | IR238 | 8 | 8 | 2 ICLK | | |
| 0008 70EFh | ICU | Interrupt request register 239 | IR239 | 8 | 8 | 2 ICLK | | |
| 0008 70F0h | ICU | Interrupt request register 240 | IR240 | 8 | 8 | 2 ICLK | | |
| 0008 70F1h | ICU | Interrupt request register 241 | IR241 | 8 | 8 | 2 ICLK | | |
| 0008 70F2h | ICU | Interrupt request register 242 | IR242 | 8 | 8 | 2 ICLK | | |
| 0008 70F3h | ICU | Interrupt request register 243 | IR243 | 8 | 8 | 2 ICLK | | |
| 0008 70F4h | ICU | Interrupt request register 244 | IR244 | 8 | 8 | 2 ICLK | | |
| 0008 70F5h | ICU | Interrupt request register 245 | IR245 | 8 | 8 | 2 ICLK | | |
| 0008 70F6h | ICU | Interrupt request register 246 | IR246 | 8 | 8 | 2 ICLK | | |
| 0008 70F7h | ICU | Interrupt request register 247 | IR247 | 8 | 8 | 2 ICLK | | |
| 0008 70F8h | ICU | Interrupt request register 248 | IR248 | 8 | 8 | 2 ICLK | | |
| 0008 70F9h | ICU | Interrupt request register 249 | IR249 | 8 | 8 | 2 ICLK | | |
| 0008 70FAh | ICU | Interrupt request register 250 | IR250 | 8 | 8 | 2 ICLK | | |
| 0008 70FBh | ICU | Interrupt request register 251 | IR251 | 8 | 8 | 2 ICLK | | |
| 0008 70FCh | ICU | Interrupt request register 252 | IR252 | 8 | 8 | 2 ICLK | | |
| 0008 70FDh | ICU | Interrupt request register 253 | IR253 | 8 | 8 | 2 ICLK | | |
| 0008 711Bh | ICU | DTC activation enable register 027 | DTCER027 | 8 | 8 | 2 ICLK | | |
| 0008 711Ch | ICU | DTC activation enable register 028 | DTCER028 | 8 | 8 | 2 ICLK | | |
| 0008 711Dh | ICU | DTC activation enable register 029 | DTCER029 | 8 | 8 | 2 ICLK | | |
| 0008 711Eh | ICU | DTC activation enable register 030 | DTCER030 | 8 | 8 | 2 ICLK | | |
| 0008 711Fh | ICU | DTC activation enable register 031 | DTCER031 | 8 | 8 | 2 ICLK | | |
| 0008 7121h | ICU | DTC activation enable register 033 | DTCER033 | 8 | 8 | 2 ICLK | | |
| 0008 7122h | ICU | DTC activation enable register 034 | DTCER034 | 8 | 8 | 2 ICLK | | |
| 0008 7124h | ICU | DTC activation enable register 036 | DTCER036 | 8 | 8 | 2 ICLK | | |
| 0008 7125h | ICU | DTC activation enable register 037 | DTCER037 | 8 | 8 | 2 ICLK | | |
| 0008 7127h | ICU | DTC activation enable register 039 | DTCER039 | 8 | 8 | 2 ICLK | | |

**Table 4.1 List of I/O Registers (Address Order) (16/50)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access States | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK≥PCLK | ICLK<PCLK | |
| 0008 814Ch | TPU3 | Timer general register C | TGRC | 16 | 16 | 2, 3 PCLKB | 2 ICLK | TPUa |
| 0008 814Eh | TPU3 | Timer general register D | TGRD | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8150h | TPU4 | Timer control register | TCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8151h | TPU4 | Timer mode register | TMDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8152h | TPU4 | Timer I/O control register | TIOR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8154h | TPU4 | Timer interrupt enable register | TIER | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8155h | TPU4 | Timer status register | TSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8156h | TPU4 | Timer counter | TCNT | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8158h | TPU4 | Timer general register A | TGRA | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 815Ah | TPU4 | Timer general register B | TGRB | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8160h | TPU5 | Timer control register | TCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8161h | TPU5 | Timer mode register | TMDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8162h | TPU5 | Timer I/O control register | TIOR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8164h | TPU5 | Timer interrupt enable register | TIER | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8165h | TPU5 | Timer status register | TSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8166h | TPU5 | Timer counter | TCNT | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8168h | TPU5 | Timer general register A | TGRA | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 816Ah | TPU5 | Timer general register B | TGRB | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8170h | TPUB | Timer start register | TSTR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8171h | TPUB | Timer synchronous register | TSYR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8178h | TPU6 | Noise filter control register | NFCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8179h | TPU7 | Noise filter control register | NFCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 817Ah | TPU8 | Noise filter control register | NFCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 817Bh | TPU9 | Noise filter control register | NFCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 817Ch | TPU10 | Noise filter control register | NFCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 817Dh | TPU11 | Noise filter control register | NFCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8180h | TPU6 | Timer control register | TCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8181h | TPU6 | Timer mode register | TMDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8182h | TPU6 | Timer I/O control register H | TIORH | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8183h | TPU6 | Timer I/O control register L | TIORL | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8184h | TPU6 | Timer interrupt enable register | TIER | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8185h | TPU6 | Timer status register | TSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8186h | TPU6 | Timer counter | TCNT | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8188h | TPU6 | Timer general register A | TGRA | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 818Ah | TPU6 | Timer general register B | TGRB | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 818Ch | TPU6 | Timer general register C | TGRC | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 818Eh | TPU6 | Timer general register D | TGRD | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8190h | TPU7 | Timer control register | TCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8191h | TPU7 | Timer mode register | TMDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8192h | TPU7 | Timer I/O control register | TIOR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8194h | TPU7 | Timer interrupt enable register | TIER | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8195h | TPU7 | Timer status register | TSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8196h | TPU7 | Timer counter | TCNT | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 8198h | TPU7 | Timer general register A | TGRA | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 819Ah | TPU7 | Timer general register B | TGRB | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 81A0h | TPU8 | Timer control register | TCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 81A1h | TPU8 | Timer mode register | TMDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 81A2h | TPU8 | Timer I/O control register | TIOR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 81A4h | TPU8 | Timer interrupt enable register | TIER | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 81A5h | TPU8 | Timer status register | TSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 81A6h | TPU8 | Timer counter | TCNT | 16 | 16 | 2, 3 PCLKB | 2 ICLK | |

**Table 4.1 List of I/O Registers (Address Order) (30/50)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access States | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK≥PCLK | ICLK<PCLK | |
| 0008 C046h | PORT6 | Port input data register | PIDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C047h | PORT7 | Port input data register | PIDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C048h | PORT8 | Port input data register | PIDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C049h | PORT9 | Port input data register | PIDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C04Ah | PORTA | Port input data register | PIDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C04Bh | PORTB | Port input data register | PIDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C04Ch | PORTC | Port input data register | PIDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C04Dh | PORTD | Port input data register | PIDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C04Eh | PORTE | Port input data register | PIDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C04Fh | PORTF | Port input data register | PIDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C050h | PORTG | Port input data register | PIDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C052h | PORTJ | Port input data register | PIDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C060h | PORT0 | Port input data register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C061h | PORT1 | Port input data register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C062h | PORT2 | Port mode register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C063h | PORT3 | Port mode register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C064h | PORT4 | Port mode register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C065h | PORT5 | Port mode register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C066h | PORT6 | Port mode register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C067h | PORT7 | Port mode register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C068h | PORT8 | Port mode register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C069h | PORT9 | Port mode register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C06Ah | PORTA | Port mode register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C06Bh | PORTB | Port mode register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C06Ch | PORTC | Port mode register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C06Dh | PORTD | Port mode register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C06Eh | PORTE | Port mode register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C06Fh | PORTF | Port mode register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C070h | PORTG | Port mode register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C072h | PORTJ | Port mode register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C080h | PORT0 | Open drain control register 0 | ODR0 | 8 | 8, 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C081h | PORT0 | Open drain control register 1 | ODR1 | 8 | 8, 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C082h | PORT1 | Open drain control register 0 | ODR0 | 8 | 8, 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C083h | PORT1 | Open drain control register 1 | ODR1 | 8 | 8, 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C084h | PORT2 | Open drain control register 0 | ODR0 | 8 | 8, 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C085h | PORT2 | Open drain control register 1 | ODR1 | 8 | 8, 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C086h | PORT3 | Open drain control register 0 | ODR0 | 8 | 8, 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C087h | PORT3 | Open drain control register 1 | ODR1 | 8 | 8, 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C088h | PORT4 | Open drain control register 0 | ODR0 | 8 | 8, 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C089h | PORT4 | Open drain control register 1 | ODR1 | 8 | 8, 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C08Ah | PORT5 | Open drain control register 0 | ODR0 | 8 | 8, 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C08Bh | PORT5 | Open drain control register 1 | ODR1 | 8 | 8, 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C08Ch | PORT6 | Open drain control register 0 | ODR0 | 8 | 8, 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C08Dh | PORT6 | Open drain control register 1 | ODR1 | 8 | 8, 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C08Eh | PORT7 | Open drain control register 0 | ODR0 | 8 | 8, 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C08Fh | PORT7 | Open drain control register 1 | ODR1 | 8 | 8, 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C090h | PORT8 | Open drain control register 0 | ODR0 | 8 | 8, 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C091h | PORT8 | Open drain control register 1 | ODR1 | 8 | 8, 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C092h | PORT9 | Open drain control register 0 | ODR0 | 8 | 8, 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C093h | PORT9 | Open drain control register 1 | ODR1 | 8 | 8, 16 | 2, 3 PCLKB | 2 ICLK | |
| 0008 C094h | PORTA | Open drain control register 0 | ODR0 | 8 | 8, 16 | 2, 3 PCLKB | 2 ICLK | |

**Table 4.1 List of I/O Registers (Address Order) (43/50)**

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access States | | Related Function |
|---|---|---|---|---|---|---|---|---|
| | | | | | | ICLK≥PCLK | ICLK<PCLK | |
| 000A 00D0h | USB0 | Device address 0 configuration register | DEVADD0 | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6 | |
| 000A 00D2h | USB0 | Device address 1 configuration register | DEVADD1 | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6 | USBa |
| 000A 00D4h | USB0 | Device address 2 configuration register | DEVADD2 | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6 | |
| 000A 00D6h | USB0 | Device address 3 configuration register | DEVADD3 | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6 | |
| 000A 00D8h | USB0 | Device address 4 configuration register | DEVADD4 | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6 | |
| 000A 00DAh | USB0 | Device address 5 configuration register | DEVADD5 | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6 | |
| 000A 0200h | USB1 | System configuration control register | SYSCFG | 16 | 16 | 3 to 4 PCLKB | 2, 3 ICLK | |
| 000A 0204h | USB1 | System configuration status register 0 | SYSSTS0 | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6 | |
| 000A 0208h | USB1 | Device state control register 0 | DVSTCTR0 | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB)*6 | |
| 000A 0214h | USB1 | CFIFO port register | CFIFO | 16 | 8, 16 | 3 to 4 PCLKB | 2, 3 ICLK | |
| 000A 0218h | USB1 | D0FIFO port register | D0FIFO | 16 | 8, 16 | 3 to 4 PCLKB | 2, 3 ICLK | |
| 000A 021Ch | USB1 | D1FIFO port register | D1FIFO | 16 | 8, 16 | 3 to 4 PCLKB | 2, 3 ICLK | |
| 000A 0220h | USB1 | CFIFO port select register | CFIFOSEL | 16 | 16 | 3 to 4 PCLKB | 2, 3 ICLK | |
| 000A 0222h | USB1 | CFIFO port control register | CFIFOCTR | 16 | 16 | 3 to 4 PCLKB | 2, 3 ICLK | |
| 000A 0228h | USB1 | D0FIFO port select register | D0FIFOSEL | 16 | 16 | 3 to 4 PCLKB | 2, 3 ICLK | USBa |
| 000A 022Ah | USB1 | D0FIFO port control register | D0FIFOCTR | 16 | 16 | 3 to 4 PCLKB | 2, 3 ICLK | |
| 000A 022Ch | USB1 | D1FIFO port select register | D1FIFOSEL | 16 | 16 | 3 to 4 PCLKB | 2, 3 ICLK | |
| 000A 022Eh | USB1 | D1FIFO port control register | D1FIFOCTR | 16 | 16 | 3 to 4 PCLKB | 2, 3 ICLK | |

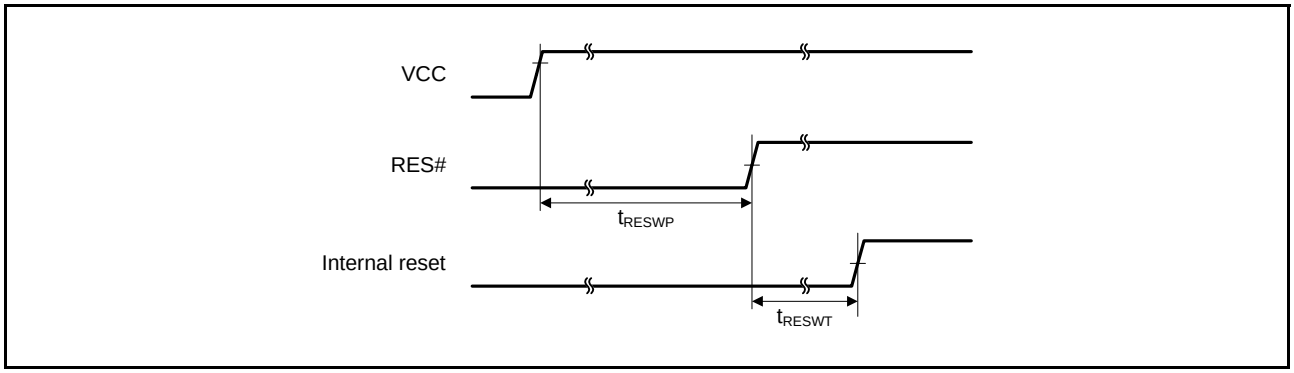



**Figure 5.1 Reset Input Timing at Power-On**

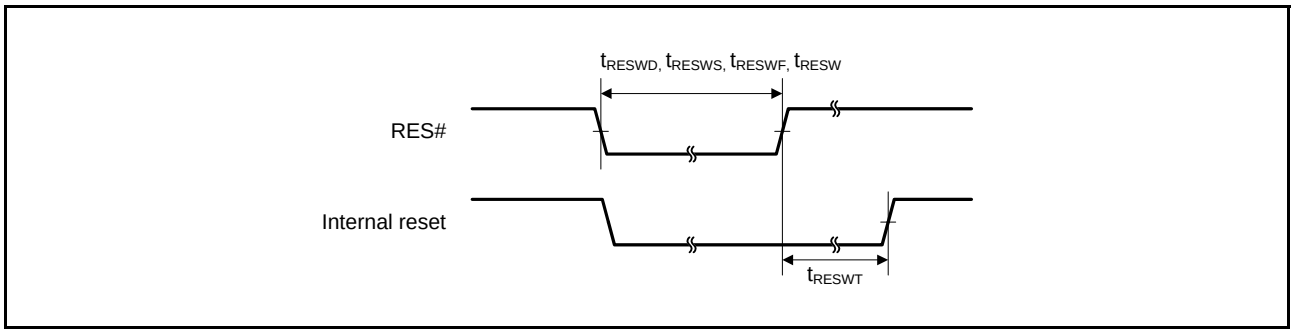



**Figure 5.2 Reset Input Timing**

### Table 5.13 Clock Timing (Sub-Clock Related)

Conditions: VCC = AVCC0 = VREFH = VCC_USB = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0, $V_{BATT}$ = 2.0 to 3.6 V (for products with 100 pins or more), $V_{BATT}$ = 2.3 to 3.6 V (for the 64-pin product),
VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V, $T_a = T_{opr}$

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Sub-clock frequency | $f_{SUB}$ | — | 32.768 | — | kHz | |
| Sub-clock oscillator start-up time | $t_{SUBOSC}$ | — | — | *1 | | Figure 5.12 |
| Sub-clock oscillation stabilization wait offset time*3 | $t_{SUBOSCWT0}$ | 1.8 | — | 2.6 | s | |
| Sub-clock oscillation stabilization wait time | $t_{SUBOSCWT}$ | — | — | *2 | s | |

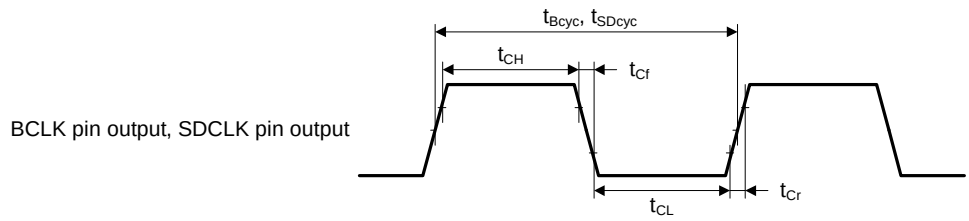
Note 1. When using a sub-clock, ask the manufacturer of the oscillator to evaluate its oscillation. Refer to the results of evaluation provided by the manufacturer for the oscillation stabilization time.

Note 2. The number of cycles n selected by the value of the SOSCWTCR.SSTS[4:0] bits determines the sub-clock oscillation stabilization waiting time in accord with the formula below.

$$t_{SUBOSCWT} = \max\left(t_{SUBOSC}, t_{SUBOSCWT0}\right) + \frac{n}{f_{SUB}}$$

The notation “max ($t_{SUBOSC}$, $t_{SUBOSCWT0}$)“ indicates whichever is higher of $t_{SUBOSC}$ and $t_{SUBOSCWT0}$.

Note 3. The minimum value and maximum value of the sub-clock oscillation stabilization wait offset time (tSUBOSCWT0) is the references only for 100-pin or more products. For 64-pin products, consider the value of tSUBOSCWT0 to be 0.




Test conditions: VOH = VCC × 0.7, VOL = VCC × 0.3, IOH = –1.0 mA, IOL = 1.0 mA, C = 30 pF

**Figure 5.3 BCLK Pin Output, SDCLK Pin Output Timing**

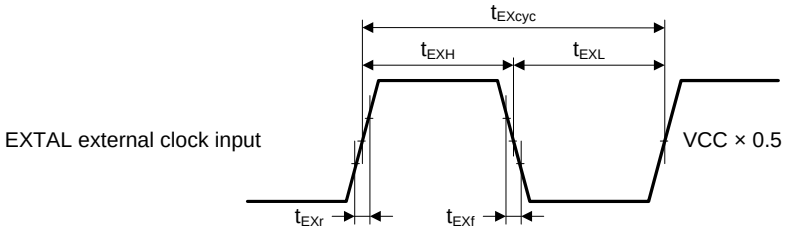



**Figure 5.4 EXTAL External Clock Input Timing**

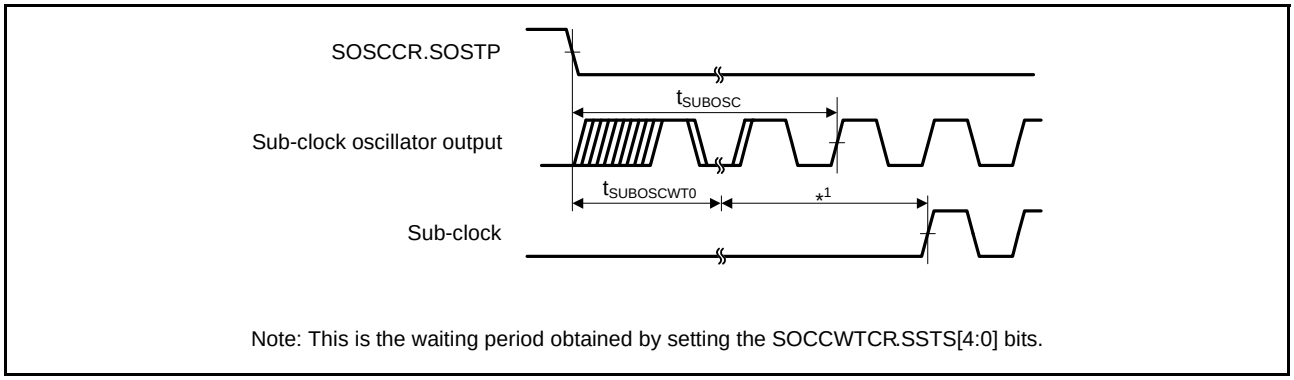



**Figure 5.12 Sub-Clock Oscillation Start Timing**

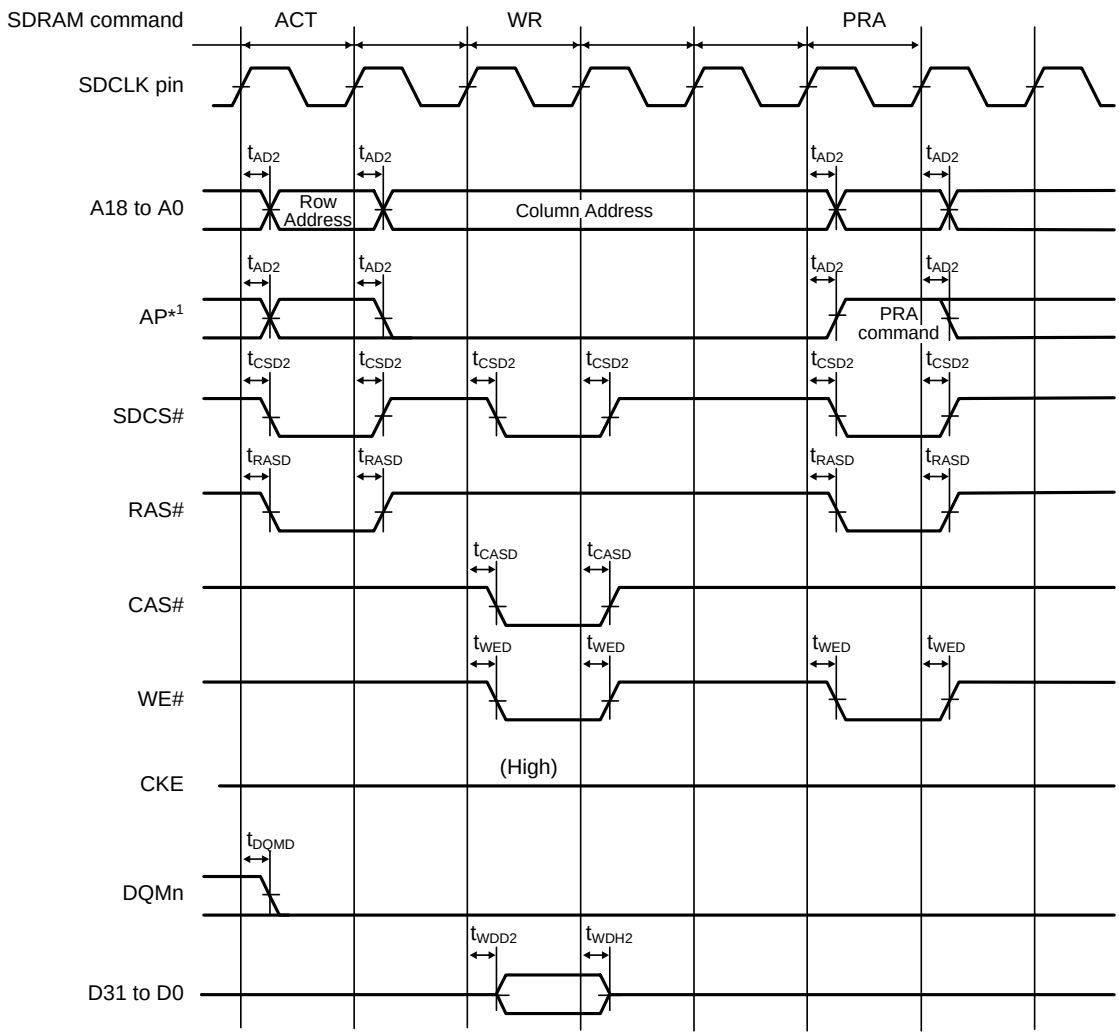
## 5.3.3 Timing of Recovery from Low Power Consumption Modes

**Table 5.14 Timing of Recovery from Low Power Consumption Modes**

Conditions: VCC = AVCC0 = VREFH = VCC_USB = $V_{BATT}$ = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0,
VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V, $T_a = T_{opr}$

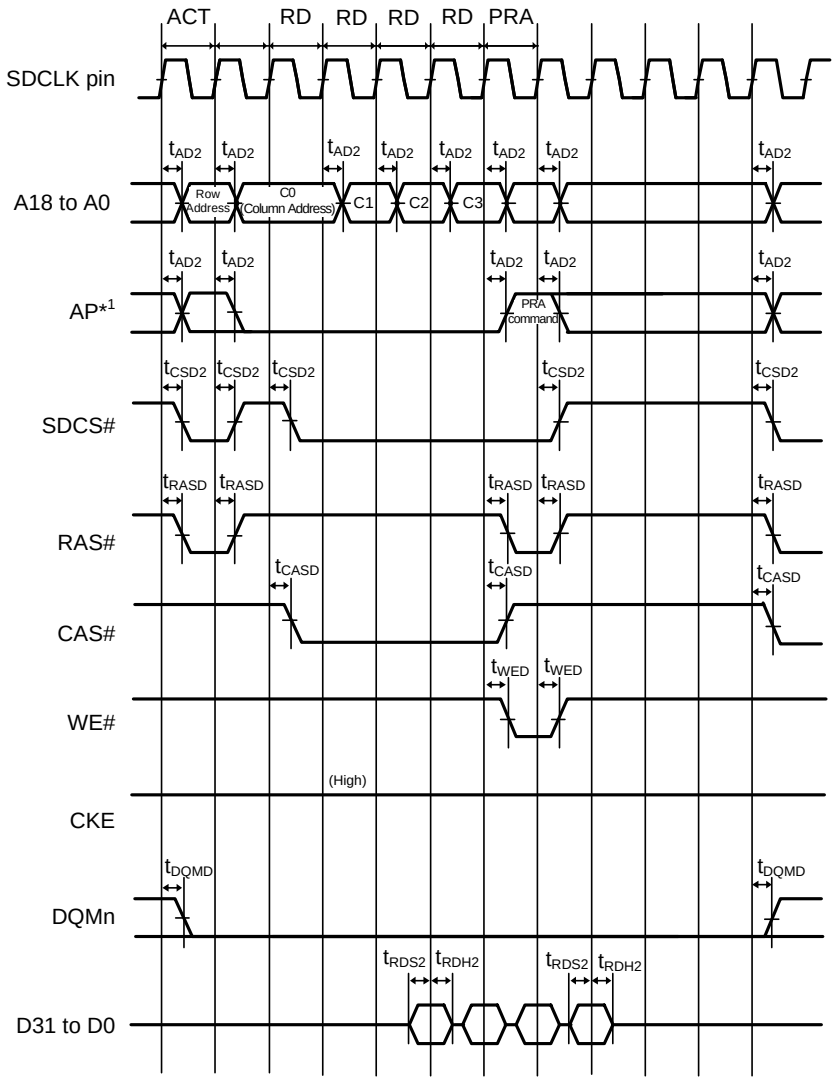
| Item | | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|---|
| Recovery time after cancellation of software standby mode | Crystal resonator connected to main clock oscillator | Main clock oscillator operating | $t_{SBYMC}$ | 10 | — | — | ms | Figure 5.13 |
| | | Main clock oscillator and PLL circuit operating | $t_{SBYPC}$ | 10 | — | — | ms | |
| | External clock input to main clock oscillator | Main clock oscillator operating | $t_{SBYEX}$ | 1 | — | — | ms | |
| | | Main clock oscillator and PLL circuit operating | $t_{SBYPE}$ | 1 | — | — | ms | |
| | Sub-clock oscillator operating | | $t_{SBYSC}$ | 2 | — | — | s | |
| | High-speed on-chip oscillator operating | | $t_{SBYHO}$ | — | — | 2 | ms | |
| | Low-speed on-chip oscillator or IWDT-dedicated on-chip oscillator operating | | $t_{SBYLO}$ | — | — | 800 | µs | |
| Recovery time after cancellation of deep software standby mode | | | $t_{DSBY}$ | — | — | 1.0 | ms | Figure 5.14 |
| Wait time after cancellation of deep software standby mode | | | $t_{DSBYWT}$ | 45 | — | 46 | $t_{cyc}$ | |

Note: The wait time varies depending on the state in which each oscillator was when the WAIT instruction was executed. The recovery time when multiple oscillators are operating is the same period as that when the oscillator which requires the longest time of all operating oscillators to recover is operating alone.




Note 1: Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

**Figure 5.25 SDRAM Space Single Write Bus Timing**




Note 1: Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

**Figure 5.26 SDRAM Space Multiple Read Bus Timing**

### Table 5.23 Timing of On-Chip Peripheral Modules (5)

Conditions: VCC = AVCC0 = VREFH = VCC_USB = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0
VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V
PCLK = 8 to 50 MHz
$T_a = T_{opr}$
High drive output is selected by the drive capacity control register.

| Item | | Symbol | Min.*1,*2 | Max.* | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| RIIC (Standard-mode, SMBus) ICFER.FMPE = 0 | SCL input cycle time | $t_{SCL}$ | 6(12) × $t_{IICcyc}$ + 1300 | — | ns | Figure 5.47 |
| | SCL input high pulse width | $t_{SCLH}$ | 3(6) × $t_{IICcyc}$ + 300 | — | ns | |
| | SCL input low pulse width | $t_{SCLL}$ | 3(6) × $t_{IICcyc}$ + 300 | — | ns | |
| | SCL, SDA input rise time | $t_{Sr}$ | — | 1000 | ns | |
| | SCL, SDA input fall time | $t_{Sf}$ | — | 300 | ns | |
| | SCL, SDA input spike pulse removal time | $t_{SP}$ | 0 | 1(4) × $t_{IICcyc}$ | ns | |
| | SDA input bus free time | $t_{BUF}$ | 3(6) × $t_{IICcyc}$ + 300 | — | ns | |
| | Start condition input hold time | $t_{STAH}$ | $t_{IICcyc}$ + 300 | — | ns | |
| | Restart condition input setup time | $t_{STAS}$ | 1000 | — | ns | |
| | Stop condition input setup time | $t_{STOS}$ | 1000 | — | ns | |
| | Data input setup time | $t_{SDAS}$ | $t_{IICcyc}$ + 50 | — | ns | |
| | Data input hold time | $t_{SDAH}$ | 0 | — | ns | |
| | SCL, SDA capacitive load | $C_b$ | — | 400 | pF | |
| RIIC (Fast-mode) | SCL input cycle time | $t_{SCL}$ | 6(12) × $t_{IICcyc}$ + 600 | — | ns | |
| | SCL input high pulse width | $t_{SCLH}$ | 3(6) × $t_{IICcyc}$ + 300 | — | ns | |
| | SCL input low pulse width | $t_{SCLL}$ | 3(6) × $t_{IICcyc}$ + 300 | — | ns | |
| | SCL, SDA input rise time | $t_{Sr}$ | 20 + 0.1$C_b$ | 300 | ns | |
| | SCL, SDA input fall time | $t_{Sf}$ | 20 + 0.1$C_b$ | 300 | ns | |
| | SCL, SDA input spike pulse removal time | $t_{SP}$ | 0 | 1(4) × $t_{IICcyc}$ | ns | |
| | SDA input bus free time | $t_{BUF}$ | 3(6) × $t_{IICcyc}$ + 300 | — | ns | |
| | Start condition input hold time | $t_{STAH}$ | $t_{IICcyc}$ + 300 | — | ns | |
| | Restart condition input setup time | $t_{STAS}$ | 300 | — | ns | |
| | Stop condition input setup time | $t_{STOS}$ | 300 | — | ns | |
| | Data input setup time | $t_{SDAS}$ | $t_{IICcyc}$ + 50 | — | ns | |
| | Data input hold time | $t_{SDAH}$ | 0 | — | ns | |
| | SCL, SDA capacitive load | $C_b$ | — | 400 | pF | |

Note: $t_{IICcyc}$: RIIC internal reference clock (IICϕ) Cycle
Note 1. The value within parentheses is applicable when the value of the ICMR3.NF[1:0] bits is 11b while the digital filter is enabled by the setting ICFER.NFE = 1.
Note 2. Cb is the total capacitance of the bus lines.

## 5.12 $E^2$ Flash Characteristics

### Table 5.38 E2 Flash Characteristics (1)

Conditions: VCC = AVCC0 = VREFH = VCC_USB = 2.7 to 3.6V, VREFH0 = 2.7V to AVCC0
VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0V
Temperature range for the programming/erasure operation: $T_a = T_{opr}$

| Item | Symbol | min | typ | max | Unit | Condition |
|---|---|---|---|---|---|---|
| Reprogram/erasure cycle*1 | $N_{DPEC}$ | 100000 | — | — | Times | |
| Data hold time | $t_{DDRP}$ | 30*2 | — | — | Year | Ta = +85°C |

Note 1. Definition of reprogram/erase cycle:
The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 100000), erasing can be performed n times for each block. For instance, when 128-byte programming is performed 16 times for different addresses in 2-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).
Note 2. The result obtained from the reliability test.

### Table 5.39 $E^2$ Flash Characteristics (2)

Conditions: VCC = AVCC0 = VREFH = VCC_USB = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0
VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V
Temperature range for the programming/erasure operation: $T_a = T_{opr}$

| Item | | Symbol | FCLK = 4 MHz | | | 20 MHz ≤ FCLK ≤ 50 MHz | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| Programming time $N_{PEC} \leq 100$ times | 2 bytes | $t_{DP2}$ | — | 0.7 | 6 | — | 0.25 | 2 | ms |
| Programming time $N_{PEC} > 100$ times | 2 bytes | $t_{DP2}$ | — | 0.7 | 6 | — | 0.25 | 2 | ms |
| Erasure time $N_{PEC} \leq 100$ times | 32 bytes | $t_{DE32}$ | — | 4 | 40 | — | 2 | 20 | ms |
| Erasure time $N_{PEC} > 100$ times | 32 bytes | $t_{DE32}$ | — | 7 | 40 | — | 4 | 20 | ms |
| Blank check time | 2 bytes | $t_{DBC2}$ | — | — | 100 | — | — | 30 | µs |
| Suspend delay time during programming | | $t_{DSPD}$ | — | — | 250 | — | — | 120 | µs |
| First suspend delay time during erasure (in suspend priority mode) | | $t_{DSESD1}$ | — | — | 250 | — | — | 120 | µs |
| Second suspend delay time during erasure (in suspend priority mode) | | $t_{DSESD2}$ | — | — | 500 | — | — | 300 | µs |
| Suspend delay time during erasure (in erasure priority mode) | | $t_{DSEED}$ | — | — | 500 | — | — | 300 | µs |

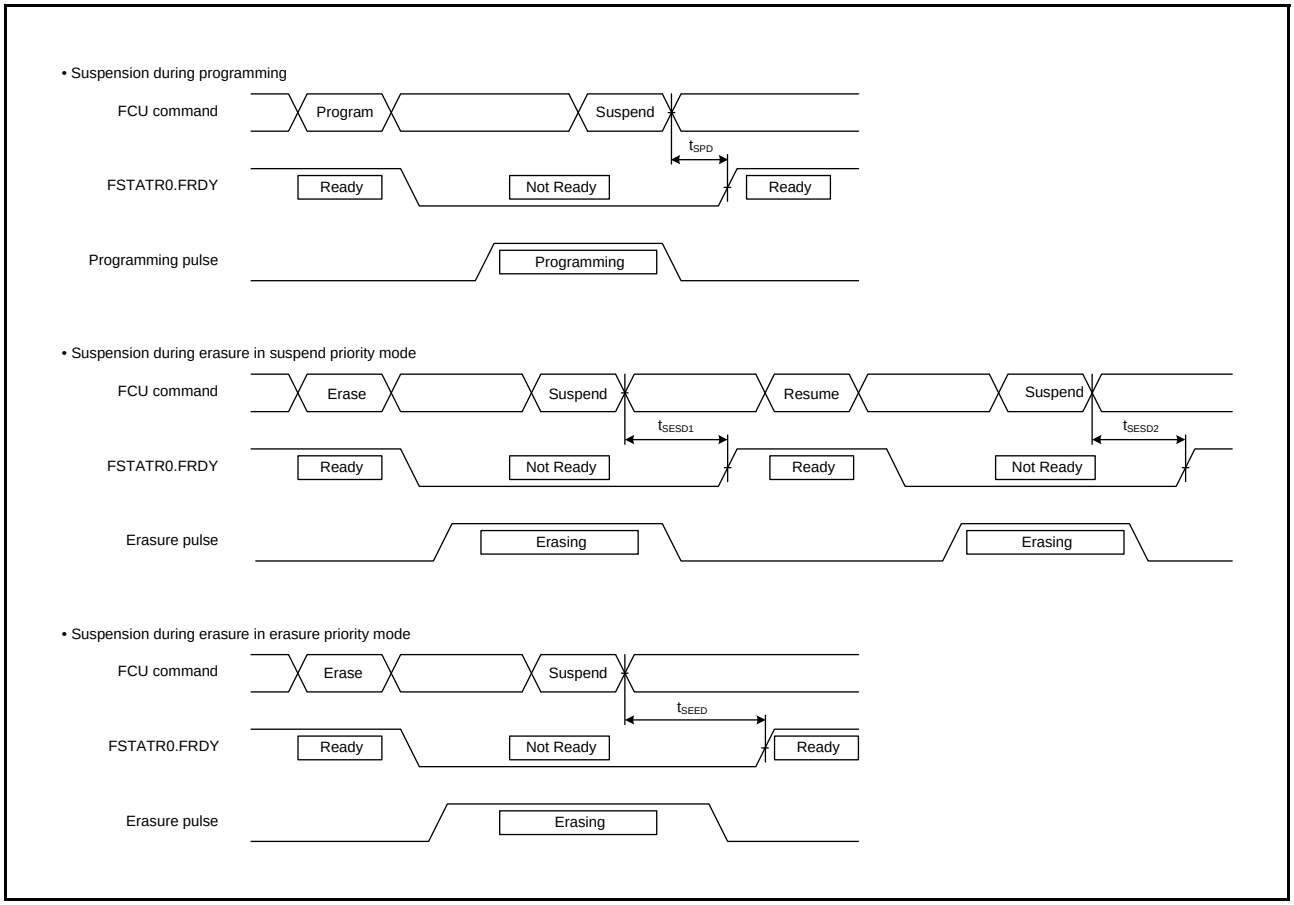



**Figure 5.69 Flash Memory Program/Erase Suspend Timing**

## 5.13 Boundary Scan

**Table 5.40** Boundary Scan

Conditions: VCC = AVCC0 = VREFH = VCC_USB = 2.7 to 3.6V, VREFH0 = 2.7V to AVCC0
VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0V
$T_a = T_{opr}$

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| TCK clock cycle time | $t_{TCKcyc}$ | 100 | — | — | ns | Figure 5.70 |
| TCK clock high pulse width | $t_{TCKH}$ | 45 | — | — | ns | |
| TCK clock low pulse width | $t_{TCKL}$ | 45 | — | — | ns | |
| TCK clock rise time | $t_{TCKr}$ | — | — | 5 | ns | |
| TCK clock fall time | $t_{TCKf}$ | — | — | 5 | ns | |
| TRST# pulse width | $t_{TRSTW}$ | 20 | — | — | $t_{TCKcyc}$ | Figure 5.71 |
| TMS setup time | $t_{TMSS}$ | 20 | — | — | ns | Figure 5.72 |
| TMS hold time | $t_{TMSH}$ | 20 | — | — | ns | |
| TDI setup time | $t_{TDIS}$ | 20 | — | — | ns | |
| TDI hold time | $t_{TDIH}$ | 20 | — | — | ns | |
| TDO data delay time | $t_{TDOD}$ | — | — | 40 | ns | |

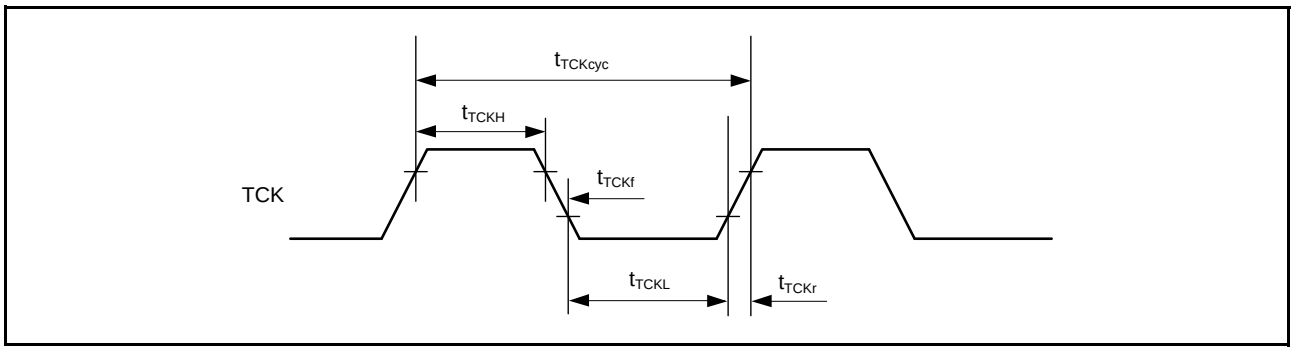



**Figure 5.70 Boundary Scan TCK Timing**

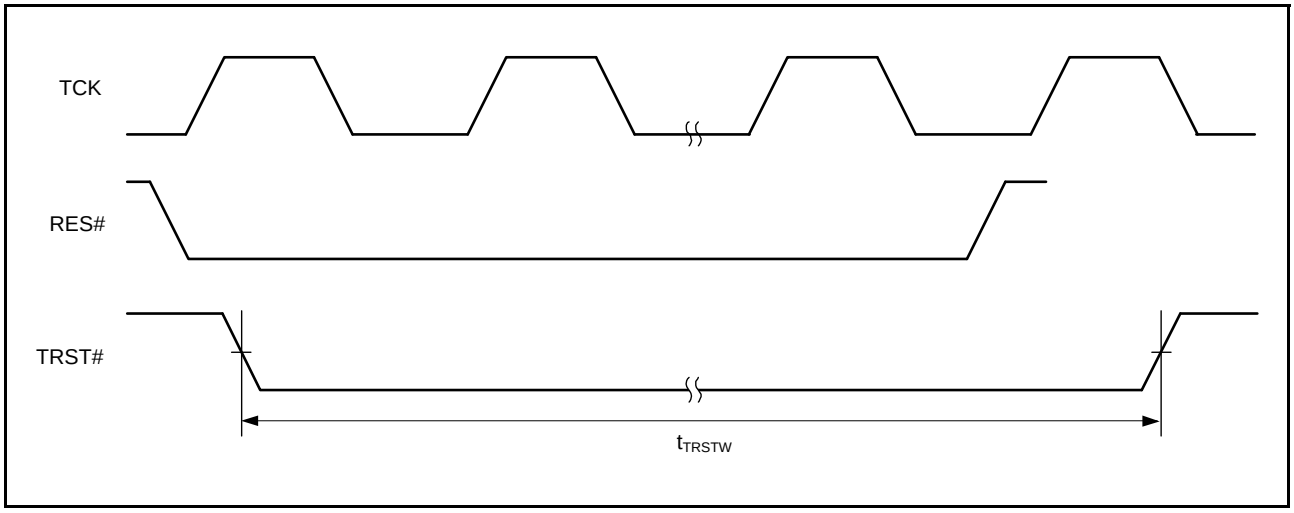
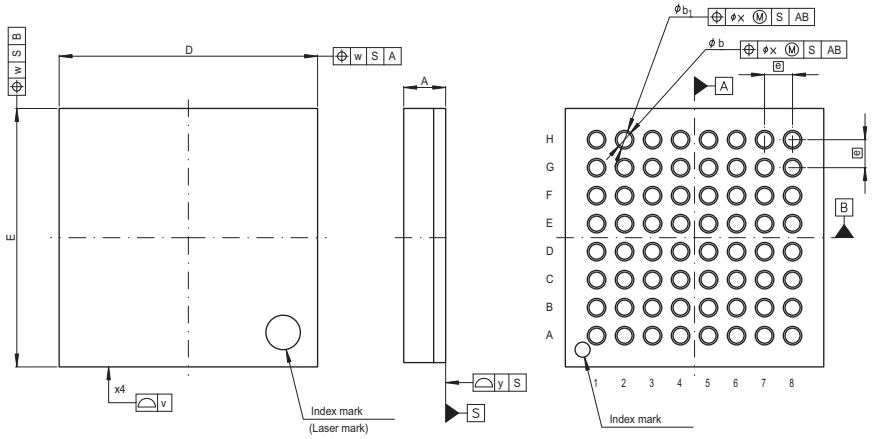



**Figure 5.71 Boundary Scan TRST# Timing**

| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-TFLGA64-6x6-0.65 | PTLG0064JA-A | 64F0G | 0.07g |




| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | — | 6.0 | — |
| E | — | 6.0 | — |
| v | — | — | 0.15 |
| w | — | — | 0.20 |
| A | — | — | 1.05 |
| e | — | 0.65 | — |
| b | 0.31 | 0.35 | 0.39 |
| $b_1$ | 0.39 | 0.43 | 0.47 |
| x | — | — | 0.08 |
| y | — | — | 0.10 |

Figure H 64-pin TFLGA (PTLG0064JA-A)