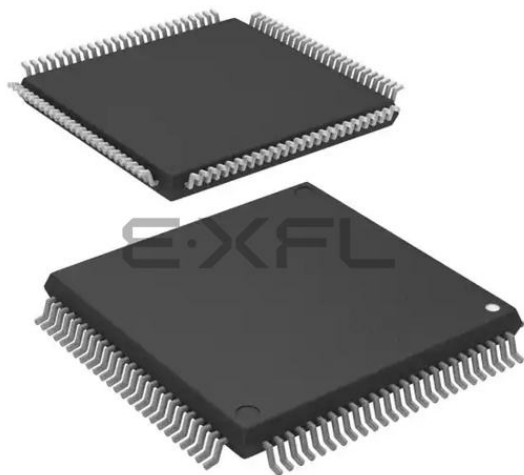




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Details

Product Status	Discontinued at Digi-Key
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, LINbus, SCI, SPI, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	78
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b, 14x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f563nwhdfp-v0

Table 1.3 List of Products (3/8)

Group	Part No.	Package	ROM Capacity	RAM Capacity	E2 Data Flash	Operating Frequency (Max.)	Operating Temp. Range
RX63N (D version)	R5F563NYHDFP	PLQP0100KB-A	1 Mbyte	256 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NYDDFP	PLQP0100KB-A	1 Mbyte	256 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NWHDFP	PLQP0100KB-A	1 Mbyte	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NWDDFP	PLQP0100KB-A	1 Mbyte	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NWGDFP	PLQP0100KB-A*1	1 Mbyte	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NWCDFP	PLQP0100KB-A*1	1 Mbyte	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NBCDFP	PLQP0100KB-A	1 Mbyte	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NBDDFP	PLQP0100KB-A	1 Mbyte	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NACDFP	PLQP0100KB-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NADDFP	PLQP0100KB-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
RX63N (G version) *2	R5F563NFHGFC	PLQP0176KB-A	2 Mbytes	256 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NFDGFC	PLQP0176KB-A	2 Mbytes	256 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NKDGFC	PLQP0176KB-A	2 Mbytes	192 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NEDGFC	PLQP0176KB-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NDDGFC	PLQP0176KB-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NYHGFC	PLQP0176KB-A	1 Mbyte	256 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NYDGFC	PLQP0176KB-A	1 Mbyte	256 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NWHGFC	PLQP0176KB-A	1 Mbyte	192 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NWDGFC	PLQP0176KB-A	1 Mbyte	192 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NBDGFC	PLQP0176KB-A	1 Mbyte	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NADGFC	PLQP0176KB-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NFHGF	PLQP0144KA-A	2 Mbytes	256 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NFDGF	PLQP0144KA-A	2 Mbytes	256 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NKDGF	PLQP0144KA-A	2 Mbytes	192 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NEDGF	PLQP0144KA-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NDDGF	PLQP0144KA-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NYHGF	PLQP0144KA-A	1 Mbyte	256 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NYDGF	PLQP0144KA-A	1 Mbyte	256 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NWHGF	PLQP0144KA-A	1 Mbyte	192 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NWDGF	PLQP0144KA-A	1 Mbyte	192 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NBDGF	PLQP0144KA-A	1 Mbyte	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NADGF	PLQP0144KA-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NFHGF	PLQP0100KB-A	2 Mbytes	256 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NFDGF	PLQP0100KB-A	2 Mbytes	256 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NKDGF	PLQP0100KB-A	2 Mbytes	192 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NEDGF	PLQP0100KB-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NDDGF	PLQP0100KB-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NYHGF	PLQP0100KB-A	1 Mbyte	256 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NYDGF	PLQP0100KB-A	1 Mbyte	256 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NWHGF	PLQP0100KB-A	1 Mbyte	192 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NWDGF	PLQP0100KB-A	1 Mbyte	192 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NBDGF	PLQP0100KB-A	1 Mbyte	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
	R5F563NADGF	PLQP0100KB-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +105°C
RX631 (D version)	R5F5631ECDLC	PTLG0177KA-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F5631EDDLC	PTLG0177KA-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C

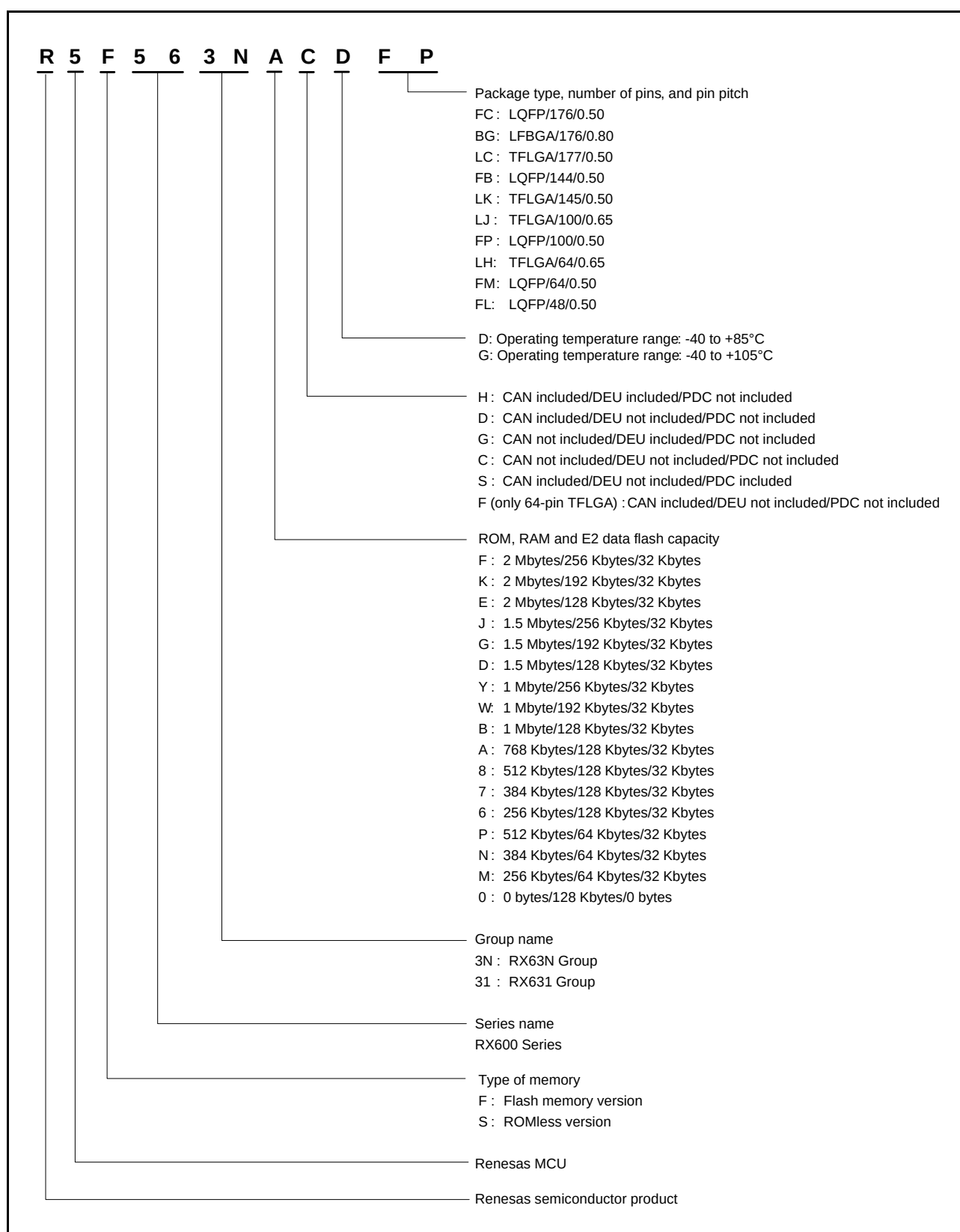


Figure 1.1 How to Read the Product Part No.

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	
15	PE2	PE3	P70	P65	P67	VSS	VCC	PG7	PA6	PB0	P72	PB4	VSS	VCC	PC1	15
14	PE1	PE0	VSS	PE7	PG3	PA0	PA1	PA2	PA7	VCC	PB1	PB5	P73	P75	P74	14
13	P63	P64	PE4	VCC	PG2	PG4	PG6	PA3	VSS	P71	PB3	PB7	PC0	PC2	P76	13
12	P60	VSS	P62	PE5	PE6	P66	PG5	PA4	PA5	PB2	PB6	P77	PC3	PC4	P80	12
11	PD6	PG1	VCC	P61	RX63N Group RX631 Group PTBG0176GA-A (176-pin LFBGA) (Top perspective view)							P81	P82	PC6	VCC	11
10	P97	PD4	PG0	PD7								PC5	PC7	P83	VSS	10
9	VCC	P96	PD3	PD5								P50	P51	P52	P84	9
8	P94	PD1	PD2	VSS								P53	VCC_USB	USB1_DP	USB1_DM	8
7	VSS	P92	PD0	P95								P54	P55	VSS_USB	USB0_DP	7
6	VCC	P91	P90	P93								P56	P57	VCC_USB	USB0_DM	6
5	P46	P47	P45	P44								P13	P12	P10	P11	5
4	P42	P41	P43	P00	VSS	BSCANP	PF4	P35	PF3	PF1	P25	P86	P15	P14	P85	4
3	VREFL0	P40	VREFH0	P03	PF5	PJ3	MD/FINED	RES#	P34	PF2	PF0	P24	P22	P87	P16	3
2	AVCC0	P07	VREFH	P02	EMLE	VCL	XCOUT	VSS	VCC	P32	P30	P26	P23	P17	P20	2
1	AVSS0	P05	VREFL	P01	PJ5	VBATT	XCIN	XTAL	EXTAL	P33	P31	P27	VCC	VSS	P21	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	

Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.5, List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA).

Figure 1.4 Pin Assignment (176-Pin LFBGA)

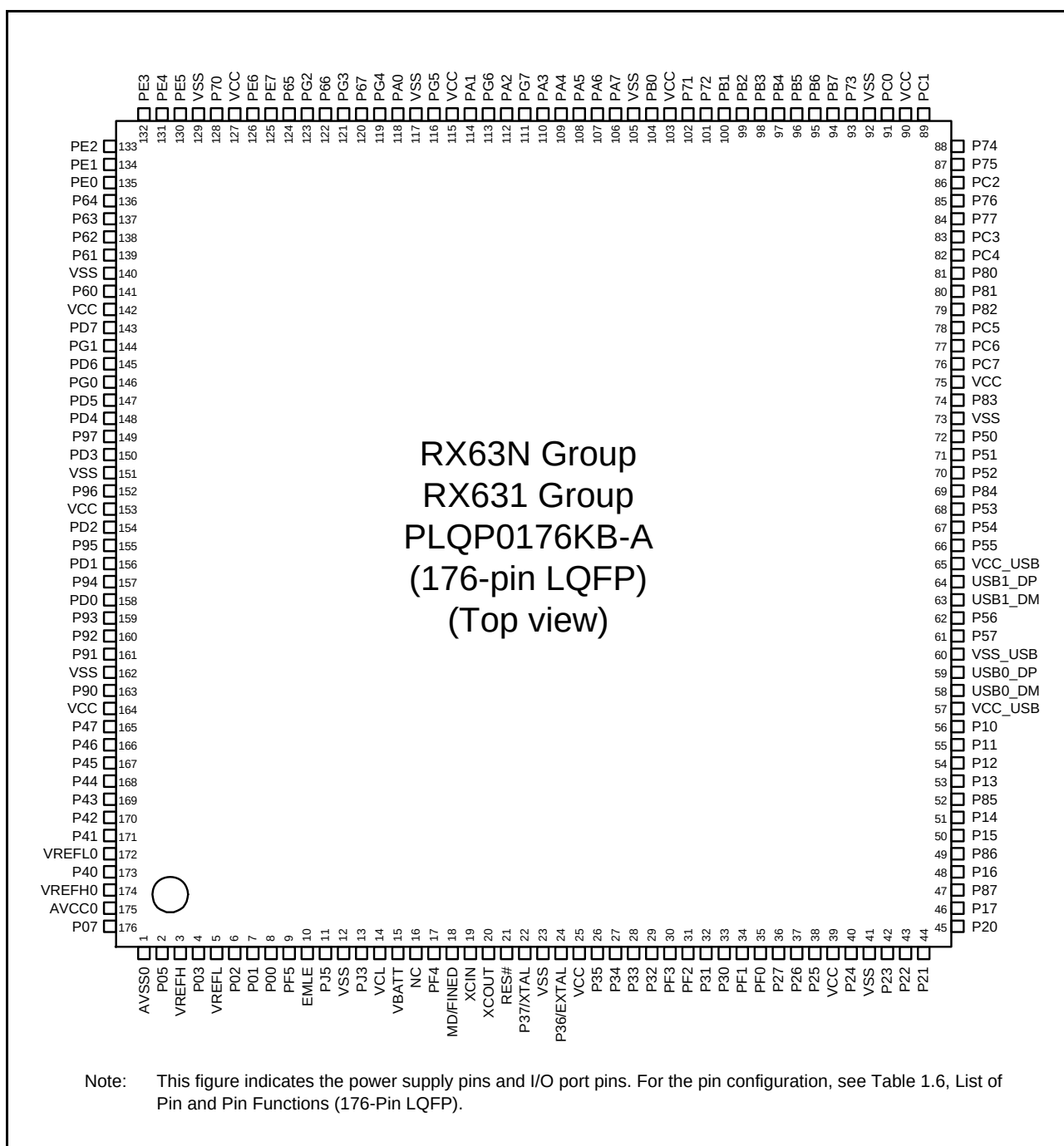
**Figure 1.5 Pin Assignment (176-Pin LQFP)**

Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (1/5)

Pin Number 177-Pin TFLGA 176-Pin LFBGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SCIC, SCID, RSPI, RIIC, CAN, IEB, USB, and PDC)	Interrupt	S12AD, AD, DA
A1	AVSS0						
A2	AVCC0						
A3	VREFL0						
A4		P42				IRQ10-DS	AN002
A5		P46				IRQ14-DS	AN006
A6	VCC						
A7	VSS						
A8		P94	A20/D20				
A9	VCC						
A10		P97	A23/D23				
A11		PD6	D6[A6/D6]	MTIC5V/POE1#	SSLC2	IRQ6	AN6
A12		P60	CS0#				
A13		P63	CS3#/CAS#				
A14		PE1	D9[A9/D9]	MTIOC4C/TIOCD9/PO18	TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12/SSLB2/RSPCKB		ANEX1
A15		PE2	D10[A10/D10]	MTIOC4A/TIOCA9/PO23	RXD12/SMISO12/ SSCL12/RXDX12/SSLB3/ MOSIB	IRQ7-DS	AN0
B1		P05				IRQ13	DA1
B2		P07				IRQ15	ADTRG0#
B3		P40				IRQ8-DS	AN000
B4		P41				IRQ9-DS	AN001
B5		P47				IRQ15-DS	AN007
B6		P91	A17/D17		SCK7		AN015
B7		P92	A18/D18		RXD7/SMISO7/SSCL7		AN016
B8		PD1	D1[A1/D1]	MTIOC4B/TIOCB7/ TCLKG	MOSIC/CTX0	IRQ1	AN009
B9		P96	A22/D22				
B10		PD4	D4[A4/D4]	POE3#	SSLC0	IRQ4	AN012
B11		PG1	D25				
B12	VSS						
B13		P64	CS4#/WE#				
B14		PE0	D8[A8/D8]	TIOCC9	SCK12/SSLB1		ANEX0
B15		PE3	D11[A11/D11]	MTIOC4B/TIOCB9/PO26/ POE8#	ET_ERXD3/CTS12#/ RTS12#/SS12#/MISOB		AN1
C1	VREFL						
C2	VREFH						
C3	VREFH0						
C4		P43				IRQ11-DS	AN003
C5		P45				IRQ13-DS	AN005
C6		P90	A16/D16		TXD7/SMOSI7/SSDA7		AN014
C7		PD0	D0[A0/D0]	TIOCA7		IRQ0	AN008
C8		PD2	D2[A2/D2]	MTIOC4D/TIOCA8	MISOC/CRX0	IRQ2	AN010
C9		PD3	D3[A3/D3]	TIOCB8/TCLKH/POE8#	RSPCKC	IRQ3	AN011
C10		PG0	D24				
C11	VCC						
C12		P62	CS2#/RAS#				
C13		PE4	D12[A12/D12]	MTIOC4D/MTIOC1A/ TIOCA10/PO28	ET_ERXD2/SSLB0		AN2

Table 1.7 List of Pins and Pin Functions (145-Pin TFLGA) (5/5)

Pin No. 145-pin TFLGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timers (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SC1c, SC1d, RSPI, RIIC, CAN, IEB, USB, and PDC)	Interrupt	S12AD AD DA
N7	TRDATA3	P55	WAIT#/ EDREQ0	MTIOC4D/TMO3	CRX1/ET_EXOUT	IRQ10	
N8	VSS						
N9		PC7	A23/CS0#	MTIOC3A/MTCLKB/ TIOCB6/TMO2/PO31	TXD8/SMOSI8/SSDA8/ MISOA/ET_COL	IRQ14	
N10	TRSYNC	P82	EDREQ1	MTIOC4A/PO28	TXD10/SMOSI10/SSDA10/ ET_ETXD1/RMII_TXD1		
N11		PC3	A19	MTIOC4D/TCLKB/PO24	TXD5/SMOSI5/SSDA5/ IETXD/ET_TX_ER		
N12		P75	CS5#	PO20	SCK11/ET_ERXD0/ RMII_RXD0		
N13		P74	CS4#	PO19	CTS11#/RTS11#/SS11#/ ET_ERXD1/RMII_RXD1		

Note 1. The BCLK function is multiplexed with the I/O port function for pin P53, so the port function is not available if the external bus is enabled.

Note 2. Enabled only for the ROM capacity: 2 Mbytes/1.5 Mbytes

Table 1.8 List of Pins and Pin Functions (144-Pin LQFP) (5/5)

Pin No. 144-pin LQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timers (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SC1c, SC1d, RSPI, RIIC, CAN, IEB, USB, and PDC)	Interrupt	S12AD AD DA
125		PD1	D1[A1/D1]	MTIOC4B/TIOCB7/ TCLKG	MOSIC/CTX0	IRQ1	AN009
126		PD0	D0[A0/D0]	TIOCA7		IRQ0	AN008
127		P93	A19		CTS7#/RTS7#/SS7#		AN017
128		P92	A18		RXD7/SMISO7/SSCL7		AN016
129		P91	A17		SCK7		AN015
130	VSS						
131		P90	A16		TXD7/SMOSI7/SSDA7		AN014
132	VCC						
133		P47				IRQ15-DS	AN007
134		P46				IRQ14-DS	AN006
135		P45				IRQ13-DS	AN005
136		P44				IRQ12-DS	AN004
137		P43				IRQ11-DS	AN003
138		P42				IRQ10-DS	AN002
139		P41				IRQ9-DS	AN001
140	VREFL0						
141		P40				IRQ8-DS	AN000
142	VREFH0						
143	AVCC0						
144		P07				IRQ15	ADTRG0#

Note 1. The BCLK function is multiplexed with the I/O port function for pin P53, so the port function is not available if the external bus is enabled.

Note 2. Enabled only for the ROM capacity: 2 Mbytes/1.5 Mbytes

2.1 General-Purpose Registers (R0 to R15)

This CPU has sixteen general-purpose registers (R0 to R15). R1 to R15 can be used as data registers or address registers. R0, a general-purpose register, also functions as the stack pointer (SP).

The stack pointer is switched to operate as the interrupt stack pointer (ISP) or user stack pointer (USP) by the value of the stack pointer select bit (U) in the processor status word (PSW).

2.2 Control Registers

(1) Interrupt Stack Pointer (ISP)/User Stack Pointer (USP)

The stack pointer (SP) can be either of two types, the interrupt stack pointer (ISP) or the user stack pointer (USP). Whether the stack pointer operates as the ISP or USP depends on the value of the stack pointer select bit (U) in the processor status word (PSW).

Set the ISP or USP to a multiple of four, as this reduces the numbers of cycles required to execute interrupt sequences and instructions entailing stack manipulation.

(2) Interrupt Table Register (INTB)

The interrupt table register (INTB) specifies the address where the relocatable vector table starts.

(3) Program Counter (PC)

The program counter (PC) indicates the address of the instruction being executed.

(4) Processor Status Word (PSW)

The processor status word (PSW) indicates the results of instruction execution or the state of the CPU.

(5) Backup PC (BPC)

The backup PC (BPC) is provided to speed up response to interrupts.

After a fast interrupt has been generated, the contents of the program counter (PC) are saved in the BPC register.

(6) Backup PSW (BPSW)

The backup PSW (BPSW) is provided to speed up response to interrupts.

After a fast interrupt has been generated, the contents of the processor status word (PSW) are saved in the BPSW. The allocation of bits in the BPSW corresponds to that in the PSW.

(7) Fast Interrupt Vector Register (FINTV)

The fast interrupt vector register (FINTV) is provided to speed up response to interrupts.

The FINTV register specifies a branch destination address when a fast interrupt has been generated.

(8) Floating-Point Status Word (FPSW)

The floating-point status word (FPSW) indicates the results of floating-point operations.

When an exception handling enable bit (Ej) enables the exception handling (Ej = 1), the exception cause can be identified by checking the corresponding Cj flag in the exception handling routine. If the exception handling is masked (Ej = 0), the occurrence of exception can be checked by reading the Fj flag at the end of a series of processing. Once the Fj flag has been set to 1, this value is retained until it is cleared to 0 by software (j = X, U, Z, O, or V).

2.3 Register Associated with DSP Instructions

(1) Accumulator (ACC)

The accumulator (ACC) is a 64-bit register used for DSP instructions. The accumulator is also used for the multiply and multiply-and-accumulate instructions; EMUL, EMULU, FMUL, MUL, and RMPA, in which case the prior value in the accumulator is modified by execution of the instruction.

Use the MVTACHI and MVTACLO instructions for writing to the accumulator. The MVTACHI and MVTACLO instructions write data to the higher-order 32 bits (bits 63 to 32) and the lower-order 32 bits (bits 31 to 0), respectively. Use the MVFACHI and MVFACMI instructions for reading data from the accumulator. The MVFACHI and MVFACMI instructions read data from the higher-order 32 bits (bits 63 to 32) and the middle 32 bits (bits 47 to 16), respectively.

Table 4.1 List of I/O Registers (Address Order) (3/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK>PCLK	ICLK<PCLK	
0008 2818h	EXDMAC0	EXDMA offset register	EDMOFR	32	32	1, 2 BCLK		EXDMACa
0008 281Ch	EXDMAC0	EXDMA transfer enable register	EDMCNT	8	8	1, 2 BCLK		
0008 281Dh	EXDMAC0	EXDMA software start register	EDMREQ	8	8	1, 2 BCLK		
0008 281Eh	EXDMAC0	EXDMA status register	EDMSTS	8	8	1, 2 BCLK		
0008 2820h	EXDMAC0	EXDMA external request sense mode register	EDMRMD	8	8	1, 2 BCLK		
0008 2821h	EXDMAC0	EXDMA external request flag register	EDMERF	8	8	1, 2 BCLK		
0008 2822h	EXDMAC0	EXDMA peripheral request flag register	EDMPRF	8	8	1, 2 BCLK		
0008 2840h	EXDMAC1	EXDMA source address register	EDMSAR	32	32	1, 2 BCLK		
0008 2844h	EXDMAC1	EXDMA destination address register	EDMDAR	32	32	1, 2 BCLK		
0008 2848h	EXDMAC1	EXDMA transfer count register	EDMCRA	32	32	1, 2 BCLK		
0008 284Ch	EXDMAC1	EXDMA block transfer count register	EDMCRB	16	16	1, 2 BCLK		
0008 2850h	EXDMAC1	EXDMA transfer mode register	EDMTMD	16	16	1, 2 BCLK		
0008 2852h	EXDMAC1	EXDMA output setting register	EDMOMD	8	8	1, 2 BCLK		
0008 2853h	EXDMAC1	EXDMA interrupt setting register	EDMINT	8	8	1, 2 BCLK		
0008 2854h	EXDMAC1	EXDMA address mode register	EDMAMD	32	32	1, 2 BCLK		
0008 285Ch	EXDMAC1	EXDMA transfer enable register	EDMCNT	8	8	1, 2 BCLK		
0008 285Dh	EXDMAC1	EXDMA software start register	EDMREQ	8	8	1, 2 BCLK		
0008 285Eh	EXDMAC1	EXDMA status register	EDMSTS	8	8	1, 2 BCLK		
0008 2860h	EXDMAC1	EXDMA external request sense mode register	EDMRMD	8	8	1, 2 BCLK		
0008 2861h	EXDMAC1	EXDMA external request flag register	EDMERF	8	8	1, 2 BCLK		
0008 2862h	EXDMAC1	EXDMA peripheral request flag register	EDMPRF	8	8	1, 2 BCLK		
0008 2A00h	EXDMAC	EXDMA module start register	EDMAST	8	8	1, 2 BCLK		
0008 2BE0h	EXDMAC	Cluster buffer register 0	CLSBR0	32	32	1, 2 BCLK		
0008 2BE4h	EXDMAC	Cluster buffer register 1	CLSBR1	32	32	1, 2 BCLK		
0008 2BE8h	EXDMAC	Cluster buffer register 2	CLSBR2	32	32	1, 2 BCLK		
0008 2BECh	EXDMAC	Cluster buffer register 3	CLSBR3	32	32	1, 2 BCLK		
0008 2BF0h	EXDMAC	Cluster buffer register 4	CLSBR4	32	32	1, 2 BCLK		
0008 2BF4h	EXDMAC	Cluster buffer register 5	CLSBR5	32	32	1, 2 BCLK		
0008 2BF8h	EXDMAC	Cluster buffer register 6	CLSBR6	32	32	1, 2 BCLK		
0008 2BFCh	EXDMAC	Cluster buffer register 7	CLSBR7	32	32	1, 2 BCLK		
0008 3002h	BSC	CS0 mode register	CS0MOD	16	16	1, 2 BCLK		Buses
0008 3004h	BSC	CS0 wait control register 1	CS0WCR1	32	32	1, 2 BCLK		
0008 3008h	BSC	CS0 wait control register 2	CS0WCR2	32	32	1, 2 BCLK		
0008 3012h	BSC	CS1 mode register	CS1MOD	16	16	1, 2 BCLK		
0008 3014h	BSC	CS1 wait control register 1	CS1WCR1	32	32	1, 2 BCLK		
0008 3018h	BSC	CS1 wait control register 2	CS1WCR2	32	32	1, 2 BCLK		
0008 3022h	BSC	CS2 mode register	CS2MOD	16	16	1, 2 BCLK		
0008 3024h	BSC	CS2 wait control register 1	CS2WCR1	32	32	1, 2 BCLK		
0008 3028h	BSC	CS2 wait control register 2	CS2WCR2	32	32	1, 2 BCLK		
0008 3032h	BSC	CS3 mode register	CS3MOD	16	16	1, 2 BCLK		
0008 3034h	BSC	CS3 wait control register 1	CS3WCR1	32	32	1, 2 BCLK		
0008 3038h	BSC	CS3 wait control register 2	CS3WCR2	32	32	1, 2 BCLK		
0008 3042h	BSC	CS4 mode register	CS4MOD	16	16	1, 2 BCLK		
0008 3044h	BSC	CS4 wait control register 1	CS4WCR1	32	32	1, 2 BCLK		
0008 3048h	BSC	CS4 wait control register 2	CS4WCR2	32	32	1, 2 BCLK		
0008 3052h	BSC	CS5 mode register	CS5MOD	16	16	1, 2 BCLK		
0008 3054h	BSC	CS5 wait control register 1	CS5WCR1	32	32	1, 2 BCLK		
0008 3058h	BSC	CS5 wait control register 2	CS5WCR2	32	32	1, 2 BCLK		
0008 3062h	BSC	CS6 mode register	CS6MOD	16	16	1, 2 BCLK		
0008 3064h	BSC	CS6 wait control register 1	CS6WCR1	32	32	1, 2 BCLK		
0008 3068h	BSC	CS6 wait control register 2	CS6WCR2	32	32	1, 2 BCLK		

Table 4.1 List of I/O Registers (Address Order) (5/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 650Ch	MPU	Memory-protection error status register	MPESTS	32	32	1	ICLK	MPU
0008 6514h	MPU	Data memory-protection error address register	MPDEA	32	32	1	ICLK	
0008 6520h	MPU	Region search address register	MPSA	32	32	1	ICLK	
0008 6524h	MPU	Region search operation register	MPOPS	16	16	1	ICLK	
0008 6526h	MPU	Region invalidation operation register	MPOPI	16	16	1	ICLK	
0008 6528h	MPU	Instruction-hit region register	MHITI	32	32	1	ICLK	
0008 652Ch	MPU	Data-hit region register	MHITD	32	32	1	ICLK	
0008 7010h	ICU	Interrupt request register 016	IR016	8	8	2	ICLK	ICUb
0008 7015h	ICU	Interrupt request register 021	IR021	8	8	2	ICLK	
0008 7017h	ICU	Interrupt request register 023	IR023	8	8	2	ICLK	
0008 701Bh	ICU	Interrupt request register 027	IR027	8	8	2	ICLK	
0008 701Ch	ICU	Interrupt request register 028	IR028	8	8	2	ICLK	
0008 701Dh	ICU	Interrupt request register 029	IR029	8	8	2	ICLK	
0008 701Eh	ICU	Interrupt request register 030	IR030	8	8	2	ICLK	
0008 701Fh	ICU	Interrupt request register 031	IR031	8	8	2	ICLK	
0008 7020h	ICU	Interrupt request register 032	IR032	8	8	2	ICLK	
0008 7021h	ICU	Interrupt request register 033	IR033	8	8	2	ICLK	
0008 7022h	ICU	Interrupt request register 034	IR034	8	8	2	ICLK	
0008 7023h	ICU	Interrupt request register 035	IR035	8	8	2	ICLK	
0008 7024h	ICU	Interrupt request register 036	IR036	8	8	2	ICLK	
0008 7025h	ICU	Interrupt request register 037	IR037	8	8	2	ICLK	
0008 7026h	ICU	Interrupt request register 038	IR038	8	8	2	ICLK	
0008 7027h	ICU	Interrupt request register 039	IR039	8	8	2	ICLK	
0008 7028h	ICU	Interrupt request register 040	IR040	8	8	2	ICLK	
0008 7029h	ICU	Interrupt request register 041	IR041	8	8	2	ICLK	
0008 702Ah	ICU	Interrupt request register 042	IR042	8	8	2	ICLK	
0008 702Bh	ICU	Interrupt request register 043	IR043	8	8	2	ICLK	
0008 702Ch	ICU	Interrupt request register 044	IR044	8	8	2	ICLK	
0008 702Dh	ICU	Interrupt request register 045	IR045	8	8	2	ICLK	
0008 702Eh	ICU	Interrupt request register 046	IR046	8	8	2	ICLK	
0008 702Fh	ICU	Interrupt request register 047	IR047	8	8	2	ICLK	
0008 7030h	ICU	Interrupt request register 048	IR048	8	8	2	ICLK	
0008 7031h	ICU	Interrupt request register 049	IR049	8	8	2	ICLK	
0008 7032h	ICU	Interrupt request register 050	IR050	8	8	2	ICLK	
0008 7033h	ICU	Interrupt request register 051	IR051	8	8	2	ICLK	
0008 7034h	ICU	Interrupt request register 052	IR052	8	8	2	ICLK	
0008 7035h	ICU	Interrupt request register 053	IR053	8	8	2	ICLK	
0008 7036h	ICU	Interrupt request register 054	IR054	8	8	2	ICLK	
0008 7037h	ICU	Interrupt request register 055	IR055	8	8	2	ICLK	
0008 7038h	ICU	Interrupt request register 056	IR056	8	8	2	ICLK	
0008 7039h	ICU	Interrupt request register 057	IR057	8	8	2	ICLK	
0008 703Ah	ICU	Interrupt request register 058	IR058	8	8	2	ICLK	
0008 703Bh	ICU	Interrupt request register 059	IR059	8	8	2	ICLK	
0008 703Eh	ICU	Interrupt request register 062	IR062	8	8	2	ICLK	
0008 7040h	ICU	Interrupt request register 064	IR064	8	8	2	ICLK	
0008 7041h	ICU	Interrupt request register 065	IR065	8	8	2	ICLK	
0008 7042h	ICU	Interrupt request register 066	IR066	8	8	2	ICLK	
0008 7043h	ICU	Interrupt request register 067	IR067	8	8	2	ICLK	
0008 7044h	ICU	Interrupt request register 068	IR068	8	8	2	ICLK	
0008 7045h	ICU	Interrupt request register 069	IR069	8	8	2	ICLK	
0008 7046h	ICU	Interrupt request register 070	IR070	8	8	2	ICLK	

Table 4.1 List of I/O Registers (Address Order) (20/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 8368h	RIIC3	I ² C bus status register 1	ICSR1	8	8	2, 3 PCLKB	2 ICLK	RSPI
0008 8369h	RIIC3	I ² C bus status register 2	ICSR2	8	8	2, 3 PCLKB	2 ICLK	
0008 836Ah	RIIC3	Slave address register L0	SARL0	8	8	2, 3 PCLKB	2 ICLK	
0008 836Bh	RIIC3	Slave address register U0	SARU0	8	8	2, 3 PCLKB	2 ICLK	
0008 836Ch	RIIC3	Slave address register L1	SARL1	8	8	2, 3 PCLKB	2 ICLK	
0008 836Dh	RIIC3	Slave address register U1	SARU1	8	8	2, 3 PCLKB	2 ICLK	
0008 836Eh	RIIC3	Slave address register L2	SARL2	8	8	2, 3 PCLKB	2 ICLK	
0008 836Fh	RIIC3	Slave address register U2	SARU2	8	8	2, 3 PCLKB	2 ICLK	
0008 8370h	RIIC3	I ² C bus bit rate low-level register	ICBRL	8	8	2, 3 PCLKB	2 ICLK	
0008 8371h	RIIC3	I ² C bus bit rate high-level register	ICBRH	8	8	2, 3 PCLKB	2 ICLK	
0008 8372h	RIIC3	I ² C bus transmit data register	ICDRT	8	8	2, 3 PCLKB	2 ICLK	
0008 8373h	RIIC3	I ² C bus receive data register	ICDRR	8	8	2, 3 PCLKB	2 ICLK	
0008 8380h	RSPI0	RSPI control register	SPCR	8	8	2, 3 PCLKB	2 ICLK	
0008 8381h	RSPI0	RSPI slave select polarity register	SSLP	8	8	2, 3 PCLKB	2 ICLK	
0008 8382h	RSPI0	RSPI pin control register	SPPCR	8	8	2, 3 PCLKB	2 ICLK	
0008 8383h	RSPI0	RSPI status register	SPSR	8	8	2, 3 PCLKB	2 ICLK	
0008 8384h	RSPI0	RSPI data register	SPDR	32	16, 32	2, 3 PCLKB	2 ICLK	
0008 8388h	RSPI0	RSPI sequence control register	SPSCR	8	8	2, 3 PCLKB	2 ICLK	
0008 8389h	RSPI0	RSPI sequence status register	SPSSR	8	8	2, 3 PCLKB	2 ICLK	
0008 838Ah	RSPI0	RSPI bit rate register	SPBR	8	8	2, 3 PCLKB	2 ICLK	
0008 838Bh	RSPI0	RSPI data control register	SPDCR	8	8	2, 3 PCLKB	2 ICLK	
0008 838Ch	RSPI0	RSPI clock delay register	SPCKD	8	8	2, 3 PCLKB	2 ICLK	
0008 838Dh	RSPI0	RSPI slave select negation delay register	SSLND	8	8	2, 3 PCLKB	2 ICLK	
0008 838Eh	RSPI0	RSPI next-access delay register	SPND	8	8	2, 3 PCLKB	2 ICLK	
0008 838Fh	RSPI0	RSPI control register 2	SPCR2	8	8	2, 3 PCLKB	2 ICLK	
0008 8390h	RSPI0	RSPI command register 0	SPCMD0	16	16	2, 3 PCLKB	2 ICLK	
0008 8392h	RSPI0	RSPI command register 1	SPCMD1	16	16	2, 3 PCLKB	2 ICLK	
0008 8394h	RSPI0	RSPI command register 2	SPCMD2	16	16	2, 3 PCLKB	2 ICLK	
0008 8396h	RSPI0	RSPI command register 3	SPCMD3	16	16	2, 3 PCLKB	2 ICLK	
0008 8398h	RSPI0	RSPI command register 4	SPCMD4	16	16	2, 3 PCLKB	2 ICLK	
0008 839Ah	RSPI0	RSPI command register 5	SPCMD5	16	16	2, 3 PCLKB	2 ICLK	RSPI
0008 839Ch	RSPI0	RSPI command register 6	SPCMD6	16	16	2, 3 PCLKB	2 ICLK	
0008 839Eh	RSPI0	RSPI command register 7	SPCMD7	16	16	2, 3 PCLKB	2 ICLK	
0008 83A0h	RSPI1	RSPI control register	SPCR	8	8	2, 3 PCLKB	2 ICLK	
0008 83A1h	RSPI1	RSPI slave select polarity register	SSLP	8	8	2, 3 PCLKB	2 ICLK	
0008 83A2h	RSPI1	RSPI pin control register	SPPCR	8	8	2, 3 PCLKB	2 ICLK	
0008 83A3h	RSPI1	RSPI status register	SPSR	8	8	2, 3 PCLKB	2 ICLK	
0008 83A4h	RSPI1	RSPI data register	SPDR	32	16, 32	2, 3 PCLKB	2 ICLK	
0008 83A8h	RSPI1	RSPI sequence control register	SPSCR	8	8	2, 3 PCLKB	2 ICLK	
0008 83A9h	RSPI1	RSPI sequence status register	SPSSR	8	8	2, 3 PCLKB	2 ICLK	
0008 83AAh	RSPI1	RSPI bit rate register	SPBR	8	8	2, 3 PCLKB	2 ICLK	
0008 83ABh	RSPI1	RSPI data control register	SPDCR	8	8	2, 3 PCLKB	2 ICLK	
0008 83ACh	RSPI1	RSPI clock delay register	SPCKD	8	8	2, 3 PCLKB	2 ICLK	
0008 83ADh	RSPI1	RSPI slave select negation delay register	SSLND	8	8	2, 3 PCLKB	2 ICLK	
0008 83AEh	RSPI1	RSPI next-access delay register	SPND	8	8	2, 3 PCLKB	2 ICLK	
0008 83AFh	RSPI1	RSPI control register 2	SPCR2	8	8	2, 3 PCLKB	2 ICLK	
0008 83B0h	RSPI1	RSPI command register 0	SPCMD0	16	16	2, 3 PCLKB	2 ICLK	
0008 83B2h	RSPI1	RSPI command register 1	SPCMD1	16	16	2, 3 PCLKB	2 ICLK	
0008 83B4h	RSPI1	RSPI command register 2	SPCMD2	16	16	2, 3 PCLKB	2 ICLK	
0008 83B6h	RSPI1	RSPI command register 3	SPCMD3	16	16	2, 3 PCLKB	2 ICLK	
0008 83B8h	RSPI1	RSPI command register 4	SPCMD4	16	16	2, 3 PCLKB	2 ICLK	

Table 5.3 DC Characteristics (2)

Conditions: $V_{CC} = AV_{CC0} = V_{REFH} = V_{CC_USB} = 2.7$ to 3.6 V, $V_{REFH0} = 2.7$ V to AV_{CC0} ,
 $V_{SS} = AV_{SS0} = V_{REFL}/V_{REFL0} = V_{SS_USB} = 0$ V, $T_a = T_{opr}$

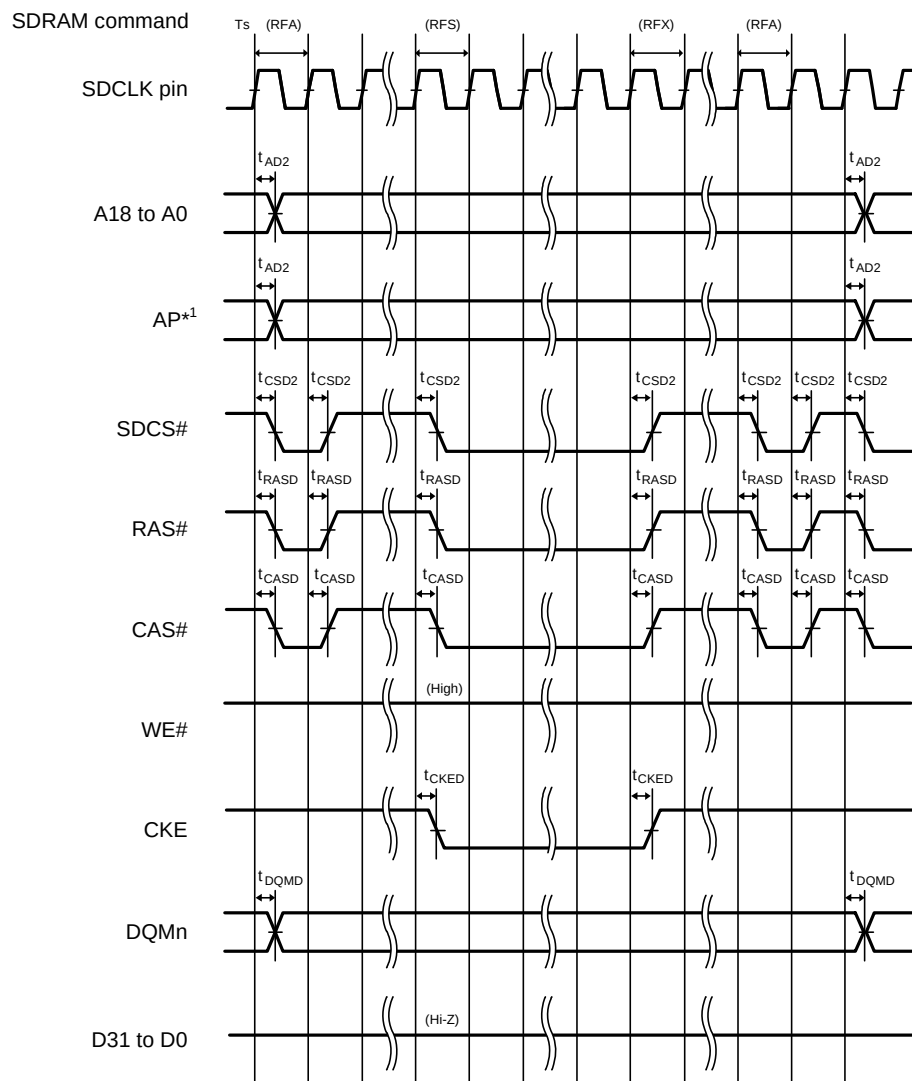
Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Output high voltage	All output pins	V_{OH}	$V_{CC} - 0.5$	—	V	$I_{OH} = -1$ mA
Output low voltage	All output pins (except for RIIC pins, and ETHERC)	V_{OL}	—	0.5	V	$I_{OL} = 1.0$ mA
	RIIC pins	—	—	0.4	V	$I_{OL} = 3.0$ mA
		—	—	0.6		$I_{OL} = 6.0$ mA
	RIIC pins (only P12 and P13 in channel 0)	V_{OL}	—	0.4	V	$I_{OL} = 15.0$ mA (ICFER.FMPE = 1)
		—	0.4	—		$I_{OL} = 20.0$ mA (ICFER.FMPE = 1)
	ETHERC	V_{OL}	—	0.4	V	$I_{OL} = 1.0$ mA
Input leakage current	RES#, MD pin, EMLE*1, NMI	$ I_{in} $	—	1.0	μ A	$V_{in} = 0$ V $V_{in} = V_{CC}$
Three-state leakage current (off state)	Other than ports for 5 V tolerant	$ I_{TSI} $	—	1.0	μ A	$V_{in} = 0$ V $V_{in} = V_{CC}$
	Ports for 5 V tolerant		—	5.0		$V_{in} = 0$ V $V_{in} = 5.5$ V
Input pull-up MOS current	Ports 0 to 2, 30 to 34, 36, 37, 4 to G, J3, J5	I_p	-10	—	-300	μ A $V_{CC} = 2.7$ to 3.6 V $V_{in} = 0$ V
Input capacitance	All input pins (except for ports 12, 13, 16, 17, 20, 21, 4, C0, C1, and EMLE)	C_{in}	—	—	15	pF $V_{in} = 0$ V $f = 1$ MHz $T_a = 25^\circ\text{C}$
	Ports 12, 13, 16, 17, 20, 21, 4, C0, C1, EMLE		—	—	30	
Input pull-down MOS current	EMLE, BSCANP	I_p	10	—	300	μ A $V_{in} = V_{CC}$

Note 1. The input leakage current value at the EMLE pin is only when $V_{in} = 0$ V.

Table 5.5 DC Characteristics (4) (for G Version (+85 < Ta ≤ +105°C))

Conditions: VCC = AVCC0 = VREFH = VCC_USB = V_{BATT} = 2.7 to 3.6 V, VREFH0 = 2.7 V to AVCC0,
VSS = AVSS0 = VREFL/VREFL0 = VSS_USB = 0 V, T_a = T_{opr}

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions		
Supply current*1	High-speed operating mode	Max.*2		I _{CC} *3	—	—	115	mA	ICLK = 100 MHz PCLKA = 100MHz PCLKB = 50 MHz FCLK = 50 MHz BCLK = 100MHz	
		Normal*4	Peripheral function: clock signal supplied*4		—	52	—			
			Peripheral function: clock signal stopped*4		—	40	—			
		Sleep mode			—	25	80			
		All-module-clock-stop mode (reference value)			—	20	53			
		Increased by BGO operation*5			—	15	—			
	Low-speed operating mode 1*6		—		4	—	ICLK = 1 MHz			
	Low-speed operating mode 2		—		1	—	ICLK = 32.768 kHz			
	Software standby mode		—		0.2	9				
	Deep software standby mode	Power supplied to RAM and USB resume detecting unit			—	22	200	μA		
		Power not supplied to RAM and USB resume detecting unit	Power-on reset circuit and low-power consumption function disabled	—	21	60				
			Power-on reset circuit and low-power consumption function enabled	—	6.2	28				
	Increase when the RTC is operating	When a crystal oscillator for low clock loads is in use		—	1.0	—				
		When a crystal oscillator for standard clock loads is in use		—	3.0	—				
	RTC operating while VCC is off (with the battery backup function, only the RTC and sub-clock oscillator operate)	When a crystal oscillator for low clock loads is in use		—	0.9	—	V _{BATT} = 2.0 V, VCC = 0V			
		When a crystal oscillator for standard clock loads is in use		—	1.6	—	V _{BATT} = 3.3 V, VCC = 0V			
				—	1.7	—	V _{BATT} = 2.0 V(for products with 100 pins or more), V _{BATT} = 2.3 V (for the 64-pin product), VCC = 0V			
			—	3.3	—	V _{BATT} = 3.3 V, VCC = 0V				
Analog power supply current*7	During 12-bit A/D conversion (including temperature sensor)		I _{AVCC0}	—	2.3	3.2	mA			
	During 10-bit A/D conversion		I _{VREFH} *9	—	1.0	1.65				
	During D/A conversion (per unit)			—	0.7	1.0				
	Waiting for A/D, D/A conversion (all units)*10		—	—	25	35		μA		
	A/D, D/A converter in standby mode (all units)*10			—	0.1	5		μA		
Reference power supply current	During 12-bit A/D conversion		I _{VREFH0}	—	0.6	0.7	mA			
	Waiting for 12-bit A/D conversion (per unit)			—	0.5	0.6				
	12-bit A/D converter in standby mode (per unit)			—	0.1	2.0		μA		
RAM standby voltage			V _{RAM}	2.7	—	—	V			
VCC rising gradient			SrVCC	8.4	—	20000	μs/V			
VCC falling gradient*8			SfVCC	8.4	—	—	μs/V			



Note 1: Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

Figure 5.30 SDRAM Space Self-Refresh Bus Timing

5.3.6 EXDMAC Timing

Table 5.18 EXDMAC Timing

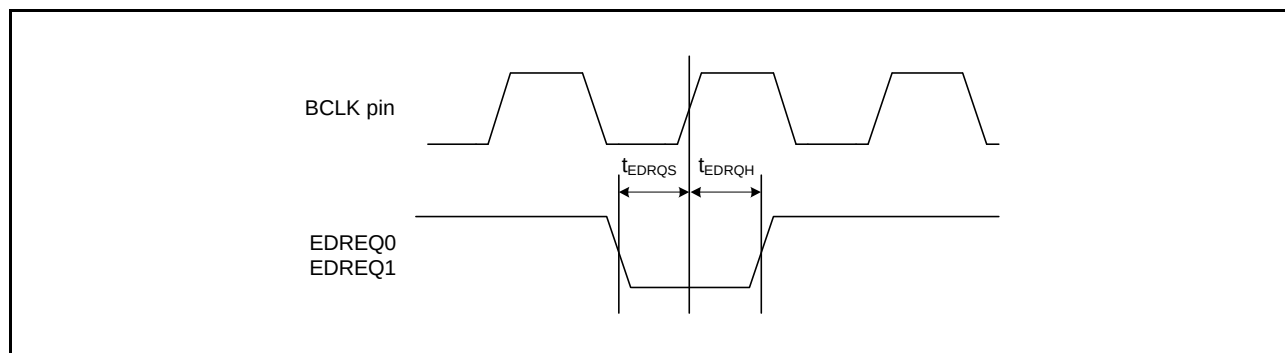
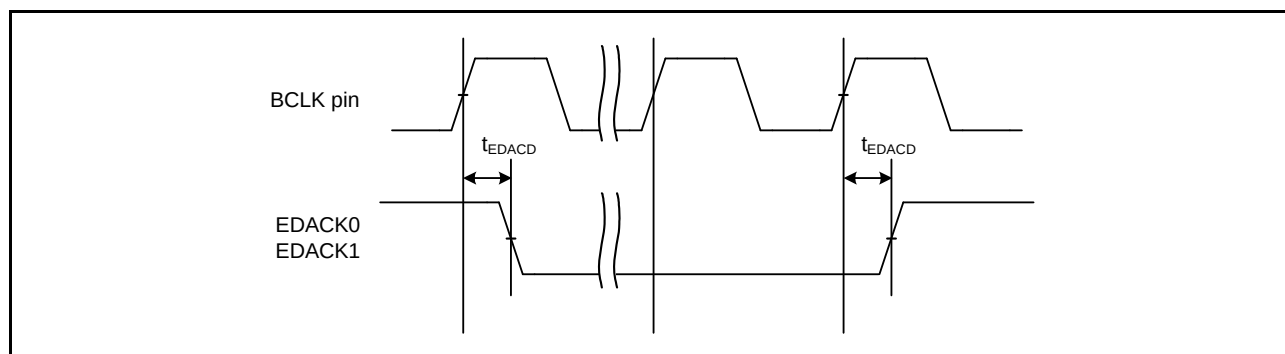
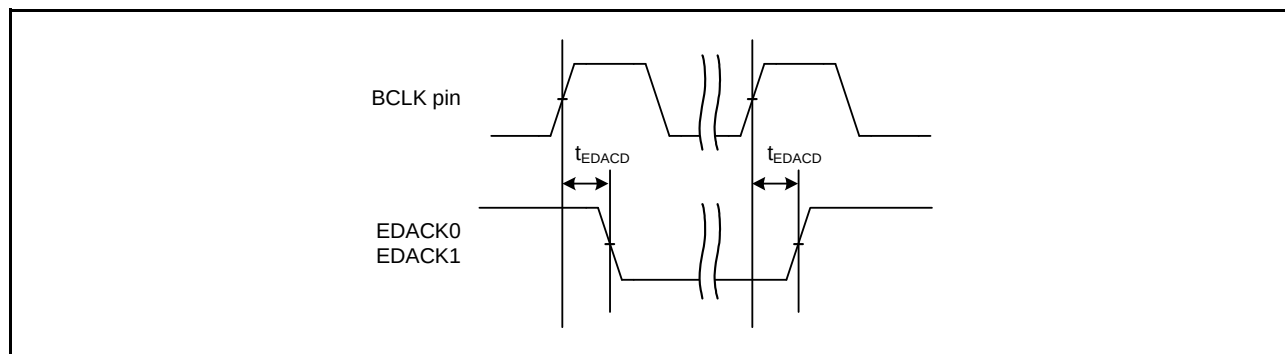
Conditions: $V_{CC} = AV_{CC0} = V_{REFH} = V_{CC_USB} = 2.7$ to 3.6 V, $V_{REFH0} = 2.7$ V to AV_{CC0} ,

$V_{SS} = AV_{SS0} = V_{REFL}/V_{REFL0} = V_{SS_USB} = 0$ V

$ICLK = 8$ to 100 MHz, $PCLK = 8$ to 50 MHz, $BCLK$ pin = 8 to 100 MHz, $SDCLK$ pin = 8 to 50 MHz, $T_a = T_{opr}$

High drive output is selected by the drive capacity control register

	Item	Symbol	Min.	Max.	Unit	Test Conditions
EXDMAC	EDREQ setup time	t_{EDRQS}	20	—	ns	Figure 5.31
	EDREQ hold time	t_{EDRQH}	5	—	ns	Figure 5.32 and Figure 5.33
	EDACK delay time	t_{EDACD}	—	15	ns	Figure 5.33

**Figure 5.31 EDREQ0 and EDREQ1 Input Timing****Figure 5.32 EDACK0 and EDACK1 Single-Address Transfer Timing (for a CS Area)****Figure 5.33 EDACK0 and EDACK1 Single-Address Transfer Timing (for SDRAM)**

5.4 USB Characteristics

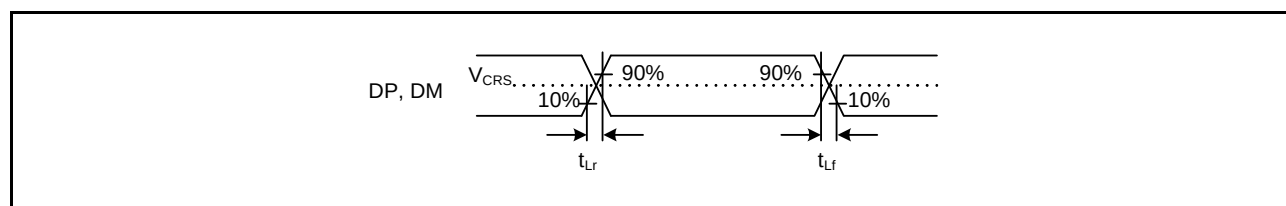
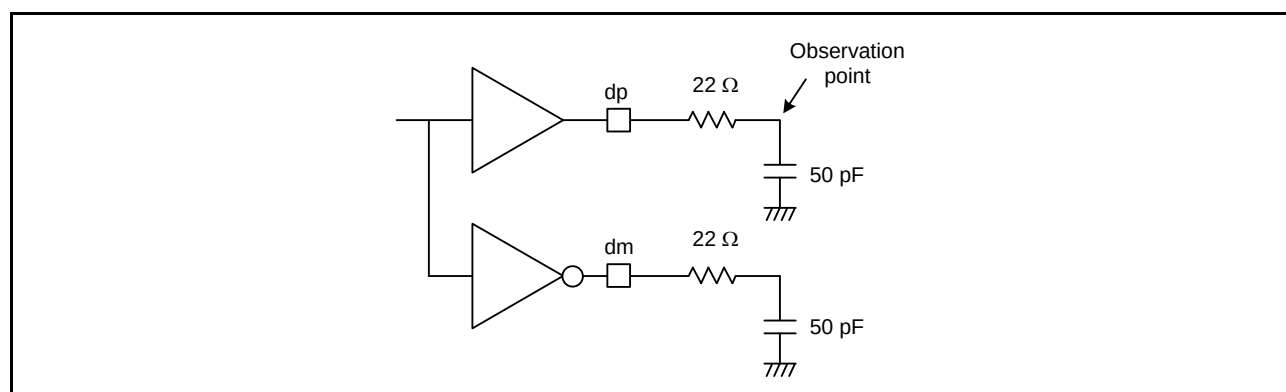
Table 5.27 On-Chip USB Full-Speed Characteristics (DP and DM Pin Characteristics)Conditions: $V_{CC} = AV_{CC0} = V_{REFH} = V_{CC_USB} = 3.0$ to 3.6 V, $V_{REFH0} = 3.0$ V to AV_{CC0} $V_{SS} = AV_{SS0} = V_{REFL}/V_{REFL0} = V_{SS_USB} = 0$ V

PCLK = 24 to 50 MHz

 $T_a = T_{opr}$

High drive output is selected by the drive capacity control register.

Item		Symbol	Min.	Max.	Unit	Test Conditions	
Input characteristics	Input high level voltage	V_{IH}	2.0	—	V		
	Input low level voltage	V_{IL}	—	0.8	V		
	Differential input sensitivity	V_{DI}	0.2	—	V	DP – DM	
	Differential common mode range	V_{CM}	0.8	2.5	V		
Output characteristics	Output high level voltage	V_{OH}	2.8	3.6	V	$I_{OH} = -200 \mu A$	
	Output low level voltage	V_{OL}	0.0	0.3	V	$I_{OL} = 2$ mA	
	Cross-over voltage	V_{CRS}	1.3	2.0	V		Figure 5.61
	Rise time	t_{Lr}	4	20	ns		
	Fall time	t_{Lf}	4	20	ns		
	Rise/fall time ratio	t_{Lr} / t_{Lf}	90	111.11	%	t_{Lr} / t_{Lf}	
	Output resistance	Z_{DRV}	28	44	Ω	$R_s = 22 \Omega$ included	

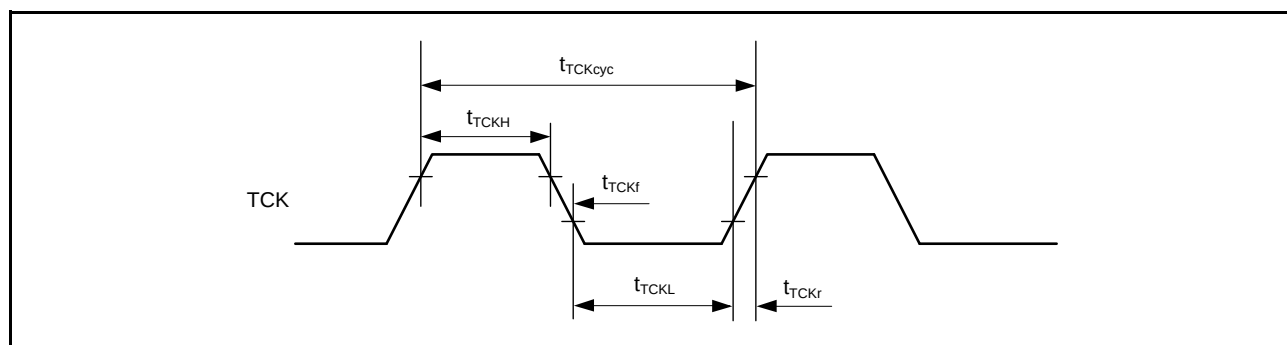
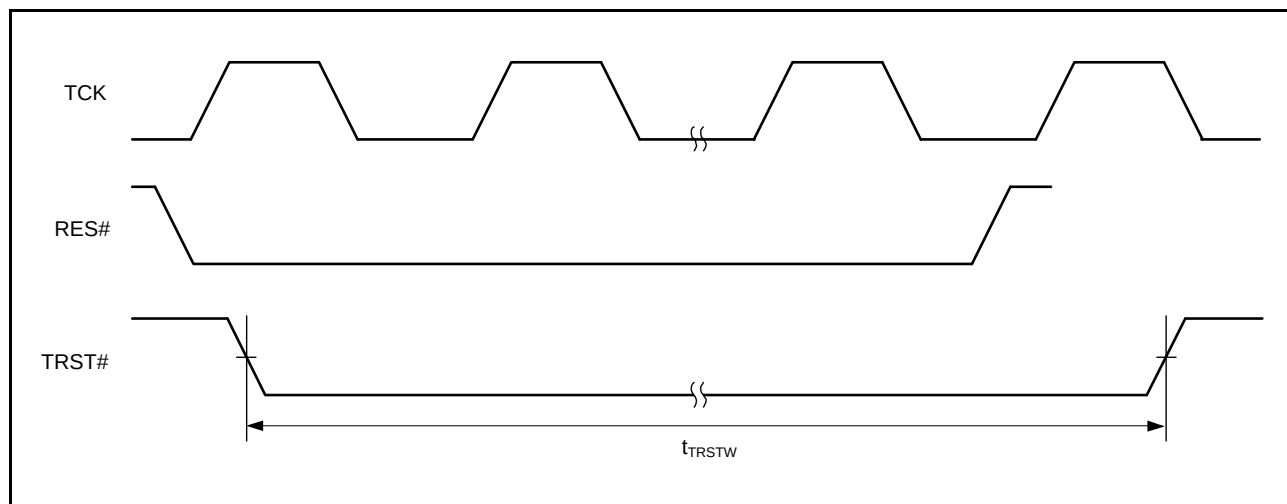
**Figure 5.61 DP and DM Output Timing (Full-Speed)****Figure 5.62 Test Circuit (Full-Speed)**

5.13 Boundary Scan

Table 5.40 Boundary Scan

Conditions: $V_{CC} = AV_{CC0} = V_{REFH} = V_{CC_USB} = 2.7$ to $3.6V$, $V_{REFH0} = 2.7V$ to AV_{CC0}
 $V_{SS} = AV_{SS0} = V_{REFL}/V_{REFL0} = V_{SS_USB} = 0V$
 $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
TCK clock cycle time	t_{TCKcyc}	100	—	—	ns	Figure 5.70
TCK clock high pulse width	t_{TCKH}	45	—	—	ns	
TCK clock low pulse width	t_{TCKL}	45	—	—	ns	
TCK clock rise time	t_{TCKr}	—	—	5	ns	
TCK clock fall time	t_{TCKf}	—	—	5	ns	
TRST# pulse width	t_{TRSTW}	20	—	—	t_{TCKcyc}	Figure 5.71
TMS setup time	t_{TMSS}	20	—	—	ns	Figure 5.72
TMS hold time	t_{TMSH}	20	—	—	ns	
TDI setup time	t_{TDIS}	20	—	—	ns	
TDI hold time	t_{TDIH}	20	—	—	ns	
TDO data delay time	t_{TDOD}	—	—	40	ns	


Figure 5.70 Boundary Scan TCK Timing

Figure 5.71 Boundary Scan TRST# Timing

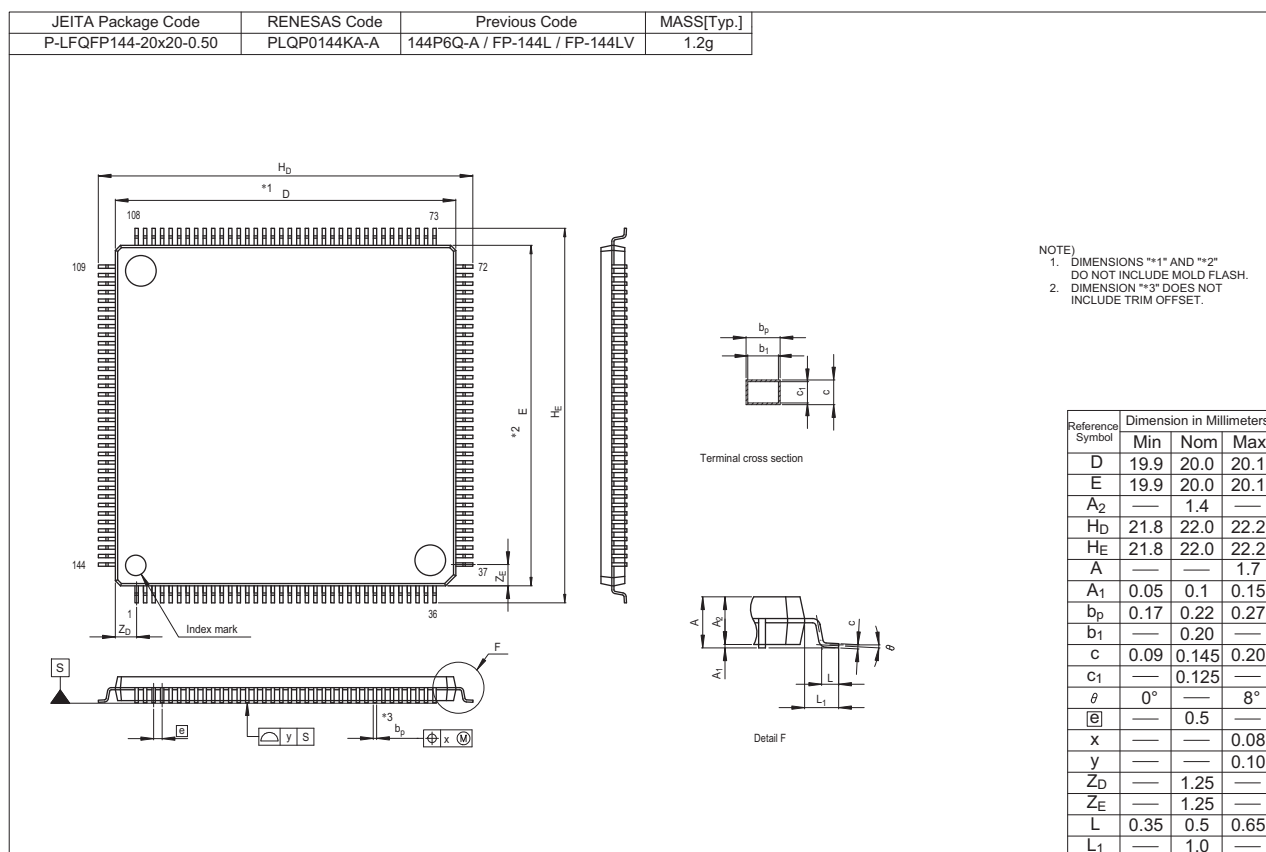


Figure E 144-pin LQFP (PLQP0144KA-A)

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

- The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

- The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

- The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

- When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

- The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.