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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Not For New Designs
Core Processor	RX
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, LINbus, SCI, SPI, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	111
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	32K x 8
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b, 21x12b; D/A 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LFQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f563nyddfb-v0

Table 1.3 List of Products (2/8)

Group	Part No.	Package	ROM Capacity	RAM Capacity	E2 Data Flash	Operating Frequency (Max.)	Operating Temp. Range
RX63N (D version)	R5F563NDDDLK	PTLG0145KA-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NBCDLK	PTLG0145KA-A	1 Mbyte	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NBDDLK	PTLG0145KA-A	1 Mbyte	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NACDLK	PTLG0145KA-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NADDLK	PTLG0145KA-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NFHDFB	PLQP0144KA-A	2 Mbytes	256 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NFDDFB	PLQP0144KA-A	2 Mbytes	256 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NKHDFB	PLQP0144KA-A*1	2 Mbytes	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NKDDFB	PLQP0144KA-A	2 Mbytes	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NECDFB	PLQP0144KA-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NEDDFB	PLQP0144KA-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NJHDFB	PLQP0144KA-A*1	1.5 Mbytes	256 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NJDDFB	PLQP0144KA-A*1	1.5 Mbytes	256 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NGHDFB	PLQP0144KA-A*1	1.5 Mbytes	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NGDDFB	PLQP0144KA-A*1	1.5 Mbytes	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NDCDFB	PLQP0144KA-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NDDDFB	PLQP0144KA-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NYHDFB	PLQP0144KA-A	1 Mbyte	256 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NYDDFB	PLQP0144KA-A	1 Mbyte	256 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NWHDFB	PLQP0144KA-A	1 Mbyte	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NWDDFB	PLQP0144KA-A	1 Mbyte	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NBCDFB	PLQP0144KA-A	1 Mbyte	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NBDDFB	PLQP0144KA-A	1 Mbyte	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NACDFB	PLQP0144KA-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NADDFB	PLQP0144KA-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NECDLJ	PTLG0100JA-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NEDDLJ	PTLG0100JA-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NDCDLJ	PTLG0100JA-A*1	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NDDDLJ	PTLG0100JA-A*1	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NBCDLJ	PTLG0100JA-A	1 Mbyte	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NBDDLJ	PTLG0100JA-A	1 Mbyte	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NACDLJ	PTLG0100JA-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NADDLJ	PTLG0100JA-A	768 Kbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NFHDFP	PLQP0100KB-A	2 Mbytes	256 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NFDDFP	PLQP0100KB-A	2 Mbytes	256 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NKHDFP	PLQP0100KB-A*1	2 Mbytes	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NKDDFP	PLQP0100KB-A	2 Mbytes	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NECDFP	PLQP0100KB-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NEDDFP	PLQP0100KB-A	2 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NJHDFP	PLQP0100KB-A*1	1.5 Mbytes	256 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NJDDFP	PLQP0100KB-A*1	1.5 Mbytes	256 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NGHDFP	PLQP0100KB-A*1	1.5 Mbytes	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NGDDFP	PLQP0100KB-A*1	1.5 Mbytes	192 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NDCDFP	PLQP0100KB-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C
	R5F563NDDDFP	PLQP0100KB-A	1.5 Mbytes	128 Kbytes	32 Kbytes	100 MHz	-40 to +85°C

Table 1.4 Pin Functions (2/6)

Classifications	Pin Name	I/O	Description
Bus control	RD#	Output	Strobe signal which indicates that reading from the external bus interface space is in progress.
	WR#	Output	Strobe signal which indicates that writing to the external bus interface space is in progress, in 1-write strobe mode.
	WR0# to WR3#	Output	Strobe signals which indicate that either group of data bus pins (D7 to D0, D15 to D8, D23 to D16, and D31 to D24) is valid in writing to the external bus interface space, in byte strobe mode.
	BC0# to BC3#	Output	Strobe signals which indicate that either group of data bus pins (D7 to D0, D15 to D8, D23 to D16, and D31 to D24) is valid in access to the external bus interface space, in 1-write strobe mode.
	ALE	Output	Address latch signal when address/data multiplexed bus is selected.
	CKE	Output	Output pin for SDRAM clock enable signals.
	SDCS#	Output	Output pin for SDRAM chip select signals.
	RAS#	Output	Output pin for SDRAM row address strobe signals.
	CAS#	Output	Output pin for SDRAM column address strobe signals.
	WE#	Output	Output pin for SDRAM write enable signals.
	DQM0 to DQM3	Output	Output pins for SDRAM I/O data mask enable signals.
	CS0# to CS7#	Output	Select signals for CS area.
	WAIT#	Input	Input pins for wait request signals in access to the external space.
EXDMA controller	EDREQ0, EDREQ1		Input pins for external DMA transfer requests.
	EDACK0, EDACK1		Output pins for single address transfer acknowledge signals.
Interrupt	NMI	Input	Non-maskable interrupt request signal.
	IRQ0 to IRQ15	Input	Maskable interrupt request signals.
Multi-function timer pulse unit 2	MTIOC0A, MTIOC0B MTIOC0C, MTIOC0D	I/O	The TGRA0 to TGRD0 input capture input/output compare output/PWM output pins.
	MTIOC1A, MTIOC1B	I/O	The TGRA1 and TGRB1 input capture input/output compare output/PWM output pins.
	MTIOC2A, MTIOC2B	I/O	The TGRA2 and TGRB2 input capture input/output compare output/PWM output pins.
	MTIOC3A, MTIOC3B MTIOC3C, MTIOC3D	I/O	The TGRA3 to TGRD3 input capture input/output compare output/PWM output pins.
	MTIOC4A, MTIOC4B MTIOC4C, MTIOC4D	I/O	The TGRA4 to TGRD4 input capture input/output compare output/PWM output pins.
	MTIC5U, MTIC5V MTIC5W	Input	The TGRU5, TGRV5, and TGRW5 input capture input/dead time compensation input pins.
	MTCLKA, MTCLKB MTCLKC, MTCLKD	Input	Input pins for external clock signals.
Port output enable 2	POE0# to POE3# POE8#	Input	Input pins for request signals to place the MTU large-current pins in the high impedance state.

Table 1.4 Pin Functions (4/6)

Classifications	Pin Name	I/O	Description
Serial communications interface (SCId)	• Asynchronous mode/clock synchronous mode		
	SCK12	I/O	Input/output pin for clock signals.
	RXD12	Input	Input pin for data reception.
	TXD12	Output	Output pin for data transmission.
	CTS12#	Input	Transmit/receive start control input pins
	RTS12#	Output	Transmit/receive start control output pins
	• Simple I ² C mode		
	SSCL12	I/O	Input/output pins for the I ² C clock
	SSDA12	I/O	Input/output pins for the I ² C data
	• Simple SPI mode		
	SCK12	I/O	Input/output pins for the clock
	SMISO12	I/O	Input/output pins for slave transmit data.
	SMOSI12	I/O	Input/output pins for master transmit data.
	SS12#	Input	Input pins for chip select signals
	• Extended serial mode		
	RXDX12	Input	Input pin for receive data
	TXDX12	Output	Output pin for transmit data
	SIOX12	I/O	Input/output pin for Transmit/receive data
I ² C bus interface	SCL0[FM+], SCL1 to SCL3	I/O	Input/output pin for clocks. Bus can be directly driven by the N-channel open drain output.
	SDA0[FM+], SDA1 to SDA3	I/O	Input/output pin for data. Bus can be directly driven by the N-channel open drain output.
Ethernet controller	REF50CK	Input	50-MHz reference clock. This pin inputs reference signals for transmission/reception timings in RMII mode.
	RMII_CRS_DV	Input	Indicates that there are carrier detection signals and valid receive data on RMII_RXD1 and RMII_RXD0 in RMII mode.
	RMII_TXD0, RMII_TXD1	Output	2-bit transmit data in RMII mode.
	RMII_RXD0, RMII_RXD1	Input	2-bit receive data in RMII mode.
	RMII_TXD_EN	Output	Output pin for data transmit enable signals in RMII mode.
	RMII_RX_ER	Input	Indicates an error has occurred during reception of data in RMII mode.
	ET_CRS	Input	Carrier detection/data reception enable pin.
	ET_RX_DV	Input	Indicates that there are valid receive data on ET_ERXD3 to ET_ERXD0.
	ET_EXOUT	Output	General-purpose external output pin.
	ET_LINKSTA	Input	Inputs link status from the PHY-LSI.
	ET_ETXD0 to ET_ETXD3	Output	4 bits of MII transmit data.
	ET_ERXD0 to ET_ERXD3	Input	4 bits of MII receive data.
	ET_TX_EN	Output	Transmit enable pin. Indicates that transmit data is ready on ET_ETXD3 to ET_ETXD0.
	ET_TX_ER	Output	Transmit error pin. Notifies the PHY_LSI of an error during transmission.
	ET_RX_ER	Input	Receive error pin. Recognizes an error during reception.
	ET_TX_CLK	Input	Transmit clock pin. This pin inputs reference signals for output timings from ET_TX_EN, ET_ETXD3 to ET_ETXD0, and ET_TX_ER.
	ET_RX_CLK	Input	Receive clock pin. This pin inputs reference signals for input timings to ET_RX_DV, ET_ERXD3 to ET_ERXD0, and ET_RX_ER.
	ET_COL	Input	Inputs collision detection signals.
	ET_WOL	Output	Receives Magic packets.
	ET_MDC	Output	Outputs reference clock signals for information transfer via ET_MDIO.

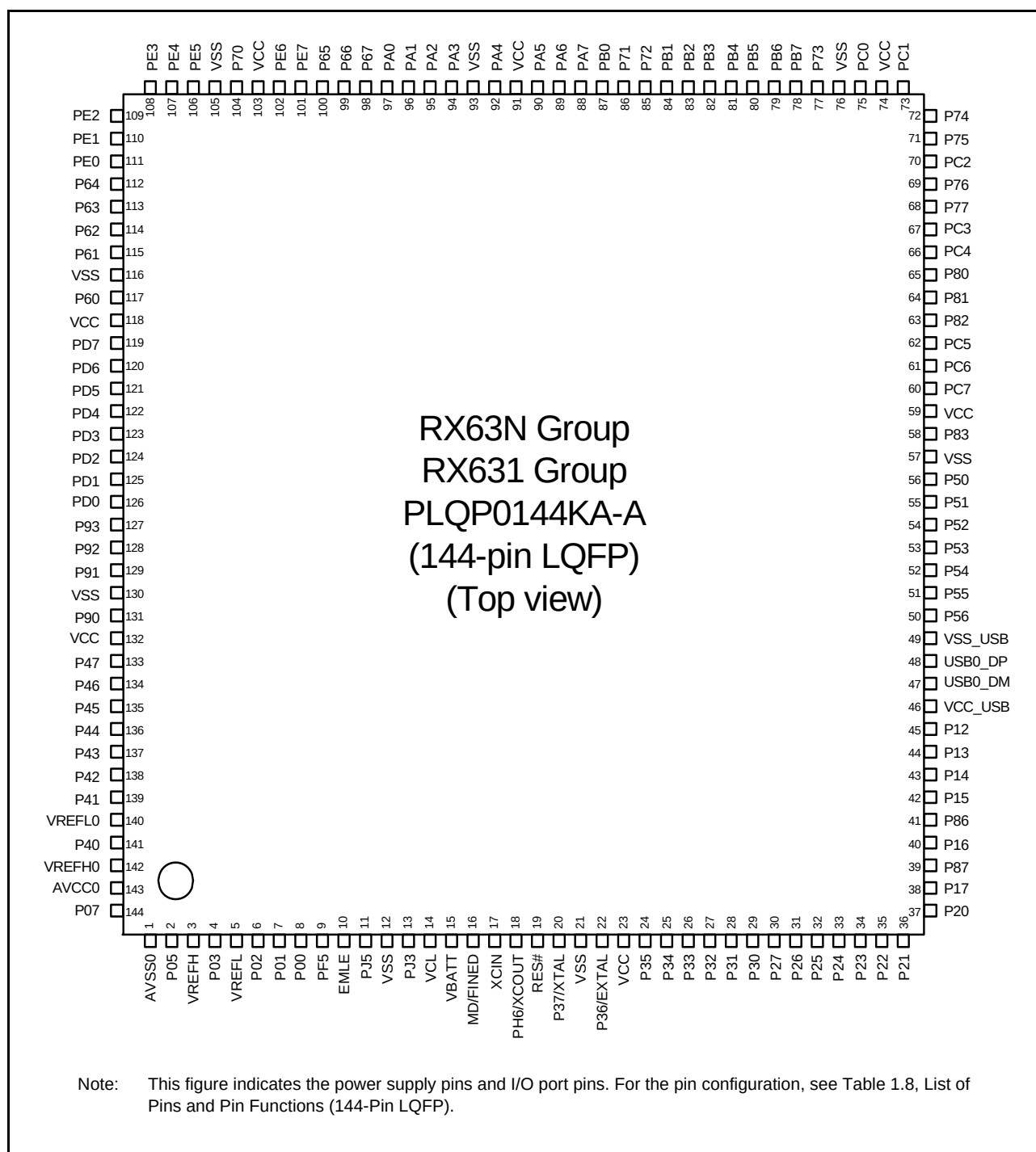
**Figure 1.7 Pin Assignment (144-Pin LQFP)**

Table 1.5 List of Pin and Pin Functions (177-Pin TFLGA, 176-Pin LFBGA) (4/5)

Pin Number 177-Pin TFLGA 176-Pin LFBGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SCIC, SCID, RSPI, RIIC, CAN, IEB, USB, and PDC)	Interrupt	S12AD, AD, DA
M2		P26	CS6#	MTIOC2A/TMO1/PO6	TXD1/CTS3#/RTS3#/ SMOSI1/SS3#/SSDA1/ MOSIB		
M3		P24	CS4#/EDREQ1	MTIOC4A/MTCLKA/ TIOCB4/TMRI1/PO4	SCK3/USB0_VBUSEN/ PIXCLK		
M4		P86		TIOCA0	PIXD1		
M5		P13		MTIOC0B/TIOCA5/TMO3/ PO13	TXD2/SMOSI2/SSDA2/ SDA0[FM+]	IRQ3	ADTRG#
M6		P56	WR2#/BC2#/ EDACK1	MTIOC3C/TIOCA1			
M7		P54	ALE/EDACK0	MTIOC4B/TMCI1	ET_LINKSTA/CTS2#/ RTS2#/SS2#/CTX1		
M8		P53*2	BCLK				
M9		P50	WR0#/WR#		TXD2/SMOSI2/SSDA2/ SSLB1		
M10		PC5	A21/CS2#/ WAIT#	MTIOC3B/MTCLKD/ TIOCD6/TCLKF/TMRI2/ PO29	ET_ETXD2/SCK8/ RSPCKA		
M11		P81	EDACK0	MTIOC3D/PO27	ET_ETXD0/RMII_TXD0/ RXD10/SMISO10/SSCL10		
M12		P77	CS7#	PO23	ET_RX_ER/RMII_RX_ER/ TXD11/SMOSI11/SSDA11		
M13		PB7	A15	MTIOC3B/TIOCB5/PO31	ET_CRS/RMII_CRS_DV/ TXD9/SMOSI9/SSDA9		
M14		PB5	A13	MTIOC2A/MTIOC1B/ TIOCB4/TMRI1/PO29/ POE1#	ET_ETXD0/RMII_TXD0/ SCK9		
M15		PB4	A12	TIOCA4/PO28	ET_TX_EN/ RMII_TXD_EN/CTS9#/ RTS9#/SS9#		
N1	VCC						
N2		P23	EDACK0	MTIOC3D/MTCLKD/ TIOCD3/PO3	TXD3/CTS0#/RTS0#/ SMOSI3/SS0#/SSDA3/ USB0_DPUPE/PIXD7		
N3		P22	EDREQ0	MTIOC3B/MTCLKC/ TIOCC3/TMO0/PO2	SCK0/USB0_DRPD/ PIXD6		
N4		P15		MTIOC0B/MTCLKB/ TIOCB2/TCLKB/TMCI2/ PO13	RXD1/SCK3/SMISO1/ SSCL1/CRX1-DS/ USB1_DPUPE/PIXD0	IRQ5	
N5		P12		MTIC5U/TMCI1	RXD2/SMISO2/SSCL2/ SCL0[FM+]	IRQ2	
N6		P57	WAIT#/WR3#/ BC3#/EDREQ1				
N7		P55	WAIT#/ EDREQ0	MTIOC4D/TMO3	ET_EXOUT/CRX1	IRQ10	
N8	VCC_USB						
N9		P51	WR1#/BC1#/ WAIT#		SCK2/SSLB2		
N10		PC7	A23/CS0#	MTIOC3A/MTCLKB/ TIOCB6/TMO2/PO31	ET_COL/TXD8/SMOSI8/ SSDA8/MISOA	IRQ14	
N11		P82	EDREQ1	MTIOC4A/PO28	ET_ETXD1/RMII_TXD1/ TXD10/SMOSI10/SSDA10		
N12		PC3	A19	MTIOC4D/TCLKB/PO24	ET_TX_ER/TXD5/ SMOSI5/SSDA5/IETXD		
N13		PC0	A16	MTIOC3C/TCLKC/PO17	ET_ERXD3/CTS5#/ RTS5#/SS5#/SSLA1/ SCL3	IRQ14	
N14		P73	CS3#	PO16	ET_WOL		
N15	VSS						

Table 1.6 List of Pin and Pin Functions (176-Pin LQFP) (4/5)

Pin Number 176-Pin LQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	Timer (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SCIC, SCID, RSPI, RIIC, CAN, IEB, USB, and PDC)	Interrupt	S12AD, AD, DA
100		PB1	A9	MTIOC0C/MTIOC4C/ TIOCB3/TMCI0/PO25	ET_ERXD0/RMII_RXD0/ TXD4/TXD6/SMOSI4/ SMOSI6/SSDA4/SSDA6	IRQ4-DS	
101		P72	CS2#		ET_MDC		
102		P71	CS1#		ET_MDIO		
103	VCC						
104		PB0	A8	MTIC5W/TIOCA3/PO24	ET_ERXD1/RMII_RXD1/ RXD4/RXD6/SMISO4/ SMISO6/SSCL4/SSCL6/ RSPCKA	IRQ12	
105	VSS						
106		PA7	A7	TIOCB2/PO23	ET_WOL/MISOA		
107		PA6	A6	MTIC5V/MTCLKB/ TIOCA2/TMCI3/PO22/ POE2#	ET_EXOUT/CTS5#/ RTS5#/SS5#/MOSIA		
108		PA5	A5	TIOCB1/PO21	ET_LINKSTA/RSPCKA		
109		PA4	A4	MTIC5U/MTCLKA/ TIOCA1/TMRI0/PO20	ET_MDC/TXD5/SMOSI5/ SSDA5/SSLA0	IRQ5-DS	
110		PA3	A3	MTIOC0D/MTCLKD/ TIOC0D/TCLKB/PO19	ET_MDIO/RXD5/SMISO5/ SSCL5	IRQ6-DS	
111	TRDATA3	PG7	D31				
112		PA2	A2	PO18	RXD5/SMISO5/SSCL5/ SSLA3		
113	TRDATA2	PG6	D30				
114		PA1	A1/DQM3	MTIOC0B/MTCLKC/ TIOCB0/PO17	ET_WOL/SCK5/SSLA2	IRQ11	
115	VCC						
116	TRCLK	PG5	D29				
117	VSS						
118		PA0	A0/BC0#/DQM2	MTIOC4A/TIOCA0/PO16	ET_TX_EN/ RMII_TXD_EN/SSLA1		
119	TRSYNC	PG4	D28				
120		P67	CS7#/DQM1		CRX2*2	IRQ15	
121	TRDATA1	PG3	D27				
122		P66	CS6#/DQM0		CTX2*2		
123	TRDATA0	PG2	D26				
124		P65	CS5#/CKE				
125		PE7	D15[A15/D15]	TIOCB11	MISOB	IRQ7	AN5
126		PE6	D14[A14/D14]	TIOCA11	MOSIB	IRQ6	AN4
127	VCC						
128	SDCLK	P70					
129	VSS						
130		PE5	D13[A13/D13]	MTIOC4C/MTIOC2B/ TIOCB10	ET_RX_CLK/REF50CK/ RSPCKB	IRQ5	AN3
131		PE4	D12[A12/D12]	MTIOC4D/MTIOC1A/ TIOCA10/PO28	ET_ERXD2/SSLB0		AN2
132		PE3	D11[A11/D11]	MTIOC4B/TIOCB9/PO26/ POE8#	ET_ERXD3/CTS12#/ RTS12#/SS12#/MISOB		AN1
133		PE2	D10[A10/D10]	MTIOC4A/TIOCA9/PO23	RXD12/SMISO12/ SSCL12/RXD12/SSLB3/ MOSIB	IRQ7-DS	AN0
134		PE1	D9[A9/D9]	MTIOC4C/TIOC0D/PO18	TXD12/SMOSI12/ SSDA12/TXD12/ SIOX12/SSLB2/RSPCKB		ANEX1
135		PE0	D8[A8/D8]	TIOCC9	SCK12/SSLB1		ANEX0

Table 1.10 List of Pins and Pin Functions (100-Pin LQFP) (2/4)

Pin No. 100-pin LQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC	Timers (MTU, TPU, TMR, PPG, RTC, POE)	Communications (ETHERC, SCIC, SCID, RSPI, RIIC, CAN, IEB, USB)	Interrupt	S12AD AD DA
31		P15		MTIOC0B/MTCLKB/ TIOCB2/TCLKB/TMC12/ PO13	RXD1/SCK3/SMISO1/ SSCL1/CRX1-DS	IRQ5	
32		P14		MTIOC3A/MTCLKA/ TIOCB5/TCLKA/TMR12/ PO15	CTS1#/RTS1#/SS1#/ CTX1/USB0_DPUPE/ USB0_OVRCURA	IRQ4	
33		P13		MTIOC0B/TIOCA5/ TMO3/PO13	TXD2/SMOSI2/SSDA2/ SDA0[FM+]	IRQ3	ADTRG#
34		P12		TMC11	RXD2/SMISO2/SSCL2/ SCL0[FM+]	IRQ2	
35	VCC_USB						
36					USB0_DM		
37					USB0_DP		
38	VSS_USB						
39		P55	WAIT#/ EDREQ0	MTIOC4D/TMO3	CRX1/ET_EXOUT	IRQ10	
40		P54	ALE/EDACK0	MTIOC4B/TMC11	CTS2#/RTS2#/SS2#/ CTX1/ET_LINKSTA		
41		P53*2	BCLK				
42		P52	RD#		RXD2/SMISO2/SSCL2/ SSLB3		
43		P51	WR1#/BC1#/ WAIT#		SCK2/SSLB2		
44		P50	WR0#/WR#		TXD2/SMOSI2/SSDA2/ SSLB1		
45		PC7	A23/CS0#	MTIOC3A/MTCLKB/ TMO2/PO31	TXD8/SMOSI8/SSDA8/ MISOA/ET_COL	IRQ14	
46		PC6	A22/CS1#	MTIOC3C/MTCLKA/ TMC12/PO30	RXD8/SMISO8/SSCL8/ MOSIA/ET_ETXD3	IRQ13	
47		PC5	A21/CS2#/ WAIT#	MTIOC3B/MTCLKD/ TMR12/PO29	SCK8/RSPCKA/ ET_ETXD2		
48		PC4	A20/CS3#	MTIOC3D/MTCLKC/ TMC11/PO25/POE0#	SCK5/CTS8#/RTS8#/ SS8#/SSLA0/ ET_TX_CLK		
49		PC3	A19	MTIOC4D/TCLKB/ PO24	TXD5/SMOSI5/SSDA5/ IETXD/ET_TX_ER		
50		PC2	A18	MTIOC4B/TCLKA/PO21	RXD5/SMISO5/SSCL5/ SSLA3/IERXD/ ET_RX_DV		
51		PC1	A17	MTIOC3A/TCLKD/ PO18	SCK5/SSLA2/ ET_ERXD2	IRQ12	
52		PC0	A16	MTIOC3C/TCLKC/ PO17	CTS5#/RTS5#/SS5#/ SSLA1/ET_ERXD3	IRQ14	
53		PB7	A15	MTIOC3B/TIOCB5/ PO31	TXD9/SMOSI9/SSDA9/ ET_CRS/ RMII_CRS_DV		
54		PB6	A14	MTIOC3D/TIOCA5/ PO30	RXD9/SMISO9/SSCL9/ ET_ETXD1/RMII_TXD1		
55		PB5	A13	MTIOC2A/MTIOC1B/ TIOCB4/TMR11/PO29/ POE1#	SCK9/ET_ETXD0/ RMII_TXD0		
56		PB4	A12	TIOCA4/PO28	CTS9#/RTS9#/SS9#/ ET_TX_EN/ RMII_TXD_EN		
57		PB3	A11	MTIOC0A/MTIOC4A/ TIOCD3/TCLKD/TMO0/ PO27/POE3#	SCK6/ET_RX_ER/ RMII_RX_ER		
58		PB2	A10	TIOCC3/TCLKC/PO26	CTS6#/RTS6#/SS6#/ ET_RX_CLK/REF50CK		

Table 1.11 List of Pins and Pin Functions (64-Pin TFLGA) (2/2)

Pin No. 64-pin TFLGA	Power Supply Clock System Control	I/O Port	Timers (MTU2a, TPUa, TMR, PPG, RTCa, POE2a)	Communications (SClC, SClD, RSPI, RIIC, CAN, IEB, USB)	Interrupt	S12ADa, DAa
E4	TMS	P16	MTIOC3C/MTIOC3D/ TIOCB1/TCLKC/TMO2/ RTCOUT	TXD1/SMOSI1/SSDA1/ MOSIA/SCL2-DS/IERXD/ USB0_VBUS/ USB0_VBUSEN/ USB0_OVRCURB	IRQ6	ADTRG0#
E5		PC4	MTIOC3D/MTCLKC/TMC1/ PO25/POE0#	SCK5/SSLA0/ USB0_DPRPD		
E6	VCC					
E7	VSS					
E8		PB0	MTIC5W/TIOCA3/PO24	RXD6/SMISO6/SSCL6/ RSPCKA	IRQ12	
F1	VCC					
F2		P35			NMI	
F3		P31	MTIOC4D/TMC12/RTCIC1	CTS1#/RTS1#/SS1#/ SSLB0/USB0_DPUPE	IRQ1-DS	
F4		PC5	MTIOC3B/MTCLKD/TMR12/ PO29	RSPCKA/USB0_ID		
F5		P15	MTIOC0B/MTCLKB/ TIOCB2/TCLKB/TMC12	RXD1/SMISO1/SSCL1/ CRX1-DS/USB1_DPUPE	IRQ5	
F6		PB1	MTIOC0C/MTIOC4C/ TIOCB3/TMC10/PO25	TXD6/SMOSI6/SSDA6	IRQ4-DS	
F7		PB5	MTIOC2A/MTIOC1B/ TIOCB4/TMR11/PO29/ POE1#	SCK9		
F8		PB3	MTIOC0A/MTIOC4A/ TIOCD3/TCLKD/TMO0/ PO27/POE3#	SCK6		
G1	EXTAL	P36				
G2	TDO	P26	MTIOC2A/TMO1	TXD1/SMOSI1/SSDA1/ MOSIB/USB0_VBUSEN		
G3	VCC_USB					
G4	VSS_USB					
G5	VCC_USB					
G6		PC6	MTIOC3C/MTCLKA/TMC12/ PO30	MOSIA/USB0_EXICEN	IRQ13	
G7		PC3	MTIOC4D/TCLKB/PO24	TXD5/SMOSI5/SSDA5/ SDA2/IETXD		
G8		PB6	MTIOC3D/TIOCA5/PO30	RXD9/SMISO9/SSCL9		
H1	XTAL	P37				
H2	TRST#	P17	MTIOC3A/MTIOC3B/ TIOCB0/TCLKD/TMO1/ POE8#	SCK1/MISOA/SDA2-DS/ IETXD/USB1_VBUS	IRQ7	
H3				USB0_DM		
H4				USB0_DP		
H5				USB1_DM		
H6				USB1_DP		
H7		PC2	MTIOC4B/TCLKA/PO21	RXD5/SMISO5/SSCL5/ SSLA3/SCL2/IERXD		
H8		PB7	MTIOC3B/TIOCB5/PO31	TXD9/SMOSI9/SSDA9		

Table 1.13 List of Pins and Pin Functions (48-Pin LQFP) (1/2)

Pin Number 48-Pin LQFP	Power Supply Clock System Control	I/O Port	Timer (MTU2a, TPUa, TMR, PPG, POE2a)	Communications (SC1c, SC1d, RSPI, RIIC, CAN, IEB, USB)	Interrupt	S12ADa, DAa
1	VCL					
2	MD/FINED					
3	RES#					
4	XTAL	P37				
5	VSS					
6	EXTAL	P36				
7	VCC					
8		P35			NMI	
9		P31	MTIOC4D/TMC12/PO9	CTS1#/RTS1#/SS1#/ SSLB0/USB0_DPUPE	IRQ1-DS	
10		P30	MTIOC4B/TMR13/PO8/ POE8#	RXD1/SMISO1/SSCL1/ MISOB/USB0_DRPD	IRQ0-DS	
11	FINEC	P27	MTIOC2B/TMC13/PO7	SCK1/RSPCKB		
12		P26	MTIOC2A/TMO1/PO6	TXD1/SMOSI1/SSDA1/ MOSIB/USB0_VBUSEN		
13		P17	MTIOC3A/MTIOC3B/ TIOCB0/TCLKD/TMO1/ PO15/POE8#	SCK1/MISOA/SDA2-DS/ IETXD	IRQ7	
14		P16	MTIOC3C/MTIOC3D/ TIOCB1/TCLKC/TMO2/ PO14	TXD1/SMOSI1/SSDA1/ MOSIA/SCL2-DS/IERXD/ USB0_VBUS/ USB0_VBUSEN/ USB0_OVRCURB	IRQ6	ADTRG0#
15		P15	MTIOC0B/MTCLKB/ TIOCB2/TCLKB/TMC12/ PO13	RXD1/SMISO1/SSCL1/ CRX1-DS	IRQ5	
16		P14	MTIOC3A/MTCLKA/ TIOCB5/TCLKA/TMR12/ PO15	CTS1#/RTS1#/SS1#/ CTX1/USB0_DPUPE/ USB0_OVRCURA	IRQ4	
17	VCC_USB					
18				USB0_DM		
19				USB0_DP		
20	VSS_USB					
21		PC7	MTIOC3A/MTCLKB/ TMO2 /PO31	TXD8/SMOSI8/SSDA8/ MISOA	IRQ14	
22		PC6	MTIOC3C/MTCLKA/ TMC12/PO30	RXD8/SMISO8/SSCL8/ MOSIA/USB0_EXICEN	IRQ13	
23		PC5	MTIOC3B/MTCLKD/ TMR12/PO29	SCK8/RSPCKA/USB0_ID		
24		PC4	MTIOC3D/MTCLKC/ TMC11/PO25/POE0#	SCK5/CTS8#/RTS8#/SS8#/ /SSLA0/ USB0_DPRPD		
25		PB5/ PC3	MTIOC2A/MTIOC1B/ TIOCB4/TMR11/PO29/ POE1#			
26		PB3/ PC2	MTIOC0A/MTIOC4A/ TIOC3D/TCLKD/TMO0/ PO27/POE3#	SCK6		
27		PB1/ PC1	MTIOC0C/MTIOC4C/ TIOCB3/TMC10/PO25	TXD6/SMOSI6/SSDA6	IRQ4-DS	
28	VCC					

3. Address Space

3.1 Address Space

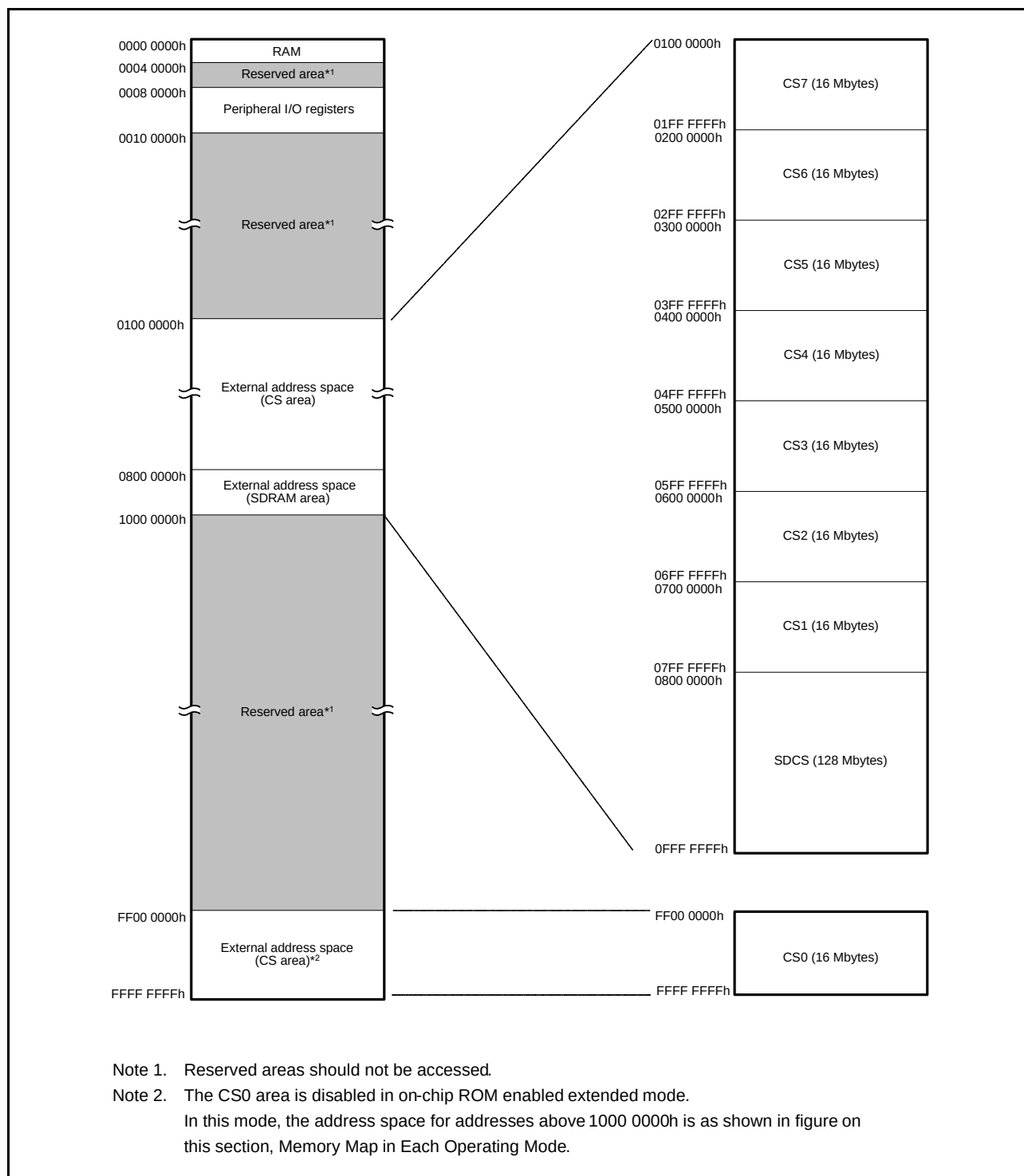
This LSI has a 4-Gbyte address space, consisting of the range of addresses from 0000 0000h to FFFF FFFFh. That is, linear access to an address space of up to 4 Gbytes is possible, and this contains both program and data areas.

Figure 3.1 shows the memory maps in the respective operating modes. Accessible areas will differ according to the operating mode and states of control bits.

3.2 External Address Space

The external address space is classified into CS areas (CS0 to CS7) and SDRAM area (SDCS). CS areas can be divided into up to eight areas (CS0 to CS7) corresponding to the CSn# signal to be output from the CSn# pin.

Figure 3.2 shows the address ranges corresponding to the individual CS areas (CS0 to CS7) and SDRAM area (SDCS) in on-chip ROM disabled extended mode.



**Figure 3.2 Correspondence between External Address Spaces and CS Areas
(In On-Chip ROM Disabled Extended Mode)**

- Longword-size I/O registers

```
MOV.L #SFR_ADDR, R1
MOV.L #SFR_DATA, [R1]
CMP [R1].L, R1
;; Next process
```

If multiple registers are written to and a subsequent instruction should be executed after the write operations are entirely completed, only read the I/O register that was last written to and execute the operation using the value; it is not necessary to read or execute operation for all the registers that were written to.

(3) Number of Access Cycles to I/O Registers

For the number of I/O register access cycles, refer to Table 4.1, List of I/O Registers (Address Order).

The number of access cycles to I/O registers is obtained by following equation.*1

$$\begin{aligned} \text{Number of access cycles to I/O registers} = & \text{Number of bus cycles for internal main bus 1} + \\ & \text{Number of divided clock synchronization cycles} + \\ & \text{Number of bus cycles for internal peripheral busses 1 to 6} \end{aligned}$$

The number of bus cycles of internal peripheral bus 1 to 6 differs according to the register to be accessed.

When peripheral functions connected to internal peripheral bus 2 to 6 or registers for the external bus control unit (except for bus error related registers) are accessed, the number of divided clock synchronization cycles is added.

The number of divided clock synchronization cycles differs depending on the frequency ratio between ICLK and PCLK (or FCLK, BCLK) or bus access timing.

In the peripheral function unit, when the frequency ratio of ICLK is equal to or greater than that of PCLK (or FCLK), the sum of the number of bus cycles for internal main bus 1 and the number of the divided clock synchronization cycles will be one cycle of PCLK (or FCLK) at a maximum. Therefore, one PCLK (or FCLK) has been added to the number of access states shown in Table 4.1.

When the frequency ratio of ICLK is lower than that of PCLK (or FCLK), the subsequent bus access is started from the ICLK cycle following the completion of the access to the peripheral functions. Therefore, the access cycles are described on an ICLK basis.

In the external bus control unit, the sum of the number of bus cycles for internal main bus 1 and the number of divided clock synchronization cycles will be one cycle of BCLK at a maximum. Therefore, one BCLK is added to the number of access cycles shown in Table 4.1.

Note 1. This applies to the number of cycles when the access from the CPU does not conflict with the instruction fetching to the external memory or bus access from the different bus master (DMAC or DTC).

(4) Restrictions in Relation to RMPA and String-Manipulation Instructions

The allocation of data to be handled by RMPA or string-manipulation instructions to I/O registers is prohibited, and operation is not guaranteed if this restriction is not observed.

4.1 I/O Register Addresses (Address Order)

Table 4.1 List of I/O Registers (Address Order) (1/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 0000h	SYSTEM	Mode monitor register	MDMONR	16	16	3 ICLK		Operating Modes
0008 0002h	SYSTEM	Mode status register	MDSR	16	16	3 ICLK		
0008 0006h	SYSTEM	System control register 0	SYSCR0	16	16	3 ICLK		
0008 0008h	SYSTEM	System control register 1	SYSCR1	16	16	3 ICLK		
0008 000Ch	SYSTEM	Standby control register	SBYCR	16	16	3 ICLK		Low Power Consumption
0008 0010h	SYSTEM	Module stop control register A	MSTPCRA	32	32	3 ICLK		
0008 0014h	SYSTEM	Module stop control register B	MSTPCRB	32	32	3 ICLK		
0008 0018h	SYSTEM	Module stop control register C	MSTPCRC	32	32	3 ICLK		
0008 001Ch	SYSTEM	Module stop control register D	MSTPCRD	32	32	3 ICLK		Clock Generation Circuit
0008 0020h	SYSTEM	System clock control register	SCKCR	32	32	3 ICLK		
0008 0024h	SYSTEM	System clock control register 2	SCKCR2	16	16	3 ICLK		
0008 0026h	SYSTEM	System clock control register 3	SCKCR3	16	16	3 ICLK		
0008 0028h	SYSTEM	PLL control register	PLLCR	16	16	3 ICLK		
0008 002Ah	SYSTEM	PLL control register 2	PLLCR2	8	8	3 ICLK		
0008 0030h	SYSTEM	External bus clock control register	BCKCR	8	8	3 ICLK		
0008 0032h	SYSTEM	Main clock oscillator control register	MOSCCR	8	8	3 ICLK		
0008 0033h	SYSTEM	Sub-clock oscillator control register	SOSCCR	8	8	3 ICLK		
0008 0034h	SYSTEM	Low-speed on-chip oscillator control register	LOCOCR	8	8	3 ICLK		
0008 0035h	SYSTEM	IWDT-dedicated on-chip oscillator control register	ILOCOCR	8	8	3 ICLK		
0008 0036h	SYSTEM	High-speed on-chip oscillator control register	HOCOCR	8	8	3 ICLK		
0008 0040h	SYSTEM	Oscillation stop detection control register	OSTDCR	8	8	3 ICLK		
0008 0041h	SYSTEM	Oscillation stop detection status register	OSTDSR	8	8	3 ICLK		
0008 00A0h	SYSTEM	Operating power control register	OPCCR	8	8	3 ICLK		Low Power Consumption
0008 00A1h	SYSTEM	Sleep mode return clock source switching register	RSTCKCR	8	8	3 ICLK		
0008 00A2h	SYSTEM	Main clock oscillator wait control register	MOSCWTCR	8	8	3 ICLK		
0008 00A3h	SYSTEM	Sub-clock oscillator wait control register	SOSCWTCR	8	8	3 ICLK		
0008 00A6h	SYSTEM	PLL wait control register	PLLWTCR	8	8	3 ICLK		Resets
0008 00C0h	SYSTEM	Reset status register 2	RSTS2	8	8	3 ICLK		
0008 00C2h	SYSTEM	Software reset register	SWRR	16	16	3 ICLK		LVDA
0008 00E0h	SYSTEM	Voltage monitoring 1 circuit control register 1	LVD1CR1	8	8	3 ICLK		
0008 00E1h	SYSTEM	Voltage monitoring 1 circuit status register	LVD1SR	8	8	3 ICLK		
0008 00E2h	SYSTEM	Voltage monitoring 2 circuit control register 1	LVD2CR1	8	8	3 ICLK		
0008 00E3h	SYSTEM	Voltage monitoring 2 circuit status register	LVD2SR	8	8	3 ICLK		Register Write Protection Function
0008 03FEh	SYSTEM	Protect register	PRCR	16	16	3 ICLK		
0008 1300h	BSC	Bus error status clear register	BERCLR	8	8	2 ICLK		Buses
0008 1304h	BSC	Bus error monitoring enable register	BEREN	8	8	2 ICLK		
0008 1308h	BSC	Bus error status register 1	BERSR1	8	8	2 ICLK		
0008 130Ah	BSC	Bus error status register 2	BERSR2	16	16	2 ICLK		
0008 1310h	BSC	Bus priority control register	BUSPRI	16	16	2 ICLK		
0008 2000h	DMAC0	DMA source address register	DMSAR	32	32	2 ICLK		DMACA
0008 2004h	DMAC0	DMA destination address register	DMDAR	32	32	2 ICLK		
0008 2008h	DMAC0	DMA transfer count register	DMCRA	32	32	2 ICLK		
0008 200Ch	DMAC0	DMA block transfer count register	DMCRB	16	16	2 ICLK		
0008 2010h	DMAC0	DMA transfer mode register	DMTMD	16	16	2 ICLK		
0008 2013h	DMAC0	DMA interrupt setting register	DMINT	8	8	2 ICLK		
0008 2014h	DMAC0	DMA address mode register	DMAMD	16	16	2 ICLK		
0008 2018h	DMAC0	DMA offset register	DMOFR	32	32	2 ICLK		

Table 4.1 List of I/O Registers (Address Order) (21/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0008 83BAh	RSPI1	RSPI command register 5	SPCMD5	16	16	2, 3 PCLKB	2 ICLK	RSPI
0008 83BCh	RSPI1	RSPI command register 6	SPCMD6	16	16	2, 3 PCLKB	2 ICLK	
0008 83BEh	RSPI1	RSPI command register 7	SPCMD7	16	16	2, 3 PCLKB	2 ICLK	
0008 83C0h	RSPI2	RSPI control register	SPCR	8	8	2, 3 PCLKB	2 ICLK	
0008 83C1h	RSPI2	RSPI slave select polarity register	SSLP	8	8	2, 3 PCLKB	2 ICLK	
0008 83C2h	RSPI2	RSPI pin control register	SPPCR	8	8	2, 3 PCLKB	2 ICLK	
0008 83C3h	RSPI2	RSPI status register	SPSR	8	8	2, 3 PCLKB	2 ICLK	
0008 83C4h	RSPI2	RSPI data register	SPDR	32	16, 32	2, 3 PCLKB	2 ICLK	
0008 83C8h	RSPI2	RSPI sequence control register	SPSCR	8	8	2, 3 PCLKB	2 ICLK	
0008 83C9h	RSPI2	RSPI sequence status register	SPSSR	8	8	2, 3 PCLKB	2 ICLK	
0008 83CAh	RSPI2	RSPI bit rate register	SPBR	8	8	2, 3 PCLKB	2 ICLK	
0008 83CBh	RSPI2	RSPI data control register	SPDCR	8	8	2, 3 PCLKB	2 ICLK	
0008 83CCh	RSPI2	RSPI clock delay register	SPCKD	8	8	2, 3 PCLKB	2 ICLK	
0008 83CDh	RSPI2	RSPI slave select negation delay register	SSLND	8	8	2, 3 PCLKB	2 ICLK	
0008 83CEh	RSPI2	RSPI next-access delay register	SPND	8	8	2, 3 PCLKB	2 ICLK	
0008 83CFh	RSPI2	RSPI control register 2	SPCR2	8	8	2, 3 PCLKB	2 ICLK	
0008 83D0h	RSPI2	RSPI command register 0	SPCMD0	16	16	2, 3 PCLKB	2 ICLK	
0008 83D2h	RSPI2	RSPI command register 1	SPCMD1	16	16	2, 3 PCLKB	2 ICLK	
0008 83D4h	RSPI2	RSPI command register 2	SPCMD2	16	16	2, 3 PCLKB	2 ICLK	
0008 83D6h	RSPI2	RSPI command register 3	SPCMD3	16	16	2, 3 PCLKB	2 ICLK	
0008 83D8h	RSPI2	RSPI command register 4	SPCMD4	16	16	2, 3 PCLKB	2 ICLK	
0008 83DAh	RSPI2	RSPI command register 5	SPCMD5	16	16	2, 3 PCLKB	2 ICLK	
0008 83DCh	RSPI2	RSPI command register 6	SPCMD6	16	16	2, 3 PCLKB	2 ICLK	
0008 83DEh	RSPI2	RSPI command register 7	SPCMD7	16	16	2, 3 PCLKB	2 ICLK	
0008 8600h	MTU3	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK	MTU2a
0008 8601h	MTU4	Timer control register	TCR	8	8	2, 3 PCLKB	2 ICLK	
0008 8602h	MTU3	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK	
0008 8603h	MTU4	Timer mode register	TMDR	8	8	2, 3 PCLKB	2 ICLK	
0008 8604h	MTU3	Timer I/O control register H	TIORH	8	8	2, 3 PCLKB	2 ICLK	
0008 8605h	MTU3	Timer I/O control register L	TIORL	8	8	2, 3 PCLKB	2 ICLK	
0008 8606h	MTU4	Timer I/O control register H	TIORH	8	8	2, 3 PCLKB	2 ICLK	
0008 8607h	MTU4	Timer I/O control register L	TIORL	8	8	2, 3 PCLKB	2 ICLK	
0008 8608h	MTU3	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK	
0008 8609h	MTU4	Timer interrupt enable register	TIER	8	8	2, 3 PCLKB	2 ICLK	
0008 860Ah	MTU	Timer output master enable register	TOER	8	8	2, 3 PCLKB	2 ICLK	
0008 860Dh	MTU	Timer gate control register	TGCR	8	8	2, 3 PCLKB	2 ICLK	
0008 860Eh	MTU	Timer output control register 1	TOCR1	8	8	2, 3 PCLKB	2 ICLK	
0008 860Fh	MTU	Timer output control register 2	TOCR2	8	8	2, 3 PCLKB	2 ICLK	
0008 8610h	MTU3	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	
0008 8612h	MTU4	Timer counter	TCNT	16	16	2, 3 PCLKB	2 ICLK	
0008 8614h	MTU	Timer cycle data register	TCDR	16	16	2, 3 PCLKB	2 ICLK	
0008 8616h	MTU	Timer dead time data register	TDDR	16	16	2, 3 PCLKB	2 ICLK	
0008 8618h	MTU3	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	
0008 861Ah	MTU3	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	
0008 861Ch	MTU4	Timer general register A	TGRA	16	16	2, 3 PCLKB	2 ICLK	
0008 861Eh	MTU4	Timer general register B	TGRB	16	16	2, 3 PCLKB	2 ICLK	
0008 8620h	MTU	Timer subcounter	TCNTS	16	16	2, 3 PCLKB	2 ICLK	
0008 8622h	MTU	Timer cycle buffer register	TCBR	16	16	2, 3 PCLKB	2 ICLK	
0008 8624h	MTU3	Timer general register C	TGRC	16	16	2, 3 PCLKB	2 ICLK	
0008 8626h	MTU3	Timer general register D	TGRD	16	16	2, 3 PCLKB	2 ICLK	
0008 8628h	MTU4	Timer general register C	TGRC	16	16	2, 3 PCLKB	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (37/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK≥PCLK	ICLK<PCLK	
0009 1428h	CAN1	Mask invalid register	MKIVLR	32	8, 16, 32	2, 3 PCLKB	2 ICLK	CAN
0009 142Ch	CAN1	Mailbox interrupt enable register	MIER	32	8, 16, 32	2, 3 PCLKB	2 ICLK	
0009 1820h to 0009 183Fh	CAN1	Message control registers 0 to 31	MCTL0 to 31	8	8	2, 3 PCLKB	2 ICLK	
0009 1840h	CAN1	Control register	CTLR	16	8, 16	2, 3 PCLKB	2 ICLK	
0009 1842h	CAN1	Status register	STR	16	8, 16	2, 3 PCLKB	2 ICLK	
0009 1844h	CAN1	Bit configuration register	BCR	32	8, 16, 32	2, 3 PCLKB	2 ICLK	
0009 1848h	CAN1	Receive FIFO control register	RFCR	8	8	2, 3 PCLKB	2 ICLK	
0009 1849h	CAN1	Receive FIFO pointer control register	RFPCR	8	8	2, 3 PCLKB	2 ICLK	
0009 184Ah	CAN1	Transmit FIFO control register	TFCR	8	8	2, 3 PCLKB	2 ICLK	
0009 184Bh	CAN1	Transmit FIFO pointer control register	TFPCR	8	8	2, 3 PCLKB	2 ICLK	
0009 184Ch	CAN1	Error interrupt enable register	EIER	8	8	2, 3 PCLKB	2 ICLK	
0009 184Dh	CAN1	Error interrupt factor judge register	EIFR	8	8	2, 3 PCLKB	2 ICLK	
0009 184Eh	CAN1	Receive error count register	RECR	8	8	2, 3 PCLKB	2 ICLK	
0009 184Fh	CAN1	Transmit error count register	TECR	8	8	2, 3 PCLKB	2 ICLK	
0009 1850h	CAN1	Error code store register	ECSR	8	8	2, 3 PCLKB	2 ICLK	
0009 1851h	CAN1	Channel search support register	CSSR	8	8	2, 3 PCLKB	2 ICLK	
0009 1852h	CAN1	Mailbox search status register	MSSR	8	8	2, 3 PCLKB	2 ICLK	
0009 1853h	CAN1	Mailbox search mode register	MSMR	8	8	2, 3 PCLKB	2 ICLK	
0009 1854h	CAN1	Time stamp register	TSR	16	8, 16	2, 3 PCLKB	2 ICLK	
0009 1856h	CAN1	Acceptance filter support register	AFSR	16	8, 16	2, 3 PCLKB	2 ICLK	
0009 1858h	CAN1	Test control register	TCR	8	8	2, 3 PCLKB	2 ICLK	
0009 2200h to 0009 23FFh	CAN2	Mailbox registers 0 to 31	MB0 to 31	128	8, 16, 32	2, 3 PCLKB	2 ICLK	
0009 2400h to 0009 241Fh	CAN2	Mask register 0 to 7	MKR0 to 7	32	8, 16, 32	2, 3 PCLKB	2 ICLK	
0009 2420h	CAN2	FIFO received ID compare register 0	FIDCR0	32	8, 16, 32	2, 3 PCLKB	2 ICLK	
0009 2424h	CAN2	FIFO received ID compare register 1	FIDCR1	32	8, 16, 32	2, 3 PCLKB	2 ICLK	
0009 2428h	CAN2	Mask invalid register	MKIVLR	32	8, 16, 32	2, 3 PCLKB	2 ICLK	
0009 242Ch	CAN2	Mailbox interrupt enable register	MIER	32	8, 16, 32	2, 3 PCLKB	2 ICLK	
0009 2820h to 0009 283Fh	CAN2	Message control registers 0 to 31	MCTL0 to 31	8	8	2, 3 PCLKB	2 ICLK	
0009 2840h	CAN2	Control register	CTLR	16	8, 16	2, 3 PCLKB	2 ICLK	
0009 2842h	CAN2	Status register	STR	16	8, 16	2, 3 PCLKB	2 ICLK	
0009 2844h	CAN2	Bit configuration register	BCR	32	8, 16, 32	2, 3 PCLKB	2 ICLK	
0009 2848h	CAN2	Receive FIFO control register	RFCR	8	8	2, 3 PCLKB	2 ICLK	
0009 2849h	CAN2	Receive FIFO pointer control register	RFPCR	8	8	2, 3 PCLKB	2 ICLK	
0009 284Ah	CAN2	Transmit FIFO control register	TFCR	8	8	2, 3 PCLKB	2 ICLK	
0009 284Bh	CAN2	Transmit FIFO pointer control register	TFPCR	8	8	2, 3 PCLKB	2 ICLK	
0009 284Ch	CAN2	Error interrupt enable register	EIER	8	8	2, 3 PCLKB	2 ICLK	
0009 284Dh	CAN2	Error interrupt factor judge register	EIFR	8	8	2, 3 PCLKB	2 ICLK	
0009 284Eh	CAN2	Receive error count register	RECR	8	8	2, 3 PCLKB	2 ICLK	
0009 284Fh	CAN2	Transmit error count register	TECR	8	8	2, 3 PCLKB	2 ICLK	
0009 2850h	CAN2	Error code store register	ECSR	8	8	2, 3 PCLKB	2 ICLK	
0009 2851h	CAN2	Channel search support register	CSSR	8	8	2, 3 PCLKB	2 ICLK	
0009 2852h	CAN2	Mailbox search status register	MSSR	8	8	2, 3 PCLKB	2 ICLK	
0009 2853h	CAN2	Mailbox search mode register	MSMR	8	8	2, 3 PCLKB	2 ICLK	
0009 2854h	CAN2	Time stamp register	TSR	16	16	2, 3 PCLKB	2 ICLK	
0009 2856h	CAN2	Acceptance filter support register	AFSR	16	16	2, 3 PCLKB	2 ICLK	
0009 2858h	CAN2	Test control register	TCR	8	8	2, 3 PCLKB	2 ICLK	

Table 4.1 List of I/O Registers (Address Order) (46/50)

Address	Module Symbol	Register Name	Register Symbol	Number of Bits	Access Size	Number of Access States		Related Function
						ICLK $\geq$ PCLK	ICLK<PCLK	
000A 0268h	USB1	Pipe configuration register	PIPECFG	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 026Ch	USB1	Pipe maximum packet size register	PEMAXP	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 026Eh	USB1	Pipe cycle control register	PIPEPERI	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 0270h	USB1	Pipe 1 control register	PIPE1CTR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	USBa
000A 0272h	USB1	Pipe 2 control register	PIPE2CTR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 0274h	USB1	Pipe 3 control register	PIPE3CTR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 0276h	USB1	Pipe 4 control register	PIPE4CTR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 0278h	USB1	Pipe 5 control register	PIPE5CTR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 027Ah	USB1	Pipe 6 control register	PIPE6CTR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	
000A 027Ch	USB1	Pipe 7 control register	PIPE7CTR	16	16	9 PCLKB or more	Rounded up to the nearest integer greater than 1 + 9/ (frequency ratio of ICLK/ PCLKB) ^{*6}	

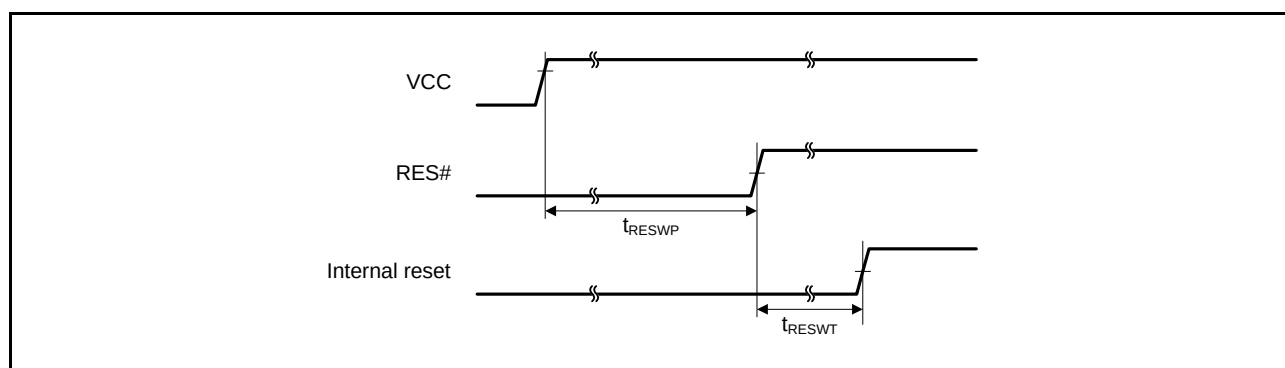


Figure 5.1 Reset Input Timing at Power-On

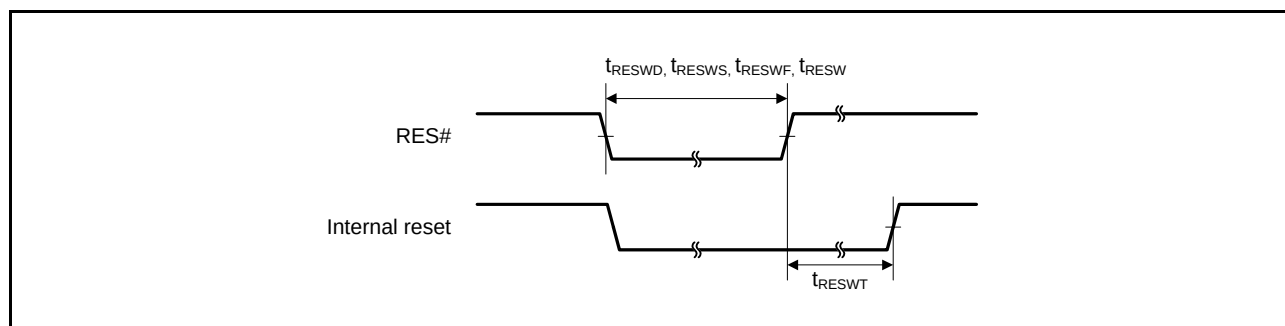
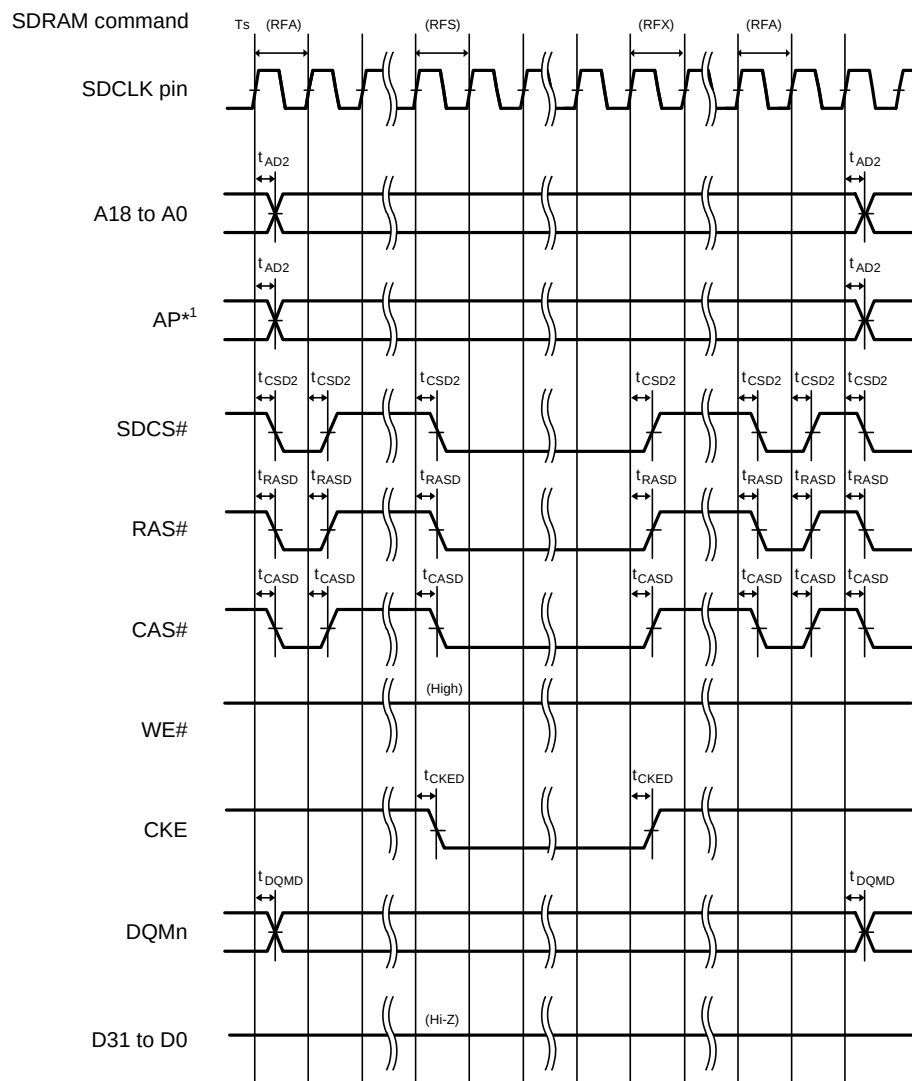


Figure 5.2 Reset Input Timing



Note 1: Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

Figure 5.30 SDRAM Space Self-Refresh Bus Timing

5.3.6 EXDMAC Timing

Table 5.18 EXDMAC Timing

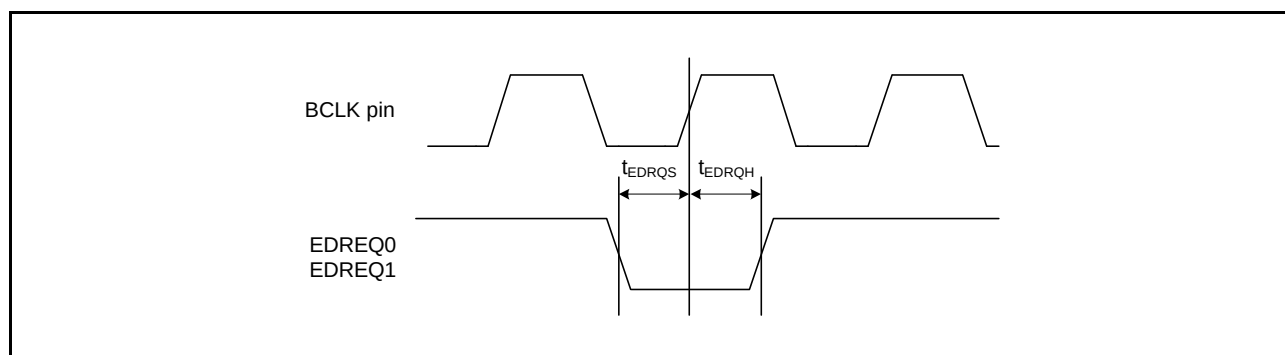
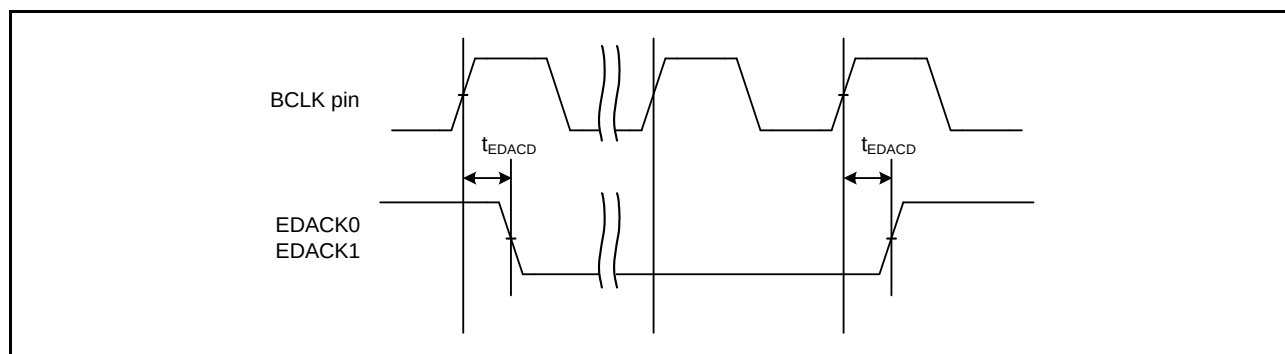
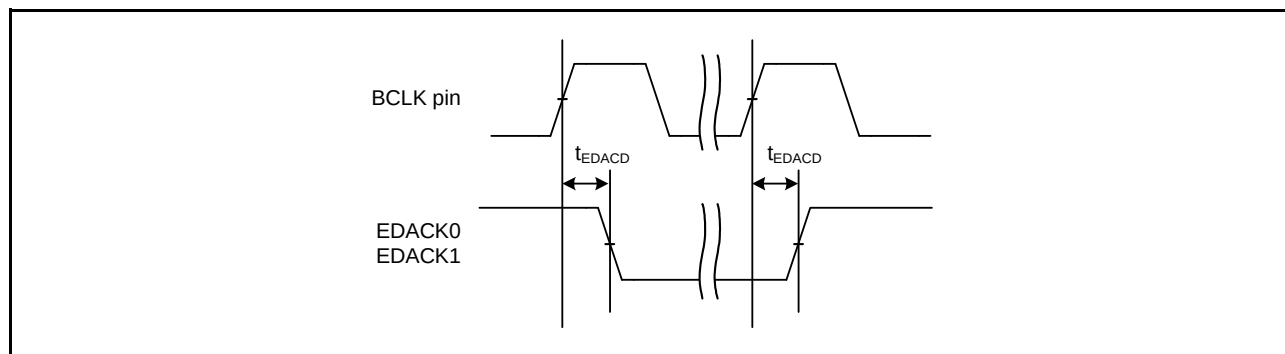
Conditions: $V_{CC} = AV_{CC0} = V_{REFH} = V_{CC_USB} = 2.7$ to 3.6 V, $V_{REFH0} = 2.7$ V to AV_{CC0} ,

$V_{SS} = AV_{SS0} = V_{REFL}/V_{REFL0} = V_{SS_USB} = 0$ V

$ICLK = 8$ to 100 MHz, $PCLK = 8$ to 50 MHz, $BCLK$ pin = 8 to 100 MHz, $SDCLK$ pin = 8 to 50 MHz, $T_a = T_{opr}$

High drive output is selected by the drive capacity control register

	Item	Symbol	Min.	Max.	Unit	Test Conditions
EXDMAC	EDREQ setup time	t_{EDRQS}	20	—	ns	Figure 5.31
	EDREQ hold time	t_{EDRQH}	5	—	ns	Figure 5.32 and Figure 5.33
	EDACK delay time	t_{EDACD}	—	15	ns	Figure 5.33

**Figure 5.31 EDREQ0 and EDREQ1 Input Timing****Figure 5.32 EDACK0 and EDACK1 Single-Address Transfer Timing (for a CS Area)****Figure 5.33 EDACK0 and EDACK1 Single-Address Transfer Timing (for SDRAM)**

5.9 Oscillation Stop Detection Timing

Table 5.34 Oscillation Stop Detection Circuit Characteristics

Conditions: $V_{CC} = AV_{CC0} = V_{REFH} = V_{CC_USB} = V_{BATT} = 2.7$ to 3.6 V, $V_{REFH0} = 2.7$ V to AV_{CC0}
 $V_{SS} = AV_{SS0} = V_{REFL}/V_{REFL0} = V_{SS_USB} = 0$ V
 $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Detection time	t_{dr}	—	—	1	ms	Figure 5.67

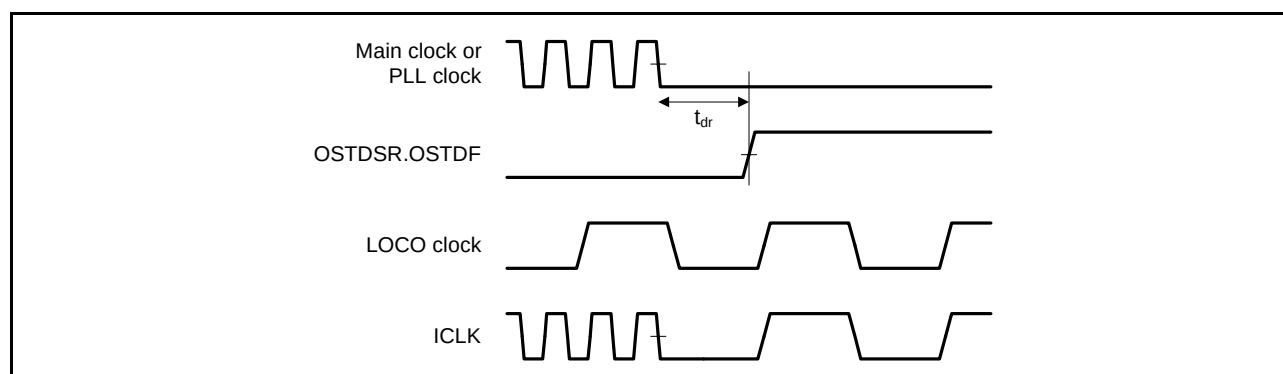


Figure 5.67 Oscillation Stop Detection Timing