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Embedded - Microcontrollers - Application Specific: Tailored Solutions for Precision and Performance

Embedded - Microcontrollers - Application Specific represents a category of microcontrollers designed with unique features and capabilities tailored to specific application needs. Unlike general-purpose microcontrollers, application-specific microcontrollers are optimized for particular tasks, offering enhanced performance, efficiency, and functionality to meet the demands of specialized applications.

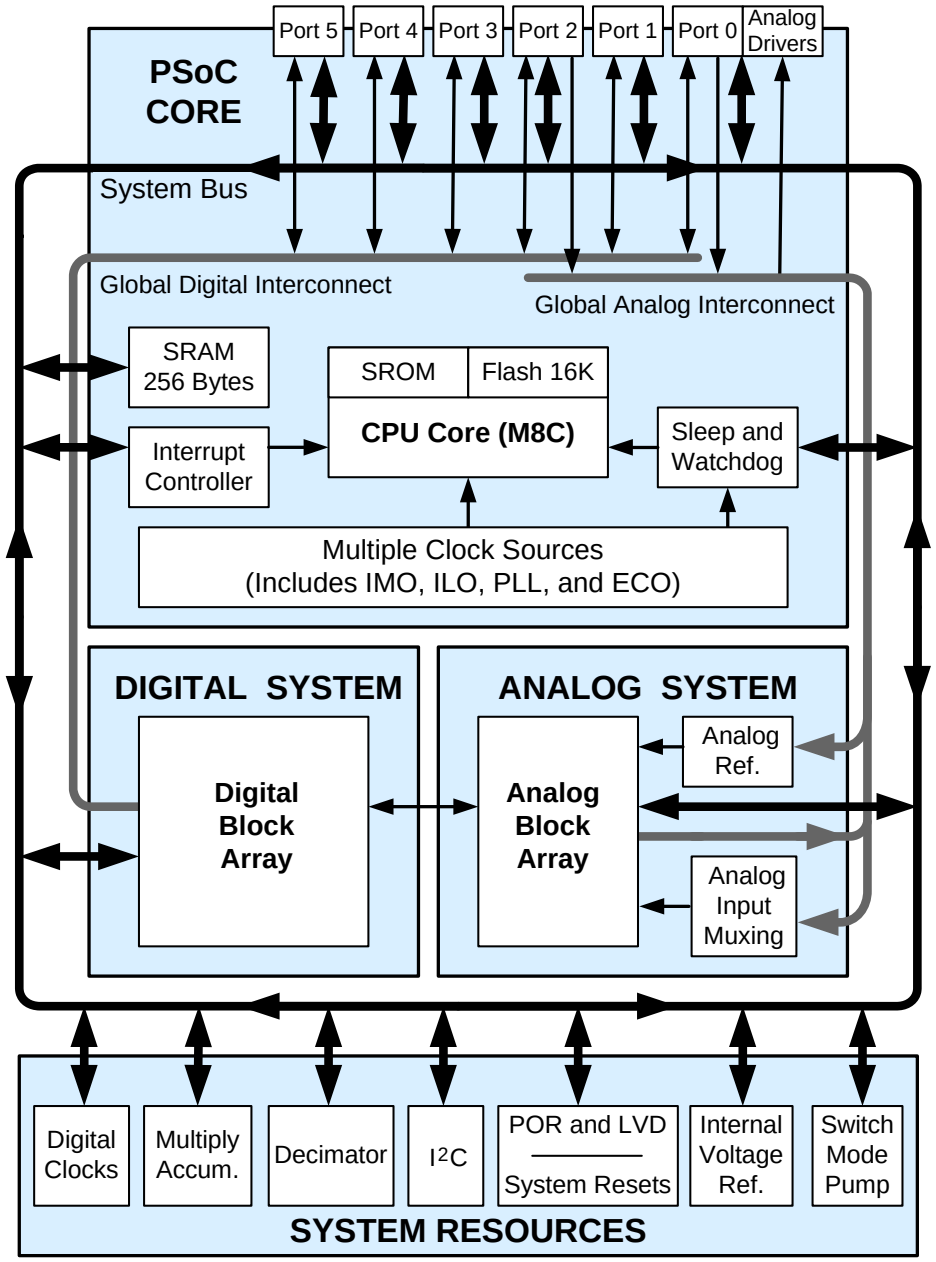
What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	HB LED Controller
Core Processor	M8C
Program Memory Type	FLASH (16KB)
Controller Series	CY8CLED
RAM Size	256 x 8
Interface	I²C, SPI, UART/USART
Number of I/O	44
Voltage - Supply	3V ~ 5.25V
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8cled08-48lfxi

Overview

Block Diagram



EZ-Color Functional Overview

Cypress' EZ-Color family of devices offers the ideal control solution for High Brightness LED applications requiring intelligent dimming control. EZ-Color devices combine the power and flexibility of PSoC (Programmable System-on-Chip™); with Cypress' PrISM (precise illumination signal modulation) modulation technology providing lighting designers a fully customizable and integrated lighting solution platform.

The EZ-Color family supports up to 16 independent LED channels with up to 32 bits of resolution per channel, enabling lighting designers the flexibility to choose the LED array size and color quality. PSoC Express software, with lighting specific drivers, can significantly cut development time and simplify implementation of fixed color points through temperature and LED binning compensation. EZ-Color's virtually limitless analog and digital customization allow for simple integration of features in addition to intelligent lighting, such as Battery Charging, Image Stabilization, and Motor Control during the development process. These features, along with Cypress' best-in-class quality and design support, make EZ-Color the ideal choice for intelligent HB LED control applications.

Target Applications

- LCD Backlight
- Large Signs
- General Lighting
- Architectural Lighting
- Camera/Cell Phone Flash
- Flashlights

The PSoC Core

The PSoC Core is a powerful engine that supports a rich feature set. The core includes a CPU, memory, clocks, and configurable GPIO (General Purpose IO).

The M8C CPU core is a powerful processor with speeds up to 48 MHz, providing a four MIPS 8-bit Harvard architecture microprocessor. The CPU utilizes an interrupt controller with 17 vectors, to simplify programming of real time embedded events. Program execution is timed and protected using the included Sleep and Watch Dog Timers (WDT).

Memory encompasses 16K of Flash for program storage, 256 bytes of SRAM for data storage, and up to 2K of EEPROM emulated using the Flash. Program Flash utilizes four protection levels on blocks of 64 bytes, allowing customized software IP protection.

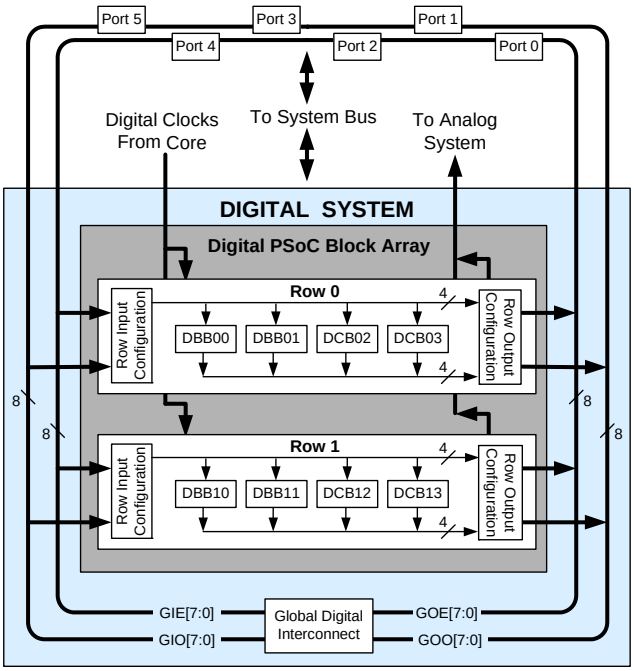
The EZ-Color family incorporates flexible internal clock generators, including a 24 MHz IMO (internal main oscillator) accurate to 2.5% over temperature and voltage. The 24 MHz IMO can also be doubled to 48 MHz for use by the digital system. A low power 32 kHz ILO (internal low speed oscillator) is provided for the Sleep timer and WDT. If crystal accuracy is desired, the ECO (32.768 kHz external crystal oscillator) is available for use as a Real Time Clock (RTC) and can optionally generate a crystal-accurate 24 MHz system clock using a PLL. The clocks, together with programmable clock dividers (as a System Resource), provide the flexibility to integrate almost any timing requirement into the EZ-Color device.

EZ-Color GPIOs provide connection to the CPU, digital and analog resources of the device. Each pin's drive mode may be selected from eight options, allowing great flexibility in external interfacing. Every pin also has the capability to generate a system interrupt on high level, low level, and change from last read.

The Digital System

The Digital System is composed of 8 digital blocks. Each block is an 8-bit resource that can be used alone or combined with other blocks to form 8, 16, 24, and 32-bit peripherals, which are called user module references.

Figure 1. Digital System Block Diagram



Digital peripheral configurations include those listed below.

- PrISM (8 to 32 bit)
- PWMs (8 to 32 bit)
- PWMs with Dead band (8 to 32 bit)
- Counters (8 to 32 bit)
- Timers (8 to 32 bit)
- UART 8 bit with selectable parity (up to 2)
- SPI slave and master (up to 2)
- I2C slave and multi-master (1 available as a System Resource)
- Cyclical Redundancy Checker/Generator (8 to 32 bit)
- IrDA (up to 2)
- Generators (8 to 32 bit)

Additional System Resources

System Resources, some of which have been previously listed, provide additional capability useful to complete systems. Additional resources include a multiplier, decimator, switch mode pump, low voltage detection, and power on reset. Statements describing the merits of each system resource are below.

- Digital clock dividers provide three customizable clock frequencies for use in applications. The clocks can be routed to both the digital and analog systems. Additional clocks can be generated using digital blocks as clock dividers.
- Multiply accumulate (MAC) provides fast 8-bit multiplier with 32-bit accumulate, to assist in general math and digital filters.
- The decimator provides a custom hardware filter for digital signal processing applications including the creation of Delta Sigma ADCs.
- The I2C module provides 100 and 400 kHz communication over two wires. Slave, master, and multi-master modes are all supported.
- Low Voltage Detection (LVD) interrupts can signal the application of falling voltage levels, while the advanced POR (Power On Reset) circuit eliminates the need for a system supervisor.
- An internal 1.3V reference provides an absolute reference for the analog system, including ADCs and DACs.
- An integrated switch mode pump (SMP) generates normal operating voltages from a single 1.2V battery cell, providing a low cost boost converter.

EZ-Color Device Characteristics

Depending on your EZ-Color device characteristics, the digital and analog systems can have 16, 8, or 4 digital blocks and 12, 6, or 4 analog blocks. The following table lists the resources available for specific EZ-Color device groups. The device covered by this data sheet is shown in the highlighted row of the table

Table 1. EZ-Color Device Characteristics

Part Number	LED Channels	Digital IO	Digital Rows	Digital Blocks	Analog Inputs	Analog Outputs	Analog Columns	Analog Blocks	SRAM Size	Flash Size	CapSense
CY8CLED02	2	16	1	4	8	0	2	4	256 Bytes	4K	No
CY8CLED04	4	56	1	4	48	2	2	6	1K	16K	Yes
CY8CLED08	8	44	2	8	12	4	4	12	256 Bytes	16K	No
CY8CLED16	16	64	4	16	12	4	4	12	2K	32K	No

Getting Started

The quickest path to understanding the EZ-Color silicon is by reading this data sheet and using the PSoC Express Integrated Development Environment (IDE). This data sheet is an overview of the EZ-Color integrated circuit and presents specific pin, register, and electrical specifications.

For up-to-date Ordering, Packaging, and Electrical Specification information, reference the latest device data sheets on the web at http://www.cypress.com/ez-color.

Development Kits

Development Kits are available from the following distributors: Digi-Key, Avnet, Arrow, and Future. The Cypress Online Store contains development kits, **C** compilers, and all accessories for PSoC development. Go to the Cypress Online Store web site at http://www.cypress.com, click the Online Store shopping cart icon at the bottom of the web page, and click **EZ-Color** to view a current list of available items.

Technical Training Modules

Free PSoC technical training modules are available for users new to PSoC. Training modules cover designing, debugging, advanced analog and CapSense. Go to http://www.cypress.com/techtrain.

Consultants

Certified PSoC Consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC Consultant go to http://www.cypress.com, click on Design Support located on the left side of the web page, and select CYPros Consultants.

Technical Support

PSoC application engineers take pride in fast and accurate response. They can be reached with a 4-hour guaranteed response at http://www.cypress.com/support/login.cfm.

Application Notes

A long list of application notes will assist you in every aspect of your design effort. To view the PSoC application notes, go to the http://www.cypress.com web site and select Application Notes under the Design Resources list located in the center of the web page. Application Notes are sorted by date by default.

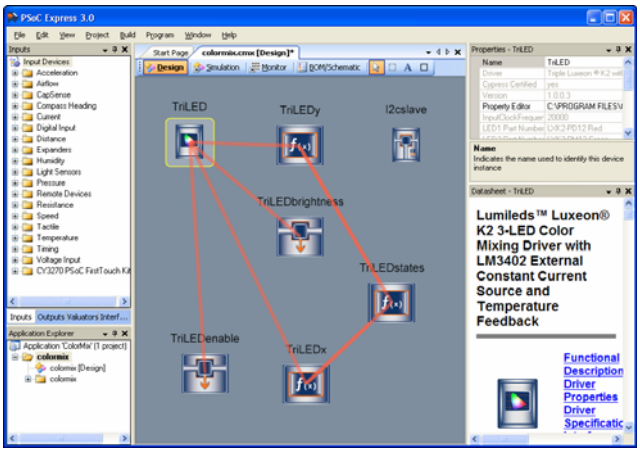
Development Tools

PSoC Express is a high-level design tool for creating embedded systems with devices using Cypress's PSoC Mixed-Signal technology. With PSoC Express you create a complete embedded solution including all necessary on-chip peripherals, block configuration, interrupt handling and application software without writing a single line of assembly or C code.

PSoC Express solves design problems the way you think about the system:

- Select input and output devices based upon system requirements.
- Add a communications interface and define its interface to system (using registers).
- Define when and how an output device changes state based upon any and all other system devices.
- Based upon the design, automatically select an EZ-Color Controller that matches system requirements.

Figure 3. PSoC Express



PSoC Express Subsystems

Express Editor

The Express Editor allows you to create designs visually by dragging and dropping inputs, outputs, communication interfaces, and other design elements, and then describing the logic that controls them.

Project Manager

The Project Manager allows you to work with your applications and projects in PSoC Express. A PSoC Express application is a top level container for projects and their associated files. Each project contains a design that uses a single PSoC device. An application can contain multiple projects so if you are creating an application that uses multiple PSoC devices you can keep all of the projects together in a single application.

Most of the files associated with a project are automatically generated by PSoC Express during the build process, but you can make changes directly to the custom.c and custom.h files

48-Pin Part Pinout QFN

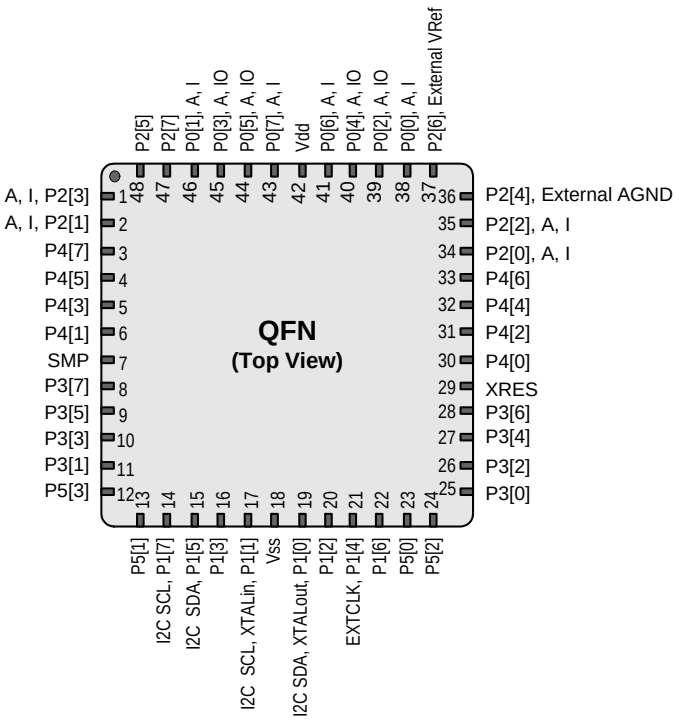
Table 3. 48-Pin Part Pinout (QFN**)

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	IO	I	P2[3]	Direct switched capacitor block input.
2	IO	I	P2[1]	Direct switched capacitor block input.
3	IO		P4[7]	
4	IO		P4[5]	
5	IO		P4[3]	
6	IO		P4[1]	
7	Power		SMP	Switch Mode Pump (SMP) connection to external components required.
8	IO		P3[7]	
9	IO		P3[5]	
10	IO		P3[3]	
11	IO		P3[1]	
12	IO		P5[3]	
13	IO		P5[1]	
14	IO		P1[7]	I2C Serial Clock (SCL).
15	IO		P1[5]	I2C Serial Data (SDA).
16	IO		P1[3]	
17	IO		P1[1]	Crystal Input (XTALin), I2C Serial Clock (SCL), ISSP-SCLK*.
18	Power		Vss	Ground connection.
19	IO		P1[0]	Crystal Output (XTALout), I2C Serial Data (SDA), ISSP-SDATA*.
20	IO		P1[2]	
21	IO		P1[4]	Optional External Clock Input (EXTCLK).
22	IO		P1[6]	
23	IO		P5[0]	
24	IO		P5[2]	
25	IO		P3[0]	
26	IO		P3[2]	
27	IO		P3[4]	
28	IO		P3[6]	
29	Input		XRES	Active high external reset with internal pull down.
30	IO		P4[0]	
31	IO		P4[2]	
32	IO		P4[4]	
33	IO		P4[6]	
34	IO	I	P2[0]	Direct switched capacitor block input.
35	IO	I	P2[2]	Direct switched capacitor block input.
36	IO		P2[4]	External Analog Ground (AGND).
37	IO		P2[6]	External Voltage Reference (VRef).
38	IO	I	P0[0]	Analog column mux input.
39	IO	IO	P0[2]	Analog column mux input and column output.
40	IO	IO	P0[4]	Analog column mux input and column output.
41	IO	I	P0[6]	Analog column mux input.
42	Power		Vdd	Supply voltage.
43	IO	I	P0[7]	Analog column mux input.
44	IO	IO	P0[5]	Analog column mux input and column output.
45	IO	IO	P0[3]	Analog column mux input and column output.
46	IO	I	P0[1]	Analog column mux input.
47	IO		P2[7]	
48	IO		P2[5]	

LEGEND: A = Analog, I = Input, and O = Output.
* These are the ISSP pins, which are not High Z at POR (Power On Reset).

** The QFN package has a center pad that must be connected to ground (Vss).

Figure 5. 48-Pin Device



28-Pin Part Pinout

Table 4. 28-Pin Part Pinout (SSOP)

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	IO	I	P0[7]	Analog column mux input.
2	IO	IO	P0[5]	Analog column mux input and column output.
3	IO	IO	P0[3]	Analog column mux input and column output.
4	IO	I	P0[1]	Analog column mux input.
5	IO		P2[7]	
6	IO		P2[5]	
7	IO	I	P2[3]	Direct switched capacitor block input.
8	IO	I	P2[1]	Direct switched capacitor block input.
9	Power		SMP	Switch Mode Pump (SMP) connection to external components required.
10	IO		P1[7]	I2C Serial Clock (SCL).
11	IO		P1[5]	I2C Serial Data (SDA).
12	IO		P1[3]	
13	IO		P1[1]	Crystal Input (XTALin), I2C Serial Clock (SCL), ISSP-SCLK*.
14	Power		Vss	Ground connection.
15	IO		P1[0]	Crystal Output (XTALout), I2C Serial Data (SDA), ISSP-SDATA*.
16	IO		P1[2]	
17	IO		P1[4]	Optional External Clock Input (EXTCLK).
18	IO		P1[6]	
19	Input		XRES	Active high external reset with internal pull down.
20	IO	I	P2[0]	Direct switched capacitor block input.
21	IO	I	P2[2]	Direct switched capacitor block input.
22	IO		P2[4]	External Analog Ground (AGND).
23	IO		P2[6]	External Voltage Reference (VRef).
24	IO	I	P0[0]	Analog column mux input.
25	IO	IO	P0[2]	Analog column mux input and column output.
26	IO	IO	P0[4]	Analog column mux input and column output.
27	IO	I	P0[6]	Analog column mux input.
28	Power		Vdd	Supply voltage.

LEGEND: A = Analog, I = Input, and O = Output.
* These are the ISSP pins, which are not High Z at POR (Power On Reset).

Figure 6. 28-Pin Device

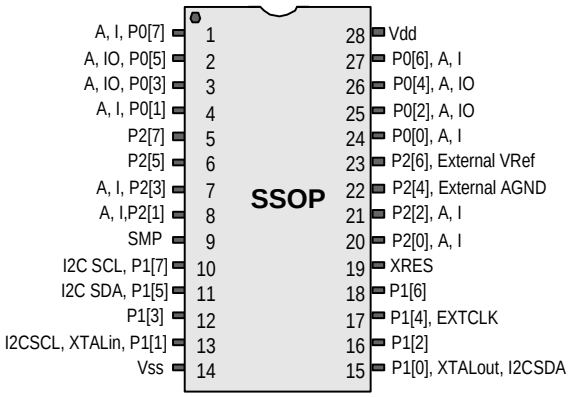


Table 5. Register Map Bank 0 Table: User Space

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
PRT0DR	00	RW		40		ASC10CR0	80	RW		C0	
PRT0IE	01	RW		41		ASC10CR1	81	RW		C1	
PRT0GS	02	RW		42		ASC10CR2	82	RW		C2	
PRT0DM2	03	RW		43		ASC10CR3	83	RW		C3	
PRT1DR	04	RW		44		ASD11CR0	84	RW		C4	
PRT1IE	05	RW		45		ASD11CR1	85	RW		C5	
PRT1GS	06	RW		46		ASD11CR2	86	RW		C6	
PRT1DM2	07	RW		47		ASD11CR3	87	RW		C7	
PRT2DR	08	RW		48		ASC12CR0	88	RW		C8	
PRT2IE	09	RW		49		ASC12CR1	89	RW		C9	
PRT2GS	0A	RW		4A		ASC12CR2	8A	RW		CA	
PRT2DM2	0B	RW		4B		ASC12CR3	8B	RW		CB	
PRT3DR	0C	RW		4C		ASD13CR0	8C	RW		CC	
PRT3IE	0D	RW		4D		ASD13CR1	8D	RW		CD	
PRT3GS	0E	RW		4E		ASD13CR2	8E	RW		CE	
PRT3DM2	0F	RW		4F		ASD13CR3	8F	RW		CF	
PRT4DR	10	RW		50		ASD20CR0	90	RW		D0	
PRT4IE	11	RW		51		ASD20CR1	91	RW		D1	
PRT4GS	12	RW		52		ASD20CR2	92	RW		D2	
PRT4DM2	13	RW		53		ASD20CR3	93	RW		D3	
PRT5DR	14	RW		54		ASC21CR0	94	RW		D4	
PRT5IE	15	RW		55		ASC21CR1	95	RW		D5	
PRT5GS	16	RW		56		ASC21CR2	96	RW	I2C_CFG	D6	RW
PRT5DM2	17	RW		57		ASC21CR3	97	RW	I2C_SCR	D7	#
	18			58		ASD22CR0	98	RW	I2C_DR	D8	RW
	19			59		ASD22CR1	99	RW	I2C_MSCR	D9	#
	1A			5A		ASD22CR2	9A	RW	INT_CLR0	DA	RW
	1B			5B		ASD22CR3	9B	RW	INT_CLR1	DB	RW
	1C			5C		ASC23CR0	9C	RW		DC	
	1D			5D		ASC23CR1	9D	RW	INT_CLR3	DD	RW
	1E			5E		ASC23CR2	9E	RW	INT_MSK3	DE	RW
	1F			5F		ASC23CR3	9F	RW		DF	
DBB00DR0	20	#	AMX_IN	60	RW		A0		INT_MSK0	E0	RW
DBB00DR1	21	W		61			A1		INT_MSK1	E1	RW
DBB00DR2	22	RW		62			A2		INT_VC	E2	RC
DBB00CR0	23	#	ARF_CR	63	RW		A3		RES_WDT	E3	W
DBB01DR0	24	#	CMP_CR0	64	#		A4		DEC_DH	E4	RC
DBB01DR1	25	W	ASY_CR	65	#		A5		DEC_DL	E5	RC
DBB01DR2	26	RW	CMP_CR1	66	RW		A6		DEC_CR0	E6	RW
DBB01CR0	27	#		67			A7		DEC_CR1	E7	RW
DCB02DR0	28	#		68			A8		MUL_X	E8	W
DCB02DR1	29	W		69			A9		MUL_Y	E9	W
DCB02DR2	2A	RW		6A			AA		MUL_DH	EA	R
DCB02CR0	2B	#		6B			AB		MUL_DL	EB	R
DCB03DR0	2C	#		6C			AC		ACC_DR1	EC	RW
DCB03DR1	2D	W		6D			AD		ACC_DR0	ED	RW
DCB03DR2	2E	RW		6E			AE		ACC_DR3	EE	RW
DCB03CR0	2F	#		6F			AF		ACC_DR2	EF	RW
DBB10DR0	30	#	ACB00CR3	70	RW	RDI0RI	B0	RW		F0	
DBB10DR1	31	W	ACB00CR0	71	RW	RDI0SYN	B1	RW		F1	
DBB10DR2	32	RW	ACB00CR1	72	RW	RDI0IS	B2	RW		F2	
DBB10CR0	33	#	ACB00CR2	73	RW	RDI0LT0	B3	RW		F3	
DBB11DR0	34	#	ACB01CR3	74	RW	RDI0LT1	B4	RW		F4	
DBB11DR1	35	W	ACB01CR0	75	RW	RDI0RO0	B5	RW		F5	
DBB11DR2	36	RW	ACB01CR1	76	RW	RDI0RO1	B6	RW		F6	
DBB11CR0	37	#	ACB01CR2	77	RW		B7		CPU_F	F7	RL
DCB12DR0	38	#	ACB02CR3	78	RW	RDI1RI	B8	RW		F8	
DCB12DR1	39	W	ACB02CR0	79	RW	RDI1SYN	B9	RW		F9	
DCB12DR2	3A	RW	ACB02CR1	7A	RW	RDI1IS	BA	RW		FA	
DCB12CR0	3B	#	ACB02CR2	7B	RW	RDI1LT0	BB	RW		FB	
DCB13DR0	3C	#	ACB03CR3	7C	RW	RDI1LT1	BC	RW		FC	
DCB13DR1	3D	W	ACB03CR0	7D	RW	RDI1RO0	BD	RW		FD	
DCB13DR2	3E	RW	ACB03CR1	7E	RW	RDI1RO1	BE	RW	CPU_SCR1	FE	#
DCB13CR0	3F	#	ACB03CR2	7F	RW		BF		CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed. # Access is bit specific.

Table 6. Register Map Bank 1 Table: Configuration Space

Name	Add (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	00	RW		40		ASC10CR0	80	RW		C0	
PRT0DM1	01	RW		41		ASC10CR1	81	RW		C1	
PRT0IC0	02	RW		42		ASC10CR2	82	RW		C2	
PRT0IC1	03	RW		43		ASC10CR3	83	RW		C3	
PRT1DM0	04	RW		44		ASD11CR0	84	RW		C4	
PRT1DM1	05	RW		45		ASD11CR1	85	RW		C5	
PRT1IC0	06	RW		46		ASD11CR2	86	RW		C6	
PRT1IC1	07	RW		47		ASD11CR3	87	RW		C7	
PRT2DM0	08	RW		48		ASC12CR0	88	RW		C8	
PRT2DM1	09	RW		49		ASC12CR1	89	RW		C9	
PRT2IC0	0A	RW		4A		ASC12CR2	8A	RW		CA	
PRT2IC1	0B	RW		4B		ASC12CR3	8B	RW		CB	
PRT3DM0	0C	RW		4C		ASD13CR0	8C	RW		CC	
PRT3DM1	0D	RW		4D		ASD13CR1	8D	RW		CD	
PRT3IC0	0E	RW		4E		ASD13CR2	8E	RW		CE	
PRT3IC1	0F	RW		4F		ASD13CR3	8F	RW		CF	
PRT4DM0	10	RW		50		ASD20CR0	90	RW	GDI_O_IN	D0	RW
PRT4DM1	11	RW		51		ASD20CR1	91	RW	GDI_E_IN	D1	RW
PRT4IC0	12	RW		52		ASD20CR2	92	RW	GDI_O_OU	D2	RW
PRT4IC1	13	RW		53		ASD20CR3	93	RW	GDI_E_OU	D3	RW
PRT5DM0	14	RW		54		ASC21CR0	94	RW		D4	
PRT5DM1	15	RW		55		ASC21CR1	95	RW		D5	
PRT5IC0	16	RW		56		ASC21CR2	96	RW		D6	
PRT5IC1	17	RW		57		ASC21CR3	97	RW		D7	
	18			58		ASD22CR0	98	RW		D8	
	19			59		ASD22CR1	99	RW		D9	
	1A			5A		ASD22CR2	9A	RW		DA	
	1B			5B		ASD22CR3	9B	RW		DB	
	1C			5C		ASC23CR0	9C	RW		DC	
	1D			5D		ASC23CR1	9D	RW	OSC_GO_EN	DD	RW
	1E			5E		ASC23CR2	9E	RW	OSC_CR4	DE	RW
	1F			5F		ASC23CR3	9F	RW	OSC_CR3	DF	RW
DBB00FN	20	RW	CLK_CR0	60	RW		A0		OSC_CR0	E0	RW
DBB00IN	21	RW	CLK_CR1	61	RW		A1		OSC_CR1	E1	RW
DBB00OU	22	RW	ABF_CR0	62	RW		A2		OSC_CR2	E2	RW
	23		AMD_CR0	63	RW		A3		VLT_CR	E3	RW
DBB01FN	24	RW		64			A4		VLT_CMP	E4	R
DBB01IN	25	RW		65			A5			E5	
DBB01OU	26	RW	AMD_CR1	66	RW		A6			E6	
	27		ALT_CR0	67	RW		A7			E7	
DCB02FN	28	RW	ALT_CR1	68	RW		A8		IMO_TR	E8	W
DCB02IN	29	RW	CLK_CR2	69	RW		A9		ILO_TR	E9	W
DCB02OU	2A	RW		6A			AA		BDG_TR	EA	RW
	2B			6B			AB		ECO_TR	EB	W
DCB03FN	2C	RW		6C			AC			EC	
DCB03IN	2D	RW		6D			AD			ED	
DCB03OU	2E	RW		6E			AE			EE	
	2F			6F			AF			EF	
DBB10FN	30	RW	ACB00CR3	70	RW	RDI0RI	B0	RW		F0	
DBB10IN	31	RW	ACB00CR0	71	RW	RDI0SYN	B1	RW		F1	
DBB10OU	32	RW	ACB00CR1	72	RW	RDI0IS	B2	RW		F2	
	33		ACB00CR2	73	RW	RDI0LT0	B3	RW		F3	
DBB11FN	34	RW	ACB01CR3	74	RW	RDI0LT1	B4	RW		F4	
DBB11IN	35	RW	ACB01CR0	75	RW	RDI0RO0	B5	RW		F5	
DBB11OU	36	RW	ACB01CR1	76	RW	RDI0RO1	B6	RW		F6	
	37		ACB01CR2	77	RW		B7		CPU_F	F7	RL
DCB12FN	38	RW	ACB02CR3	78	RW	RDI1RI	B8	RW		F8	
DCB12IN	39	RW	ACB02CR0	79	RW	RDI1SYN	B9	RW		F9	
DCB12OU	3A	RW	ACB02CR1	7A	RW	RDI1IS	BA	RW		FA	
	3B		ACB02CR2	7B	RW	RDI1LT0	BB	RW		FB	
DCB13FN	3C	RW	ACB03CR3	7C	RW	RDI1LT1	BC	RW		FC	
DCB13IN	3D	RW	ACB03CR0	7D	RW	RDI1RO0	BD	RW		FD	
DCB13OU	3E	RW	ACB03CR1	7E	RW	RDI1RO1	BE	RW	CPU_SCR1	FE	#
	3F		ACB03CR2	7F	RW		BF		CPU_SCR0	FF	#

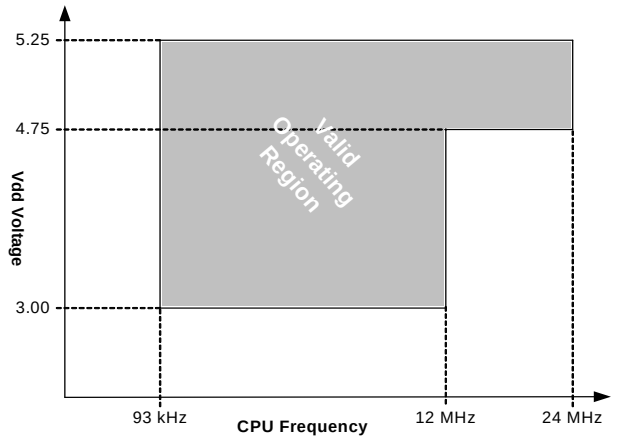
Blank fields are Reserved and should not be accessed. # Access is bit specific.

Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8CLED08 EZ-Color device. For the most up to date electrical specifications, confirm that you have the most recent data sheet by going to the web at http://www.cypress.com/ez-color.

Specifications are valid for -40°C ≤ T_A ≤ 85°C and T_J ≤ 100°C, except where noted. Specifications for devices running at greater than 12 MHz are valid for -40°C ≤ T_A ≤ 70°C and T_J ≤ 82°C.

Figure 7. Voltage versus CPU Frequency



The following table lists the units of measure that are used in this section.

Table 7. Units of Measure

Symbol	Unit of Measure	Symbol	Unit of Measure
°C	degree Celsius	µW	microwatts
dB	decibels	mA	milli-ampere
fF	femto farad	ms	milli-second
Hz	hertz	mV	milli-volts
KB	1024 bytes	nA	nanoampere
Kbit	1024 bits	ns	nanosecond
kHz	kilohertz	nV	nanovolts
kΩ	kilohm	Ω	ohm
MHz	megahertz	pA	picoampere
MΩ	megaohm	pF	picofarad
µA	microampere	pp	peak-to-peak
µF	microfarad	ppm	parts per million
µH	microhenry	ps	picosecond
µs	microsecond	sps	samples per second
µV	microvolts	σ	sigma: one standard deviation
µVrms	microvolts root-mean-square	V	volts

Absolute Maximum Ratings

Table 8. Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Units	Notes
T_{STG}	Storage Temperature	-55	25	+100	°C	Higher storage temperatures will reduce data retention time. Recommended storage temperature is +25°C ± 25°C. Extended duration storage temperatures above 65°C will degrade reliability.
T_A	Ambient Temperature with Power Applied	-40	–	+85	°C	
Vdd	Supply Voltage on Vdd Relative to Vss	-0.5	–	+6.0	V	
V_{IO}	DC Input Voltage	Vss- 0.5	–	Vdd + 0.5	V	
V_{IOZ}	DC Voltage Applied to Tri-state	Vss - 0.5	–	Vdd + 0.5	V	
I_{MIO}	Maximum Current into any Port Pin	-25	–	+50	mA	
I_{MAIO}	Maximum Current into any Port Pin Configured as Analog Driver	-50	–	+50	mA	
ESD	Electro Static Discharge Voltage	2000	–	–	V	Human Body Model ESD.
LU	Latch-up Current	–	–	200	mA	

DC General Purpose IO Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 11. DC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{PU}	Pull up Resistor	4	5.6	8	kΩ	
R_{PD}	Pull down Resistor	4	5.6	8	kΩ	
V_{OH}	High Output Level	Vdd - 1.0	–	–	V	IOH = 10 mA, Vdd = 4.75 to 5.25V (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5])).
V_{OL}	Low Output Level	–	–	0.75	V	IOL = 25 mA, Vdd = 4.75 to 5.25V (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5])).
V_{IL}	Input Low Level	–	–	0.8	V	Vdd = 3.0 to 5.25.
V_{IH}	Input High Level	2.1	–		V	Vdd = 3.0 to 5.25.
V_H	Input Hysterisis	–	60	–	mV	
I_{IL}	Input Leakage (Absolute Value)	–	1	–	nA	Gross tested to 1 μA.
C_{IN}	Capacitive Load on Pins as Input	–	3.5	10	pF	Package and pin dependent. Temp = 25°C.
C_{OUT}	Capacitive Load on Pins as Output	–	3.5	10	pF	Package and pin dependent. Temp = 25°C.

DC Operational Amplifier Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

The Operational Amplifier is a component of both the Analog Continuous Time PSoC blocks and the Analog Switched Cap PSoC blocks. The guaranteed specifications are measured in the Analog Continuous Time PSoC block. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 12. 5V DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input Offset Voltage (absolute value)					
	Power = Low, Opamp Bias = High	–	1.6	10	mV	
	Power = Medium, Opamp Bias = High	–	1.3	8	mV	
	Power = High, Opamp Bias = High	–	1.2	7.5	mV	
TCV_{OSOA}	Average Input Offset Voltage Drift	–	7.0	35.0	μV/°C	
I_{EBOA}	Input Leakage Current (Port 0 Analog Pins)	–	20	–	pA	Gross tested to 1 μA.
C_{INOA}	Input Capacitance (Port 0 Analog Pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25°C.
V_{CMOA}	Common Mode Voltage Range	0.0	–	Vdd	V	The common-mode input voltage range is measured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer.
	Common Mode Voltage Range (high power or high opamp bias)	0.5	–	Vdd - 0.5		
$CMRR_{OA}$	Common Mode Rejection Ratio		–	–	dB	Specification is applicable at high power. For all other bias modes (except high power, high opamp bias), minimum is 60 dB.
	Power = Low	60				
	Power = Medium	60				
	Power = High	60				
G_{OLOA}	Open Loop Gain		–	–	dB	Specification is applicable at high power. For all other bias modes (except high power, high opamp bias), minimum is 60 dB.
	Power = Low	60				
	Power = Medium	60				
	Power = High	80				
$V_{OHIGHOA}$	High Output Voltage Swing (internal signals)					
	Power = Low	Vdd - 0.2	–	–	V	
	Power = Medium	Vdd - 0.2	–	–	V	
	Power = High	Vdd - 0.5	–	–	V	

Table 12. 5V DC Operational Amplifier Specifications (continued)

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OLOWOA}	Low Output Voltage Swing (internal signals)					
	Power = Low	–	–	0.2	V	
	Power = Medium	–	–	0.2	V	
	Power = High	–	–	0.5	V	
I_{SOA}	Supply Current (including associated AGND buffer)					
	Power = Low, Opamp Bias = Low	–	150	200	µA	
	Power = Low, Opamp Bias = High	–	300	400	µA	
	Power = Medium, Opamp Bias = Low	–	600	800	µA	
	Power = Medium, Opamp Bias = High	–	1200	1600	µA	
	Power = High, Opamp Bias = Low	–	2400	3200	µA	
	Power = High, Opamp Bias = High	–	4600	6400	µA	
$PSRR_{OA}$	Supply Voltage Rejection Ratio	60	–	–	dB	Vss ≤ VIN ≤ (Vdd - 2.25) or (Vdd - 1.25V) ≤ VIN ≤ Vdd.

Table 13. 3.3V DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input Offset Voltage (absolute value)					
	Power = Low, Opamp Bias = High	–	1.65	10	mV	
	Power = Medium, Opamp Bias = High	–	1.32	8	mV	
	High Power is 5 Volts Only					
TCV_{OSOA}	Average Input Offset Voltage Drift	–	7.0	35.0	µV/°C	
I_{EBOA}	Input Leakage Current (Port 0 Analog Pins)	–	20	–	pA	Gross tested to 1 µA.
C_{INOA}	Input Capacitance (Port 0 Analog Pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25°C.
V_{CMOA}	Common Mode Voltage Range	0.2	–	Vdd - 0.2	V	The common-mode input voltage range is measured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer.
$CMRR_{OA}$	Common Mode Rejection Ratio		–	–	dB	Specification is applicable at high power. For all other bias modes (except high power, high opamp bias), minimum is 60 dB.
	Power = Low	50				
	Power = Medium	50				
	Power = High	50				
G_{OLOA}	Open Loop Gain		–	–	dB	Specification is applicable at high power. For all other bias modes (except high power, high opamp bias), minimum is 60 dB.
	Power = Low	60				
	Power = Medium	60				
	Power = High	80				
$V_{OHIGHOA}$	High Output Voltage Swing (internal signals)					
	Power = Low	Vdd - 0.2	–	–	V	
	Power = Medium	Vdd - 0.2	–	–	V	
	Power = High is 5V only	Vdd - 0.2	–	–	V	
V_{OLOWOA}	Low Output Voltage Swing (internal signals)					
	Power = Low	–	–	0.2	V	
	Power = Medium	–	–	0.2	V	
	Power = High	–	–	0.2	V	
I_{SOA}	Supply Current (including associated AGND buffer)					
	Power = Low, Opamp Bias = Low	–	150	200	µA	
	Power = Low, Opamp Bias = High	–	300	400	µA	
	Power = Medium, Opamp Bias = Low	–	600	800	µA	
	Power = Medium, Opamp Bias = High	–	1200	1600	µA	
	Power = High, Opamp Bias = Low	–	2400	3200	µA	
	Power = High, Opamp Bias = High	–	4600	6400	µA	
$PSRR_{OA}$	Supply Voltage Rejection Ratio	50	80	–	dB	Vss ≤ VIN ≤ (Vdd - 2.25) or (Vdd - 1.25V) ≤ VIN ≤ Vdd.

Table 16. 3.3V DC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOB}	Input Offset Voltage (Absolute Value)	–	3	12	mV	
TCV_{OSOB}	Average Input Offset Voltage Drift	–	+6	–	µV/°C	
V_{CMOB}	Common-Mode Input Voltage Range	0.5	-	Vdd - 1.0	V	
R_{OUTOB}	Output Resistance Power = Low Power = High	 – –	 1 1	 – –	 Ω Ω	
$V_{OHIGHOB}$	High Output Voltage Swing (Load = 1k ohms to Vdd/2) Power = Low Power = High	 0.5 x Vdd + 1.0 0.5 x Vdd + 1.0	 – –	 – –	 V V	
V_{OLOWOB}	Low Output Voltage Swing (Load = 1k ohms to Vdd/2) Power = Low Power = High	 – –	 – –	 0.5 x Vdd - 1.0 0.5 x Vdd - 1.0	 V V	
I_{SOB}	Supply Current Including Bias Cell (No Load) Power = Low Power = High	 –	 0.8 2.0	 2.0 4.3	 mA mA	
$PSRR_{OB}$	Supply Voltage Rejection Ratio	60	64	–	dB	

DC Switch Mode Pump Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 17. DC Switch Mode Pump (SMP) Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{PUMP} 5V	5V Output Voltage	4.75	5.0	5.25	V	Configuration of footnote.[a] Average, neglecting ripple. SMP trip voltage is set to 5.0V.
V_{PUMP} 3V	3V Output Voltage	3.00	3.25	3.60	V	Configuration of footnote.[a] Average, neglecting ripple. SMP trip voltage is set to 3.25V.
I_{PUMP}	Available Output Current V_{BAT} = 1.5V, V_{PUMP} = 3.25V V_{BAT} = 1.8V, V_{PUMP} = 5.0V	 8 5	 – –	 – –	 mA mA	Configuration of footnote.[a] SMP trip voltage is set to 3.25V. SMP trip voltage is set to 5.0V.
V_{BAT}5V	Input Voltage Range from Battery	1.8	–	5.0	V	Configuration of footnote.[a] SMP trip voltage is set to 5.0V.
V_{BAT}3V	Input Voltage Range from Battery	1.0	–	3.3	V	Configuration of footnote.[a] SMP trip voltage is set to 3.25V.
$V_{BATSTART}$	Minimum Input Voltage from Battery to Start Pump	1.1	–	–	V	Configuration of footnote.[a]
ΔV_{PUMP_Line}	Line Regulation (over V_{BAT} range)	–	5	–	$\%V_O$	Configuration of footnote.[a] V_O is the "Vdd Value for PUMP Trip" specified by the VM[2:0] setting in the DC POR and LVD Specification, Table 21 on page 22.
ΔV_{PUMP_Load}	Load Regulation	–	5	–	$\%V_O$	Configuration of footnote.[a] V_O is the "Vdd Value for PUMP Trip" specified by the VM[2:0] setting in the DC POR and LVD Specification, Table 21 on page 22.
ΔV_{PUMP_Ripple}	Output Voltage Ripple (depends on capacitor/load)	–	100	–	mVpp	Configuration of footnote.[a] Load is 5mA.
E_3	Efficiency	35	50	–	%	Configuration of footnote.[a] Load is 5 mA. SMP trip voltage is set to 3.25V.
F_{PUMP}	Switching Frequency	–	1.3	–	MHz	
DC_{PUMP}	Switching Duty Cycle	–	50	–	%	

a. L_1 = 2 µH inductor, C_1 = 10 µF capacitor, D_1 = Schottky diode.

Table 19. 3.3V DC Analog Reference Specifications

Symbol	Description	Min	Typ	Max	Units
BG	Bandgap Voltage Reference	1.28	1.30	1.32	V
–	AGND = Vdd/2[a]	Vdd/2 - 0.027	Vdd/2	Vdd/2 + 0.005	V
–	AGND = 2 x BandGap[a]	Not Allowed			
–	AGND = P2[4] (P2[4] = Vdd/2)	P2[4] - 0.008	P2[4]	P2[4] + 0.009	V
–	AGND = BandGap[a]	BG - 0.009	BG	BG + 0.009	V
–	AGND = 1.6 x BandGap[a]	1.6 x BG - 0.018	1.6 x BG	1.6 x BG + 0.018	V
–	AGND Block to Block Variation (AGND = Vdd/2)[a]	-0.034	0.000	0.034	mV
–	RefHi = Vdd/2 + BandGap	Not Allowed			
–	RefHi = 3 x BandGap	Not Allowed			
–	RefHi = 2 x BandGap + P2[6] (P2[6] = 0.5V)	Not Allowed			
–	RefHi = P2[4] + BandGap (P2[4] = Vdd/2)	Not Allowed			
–	RefHi = P2[4] + P2[6] (P2[4] = Vdd/2, P2[6] = 0.5V)	P2[4] + P2[6] - 0.06	P2[4] + P2[6] - 0.01	P2[4] + P2[6] + 0.057	V
–	RefHi = 3.2 x BandGap	Not Allowed			
–	RefLo = Vdd/2 - BandGap	Not Allowed			
–	RefLo = BandGap	Not Allowed			
–	RefLo = 2 x BandGap - P2[6] (P2[6] = 0.5V)	Not Allowed			
–	RefLo = P2[4] – BandGap (P2[4] = Vdd/2)	Not Allowed			
–	RefLo = P2[4]-P2[6] (P2[4] = Vdd/2, P2[6] = 0.5V)	P2[4] - P2[6] - 0.048	P2[4] - P2[6] + 0.01	P2[4] - P2[6] + 0.048	V

a. AGND tolerance includes the offsets of the local buffer in the PSoC block.

Note See Application Note AN2012 “Adjusting PSoC Microcontroller Trims for Dual Voltage-Range Operation” for information on trimming for operation at 3.3V.

DC Analog PSoC Block Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 20. DC Analog PSoC Block Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{CT}	Resistor Unit Value (Continuous Time)	–	12.2	–	kΩ	
C_{SC}	Capacitor Unit Value (Switch Cap)	–	80	–	fF	

DC POR and LVD Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Note The bits PORLEV and VM in the table below refer to bits in the VLT_CR register.

Table 21. DC POR and LVD Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
	Vdd Value for PPOR Trip (positive ramp)					Vdd must be greater than or equal to 2.5V during startup, reset from the XRES pin, or reset from Watchdog.
V_{PPOR0R}	PORLEV[1:0] = 00b		2.91		V	
V_{PPOR1R}	PORLEV[1:0] = 01b	–	4.39	–	V	
V_{PPOR2R}	PORLEV[1:0] = 10b		4.55		V	
	Vdd Value for PPOR Trip (negative ramp)					
V_{PPOR0}	PORLEV[1:0] = 00b		2.82		V	
V_{PPOR1}	PORLEV[1:0] = 01b	–	4.39	–	V	
V_{PPOR2}	PORLEV[1:0] = 10b		4.55		V	
	PPOR Hysteresis					
V_{PH0}	PORLEV[1:0] = 00b	–	92	–	mV	
V_{PH1}	PORLEV[1:0] = 01b	–	0	–	mV	
V_{PH2}	PORLEV[1:0] = 10b	–	0	–	mV	
	Vdd Value for LVD Trip					
V_{LVD0}	VM[2:0] = 000b	2.86	2.92	2.98[a]	V	
V_{LVD1}	VM[2:0] = 001b	2.96	3.02	3.08	V	
V_{LVD2}	VM[2:0] = 010b	3.07	3.13	3.20	V	
V_{LVD3}	VM[2:0] = 011b	3.92	4.00	4.08	V	
V_{LVD4}	VM[2:0] = 100b	4.39	4.48	4.57	V	
V_{LVD5}	VM[2:0] = 101b	4.55	4.64	4.74[b]	V	
V_{LVD6}	VM[2:0] = 110b	4.63	4.73	4.82	V	
V_{LVD7}	VM[2:0] = 111b	4.72	4.81	4.91	V	
	Vdd Value for PUMP Trip					
V_{PUMP0}	VM[2:0] = 000b	2.96	3.02	3.08	V	
V_{PUMP1}	VM[2:0] = 001b	3.03	3.10	3.16	V	
V_{PUMP2}	VM[2:0] = 010b	3.18	3.25	3.32	V	
V_{PUMP3}	VM[2:0] = 011b	4.11	4.19	4.28	V	
V_{PUMP4}	VM[2:0] = 100b	4.55	4.64	4.74	V	
V_{PUMP5}	VM[2:0] = 101b	4.63	4.73	4.82	V	
V_{PUMP6}	VM[2:0] = 110b	4.72	4.82	4.91	V	
V_{PUMP7}	VM[2:0] = 111b	4.90	5.00	5.10	V	

a. Always greater than 50 mV above PPOR (PORLEV = 00) for falling supply.
b. Always greater than 50 mV above PPOR (PORLEV = 10) for falling supply.

DC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 22. DC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
I_{DDP}	Supply Current During Programming or Verify	–	5	25	mA	
V_{ILP}	Input Low Voltage During Programming or Verify	–	–	0.8	V	
V_{IHP}	Input High Voltage During Programming or Verify	2.2	–	–	V	
I_{ILP}	Input Current when Applying Vilp to P1[0] or P1[1] During Programming or Verify	–	–	0.2	mA	Driving internal pull-down resistor.
I_{IHP}	Input Current when Applying Vihp to P1[0] or P1[1] During Programming or Verify	–	–	1.5	mA	Driving internal pull-down resistor.
V_{OLV}	Output Low Voltage During Programming or Verify	–	–	Vss + 0.75	V	
V_{OHV}	Output High Voltage During Programming or Verify	Vdd - 1.0	–	Vdd	V	
$Flash_{ENPB}$	Flash Endurance (per block)	50,000	–	–	–	Erase/write cycles per block.
$Flash_{ENT}$	Flash Endurance (total)[a]	1,800,000	–	–	–	Erase/write cycles.
$Flash_{DR}$	Flash Data Retention	10	–	–	Years	

a. A maximum of 36 x 50,000 block endurance cycles is allowed. This may be balanced between operations on 36x1 blocks of 50,000 maximum cycles each, 36x2 blocks of 25,000 maximum cycles each, or 36x4 blocks of 12,500 maximum cycles each (to limit the total number of cycles to 36x50,000 and that no single block ever sees more than 50,000 cycles).

For the full industrial range, the user must employ a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. Refer to the Flash APIs Application Note AN2015 at http://www.cypress.com under Application Notes for more information.

Figure 10. PLL Lock for Low Gain Setting Timing Diagram

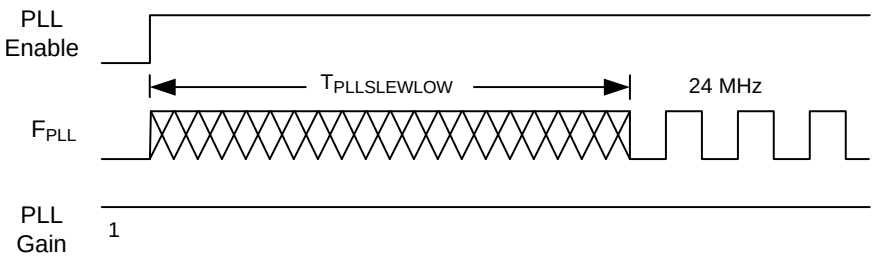


Figure 11. External Crystal Oscillator Startup Timing Diagram

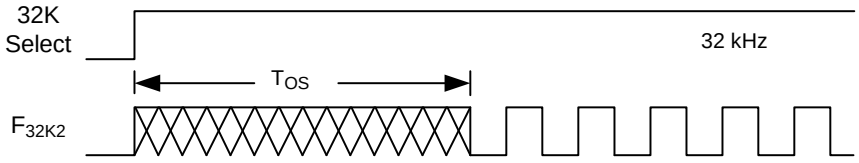


Figure 12. 24 MHz Period Jitter (IMO) Timing Diagram

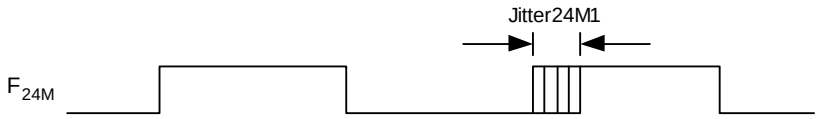
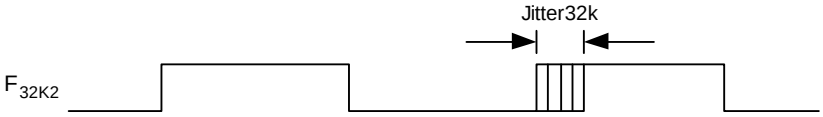


Figure 13. 32 kHz Period Jitter (ECO) Timing Diagram



AC General Purpose IO Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 24. AC GPIO Specifications

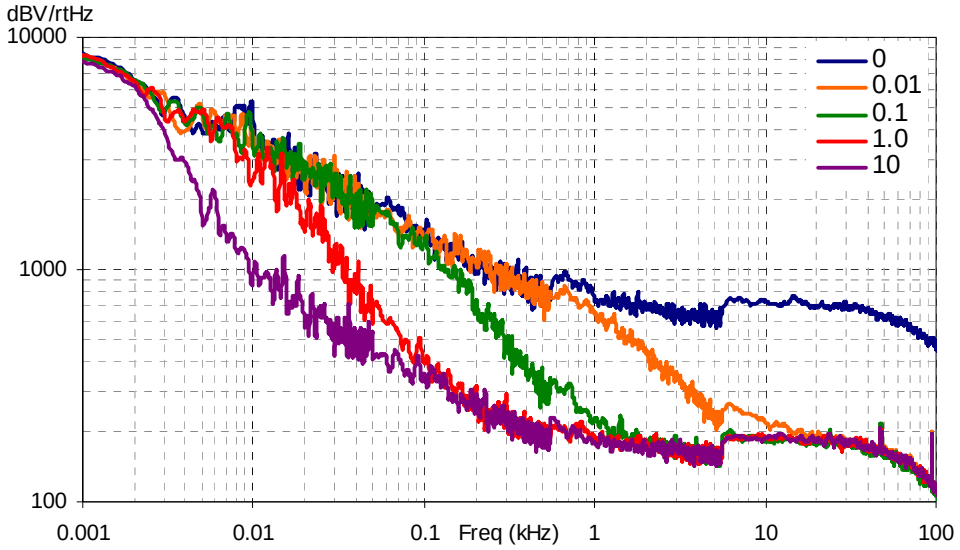
Symbol	Description	Min	Typ	Max	Units	Notes
F_{GPIO}	GPIO Operating Frequency	0	–	12	MHz	Normal Strong Mode
TRiseF	Rise Time, Normal Strong Mode, Cload = 50 pF	3	–	18	ns	Vdd = 4.5 to 5.25V, 10% - 90%
TFallF	Fall Time, Normal Strong Mode, Cload = 50 pF	2	–	18	ns	Vdd = 4.5 to 5.25V, 10% - 90%
TRiseS	Rise Time, Slow Strong Mode, Cload = 50 pF	10	27	–	ns	Vdd = 3 to 5.25V, 10% - 90%
TFallS	Fall Time, Slow Strong Mode, Cload = 50 pF	10	22	–	ns	Vdd = 3 to 5.25V, 10% - 90%

Table 26. 3.3V AC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{ROA}	Rising Settling Time from 80% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain)					
	Power = Low, Opamp Bias = Low	–	–	3.92	µs	
	Power = Low, Opamp Bias = High	–	–	0.72	µs	
T_{SOA}	Falling Settling Time from 20% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain)					
	Power = Low, Opamp Bias = Low	–	–	5.41	µs	
	Power = Medium, Opamp Bias = High	–	–	0.72	µs	
SR_{ROA}	Rising Slew Rate (20% to 80%)(10 pF load, Unity Gain)					
	Power = Low, Opamp Bias = Low	0.31	–	–	V/µs	
	Power = Medium, Opamp Bias = High	2.7	–	–	V/µs	
SR_{FOA}	Falling Slew Rate (20% to 80%)(10 pF load, Unity Gain)					
	Power = Low, Opamp Bias = Low	0.24	–	–	V/µs	
	Power = Medium, Opamp Bias = High	1.8	–	–	V/µs	
BW_{OA}	Gain Bandwidth Product					
	Power = Low, Opamp Bias = Low	0.67	–	–	MHz	
	Power = Medium, Opamp Bias = High	2.8	–	–	MHz	
E_{NOA}	Noise at 1 kHz (Power = Medium, Opamp Bias = High)	–	100	–	nV/rt-Hz	

When bypassed by a capacitor on P2[4], the noise of the analog ground signal distributed to each block is reduced by a factor of up to 5 (14 dB). This is at frequencies above the corner frequency defined by the on-chip 8.1k resistance and the external capacitor.

Figure 15. Typical AGND Noise with P2[4] Bypass



AC Digital Block Specifications

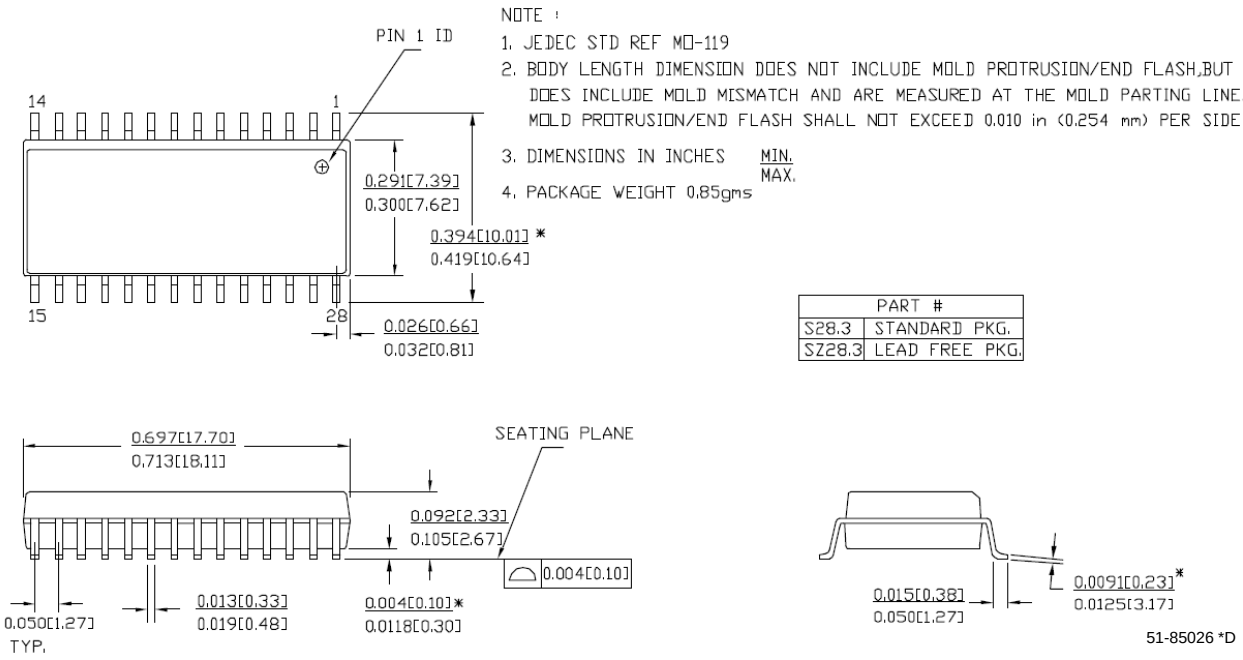
The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 28. AC Digital Block Specifications

Function	Description	Min	Typ	Max	Units	Notes
All Functions	Maximum Block Clocking Frequency (> 4.75V)			49.2		4.75V < Vdd < 5.25V.
	Maximum Block Clocking Frequency (< 4.75V)			24.6		3.0V < Vdd < 4.75V.
Timer	Capture Pulse Width	50[a]	–	–	ns	
	Maximum Frequency, No Capture	–	–	49.2	MHz	4.75V < Vdd < 5.25V.
	Maximum Frequency, With Capture	–	–	24.6	MHz	
Counter	Enable Pulse Width	50[a]	–	–	ns	
	Maximum Frequency, No Enable Input	–	–	49.2	MHz	4.75V < Vdd < 5.25V.
	Maximum Frequency, Enable Input	–	–	24.6	MHz	
Dead Band	Kill Pulse Width:					
	Asynchronous Restart Mode	20	–	–	ns	
	Synchronous Restart Mode	50[a]	–	–	ns	
	Disable Mode	50[a]	–	–	ns	
	Maximum Frequency	–	–	49.2	MHz	4.75V < Vdd < 5.25V.
CRCPRS (PRS Mode)	Maximum Input Clock Frequency	–	–	49.2	MHz	4.75V < Vdd < 5.25V.
CRCPRS (CRC Mode)	Maximum Input Clock Frequency	–	–	24.6	MHz	
SPIM	Maximum Input Clock Frequency	–	–	8.2	MHz	Maximum data rate at 4.1 MHz due to 2 x over clocking.
SPIS	Maximum Input Clock Frequency	–	–	4.1	ns	
	Width of SS_ Negated Between Transmissions	50[a]	–	–	ns	
Transmitter	Maximum Input Clock Frequency	–	–	24.6	MHz	Maximum data rate at 3.08 MHz due to 8 x over clocking.
	Maximum Input Clock Frequency with Vdd ≥ 4.75V, 2 Stop Bits	–	–	49.2	MHz	Maximum data rate at 6.15 MHz due to 8 x over clocking.
Receiver	Maximum Input Clock Frequency	–	–	24.6	MHz	Maximum data rate at 3.08 MHz due to 8 x over clocking.
	Maximum Input Clock Frequency with Vdd ≥ 4.75V, 2 Stop Bits	–	–	49.2	MHz	Maximum data rate at 6.15 MHz due to 8 x over clocking.

a. 50 ns minimum input pulse width is based on the input synchronizers running at 24 MHz (42 ns nominal period).

Figure 20. 28-Lead (210-Mil) SSOP



Important Note For information on the preferred dimensions for mounting QFN packages, see the following Application Note at http://www.amkor.com/products/notes_papers/MLFAppNote.pdf.

Important Note Pinned vias for thermal conduction are not required for the low-power device.

Thermal Impedances

Table 35. Thermal Impedances per Package

Package	Typical θ_{JA} *
48 SSOP	69 °C/W
48 QFN**	18 °C/W
28 SSOP	95 °C/W

* $T_J = T_A + POWER \times \theta_{JA}$

** To achieve the thermal impedance specified for the QFN package, the center thermal pad should be soldered to the PCB ground plane.

Capacitance on Crystal Pins

Table 36. Typical Package Capacitance on Crystal Pins

Package	Package Capacitance
48 SSOP	3.3 pF
48 QFN	2.3 pF
28 SSOP	2.8 pF

Solder Reflow Peak Temperature

Following is the minimum solder reflow peak temperature to achieve good solderability.

Table 37. Solder Reflow Peak Temperature

Package	Minimum Peak Temperature*	Maximum Peak Temperature
48 SSOP	220°C	260°C
48 QFN	240°C	260°C
28 SSOP	240°C	260°C

*Higher temperatures may be required based on the solder melting point. Typical temperatures for solder are 220 ± 5°C with Sn-Pb or 245 ± 5°C with Sn-Ag-Cu paste. Refer to the solder manufacturer specifications.

Development Tool Selection

This section presents the development tools available for all current PSoC based devices including the CY8CLED08 EZ-Color family.

Software Tools

PSoC Express™

As the newest addition to the PSoC development software suite, PSoC Express is the first visual embedded system design tool that allows a user to create an entire project and generate a schematic, BOM, and data sheet without writing a single line of code. Users work directly with application objects such as LEDs, switches, sensors, and fans. PSoC Express is available free of charge at http://www.cypress.com/psocexpress.

PSoC Designer™

Utilized by thousands of PSoC developers, this robust software has been facilitating PSoC designs for half a decade. PSoC Designer is available free of charge at http://www.cypress.com under DESIGN RESOURCES >> Software and Drivers.

PSoC Programmer

Flexible enough to be used on the bench in development, yet suitable for factory programming, PSoC Programmer works either as a standalone programming application or it can operate directly from PSoC Designer or PSoC Express. PSoC Programmer software is compatible with both PSoC ICE-Cube In-Circuit Emulator and PSoC MiniProg. PSoC programmer is available free ofcharge at http://www.cypress.com/psocprogrammer.

CY3202-C iMAGEcraft C Compiler

CY3202 is the optional upgrade to PSoC Designer that enables the iMAGEcraft C compiler. It can be purchased from the Cypress Online Store. At http://www.cypress.com, click the Online Store shopping cart icon at the bottom of the web page, and click *PSoC (Programmable System-on-Chip)* to view a current list of available items.

Hardware Tools

In-Circuit Emulator

A low cost, high functionality ICE (In-Circuit Emulator) is available for development support. This hardware has the capability to program single devices.

The emulator consists of a base unit that connects to the PC by way of the USB port. The base unit is universal and will operate with all PSoC based devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full speed (24 MHz) operation.

I2C to USB Bridge

The I2C to USB Bridge is a quick and easy link from any design or application's I2C bus to a PC via USB for design testing, debugging and communication.