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Embedded - Microcontrollers - Application Specific represents a category of microcontrollers designed with unique features and capabilities tailored to specific application needs. Unlike general-purpose microcontrollers, application-specific microcontrollers are optimized for particular tasks, offering enhanced performance, efficiency, and functionality to meet the demands of specialized applications.

What Are Embedded - Microcontrollers - Application Specific?

Application specific microcontrollers are engineered to

Details

Product Status	Obsolete
Applications	HB LED Controller
Core Processor	M8C
Program Memory Type	FLASH (16KB)
Controller Series	CY8CLED
RAM Size	256 x 8
Interface	I ² C, SPI, UART/USART
Number of I/O	44
Voltage - Supply	3V ~ 5.25V
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8cled08-48lfxit

The digital blocks can be connected to any GPIO through a series of global buses that can route any signal to any pin. The buses also allow for signal multiplexing and for performing logic operations. This configurability frees your designs from the constraints of a fixed peripheral controller.

Digital blocks are provided in rows of four, where the number of blocks varies by EZ-Color device family. This allows you the optimum choice of system resources for your application. Family resources are shown in the table titled EZ-Color Device Characteristics.

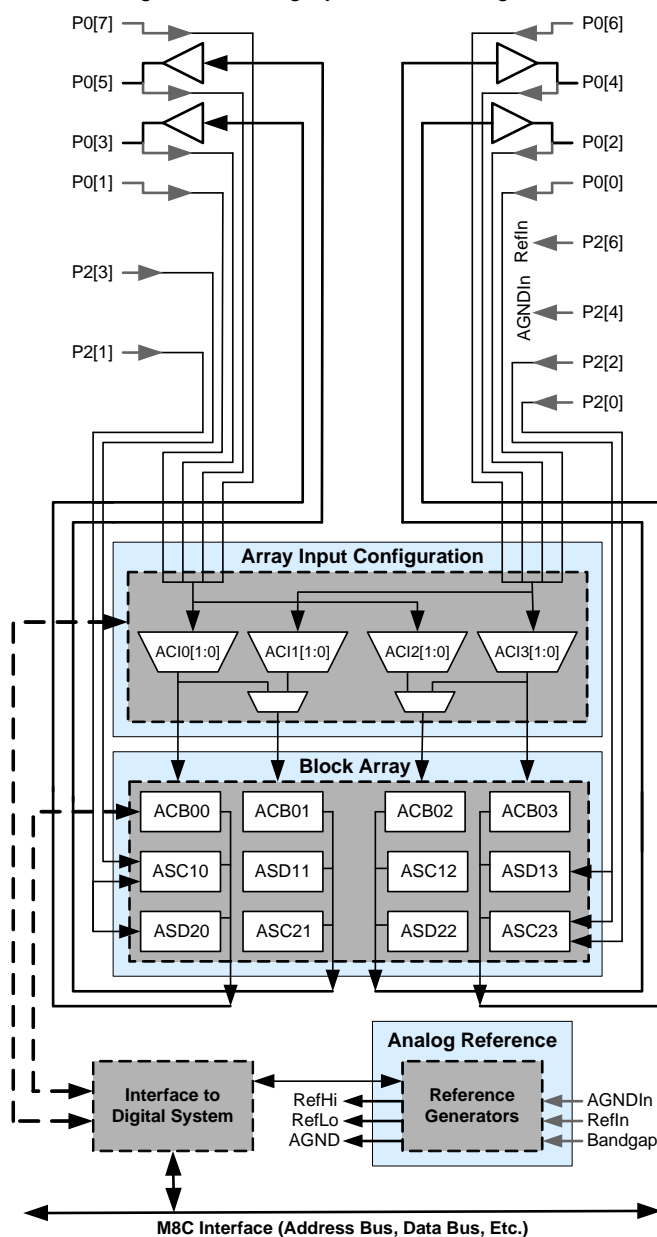
The Analog System

The Analog System is composed of 12 configurable blocks, each comprised of an opamp circuit allowing the creation of complex analog signal flows. Analog peripherals are very flexible and can be customized to support specific application requirements. Some of the more common EZ-Color analog functions (most available as user modules) are listed below.

- Analog-to-digital converters (up to 4, with 6- to 14-bit resolution, selectable as Incremental, Delta Sigma, and SAR)
- Filters (2, 4, 6, and 8 pole band-pass, low-pass, and notch)
- Amplifiers (up to 4, with selectable gain to 48x)
- Instrumentation amplifiers (up to 2, with selectable gain to 93x)
- Comparators (up to 4, with 16 selectable thresholds)
- DACs (up to 4, with 6- to 9-bit resolution)
- Multiplying DACs (up to 4, with 6- to 9-bit resolution)
- High current output drivers (four with 30 mA drive as a Core Resource)
- 1.3V reference (as a System Resource)
- DTMF Dialer
- Modulators
- Correlators
- Peak detectors
- Many other topologies possible

Analog blocks are provided in columns of three, which includes one CT (Continuous Time) and two SC (Switched Capacitor) blocks, as shown in the figure below.

Figure 2. Analog System Block Diagram



Getting Started

The quickest path to understanding the EZ-Color silicon is by reading this data sheet and using the PSoC Express Integrated Development Environment (IDE). This data sheet is an overview of the EZ-Color integrated circuit and presents specific pin, register, and electrical specifications.

For up-to-date Ordering, Packaging, and Electrical Specification information, reference the latest device data sheets on the web at <http://www.cypress.com/ez-color>.

Development Kits

Development Kits are available from the following distributors: Digi-Key, Avnet, Arrow, and Future. The Cypress Online Store contains development kits, C compilers, and all accessories for PSoC development. Go to the Cypress Online Store web site at <http://www.cypress.com>, click the Online Store shopping cart icon at the bottom of the web page, and click **EZ-Color** to view a current list of available items.

Technical Training Modules

Free PSoC technical training modules are available for users new to PSoC. Training modules cover designing, debugging, advanced analog and CapSense. Go to <http://www.cypress.com/techtrain>.

Consultants

Certified PSoC Consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC Consultant go to <http://www.cypress.com>, click on Design Support located on the left side of the web page, and select CYPros Consultants.

Technical Support

PSoC application engineers take pride in fast and accurate response. They can be reached with a 4-hour guaranteed response at <http://www.cypress.com/support/login.cfm>.

Application Notes

A long list of application notes will assist you in every aspect of your design effort. To view the PSoC application notes, go to the <http://www.cypress.com> web site and select Application Notes under the Design Resources list located in the center of the web page. Application Notes are sorted by date by default.

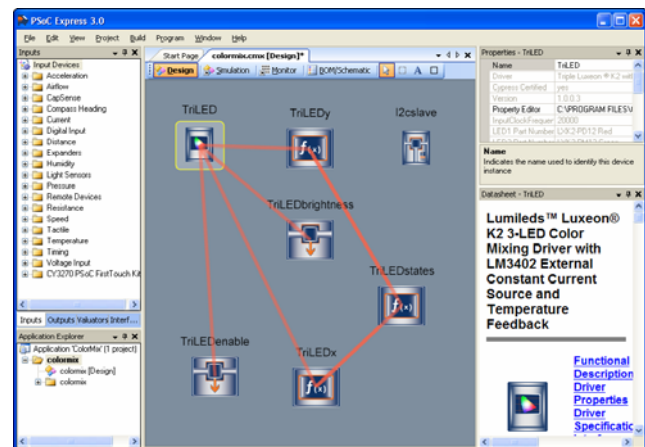
Development Tools

PSoC Express is a high-level design tool for creating embedded systems with devices using Cypress's PSoC Mixed-Signal technology. With PSoC Express you create a complete embedded solution including all necessary on-chip peripherals, block configuration, interrupt handling and application software without writing a single line of assembly or C code.

PSoC Express solves design problems the way you think about the system:

- Select input and output devices based upon system requirements.
- Add a communications interface and define its interface to system (using registers).
- Define when and how an output device changes state based upon any and all other system devices.
- Based upon the design, automatically select an EZ-Color Controller that matches system requirements.

Figure 3. PSoC Express



PSoC Express Subsystems

Express Editor

The Express Editor allows you to create designs visually by dragging and dropping inputs, outputs, communication interfaces, and other design elements, and then describing the logic that controls them.

Project Manager

The Project Manager allows you to work with your applications and projects in PSoC Express. A PSoC Express application is a top level container for projects and their associated files. Each project contains a design that uses a single PSoC device. An application can contain multiple projects so if you are creating an application that uses multiple PSoC devices you can keep all of the projects together in a single application.

Most of the files associated with a project are automatically generated by PSoC Express during the build process, but you can make changes directly to the custom.c and custom.h files

and also add your own custom code to the project in the Project Manager.

Application Editor

The Application Editor allows you to edit custom.c and custom.h as well as any C or assembly language source code that you add to your project. With PSoC Express you can create application software without writing a single line of assembly or C code, but you have a full featured application editor at your finger tips if you want it.

Build Manager

The Build Manager gives you the ability to build the application software, assign pins, and generate the data sheet, schematic, and BOM for your project.

Board Monitor

The Board Monitor is a debugging tool designed to be used while attached to a prototype board through a communication interface that allows you to monitor changes in the various design elements in real time.

The default communication for the board monitor is I²C. It uses the CY3240-I2USB I²C to USB Bridge Debugging/Communication Kit.

Tuners

A Tuner is a visual interface for the Board Monitor that allows you to view the performance of the HB LED drivers on your test board while your program is running, and manually override values and see the results.

Document Conventions

Units of Measure

A units of measure table is located in the Electrical Specifications section. [Table 7 on page 14](#) lists all the abbreviations used to measure the devices.

Numeric Naming

Hexidecimal numbers are represented with all letters in uppercase with an appended lowercase 'h' (for example, '14h' or '3Ah'). Hexidecimal numbers may also be represented by a '0x' prefix, the C coding convention. Binary numbers have an appended lowercase 'b' (e.g., 01010100b or '01000011b'). Numbers not indicated by an 'h' or 'b' are decimal.

Acronyms Used

The following table lists the acronyms that are used in this document.

Acronym	Description
AC	alternating current
ADC	analog-to-digital converter
API	application programming interface
CPU	central processing unit
CT	continuous time
DAC	digital-to-analog converter
DC	direct current
ECO	external crystal oscillator
EEPROM	electrically erasable programmable read-only memory
FSR	full scale range
GPIO	general purpose IO
GUI	graphical user interface
HBM	human body model
ICE	in-circuit emulator
ILO	internal low speed oscillator
IMO	internal main oscillator
IO	input/output
IPOR	imprecise power on reset
LSb	least-significant bit
LVD	low voltage detect
MSb	most-significant bit
PC	program counter
PLL	phase-locked loop
POR	power on reset
PPOR	precision power on reset
PSoC®	Programmable System-on-Chip™
PWM	pulse width modulator
SC	switched capacitor
SLIMO	slow IMO
SMP	switch mode pump
SRAM	static random access memory

Pin Information

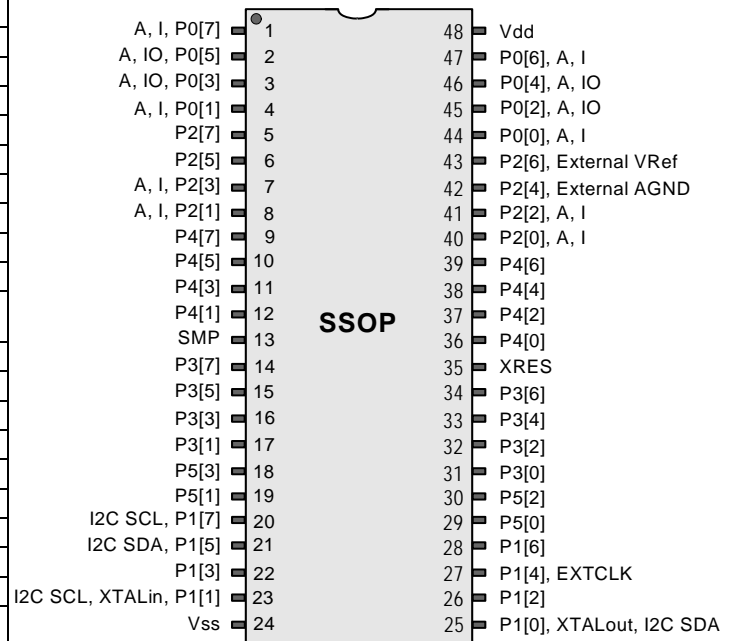
Pinouts

48-Pin Part Pinout SSOP

Table 2. 48-Pin Part Pinout (SSOP)

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	IO	I	P0[7]	Analog column mux input.
2	IO	IO	P0[5]	Analog column mux input and column output.
3	IO	IO	P0[3]	Analog column mux input and column output.
4	IO	I	P0[1]	Analog column mux input.
5	IO		P2[7]	
6	IO		P2[5]	
7	IO	I	P2[3]	Direct switched capacitor block input.
8	IO	I	P2[1]	Direct switched capacitor block input.
9	IO		P4[7]	
10	IO		P4[5]	
11	IO		P4[3]	
12	IO		P4[1]	
13	Power		SMP	Switch Mode Pump (SMP) connection to external components required.
14	IO		P3[7]	
15	IO		P3[5]	
16	IO		P3[3]	
17	IO		P3[1]	
18	IO		P5[3]	
19	IO		P5[1]	
20	IO		P1[7]	I2C Serial Clock (SCL).
21	IO		P1[5]	I2C Serial Data (SDA).
22	IO		P1[3]	
23	IO		P1[1]	Crystal Input (XTALin), I2C Serial Clock (SCL), ISSP SCLK*.
24	Power		Vss	Ground connection.
25	IO		P1[0]	Crystal Output (XTALout), I2C Serial Data (SDA), ISSP SDA.*
26	IO		P1[2]	
27	IO		P1[4]	Optional External Clock Input (EXTCLK).
28	IO		P1[6]	
29	IO		P5[0]	
30	IO		P5[2]	
31	IO		P3[0]	
32	IO		P3[2]	
33	IO		P3[4]	
34	IO		P3[6]	
35	Input		XRES	Active high external reset with internal pull down.
36	IO		P4[0]	
37	IO		P4[2]	
38	IO		P4[4]	

Figure 4. 48-Pin Device



LEGEND: A = Analog, I = Input, and O = Output.

* These are the ISSP pins, which are not High Z at POR (Power On Reset).

Register Reference

This chapter lists the registers of the CY8CLED08 EZ-Color device.

Register Conventions

The register conventions specific to this section are listed in the following table. Register Mapping Tables

Convention	Description
R	Read register or bit(s)
W	Write register or bit(s)
L	Logical register or bit(s)
C	Clearable register or bit(s)
#	Access is bit specific

Register Mapping Tables

The device has a total register address space of 512 bytes. The register space is referred to as IO space and is divided into two banks. The XO1 bit in the Flag register (CPU_F) determines which bank the user is currently in. When the XO1 bit is set the user is in Bank 1.

Note In the following register mapping tables, blank fields are reserved and should not be accessed.

Table 5. Register Map Bank 0 Table: User Space

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
PRT0DR	00	RW		40		ASC10CR0	80	RW		C0	
PRT0IE	01	RW		41		ASC10CR1	81	RW		C1	
PRT0GS	02	RW		42		ASC10CR2	82	RW		C2	
PRT0DM2	03	RW		43		ASC10CR3	83	RW		C3	
PRT1DR	04	RW		44		ASD11CR0	84	RW		C4	
PRT1IE	05	RW		45		ASD11CR1	85	RW		C5	
PRT1GS	06	RW		46		ASD11CR2	86	RW		C6	
PRT1DM2	07	RW		47		ASD11CR3	87	RW		C7	
PRT2DR	08	RW		48		ASC12CR0	88	RW		C8	
PRT2IE	09	RW		49		ASC12CR1	89	RW		C9	
PRT2GS	0A	RW		4A		ASC12CR2	8A	RW		CA	
PRT2DM2	0B	RW		4B		ASC12CR3	8B	RW		CB	
PRT3DR	0C	RW		4C		ASD13CR0	8C	RW		CC	
PRT3IE	0D	RW		4D		ASD13CR1	8D	RW		CD	
PRT3GS	0E	RW		4E		ASD13CR2	8E	RW		CE	
PRT3DM2	0F	RW		4F		ASD13CR3	8F	RW		CF	
PRT4DR	10	RW		50		ASD20CR0	90	RW		D0	
PRT4IE	11	RW		51		ASD20CR1	91	RW		D1	
PRT4GS	12	RW		52		ASD20CR2	92	RW		D2	
PRT4DM2	13	RW		53		ASD20CR3	93	RW		D3	
PRT5DR	14	RW		54		ASC21CR0	94	RW		D4	
PRT5IE	15	RW		55		ASC21CR1	95	RW		D5	
PRT5GS	16	RW		56		ASC21CR2	96	RW	I2C_CFG	D6	RW
PRT5DM2	17	RW		57		ASC21CR3	97	RW	I2C_SCR	D7	#
	18			58		ASD22CR0	98	RW	I2C_DR	D8	RW
	19			59		ASD22CR1	99	RW	I2C_MSCR	D9	#
	1A			5A		ASD22CR2	9A	RW	INT_CLR0	DA	RW
	1B			5B		ASD22CR3	9B	RW	INT_CLR1	DB	RW
	1C			5C		ASC23CR0	9C	RW		DC	
	1D			5D		ASC23CR1	9D	RW	INT_CLR3	DD	RW
	1E			5E		ASC23CR2	9E	RW	INT_MSK3	DE	RW
	1F			5F		ASC23CR3	9F	RW		DF	
DBB00DR0	20	#	AMX_IN	60	RW		A0		INT_MSK0	E0	RW
DBB00DR1	21	W		61			A1		INT_MSK1	E1	RW
DBB00DR2	22	RW		62			A2		INT_VC	E2	RC
DBB00CR0	23	#	ARF_CR	63	RW		A3		RES_WDT	E3	W
DBB01DR0	24	#	CMP_CR0	64	#		A4		DEC_DH	E4	RC
DBB01DR1	25	W	ASY_CR	65	#		A5		DEC_DL	E5	RC
DBB01DR2	26	RW	CMP_CR1	66	RW		A6		DEC_CR0	E6	RW
DBB01CR0	27	#		67			A7		DEC_CR1	E7	RW
DCB02DR0	28	#		68			A8		MUL_X	E8	W
DCB02DR1	29	W		69			A9		MUL_Y	E9	W
DCB02DR2	2A	RW		6A			AA		MUL_DH	EA	R
DCB02CR0	2B	#		6B			AB		MUL_DL	EB	R
DCB03DR0	2C	#		6C			AC		ACC_DR1	EC	RW
DCB03DR1	2D	W		6D			AD		ACC_DR0	ED	RW
DCB03DR2	2E	RW		6E			AE		ACC_DR3	EE	RW
DCB03CR0	2F	#		6F			AF		ACC_DR2	EF	RW
DBB10DR0	30	#	ACB00CR3	70	RW	RDI0RI	B0	RW		F0	
DBB10DR1	31	W	ACB00CR0	71	RW	RDI0SYN	B1	RW		F1	
DBB10DR2	32	RW	ACB00CR1	72	RW	RDI0IS	B2	RW		F2	
DBB10CR0	33	#	ACB00CR2	73	RW	RDI0LT0	B3	RW		F3	
DBB11DR0	34	#	ACB01CR3	74	RW	RDI0LT1	B4	RW		F4	
DBB11DR1	35	W	ACB01CR0	75	RW	RDI0RO0	B5	RW		F5	
DBB11DR2	36	RW	ACB01CR1	76	RW	RDI0RO1	B6	RW		F6	
DBB11CR0	37	#	ACB01CR2	77	RW		B7		CPU_F	F7	RL
DCB12DR0	38	#	ACB02CR3	78	RW	RDI1RI	B8	RW		F8	
DCB12DR1	39	W	ACB02CR0	79	RW	RDI1SYN	B9	RW		F9	
DCB12DR2	3A	RW	ACB02CR1	7A	RW	RDI1IS	BA	RW		FA	
DCB12CR0	3B	#	ACB02CR2	7B	RW	RDI1LT0	BB	RW		FB	
DCB13DR0	3C	#	ACB03CR3	7C	RW	RDI1LT1	BC	RW		FC	
DCB13DR1	3D	W	ACB03CR0	7D	RW	RDI1RO0	BD	RW		FD	
DCB13DR2	3E	RW	ACB03CR1	7E	RW	RDI1RO1	BE	RW	CPU_SCR1	FE	#
DCB13CR0	3F	#	ACB03CR2	7F	RW		BF		CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed.

Access is bit specific.

Table 6. Register Map Bank 1 Table: Configuration Space

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	00	RW		40		ASC10CR0	80	RW		C0	
PRT0DM1	01	RW		41		ASC10CR1	81	RW		C1	
PRT0IC0	02	RW		42		ASC10CR2	82	RW		C2	
PRT0IC1	03	RW		43		ASC10CR3	83	RW		C3	
PRT1DM0	04	RW		44		ASD11CR0	84	RW		C4	
PRT1DM1	05	RW		45		ASD11CR1	85	RW		C5	
PRT1IC0	06	RW		46		ASD11CR2	86	RW		C6	
PRT1IC1	07	RW		47		ASD11CR3	87	RW		C7	
PRT2DM0	08	RW		48		ASC12CR0	88	RW		C8	
PRT2DM1	09	RW		49		ASC12CR1	89	RW		C9	
PRT2IC0	0A	RW		4A		ASC12CR2	8A	RW		CA	
PRT2IC1	0B	RW		4B		ASC12CR3	8B	RW		CB	
PRT3DM0	0C	RW		4C		ASD13CR0	8C	RW		CC	
PRT3DM1	0D	RW		4D		ASD13CR1	8D	RW		CD	
PRT3IC0	0E	RW		4E		ASD13CR2	8E	RW		CE	
PRT3IC1	0F	RW		4F		ASD13CR3	8F	RW		CF	
PRT4DM0	10	RW		50		ASD20CR0	90	RW	GDI_O_IN	D0	RW
PRT4DM1	11	RW		51		ASD20CR1	91	RW	GDI_E_IN	D1	RW
PRT4IC0	12	RW		52		ASD20CR2	92	RW	GDI_O_OU	D2	RW
PRT4IC1	13	RW		53		ASD20CR3	93	RW	GDI_E_OU	D3	RW
PRT5DM0	14	RW		54		ASC21CR0	94	RW		D4	
PRT5DM1	15	RW		55		ASC21CR1	95	RW		D5	
PRT5IC0	16	RW		56		ASC21CR2	96	RW		D6	
PRT5IC1	17	RW		57		ASC21CR3	97	RW		D7	
	18			58		ASD22CR0	98	RW		D8	
	19			59		ASD22CR1	99	RW		D9	
	1A			5A		ASD22CR2	9A	RW		DA	
	1B			5B		ASD22CR3	9B	RW		DB	
	1C			5C		ASC23CR0	9C	RW		DC	
	1D			5D		ASC23CR1	9D	RW	OSC_GO_EN	DD	RW
	1E			5E		ASC23CR2	9E	RW	OSC_CR4	DE	RW
	1F			5F		ASC23CR3	9F	RW	OSC_CR3	DF	RW
DBB00FN	20	RW	CLK_CR0	60	RW		A0		OSC_CR0	E0	RW
DBB00IN	21	RW	CLK_CR1	61	RW		A1		OSC_CR1	E1	RW
DBB00OU	22	RW	ABF_CR0	62	RW		A2		OSC_CR2	E2	RW
	23		AMD_CR0	63	RW		A3		VLT_CR	E3	RW
DBB01FN	24	RW		64			A4		VLT_CMP	E4	R
DBB01IN	25	RW		65			A5			E5	
DBB01OU	26	RW	AMD_CR1	66	RW		A6			E6	
	27		ALT_CR0	67	RW		A7			E7	
DCB02FN	28	RW	ALT_CR1	68	RW		A8		IMO_TR	E8	W
DCB02IN	29	RW	CLK_CR2	69	RW		A9		ILO_TR	E9	W
DCB02OU	2A	RW		6A			AA		BDG_TR	EA	RW
	2B			6B			AB		ECO_TR	EB	W
DCB03FN	2C	RW		6C			AC			EC	
DCB03IN	2D	RW		6D			AD			ED	
DCB03OU	2E	RW		6E			AE			EE	
	2F			6F			AF			EF	
DBB10FN	30	RW	ACB00CR3	70	RW	RDIOI	B0	RW		F0	
DBB10IN	31	RW	ACB00CR0	71	RW	RDIO1SYN	B1	RW		F1	
DBB10OU	32	RW	ACB00CR1	72	RW	RDIOIS	B2	RW		F2	
	33		ACB00CR2	73	RW	RDIO1LT0	B3	RW		F3	
DBB11FN	34	RW	ACB01CR3	74	RW	RDIO1LT1	B4	RW		F4	
DBB11IN	35	RW	ACB01CR0	75	RW	RDIO1RO0	B5	RW		F5	
DBB11OU	36	RW	ACB01CR1	76	RW	RDIO1RO1	B6	RW		F6	
	37		ACB01CR2	77	RW		B7		CPU_F	F7	RL
DCB12FN	38	RW	ACB02CR3	78	RW	RDIO1RI	B8	RW		F8	
DCB12IN	39	RW	ACB02CR0	79	RW	RDIO1SYN	B9	RW		F9	
DCB12OU	3A	RW	ACB02CR1	7A	RW	RDIO1IS	BA	RW		FA	
	3B		ACB02CR2	7B	RW	RDIO1LT0	BB	RW		FB	
DCB13FN	3C	RW	ACB03CR3	7C	RW	RDIO1LT1	BC	RW		FC	
DCB13IN	3D	RW	ACB03CR0	7D	RW	RDIO1RO0	BD	RW		FD	
DCB13OU	3E	RW	ACB03CR1	7E	RW	RDIO1RO1	BE	RW	CPU_SCR1	FE	#
	3F		ACB03CR2	7F	RW		BF		CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed.

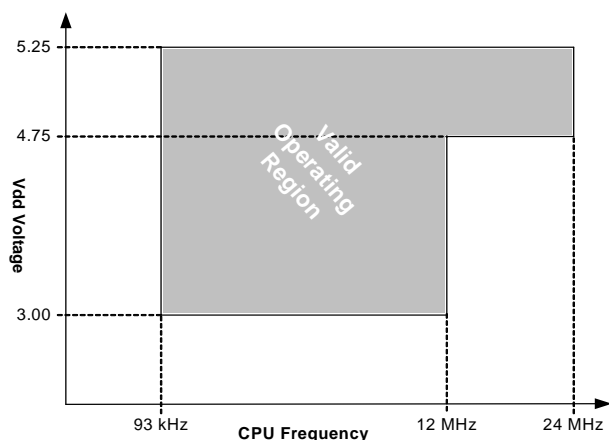
Access is bit specific.

Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8CLED08 EZ-Color device. For the most up to date electrical specifications, confirm that you have the most recent data sheet by going to the web at <http://www.cypress.com/ez-color>.

Specifications are valid for $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ and $T_J \leq 100^{\circ}\text{C}$, except where noted. Specifications for devices running at greater than 12 MHz are valid for $-40^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$ and $T_J \leq 82^{\circ}\text{C}$.

Figure 7. Voltage versus CPU Frequency



The following table lists the units of measure that are used in this section.

Table 7. Units of Measure

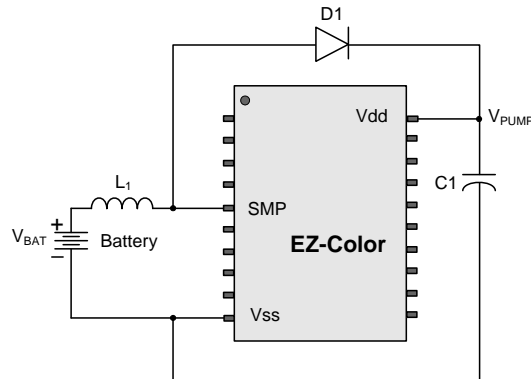
Symbol	Unit of Measure	Symbol	Unit of Measure
$^{\circ}\text{C}$	degree Celsius	μW	microwatts
dB	decibels	mA	milli-ampere
fF	femto farad	ms	milli-second
Hz	hertz	mV	milli-volts
KB	1024 bytes	nA	nanoampere
Kbit	1024 bits	ns	nanosecond
kHz	kilohertz	nV	nanovolts
k Ω	kilohm	Ω	ohm
MHz	megahertz	pA	picoampere
M Ω	megaohm	pF	picofarad
μA	microampere	pp	peak-to-peak
μF	microfarad	ppm	parts per million
μH	microhenry	ps	picosecond
μs	microsecond	sps	samples per second
μV	microvolts	σ	sigma: one standard deviation
μVrms	microvolts root-mean-square	V	volts

Absolute Maximum Ratings

Table 8. Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Units	Notes
T_{STG}	Storage Temperature	-55	25	+100	$^{\circ}\text{C}$	Higher storage temperatures will reduce data retention time. Recommended storage temperature is $+25^{\circ}\text{C} \pm 25^{\circ}\text{C}$. Extended duration storage temperatures above 65°C will degrade reliability.
T_A	Ambient Temperature with Power Applied	-40	—	+85	$^{\circ}\text{C}$	
Vdd	Supply Voltage on Vdd Relative to Vss	-0.5	—	+6.0	V	
V_{IO}	DC Input Voltage	Vss - 0.5	—	Vdd + 0.5	V	
V_{IOZ}	DC Voltage Applied to Tri-state	Vss - 0.5	—	Vdd + 0.5	V	
I_{MIO}	Maximum Current into any Port Pin	-25	—	+50	mA	
I_{MAIO}	Maximum Current into any Port Pin Configured as Analog Driver	-50	—	+50	mA	
ESD	Electro Static Discharge Voltage	2000	—	—	V	Human Body Model ESD.
LU	Latch-up Current	—	—	200	mA	

Figure 8. Basic Switch Mode Pump Circuit



DC Analog Reference Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0V to 3.6V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

The guaranteed specifications are measured through the Analog Continuous Time PSoC blocks. The power levels for AGND refer

to the power of the Analog Continuous Time PSoC block. The power levels for RefHi and RefLo refer to the Analog Reference Control register. The limits stated for AGND include the offset error of the AGND buffer local to the Analog Continuous Time PSoC block. Reference control power is high.

Table 18. 5V DC Analog Reference Specifications

Symbol	Description	Min	Typ	Max	Units
BG	Bandgap Voltage Reference	1.28	1.30	1.32	V
—	AGND = $V_{dd}/2^a$	$V_{dd}/2 - 0.030$	$V_{dd}/2$	$V_{dd}/2 + 0.007$	V
—	AGND = $2 \times \text{BandGap}^a$	$2 \times \text{BG} - 0.043$	$2 \times \text{BG}$	$2 \times \text{BG} + 0.024$	V
—	AGND = P2[4] (P2[4] = $V_{dd}/2$) ^a	$P2[4] - 0.011$	P2[4]	$P2[4] + 0.011$	V
—	AGND = BandGap^a	$\text{BG} - 0.009$	BG	$\text{BG} + 0.009$	V
—	AGND = $1.6 \times \text{BandGap}^a$	$1.6 \times \text{BG} - 0.018$	$1.6 \times \text{BG}$	$1.6 \times \text{BG} + 0.018$	V
—	AGND Block to Block Variation (AGND = $V_{dd}/2$) ^a	-0.034	0.000	0.034	V
—	RefHi = $V_{dd}/2 + \text{BandGap}$	$V_{dd}/2 + \text{BG} - 0.1$	$V_{dd}/2 + \text{BG} - 0.01$	$V_{dd}/2 + \text{BG} + 0.1$	V
—	RefHi = $3 \times \text{BandGap}$	$3 \times \text{BG} - 0.06$	$3 \times \text{BG} - 0.01$	$3 \times \text{BG} + 0.06$	V
—	RefHi = $2 \times \text{BandGap} + P2[6]$ (P2[6] = 1.3V)	$2 \times \text{BG} + P2[6] - 0.06$	$2 \times \text{BG} + P2[6] - 0.01$	$2 \times \text{BG} + P2[6] + 0.06$	V
—	RefHi = P2[4] + BandGap (P2[4] = $V_{dd}/2$)	$P2[4] + \text{BG} - 0.06$	$P2[4] + \text{BG} - 0.01$	$P2[4] + \text{BG} + 0.06$	V
—	RefHi = P2[4] + P2[6] (P2[4] = $V_{dd}/2$, P2[6] = 1.3V)	$P2[4] + P2[6] - 0.06$	$P2[4] + P2[6] - 0.01$	$P2[4] + P2[6] + 0.06$	V
—	RefHi = $3.2 \times \text{BandGap}$	$3.2 \times \text{BG} - 0.06$	$3.2 \times \text{BG} - 0.01$	$3.2 \times \text{BG} + 0.06$	V
—	RefLo = $V_{dd}/2 - \text{BandGap}$	$V_{dd}/2 - \text{BG} - 0.051$	$V_{dd}/2 - \text{BG} + 0.01$	$V_{dd}/2 - \text{BG} + 0.06$	V
—	RefLo = BandGap	$\text{BG} - 0.06$	$\text{BG} + 0.01$	$\text{BG} + 0.06$	V
—	RefLo = $2 \times \text{BandGap} - P2[6]$ (P2[6] = 1.3V)	$2 \times \text{BG} - P2[6] - 0.04$	$2 \times \text{BG} - P2[6] + 0.01$	$2 \times \text{BG} - P2[6] + 0.04$	V
—	RefLo = P2[4] - BandGap (P2[4] = $V_{dd}/2$)	$P2[4] - \text{BG} - 0.056$	$P2[4] - \text{BG} + 0.01$	$P2[4] - \text{BG} + 0.056$	V
—	RefLo = P2[4] - P2[6] (P2[4] = $V_{dd}/2$, P2[6] = 1.3V)	$P2[4] - P2[6] - 0.056$	$P2[4] - P2[6] + 0.01$	$P2[4] - P2[6] + 0.056$	V

a. AGND tolerance includes the offsets of the local buffer in the PSoC block.

DC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0V to 3.6V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 22. DC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
I_{DDP}	Supply Current During Programming or Verify	–	5	25	mA	
V_{ILP}	Input Low Voltage During Programming or Verify	–	–	0.8	V	
V_{IHP}	Input High Voltage During Programming or Verify	2.2	–	–	V	
I_{ILP}	Input Current when Applying V_{ilp} to P1[0] or P1[1] During Programming or Verify	–	–	0.2	mA	Driving internal pull-down resistor.
I_{IHP}	Input Current when Applying V_{ihp} to P1[0] or P1[1] During Programming or Verify	–	–	1.5	mA	Driving internal pull-down resistor.
V_{OLV}	Output Low Voltage During Programming or Verify	–	–	$V_{SS} + 0.75$	V	
V_{OHV}	Output High Voltage During Programming or Verify	$V_{DD} - 1.0$	–	V_{DD}	V	
Flash _{ENPB}	Flash Endurance (per block)	50,000	–	–	–	Erase/write cycles per block.
Flash _{ENT}	Flash Endurance (total) ^a	1,800,000	–	–	–	Erase/write cycles.
Flash _{DR}	Flash Data Retention	10	–	–	Years	

- a. A maximum of 36 x 50,000 block endurance cycles is allowed. This may be balanced between operations on 36x1 blocks of 50,000 maximum cycles each, 36x2 blocks of 25,000 maximum cycles each, or 36x4 blocks of 12,500 maximum cycles each (to limit the total number of cycles to 36x50,000 and that no single block ever sees more than 50,000 cycles).

For the full industrial range, the user must employ a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. Refer to the Flash APIs Application Note AN2015 at <http://www.cypress.com> under Application Notes for more information.

AC Electrical Characteristics

AC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0V to 3.6V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 23. AC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{IMO}	Internal Main Oscillator Frequency	23.4	24	24.6 ^a	MHz	Trimmed. Utilizing factory trim values.
F_{CPU1}	CPU Frequency (5V Nominal)	0.93	24	24.6 ^{a,b}	MHz	Trimmed. Utilizing factory trim values.
F_{CPU2}	CPU Frequency (3.3V Nominal)	0.93	12	12.3 ^{b,c}	MHz	Trimmed. Utilizing factory trim values.
$F_{48\text{M}}$	Digital PSoC Block Frequency	0	48	49.2 ^{a,b,d}	MHz	Refer to the AC Digital Block Specifications below.
$F_{24\text{M}}$	Digital PSoC Block Frequency	0	24	24.6 ^{b,d}	MHz	
$F_{32\text{K1}}$	Internal Low Speed Oscillator Frequency	15	32	64	kHz	
$F_{32\text{K2}}$	External Crystal Oscillator	—	32.768	—	kHz	Accuracy is capacitor and crystal dependent. 50% duty cycle.
F_{PLL}	PLL Frequency	—	23.986	—	MHz	Multiple (x732) of crystal frequency.
Jitter24M2	24 MHz Period Jitter (PLL)	—	—	600	ps	
T_{PLLSLEW}	PLL Lock Time	0.5	—	10	ms	
$T_{\text{PLLSLEWS-LOW}}$	PLL Lock Time for Low Gain Setting	0.5	—	50	ms	
T_{OS}	External Crystal Oscillator Startup to 1%	—	1700	2620	ms	
T_{OSACC}	External Crystal Oscillator Startup to 100 ppm	—	2800	3800	ms	The crystal oscillator frequency is within 100 ppm of its final value by the end of the T_{OSACC} period. Correct operation assumes a properly loaded 1 μW maximum drive level 32.768 kHz crystal. $3.0\text{V} \leq V_{\text{dd}} \leq 5.5\text{V}$, $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$.
Jitter32k	32 kHz Period Jitter	—	100	—	ns	
T_{XRST}	External Reset Pulse Width	10	—	—	μs	
DC24M	24 MHz Duty Cycle	40	50	60	%	
Step24M	24 MHz Trim Step Size	—	50	—	kHz	
F_{out48M}	48 MHz Output Frequency	46.8	48.0	49.2 ^{a,c}	MHz	Trimmed. Utilizing factory trim values.
Jitter24M1	24 MHz Period Jitter (IMO)	—	600	—	ps	
F_{MAX}	Maximum frequency of signal on row input or row output.	—	—	12.3	MHz	
T_{RAMP}	Supply Ramp Time	0	—	—	μs	

- $4.75\text{V} < V_{\text{dd}} < 5.25\text{V}$.
- Accuracy derived from Internal Main Oscillator with appropriate trim for Vdd range.
- $3.0\text{V} < V_{\text{dd}} < 3.6\text{V}$. See Application Note AN2012 "Adjusting PSoC Microcontroller Trims for Dual Voltage-Range Operation" for information on trimming for operation at 3.3V.
- See the individual user module data sheets for information on maximum frequencies for user modules.

Figure 9. PLL Lock Timing Diagram

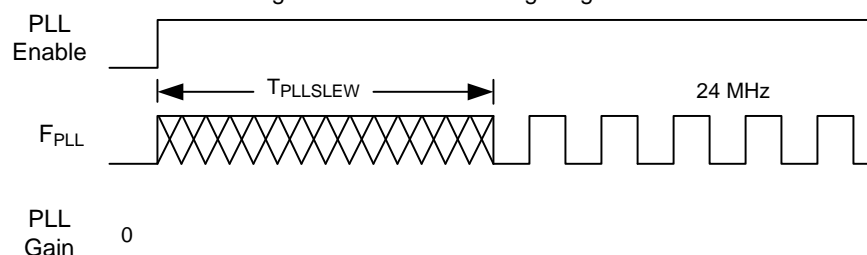
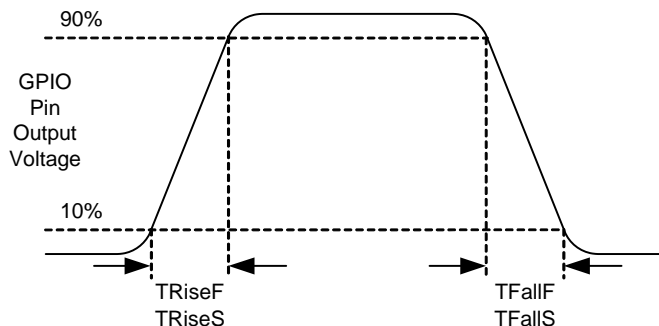


Figure 14. GPIO Timing Diagram



AC Operational Amplifier Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0V to 3.6V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only. Settling times, slew rates, and gain bandwidth are based on the Analog Continuous Time PSoC block.

Power = High and Opamp Bias = High is not supported at 3.3V.

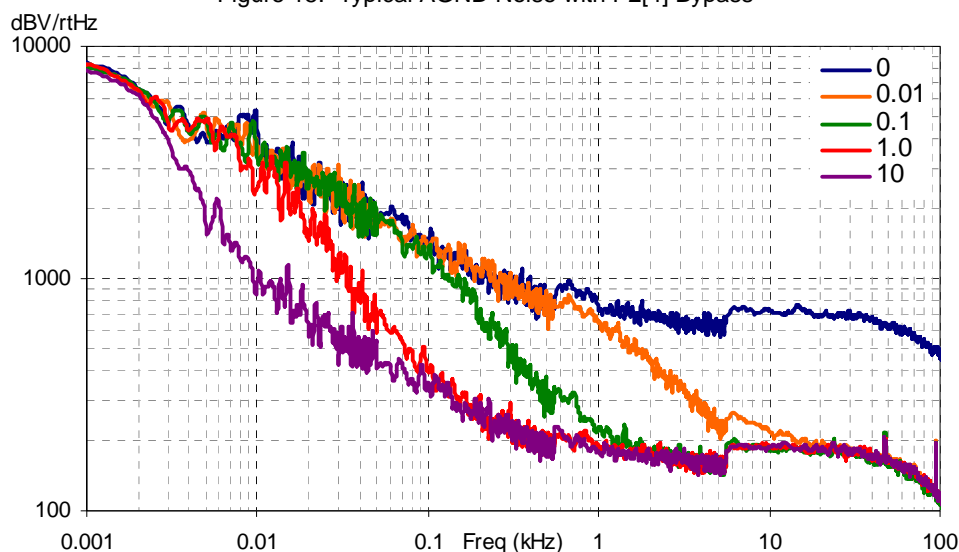
Table 25. 5V AC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{ROA}	Rising Settling Time from 80% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain)					
	Power = Low, Opamp Bias = Low	—	—	3.9	μs	
	Power = Medium, Opamp Bias = High	—	—	0.72	μs	
	Power = High, Opamp Bias = High	—	—	0.62	μs	
T_{SOA}	Falling Settling Time from 20% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain)					
	Power = Low, Opamp Bias = Low	—	—	5.9	μs	
	Power = Medium, Opamp Bias = High	—	—	0.92	μs	
	Power = High, Opamp Bias = High	—	—	0.72	μs	
SR_{ROA}	Rising Slew Rate (20% to 80%)(10 pF load, Unity Gain)					
	Power = Low, Opamp Bias = Low	0.15	—	—	$\text{V}/\mu\text{s}$	
	Power = Medium, Opamp Bias = High	1.7	—	—	$\text{V}/\mu\text{s}$	
	Power = High, Opamp Bias = High	6.5	—	—	$\text{V}/\mu\text{s}$	
SR_{FOA}	Falling Slew Rate (20% to 80%)(10 pF load, Unity Gain)					
	Power = Low, Opamp Bias = Low	0.01	—	—	$\text{V}/\mu\text{s}$	
	Power = Medium, Opamp Bias = High	0.5	—	—	$\text{V}/\mu\text{s}$	
	Power = High, Opamp Bias = High	4.0	—	—	$\text{V}/\mu\text{s}$	
BW_{OA}	Gain Bandwidth Product					
	Power = Low, Opamp Bias = Low	0.75	—	—	MHz	
	Power = Medium, Opamp Bias = High	3.1	—	—	MHz	
	Power = High, Opamp Bias = High	5.4	—	—	MHz	
E_{NOA}	Noise at 1 kHz (Power = Medium, Opamp Bias = High)	—	100	—	nV/rt-Hz	

Table 26. 3.3V AC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{ROA}	Rising Settling Time from 80% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain)					
	Power = Low, Opamp Bias = Low	—	—	3.92	μs	
	Power = Low, Opamp Bias = High	—	—	0.72	μs	
T_{SOA}	Falling Settling Time from 20% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain)					
	Power = Low, Opamp Bias = Low	—	—	5.41	μs	
	Power = Medium, Opamp Bias = High	—	—	0.72	μs	
SR_{ROA}	Rising Slew Rate (20% to 80%)(10 pF load, Unity Gain)					
	Power = Low, Opamp Bias = Low	0.31	—	—	V/ μs	
	Power = Medium, Opamp Bias = High	2.7	—	—	V/ μs	
SR_{FOA}	Falling Slew Rate (20% to 80%)(10 pF load, Unity Gain)					
	Power = Low, Opamp Bias = Low	0.24	—	—	V/ μs	
	Power = Medium, Opamp Bias = High	1.8	—	—	V/ μs	
BW_{OA}	Gain Bandwidth Product					
	Power = Low, Opamp Bias = Low	0.67	—	—	MHz	
	Power = Medium, Opamp Bias = High	2.8	—	—	MHz	
E_{NOA}	Noise at 1 kHz (Power = Medium, Opamp Bias = High)	—	100	—	nV/rt-Hz	

When bypassed by a capacitor on P2[4], the noise of the analog ground signal distributed to each block is reduced by a factor of up to 5 (14 dB). This is at frequencies above the corner frequency defined by the on-chip 8.1k resistance and the external capacitor.

Figure 15. Typical AGND Noise with P2[4] Bypass


AC External Clock Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0V to 3.6V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 31. 5V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F _{OSCEXT}	Frequency	0.093	–	24.6	MHz	
–	High Period	20.6	–	5300	ns	
–	Low Period	20.6	–	–	ns	
–	Power Up IMO to Switch	150	–	–	μs	

Table 32. 3.3V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F _{OSCEXT}	Frequency with CPU Clock divide by 1 ^a	0.093	–	12.3	MHz	
F _{OSCEXT}	Frequency with CPU Clock divide by 2 or greater ^b	0.186	–	24.6	MHz	
–	High Period with CPU Clock divide by 1	41.7	–	5300	ns	
–	Low Period with CPU Clock divide by 1	41.7	–	–	ns	
–	Power Up IMO to Switch	150	–	–	μs	

a. Maximum CPU frequency is 12 MHz at 3.3V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements.

b. If the frequency of the external clock is greater than 12 MHz, the CPU clock divider must be set to 2 or greater. In this case, the CPU clock divider will ensure that the fifty per-cent duty cycle requirement is met.

AC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0V to 3.6V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 33. AC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T _{RSCLK}	Rise Time of SCLK	1	–	20	ns	
T _{FSCLK}	Fall Time of SCLK	1	–	20	ns	
T _{SSCLK}	Data Set up Time to Falling Edge of SCLK	40	–	–	ns	
T _{HSCLK}	Data Hold Time from Falling Edge of SCLK	40	–	–	ns	
F _{SCLK}	Frequency of SCLK	0	–	8	MHz	
T _{ERASEB}	Flash Erase Time (Block)	–	10	–	ms	
T _{WRITE}	Flash Block Write Time	–	10	–	ms	
T _{DSCLK}	Data Out Delay from Falling Edge of SCLK	–	–	45	ns	V _{dd} > 3.6
T _{DSCLK3}	Data Out Delay from Falling Edge of SCLK	–	–	50	ns	3.0 ≤ V _{dd} ≤ 3.6

Packaging Information

This section illustrates the packaging specifications for the CY8CLED08 EZ-Color device, along with the thermal impedances for each package and the typical package capacitance on crystal pins.

Important Note Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, refer to the document titled *PSoC Emulator Pod Dimensions* at <http://www.cypress.com/design/MR10161>.

Packaging Dimensions

Figure 18. 48-Lead (300-Mil) SSOP

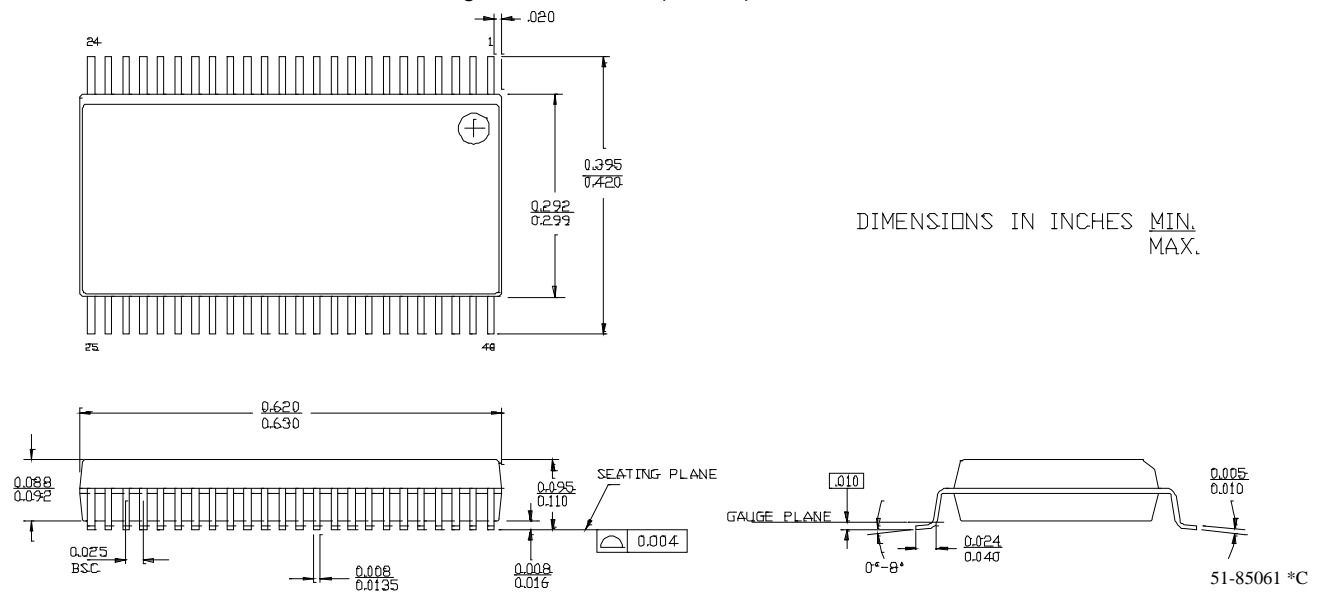
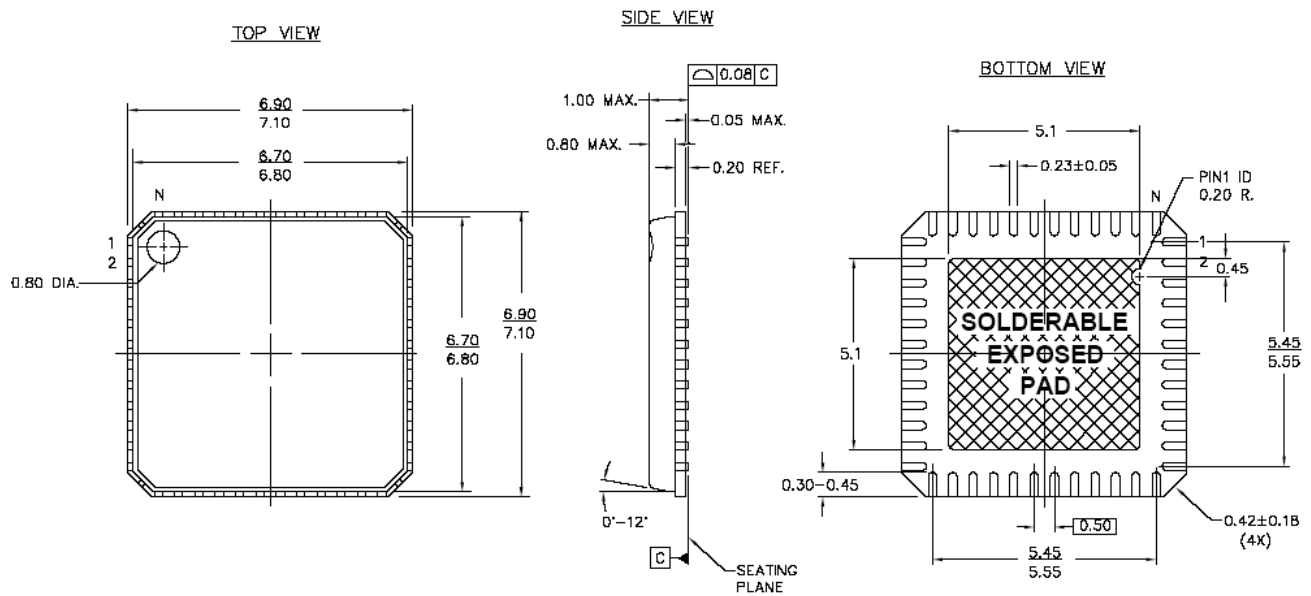



Figure 19. 48-Lead (7x7 mm) QFN



NOTES:

1.  HATCH AREA IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC#: MO-220
3. PACKAGE WEIGHT: 0.13g
4. ALL DIMENSIONS ARE IN MM [MIN/MAX]
5. PACKAGE CODE

PART #	DESCRIPTION
LF48A	STANDARD
LY48A	LEAD FREE

001-12919 *A

Thermal Impedances

Table 35. Thermal Impedances per Package

Package	Typical θ_{JA} *
48 SSOP	69 °C/W
48 QFN**	18 °C/W
28 SSOP	95 °C/W

* $T_J = T_A + \text{POWER} \times \theta_{JA}$

** To achieve the thermal impedance specified for the QFN package, the center thermal pad should be soldered to the PCB ground plane.

Capacitance on Crystal Pins

Table 36. Typical Package Capacitance on Crystal Pins

Package	Package Capacitance
48 SSOP	3.3 pF
48 QFN	2.3 pF
28 SSOP	2.8 pF

Solder Reflow Peak Temperature

Following is the minimum solder reflow peak temperature to achieve good solderability.

Table 37. Solder Reflow Peak Temperature

Package	Minimum Peak Temperature*	Maximum Peak Temperature
48 SSOP	220°C	260°C
48 QFN	240°C	260°C
28 SSOP	240°C	260°C

*Higher temperatures may be required based on the solder melting point. Typical temperatures for solder are $220 \pm 5^\circ\text{C}$ with Sn-Pb or $245 \pm 5^\circ\text{C}$ with Sn-Ag-Cu paste. Refer to the solder manufacturer specifications.

Development Tool Selection

This section presents the development tools available for all current PSoC based devices including the CY8CLED08 EZ-Color family.

Software Tools

PSoC Express™

As the newest addition to the PSoC development software suite, PSoC Express is the first visual embedded system design tool that allows a user to create an entire project and generate a schematic, BOM, and data sheet without writing a single line of code. Users work directly with application objects such as LEDs, switches, sensors, and fans. PSoC Express is available free of charge at <http://www.cypress.com/psocexpress>.

PSoC Designer™

Utilized by thousands of PSoC developers, this robust software has been facilitating PSoC designs for half a decade. PSoC Designer is available free of charge at <http://www.cypress.com> under DESIGN RESOURCES >> Software and Drivers.

PSoC Programmer

Flexible enough to be used on the bench in development, yet suitable for factory programming, PSoC Programmer works either as a standalone programming application or it can operate directly from PSoC Designer or PSoC Express. PSoC Programmer software is compatible with both PSoC ICE-Cube In-Circuit Emulator and PSoC MiniProg. PSoC programmer is available free of charge at <http://www.cypress.com/psocprogrammer>.

CY3202-C iMAGEcraft C Compiler

CY3202 is the optional upgrade to PSoC Designer that enables the iMAGEcraft C compiler. It can be purchased from the Cypress Online Store. At <http://www.cypress.com>, click the Online Store shopping cart icon at the bottom of the web page, and click *PSoC (Programmable System-on-Chip)* to view a current list of available items.

Hardware Tools

In-Circuit Emulator

A low cost, high functionality ICE (In-Circuit Emulator) is available for development support. This hardware has the capability to program single devices.

The emulator consists of a base unit that connects to the PC by way of the USB port. The base unit is universal and will operate with all PSoC based devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full speed (24 MHz) operation.

I2C to USB Bridge

The I2C to USB Bridge is a quick and easy link from any design or application's I2C bus to a PC via USB for design testing, debugging and communication.

PSoC Programmer

Flexible enough to be used on the bench in development, yet suitable for factory programming, PSoC Programmer works either as a standalone programming application or it can operate directly from PSoC Designer or PSoC Express. PSoC Programmer software is compatible with both PSoC ICE-Cube In-Circuit Emulator and PSoC MiniProg. PSoC programmer is available free of charge at <http://www.cypress.com/psocprogrammer>.

CY3202-C iMAGEcraft C Compiler

CY3202 is the optional upgrade to PSoC Designer that enables the iMAGEcraft C compiler. It can be purchased from the Cypress Online Store. At <http://www.cypress.com>, click the Online Store shopping cart icon at the bottom of the web page, and click *PSoC (Programmable System-on-Chip)* to view a current list of available items.

Evaluation Tools

All evaluation tools can be purchased from the Cypress Online Store.

CY3261A-RGB EZ-Color RGB Kit

The CY3261A-RGB board is a preprogrammed HB LED color mix board with seven pre-set colors using the CY8CLED16 EZ-Color HB LED Controller. The board is accompanied by a CD containing the color selector software application, PSoC Express 3.0 Beta 2, PSoC Programmer, and a suite of documents, schematics, and firmware examples. The color selector software application can be installed on a host PC and is used to control the EZ-Color HB LED controller using the included USB cable. The application enables you to select colors via a CIE 1931 chart or by entering coordinates. The kit includes:

- Training Board (CY8CLED16)
- One mini-A to mini-B USB Cable
- PSoC Express CD-ROM
- Design Files and Application Installation CD-ROM

To program and tune this kit via PSoC Express 3.0 you must use a Mini Programmer Unit (CY3217 Kit) and a CY3240-I2CUSB kit.

CY3210-MiniProg1

The CY3210-MiniProg1 kit allows a user to program PSoC devices via the MiniProg1 programming unit. The MiniProg is a small, compact prototyping programmer that connects to the PC via a provided USB 2.0 cable. The kit includes:

- MiniProg Programming Unit
- MiniEval Socket Programming and Evaluation Board
- 28-Pin CY8C29466-24PXI PDIP PSoC Device Sample
- 28-Pin CY8C27443-24PXI PDIP PSoC Device Sample
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

CY3210-PSoCEval1

The CY3210-PSoCEval1 kit features an evaluation board and the MiniProg1 programming unit. The evaluation board includes an LCD module, potentiometer, LEDs, and plenty of breadboarding space to meet all of your evaluation needs. The kit includes:

- Evaluation Board with LCD Module
- MiniProg Programming Unit
- 28-Pin CY8C29466-24PXI PDIP PSoC Device Sample (2)
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

Device Programmers

All device programmers can be purchased from the Cypress Online Store.

CY3216 Modular Programmer

The CY3216 Modular Programmer kit features a modular programmer and the MiniProg1 programming unit. The modular programmer includes three programming module cards and supports multiple Cypress products. The kit includes:

- Modular Programmer Base
- 3 Programming Module Cards
- MiniProg Programming Unit
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

CY3207ISSP In-System Serial Programmer (ISSP)

The CY3207ISSP is a production programmer. It includes protection circuitry and an industrial case that is more robust than the MiniProg in a production-programming environment.

Note: CY3207ISSP needs special software and is not compatible with PSoC Programmer. The kit includes:

- CY3207 Programmer Unit
- PSoC ISSP Software CD
- 110 ~ 240V Power Supply, Euro-Plug Adapter
- USB 2.0 Cable

Accessories (Emulation and Programming)

Table 38. Emulation and Programming Accessories

Part #	Pin Package	Flex-Pod Kit ^a	Foot Kit ^b	Adapter ^c
CY8CLED08-48PVXI	48 SSOP	CY3250-27XXX	CY3250-48 SSOP-FK	Adapters can be found at http://www.emulation.com .
CY8CLED08-48LFXI	48 QFN	CY3250-27XXX QFN	CY3250-48 QFN-FK	
CY8CLED08-28PVXI	28 SSOP	CY3250-27XXX	CY3250-28 SSOP-FK	

- Flex-Pod kit includes a practice flex-pod and a practice PCB, in addition to two flex-pods.
- Foot kit includes surface mount feet that can be soldered to the target PCB.
- Programming adapter converts non-DIP package to DIP footprint. Specific details and ordering information for each of the adapters can be found at <http://www.emulation.com>.

Third Party Tools

Several tools have been specially designed by the following 3rd-party vendors to accompany PSoC based devices during development and production. Specific details for each of these tools can be found at <http://www.cypress.com> under DESIGN RESOURCES >> Evaluation Boards.

Build a PSoC Emulator into Your Board

For details on how to emulate your circuit before going to volume production using an on-chip debug (OCD) non-production PSoC device, see Application Note "Debugging - Build a PSoC Emulator into Your Board - AN2323" at <http://www.cypress.com/an2323>. The following table lists the CY8CLED08 EZ-Color devices' key package features and ordering codes.

Ordering Information

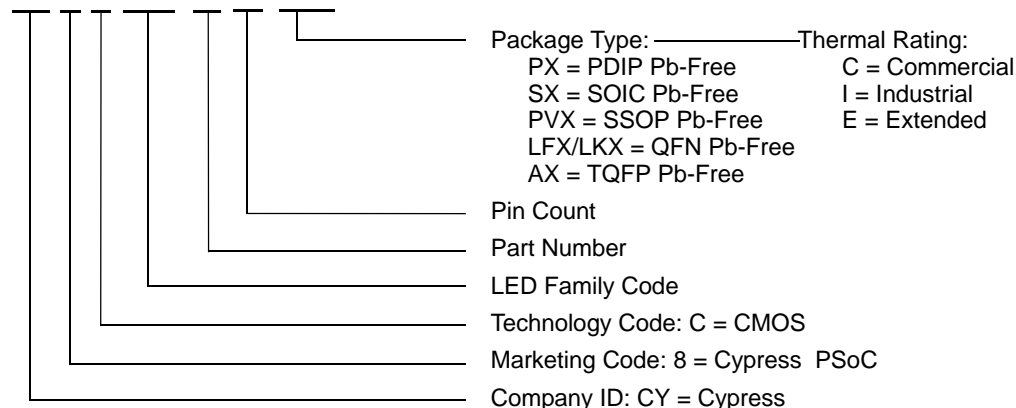
Key Device Features

Table 39. Device Key Features and Ordering Information

Package	Ordering Code	Flash (Bytes)	RAM (Bytes)	Switch Mode Pump	Temperature Range	Digital Blocks (Rows of 4)	Analog Blocks (Columns of 3)	Digital IO Pins	Analog Inputs	Analog Outputs	XRES Pin
48 Pin (300 Mil) SSOP	CY8CLED08-48PVXI	16K	256	Yes	-40C to +85C	8	12	44	12	4	Yes
48 Pin (300 Mil) SSOP (Tape and Reel)	CY8CLED08-48PVXIT	16K	256	Yes	-40C to +85C	8	12	44	12	4	Yes
48 Pin (7x7) QFN	CY8CLED08-48LFXI	16K	256	Yes	-40C to +85C	8	12	44	12	4	Yes
48 Pin (7x7) QFN (Tape and Reel)	CY8CLED08-48LFXIT	16K	256	Yes	-40C to +85C	8	12	44	12	4	Yes
28 Pin (210 Mil) SSOP	CY8CLED08-28PVXI	16K	256	Yes	-40C to +85C	8	12	24	12	4	Yes
28 Pin (210 Mil) SSOP (Tape and Reel)	CY8CLED08-28PVXIT	16K	256	Yes	-40C to +85C	8	12	24	12	4	Yes

Ordering Code Definitions

CY 8 C LED xx - xx xxxx



Document History

Table 40. CY8CLED08 Data Sheet Revision History

Document Title: CY8CLED08 EZ-Color™ HB LED Controller				
Document Number: 001-12981				
Revision	ECN #	Issue Date	Origin of Change	Description of Change
**	1148504	See ECN	SFVTMP3	New document (revision **).
*A	1391163	See ECN	AESA	Added 28 pin SSOP
Distribution: External Public			Posting: None	

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