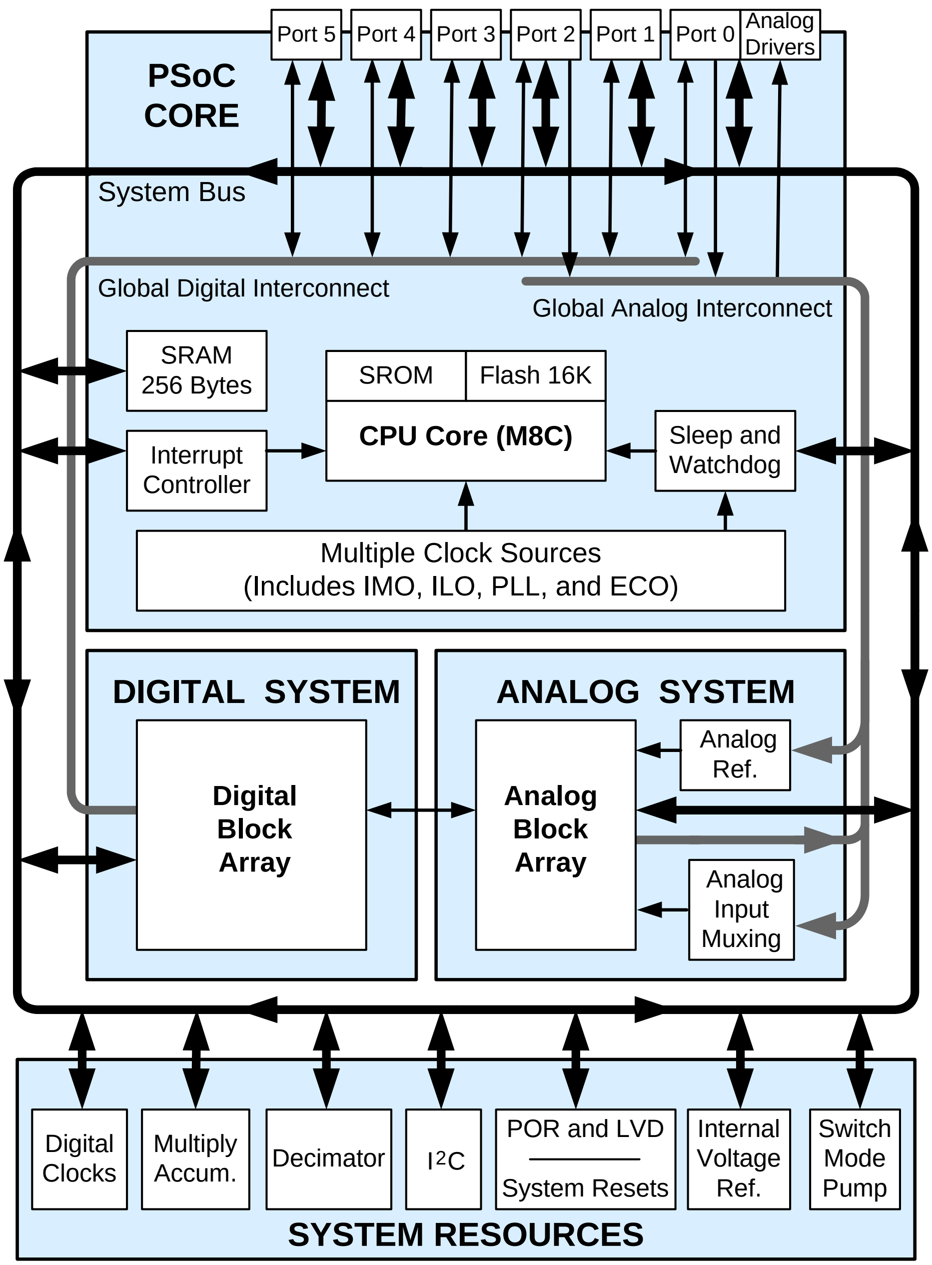


| Details | |
|---|---|
| Product Status | Obsolete |
| Applications | HB LED Controller |
| Core Processor | M8C |
| Program Memory Type | FLASH (16KB) |
| Controller Series | CY8CLED |
| RAM Size | 256 x 8 |
| Interface | I²C, SPI, UART/USART |
| Number of I/O | 44 |
| Voltage - Supply | 3V ~ 5.25V |
| Operating Temperature | -40°C ~ 85°C |
| Mounting Type | Surface Mount |
| Package / Case | 48-BSSOP (0.295", 7.50mm Width) |
| Supplier Device Package | 48-SSOP |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/cy8cled08-48pvxi |

## Overview

### Block Diagram



The digital blocks can be connected to any GPIO through a series of global buses that can route any signal to any pin. The buses also allow for signal multiplexing and for performing logic operations. This configurability frees your designs from the constraints of a fixed peripheral controller.

Digital blocks are provided in rows of four, where the number of blocks varies by EZ-Color device family. This allows you the optimum choice of system resources for your application. Family resources are shown in the table titled EZ-Color Device Characteristics.

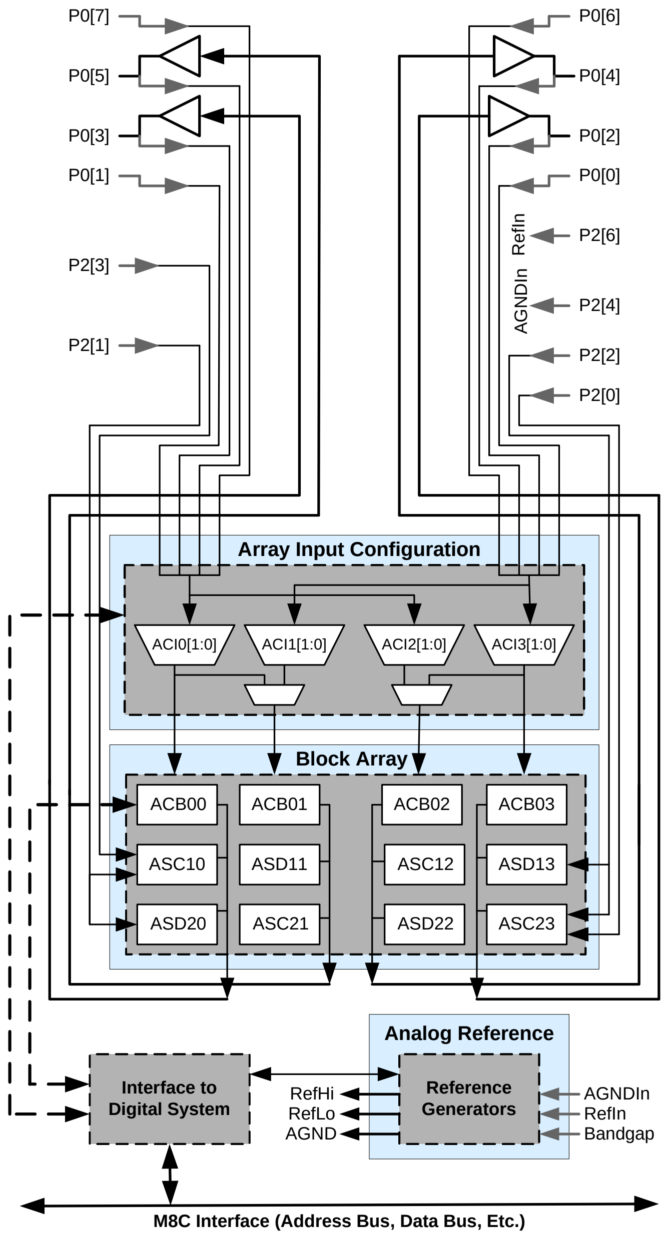
## The Analog System

The Analog System is composed of 12 configurable blocks, each comprised of an opamp circuit allowing the creation of complex analog signal flows. Analog peripherals are very flexible and can be customized to support specific application requirements. Some of the more common EZ-Color analog functions (most available as user modules) are listed below.

- Analog-to-digital converters (up to 4, with 6- to 14-bit resolution, selectable as Incremental, Delta Sigma, and SAR)
- Filters (2, 4, 6, and 8 pole band-pass, low-pass, and notch)
- Amplifiers (up to 4, with selectable gain to 48x)
- Instrumentation amplifiers (up to 2, with selectable gain to 93x)
- Comparators (up to 4, with 16 selectable thresholds)
- DACs (up to 4, with 6- to 9-bit resolution)
- Multiplying DACs (up to 4, with 6- to 9-bit resolution)
- High current output drivers (four with 30 mA drive as a Core Resource)
- 1.3V reference (as a System Resource)
- DTMF Dialer
- Modulators
- Correlators
- Peak detectors
- Many other topologies possible

Analog blocks are provided in columns of three, which includes one CT (Continuous Time) and two SC (Switched Capacitor) blocks, as shown in the figure below.

Figure 2. Analog System Block Diagram



# Pin Information

## Pinouts

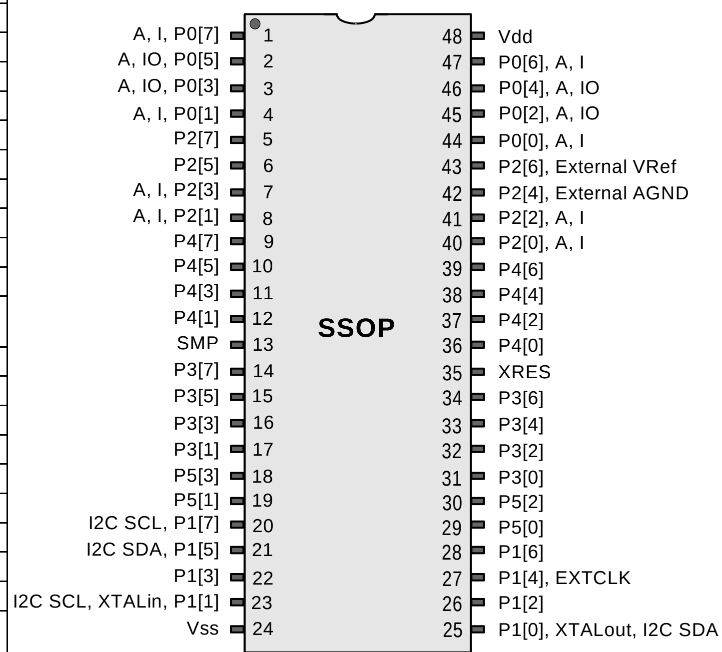
*48-Pin Part Pinout SSOP*

Table 2. 48-Pin Part Pinout (SSOP)

| Pin No. | Type Digital | Type Analog | Pin Name | Description |
|---|---|---|---|---|
| 1 | IO | I | P0[7] | Analog column mux input. |
| 2 | IO | IO | P0[5] | Analog column mux input and column output. |
| 3 | IO | IO | P0[3] | Analog column mux input and column output. |
| 4 | IO | I | P0[1] | Analog column mux input. |
| 5 | IO | | P2[7] | |
| 6 | IO | | P2[5] | |
| 7 | IO | I | P2[3] | Direct switched capacitor block input. |
| 8 | IO | I | P2[1] | Direct switched capacitor block input. |
| 9 | IO | | P4[7] | |
| 10 | IO | | P4[5] | |
| 11 | IO | | P4[3] | |
| 12 | IO | | P4[1] | |
| 13 | Power | | SMP | Switch Mode Pump (SMP) connection to external components required. |
| 14 | IO | | P3[7] | |
| 15 | IO | | P3[5] | |
| 16 | IO | | P3[3] | |
| 17 | IO | | P3[1] | |
| 18 | IO | | P5[3] | |
| 19 | IO | | P5[1] | |
| 20 | IO | | P1[7] | I2C Serial Clock (SCL). |
| 21 | IO | | P1[5] | I2C Serial Data (SDA). |
| 22 | IO | | P1[3] | |
| 23 | IO | | P1[1] | Crystal Input (XTALin), I2C Serial Clock (SCL), ISSP SCLK*. |
| 24 | Power | | Vss | Ground connection. |
| 25 | IO | | P1[0] | Crystal Output (XTALout), I2C Serial Data (SDA), ISSP SDATA.* |
| 26 | IO | | P1[2] | |
| 27 | IO | | P1[4] | Optional External Clock Input (EXTCLK). |
| 28 | IO | | P1[6] | |
| 29 | IO | | P5[0] | |
| 30 | IO | | P5[2] | |
| 31 | IO | | P3[0] | |
| 32 | IO | | P3[2] | |
| 33 | IO | | P3[4] | |
| 34 | IO | | P3[6] | |
| 35 | Input | | XRES | Active high external reset with internal pull down. |
| 36 | IO | | P4[0] | |
| 37 | IO | | P4[2] | |
| 38 | IO | | P4[4] | |
| 39 | IO | | P4[6] | |
| 39 | IO | | P4[6] | |
| 40 | IO | I | P2[0] | Direct switched capacitor block input. |
| 41 | IO | I | P2[2] | Direct switched capacitor block input. |
| 42 | IO | | P2[4] | External Analog Ground (AGND). |
| 43 | IO | | P2[6] | External Voltage Reference (VRef). |
| 44 | IO | I | P0[0] | Analog column mux input. |
| 45 | IO | IO | P0[2] | Analog column mux input and column output. |
| 46 | IO | IO | P0[4] | Analog column mux input and column output. |
| 47 | IO | I | P0[6] | Analog column mux input. |
| 48 | Power | | Vdd | Supply voltage. |

**LEGEND**: A = Analog, I = Input, and O = Output.
* These are the ISSP pins, which are not High Z at POR (Power On Reset).

Figure 4. 48-Pin Device



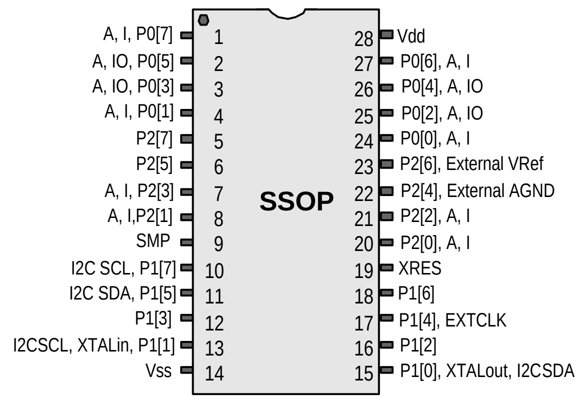
*28-Pin Part Pinout*

Table 4. 28-Pin Part Pinout (SSOP)

| Pin No. | Type | | Pin Name | Description |
|---|---|---|---|---|
| | **Digital** | **Analog** | | |
| 1 | IO | I | P0[7] | Analog column mux input. |
| 2 | IO | IO | P0[5] | Analog column mux input and column output. |
| 3 | IO | IO | P0[3] | Analog column mux input and column output. |
| 4 | IO | I | P0[1] | Analog column mux input. |
| 5 | IO | | P2[7] | |
| 6 | IO | | P2[5] | |
| 7 | IO | I | P2[3] | Direct switched capacitor block input. |
| 8 | IO | I | P2[1] | Direct switched capacitor block input. |
| 9 | Power | | SMP | Switch Mode Pump (SMP) connection to external components required. |
| 10 | IO | | P1[7] | I2C Serial Clock (SCL). |
| 11 | IO | | P1[5] | I2C Serial Data (SDA). |
| 12 | IO | | P1[3] | |
| 13 | IO | | P1[1] | Crystal Input (XTALin), I2C Serial Clock (SCL), ISSP-SCLK*. |
| 14 | Power | | Vss | Ground connection. |
| 15 | IO | | P1[0] | Crystal Output (XTALout), I2C Serial Data (SDA), ISSP-SDATA*. |
| 16 | IO | | P1[2] | |
| 17 | IO | | P1[4] | Optional External Clock Input (EXTCLK). |
| 18 | IO | | P1[6] | |
| 19 | Input | | XRES | Active high external reset with internal pull down. |
| 20 | IO | I | P2[0] | Direct switched capacitor block input. |
| 21 | IO | I | P2[2] | Direct switched capacitor block input. |
| 22 | IO | | P2[4] | External Analog Ground (AGND). |
| 23 | IO | | P2[6] | External Voltage Reference (VRef). |
| 24 | IO | I | P0[0] | Analog column mux input. |
| 25 | IO | IO | P0[2] | Analog column mux input and column output. |
| 26 | IO | IO | P0[4] | Analog column mux input and column output. |
| 27 | IO | I | P0[6] | Analog column mux input. |
| 28 | Power | | Vdd | Supply voltage. |

**LEGEND**: A = Analog, I = Input, and O = Output.
* These are the ISSP pins, which are not High Z at POR (Power On Reset).

Figure 6. 28-Pin Device



## Register Reference

This chapter lists the registers of the CY8CLED08 EZ-Color device.

### Register Conventions

The register conventions specific to this section are listed in the following table.  Register Mapping Tables

| Convention | Description |
|---|---|
| R | Read register or bit(s) |
| W | Write register or bit(s) |
| L | Logical register or bit(s) |
| C | Clearable register or bit(s) |
| # | Access is bit specific |

### Register Mapping Tables

The device has a total register address space of 512 bytes. The register space is referred to as IO space and is divided into two banks. The XOI bit in the Flag register (CPU_F) determines which bank the user is currently in. When the XOI bit is set the user is in Bank 1.

**Note**  In the following register mapping tables, blank fields are reserved and should not be accessed.

Table 5. Register Map Bank 0 Table: User Space

| Name | Addr (0,Hex) | Access | Name | Addr (0,Hex) | Access | Name | Addr (0,Hex) | Access | Name | Addr (0,Hex) | Access |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PRT0DR | 00 | RW | | 40 | | ASC10CR0 | 80 | RW | | C0 | |
| PRT0IE | 01 | RW | | 41 | | ASC10CR1 | 81 | RW | | C1 | |
| PRT0GS | 02 | RW | | 42 | | ASC10CR2 | 82 | RW | | C2 | |
| PRT0DM2 | 03 | RW | | 43 | | ASC10CR3 | 83 | RW | | C3 | |
| PRT1DR | 04 | RW | | 44 | | ASD11CR0 | 84 | RW | | C4 | |
| PRT1IE | 05 | RW | | 45 | | ASD11CR1 | 85 | RW | | C5 | |
| PRT1GS | 06 | RW | | 46 | | ASD11CR2 | 86 | RW | | C6 | |
| PRT1DM2 | 07 | RW | | 47 | | ASD11CR3 | 87 | RW | | C7 | |
| PRT2DR | 08 | RW | | 48 | | ASC12CR0 | 88 | RW | | C8 | |
| PRT2IE | 09 | RW | | 49 | | ASC12CR1 | 89 | RW | | C9 | |
| PRT2GS | 0A | RW | | 4A | | ASC12CR2 | 8A | RW | | CA | |
| PRT2DM2 | 0B | RW | | 4B | | ASC12CR3 | 8B | RW | | CB | |
| PRT3DR | 0C | RW | | 4C | | ASD13CR0 | 8C | RW | | CC | |
| PRT3IE | 0D | RW | | 4D | | ASD13CR1 | 8D | RW | | CD | |
| PRT3GS | 0E | RW | | 4E | | ASD13CR2 | 8E | RW | | CE | |
| PRT3DM2 | 0F | RW | | 4F | | ASD13CR3 | 8F | RW | | CF | |
| PRT4DR | 10 | RW | | 50 | | ASD20CR0 | 90 | RW | | D0 | |
| PRT4IE | 11 | RW | | 51 | | ASD20CR1 | 91 | RW | | D1 | |
| PRT4GS | 12 | RW | | 52 | | ASD20CR2 | 92 | RW | | D2 | |
| PRT4DM2 | 13 | RW | | 53 | | ASD20CR3 | 93 | RW | | D3 | |
| PRT5DR | 14 | RW | | 54 | | ASC21CR0 | 94 | RW | | D4 | |
| PRT5IE | 15 | RW | | 55 | | ASC21CR1 | 95 | RW | | D5 | |
| PRT5GS | 16 | RW | | 56 | | ASC21CR2 | 96 | RW | I2C_CFG | D6 | RW |
| PRT5DM2 | 17 | RW | | 57 | | ASC21CR3 | 97 | RW | I2C_SCR | D7 | # |
| | 18 | | | 58 | | ASD22CR0 | 98 | RW | I2C_DR | D8 | RW |
| | 19 | | | 59 | | ASD22CR1 | 99 | RW | I2C_MSCR | D9 | # |
| | 1A | | | 5A | | ASD22CR2 | 9A | RW | INT_CLR0 | DA | RW |
| | 1B | | | 5B | | ASD22CR3 | 9B | RW | INT_CLR1 | DB | RW |
| | 1C | | | 5C | | ASC23CR0 | 9C | RW | | DC | |
| | 1D | | | 5D | | ASC23CR1 | 9D | RW | INT_CLR3 | DD | RW |
| | 1E | | | 5E | | ASC23CR2 | 9E | RW | INT_MSK3 | DE | RW |
| | 1F | | | 5F | | ASC23CR3 | 9F | RW | | DF | |
| DBB00DR0 | 20 | # | AMX_IN | 60 | RW | | A0 | | INT_MSK0 | E0 | RW |
| DBB00DR1 | 21 | W | | 61 | | | A1 | | INT_MSK1 | E1 | RW |
| DBB00DR2 | 22 | RW | | 62 | | | A2 | | INT_VC | E2 | RC |
| DBB00CR0 | 23 | # | ARF_CR | 63 | RW | | A3 | | RES_WDT | E3 | W |
| DBB01DR0 | 24 | # | CMP_CR0 | 64 | # | | A4 | | DEC_DH | E4 | RC |
| DBB01DR1 | 25 | W | ASY_CR | 65 | # | | A5 | | DEC_DL | E5 | RC |
| DBB01DR2 | 26 | RW | CMP_CR1 | 66 | RW | | A6 | | DEC_CR0 | E6 | RW |
| DBB01CR0 | 27 | # | | 67 | | | A7 | | DEC_CR1 | E7 | RW |
| DCB02DR0 | 28 | # | | 68 | | | A8 | | MUL_X | E8 | W |
| DCB02DR1 | 29 | W | | 69 | | | A9 | | MUL_Y | E9 | W |
| DCB02DR2 | 2A | RW | | 6A | | | AA | | MUL_DH | EA | R |
| DCB02CR0 | 2B | # | | 6B | | | AB | | MUL_DL | EB | R |
| DCB03DR0 | 2C | # | | 6C | | | AC | | ACC_DR1 | EC | RW |
| DCB03DR1 | 2D | W | | 6D | | | AD | | ACC_DR0 | ED | RW |
| DCB03DR2 | 2E | RW | | 6E | | | AE | | ACC_DR3 | EE | RW |
| DCB03CR0 | 2F | # | | 6F | | | AF | | ACC_DR2 | EF | RW |
| DBB10DR0 | 30 | # | ACB00CR3 | 70 | RW | RDI0RI | B0 | RW | | F0 | |
| DBB10DR1 | 31 | W | ACB00CR0 | 71 | RW | RDI0SYN | B1 | RW | | F1 | |
| DBB10DR2 | 32 | RW | ACB00CR1 | 72 | RW | RDI0IS | B2 | RW | | F2 | |
| DBB10CR0 | 33 | # | ACB00CR2 | 73 | RW | RDI0LT0 | B3 | RW | | F3 | |
| DBB11DR0 | 34 | # | ACB01CR3 | 74 | RW | RDI0LT1 | B4 | RW | | F4 | |
| DBB11DR1 | 35 | W | ACB01CR0 | 75 | RW | RDI0RO0 | B5 | RW | | F5 | |
| DBB11DR2 | 36 | RW | ACB01CR1 | 76 | RW | RDI0RO1 | B6 | RW | | F6 | |
| DBB11CR0 | 37 | # | ACB01CR2 | 77 | RW | | B7 | | CPU_F | F7 | RL |
| DCB12DR0 | 38 | # | ACB02CR3 | 78 | RW | RDI1RI | B8 | RW | | F8 | |
| DCB12DR1 | 39 | W | ACB02CR0 | 79 | RW | RDI1SYN | B9 | RW | | F9 | |
| DCB12DR2 | 3A | RW | ACB02CR1 | 7A | RW | RDI1IS | BA | RW | | FA | |
| DCB12CR0 | 3B | # | ACB02CR2 | 7B | RW | RDI1LT0 | BB | RW | | FB | |
| DCB13DR0 | 3C | # | ACB03CR3 | 7C | RW | RDI1LT1 | BC | RW | | FC | |
| DCB13DR1 | 3D | W | ACB03CR0 | 7D | RW | RDI1RO0 | BD | RW | | FD | |
| DCB13DR2 | 3E | RW | ACB03CR1 | 7E | RW | RDI1RO1 | BE | RW | CPU_SCR1 | FE | # |
| DCB13CR0 | 3F | # | ACB03CR2 | 7F | RW | | BF | | CPU_SCR0 | FF | # |

**Blank fields are Reserved and should not be accessed.** # Access is bit specific.

Table 6. Register Map Bank 1 Table: Configuration Space

| Name | Add (1,Hex) | Access | Name | Addr (1,Hex) | Access | Name | Addr (1,Hex) | Access | Name | Addr (1,Hex) | Access |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PRT0DM0 | 00 | RW | | 40 | | ASC10CR0 | 80 | RW | | C0 | |
| PRT0DM1 | 01 | RW | | 41 | | ASC10CR1 | 81 | RW | | C1 | |
| PRT0IC0 | 02 | RW | | 42 | | ASC10CR2 | 82 | RW | | C2 | |
| PRT0IC1 | 03 | RW | | 43 | | ASC10CR3 | 83 | RW | | C3 | |
| PRT1DM0 | 04 | RW | | 44 | | ASD11CR0 | 84 | RW | | C4 | |
| PRT1DM1 | 05 | RW | | 45 | | ASD11CR1 | 85 | RW | | C5 | |
| PRT1IC0 | 06 | RW | | 46 | | ASD11CR2 | 86 | RW | | C6 | |
| PRT1IC1 | 07 | RW | | 47 | | ASD11CR3 | 87 | RW | | C7 | |
| PRT2DM0 | 08 | RW | | 48 | | ASC12CR0 | 88 | RW | | C8 | |
| PRT2DM1 | 09 | RW | | 49 | | ASC12CR1 | 89 | RW | | C9 | |
| PRT2IC0 | 0A | RW | | 4A | | ASC12CR2 | 8A | RW | | CA | |
| PRT2IC1 | 0B | RW | | 4B | | ASC12CR3 | 8B | RW | | CB | |
| PRT3DM0 | 0C | RW | | 4C | | ASD13CR0 | 8C | RW | | CC | |
| PRT3DM1 | 0D | RW | | 4D | | ASD13CR1 | 8D | RW | | CD | |
| PRT3IC0 | 0E | RW | | 4E | | ASD13CR2 | 8E | RW | | CE | |
| PRT3IC1 | 0F | RW | | 4F | | ASD13CR3 | 8F | RW | | CF | |
| PRT4DM0 | 10 | RW | | 50 | | ASD20CR0 | 90 | RW | GDI_O_IN | D0 | RW |
| PRT4DM1 | 11 | RW | | 51 | | ASD20CR1 | 91 | RW | GDI_E_IN | D1 | RW |
| PRT4IC0 | 12 | RW | | 52 | | ASD20CR2 | 92 | RW | GDI_O_OU | D2 | RW |
| PRT4IC1 | 13 | RW | | 53 | | ASD20CR3 | 93 | RW | GDI_E_OU | D3 | RW |
| PRT5DM0 | 14 | RW | | 54 | | ASC21CR0 | 94 | RW | | D4 | |
| PRT5DM1 | 15 | RW | | 55 | | ASC21CR1 | 95 | RW | | D5 | |
| PRT5IC0 | 16 | RW | | 56 | | ASC21CR2 | 96 | RW | | D6 | |
| PRT5IC1 | 17 | RW | | 57 | | ASC21CR3 | 97 | RW | | D7 | |
| | 18 | | | 58 | | ASD22CR0 | 98 | RW | | D8 | |
| | 19 | | | 59 | | ASD22CR1 | 99 | RW | | D9 | |
| | 1A | | | 5A | | ASD22CR2 | 9A | RW | | DA | |
| | 1B | | | 5B | | ASD22CR3 | 9B | RW | | DB | |
| | 1C | | | 5C | | ASC23CR0 | 9C | RW | | DC | |
| | 1D | | | 5D | | ASC23CR1 | 9D | RW | OSC_GO_EN | DD | RW |
| | 1E | | | 5E | | ASC23CR2 | 9E | RW | OSC_CR4 | DE | RW |
| | 1F | | | 5F | | ASC23CR3 | 9F | RW | OSC_CR3 | DF | RW |
| DBB00FN | 20 | RW | CLK_CR0 | 60 | RW | | A0 | | OSC_CR0 | E0 | RW |
| DBB00IN | 21 | RW | CLK_CR1 | 61 | RW | | A1 | | OSC_CR1 | E1 | RW |
| DBB00OU | 22 | RW | ABF_CR0 | 62 | RW | | A2 | | OSC_CR2 | E2 | RW |
| | 23 | | AMD_CR0 | 63 | RW | | A3 | | VLT_CR | E3 | RW |
| DBB01FN | 24 | RW | | 64 | | | A4 | | VLT_CMP | E4 | R |
| DBB01IN | 25 | RW | | 65 | | | A5 | | | E5 | |
| DBB01OU | 26 | RW | AMD_CR1 | 66 | RW | | A6 | | | E6 | |
| | 27 | | ALT_CR0 | 67 | RW | | A7 | | | E7 | |
| DCB02FN | 28 | RW | ALT_CR1 | 68 | RW | | A8 | | IMO_TR | E8 | W |
| DCB02IN | 29 | RW | CLK_CR2 | 69 | RW | | A9 | | ILO_TR | E9 | W |
| DCB02OU | 2A | RW | | 6A | | | AA | | BDG_TR | EA | RW |
| | 2B | | | 6B | | | AB | | ECO_TR | EB | W |
| DCB03FN | 2C | RW | | 6C | | | AC | | | EC | |
| DCB03IN | 2D | RW | | 6D | | | AD | | | ED | |
| DCB03OU | 2E | RW | | 6E | | | AE | | | EE | |
| | 2F | | | 6F | | | AF | | | EF | |
| DBB10FN | 30 | RW | ACB00CR3 | 70 | RW | RDI0RI | B0 | RW | | F0 | |
| DBB10IN | 31 | RW | ACB00CR0 | 71 | RW | RDI0SYN | B1 | RW | | F1 | |
| DBB10OU | 32 | RW | ACB00CR1 | 72 | RW | RDI0IS | B2 | RW | | F2 | |
| | 33 | | ACB00CR2 | 73 | RW | RDI0LT0 | B3 | RW | | F3 | |
| DBB11FN | 34 | RW | ACB01CR3 | 74 | RW | RDI0LT1 | B4 | RW | | F4 | |
| DBB11IN | 35 | RW | ACB01CR0 | 75 | RW | RDI0RO0 | B5 | RW | | F5 | |
| DBB11OU | 36 | RW | ACB01CR1 | 76 | RW | RDI0RO1 | B6 | RW | | F6 | |
| | 37 | | ACB01CR2 | 77 | RW | | B7 | | CPU_F | F7 | RL |
| DCB12FN | 38 | RW | ACB02CR3 | 78 | RW | RDI1RI | B8 | RW | | F8 | |
| DCB12IN | 39 | RW | ACB02CR0 | 79 | RW | RDI1SYN | B9 | RW | | F9 | |
| DCB12OU | 3A | RW | ACB02CR1 | 7A | RW | RDI1IS | BA | RW | | FA | |
| | 3B | | ACB02CR2 | 7B | RW | RDI1LT0 | BB | RW | | FB | |
| DCB13FN | 3C | RW | ACB03CR3 | 7C | RW | RDI1LT1 | BC | RW | | FC | |
| DCB13IN | 3D | RW | ACB03CR0 | 7D | RW | RDI1RO0 | BD | RW | | FD | |
| DCB13OU | 3E | RW | ACB03CR1 | 7E | RW | RDI1RO1 | BE | RW | CPU_SCR1 | FE | # |
| | 3F | | ACB03CR2 | 7F | RW | | BF | | CPU_SCR0 | FF | # |

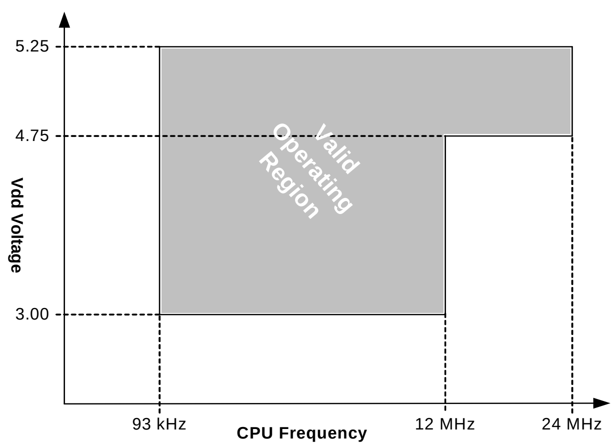
**Blank fields are Reserved and should not be accessed.** # Access is bit specific.

## Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8CLED08 EZ-Color device. For the most up to date electrical specifications, confirm that you have the most recent data sheet by going to the web at http://www.cypress.com/ez-color.

Specifications are valid for $-40^oC \le T_A \le 85^oC$ and $T_J \le 100^oC$, except where noted. Specifications for devices running at greater than 12 MHz are valid for $-40^oC \le T_A \le 70^oC$ and $T_J \le 82^oC$.

Figure 7. Voltage versus CPU Frequency




The following table lists the units of measure that are used in this section.

Table 7. Units of Measure

| Symbol | Unit of Measure | Symbol | Unit of Measure |
|---|---|---|---|
| $^oC$ | degree Celsius | µW | microwatts |
| dB | decibels | mA | milli-ampere |
| fF | femto farad | ms | milli-second |
| Hz | hertz | mV | milli-volts |
| KB | 1024 bytes | nA | nanoampere |
| Kbit | 1024 bits | ns | nanosecond |
| kHz | kilohertz | nV | nanovolts |
| kΩ | kilohm | Ω | ohm |
| MHz | megahertz | pA | picoampere |
| MΩ | megaohm | pF | picofarad |
| µA | microampere | pp | peak-to-peak |
| µF | microfarad | ppm | parts per million |
| µH | microhenry | ps | picosecond |
| µs | microsecond | sps | samples per second |
| µV | microvolts | σ | sigma: one standard deviation |
| µVrms | microvolts root-mean-square | V | volts |

### Absolute Maximum Ratings

Table 8. Absolute Maximum Ratings

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $T_{STG}$ | Storage Temperature | -55 | 25 | +100 | $^oC$ | Higher storage temperatures will reduce data retention time. Recommended storage temperature is $+25^oC \pm 25^oC$. Extended duration storage temperatures above $65^oC$ will degrade reliability. |
| $T_A$ | Ambient Temperature with Power Applied | -40 | – | +85 | $^oC$ | |
| Vdd | Supply Voltage on Vdd Relative to Vss | -0.5 | – | +6.0 | V | |
| $V_{IO}$ | DC Input Voltage | Vss- 0.5 | – | Vdd + 0.5 | V | |
| $V_{IOZ}$ | DC Voltage Applied to Tri-state | Vss - 0.5 | – | Vdd + 0.5 | V | |
| $I_{MIO}$ | Maximum Current into any Port Pin | -25 | – | +50 | mA | |
| $I_{MAIO}$ | Maximum Current into any Port Pin Configured as Analog Driver | -50 | – | +50 | mA | |
| ESD | Electro Static Discharge Voltage | 2000 | – | – | V | Human Body Model ESD. |
| LU | Latch-up Current | – | – | 200 | mA | |

## Operating Temperature

Table 9. Operating Temperature

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $T_A$ | Ambient Temperature | -40 | – | +85 | °C | |
| $T_J$ | Junction Temperature | -40 | – | +100 | °C | The temperature rise from ambient to junction is package specific. See "Thermal Impedances" on page 36. The user must limit the power consumption to comply with this requirement. |

## DC Electrical Characteristics

### *DC Chip-Level Specifications*

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ $T_A$ ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ $T_A$ ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 10. DC Chip-Level Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| Vdd | Supply Voltage | 3.00 | – | 5.25 | V | |
| $I_{DD}$ | Supply Current | – | 5 | 8 | mA | Conditions are Vdd = 5.0V, $T_A$ = 25 °C, CPU = 3 MHz, SYSCLK doubler disabled. VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 93.75 kHz. |
| $I_{DD3}$ | Supply Current | – | 3.3 | 6.0 | mA | Conditions are Vdd = 3.3V, $T_A$ = 25 °C, CPU = 3 MHz, SYSCLK doubler disabled. VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 93.75 kHz. |
| $I_{SB}$ | Sleep (Mode) Current with POR, LVD, Sleep Timer, and WDT.[a] | – | 3 | 6.5 | µA | Conditions are with internal slow speed oscillator, Vdd = 3.3V, -40 °C ≤ $T_A$ ≤ 55 °C. |
| $I_{SBH}$ | Sleep (Mode) Current with POR, LVD, Sleep Timer, and WDT at high temperature.[a] | – | 4 | 25 | µA | Conditions are with internal slow speed oscillator, Vdd = 3.3V, 55 °C < $T_A$ ≤ 85 °C. |
| $I_{SBXTL}$ | Sleep (Mode) Current with POR, LVD, Sleep Timer, WDT, and external crystal.[a] | – | 4 | 7.5 | µA | Conditions are with properly loaded, 1 µW max, 32.768 kHz crystal. Vdd = 3.3V, -40 °C ≤ $T_A$ ≤ 55 °C. |
| $I_{SBXTLH}$ | Sleep (Mode) Current with POR, LVD, Sleep Timer, WDT, and external crystal at high temperature.[a] | – | 5 | 26 | µA | Conditions are with properly loaded, 1 µW max, 32.768 kHz crystal. Vdd = 3.3V, 55 °C < $T_A$ ≤ 85 °C. |
| $V_{REF}$ | Reference Voltage (Bandgap) for Silicon A [b] | 1.275 | 1.300 | 1.325 | V | Trimmed for appropriate Vdd. |
| $V_{REF}$ | Reference Voltage (Bandgap) for Silicon B [b] | 1.280 | 1.300 | 1.320 | V | Trimmed for appropriate Vdd. |

a. Standby current includes all functions (POR, LVD, WDT, Sleep Time) needed for reliable system operation. This should be compared with devices that have similar functions enabled.

b. Refer to the "Ordering Information" on page 38.

*DC General Purpose IO Specifications*

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ $T_A$ ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ $T_A$ ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 11. DC GPIO Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $R_{PU}$ | Pull up Resistor | 4 | 5.6 | 8 | kΩ | |
| $R_{PD}$ | Pull down Resistor | 4 | 5.6 | 8 | kΩ | |
| $V_{OH}$ | High Output Level | Vdd - 1.0 | – | – | V | IOH = 10 mA, Vdd = 4.75 to 5.25V (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5])). |
| $V_{OL}$ | Low Output Level | – | – | 0.75 | V | IOL = 25 mA, Vdd = 4.75 to 5.25V (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5])). |
| $V_{IL}$ | Input Low Level | – | – | 0.8 | V | Vdd = 3.0 to 5.25. |
| $V_{IH}$ | Input High Level | 2.1 | – | | V | Vdd = 3.0 to 5.25. |
| $V_H$ | Input Hysterisis | – | 60 | – | mV | |
| $I_{IL}$ | Input Leakage (Absolute Value) | – | 1 | – | nA | Gross tested to 1 μA. |
| $C_{IN}$ | Capacitive Load on Pins as Input | – | 3.5 | 10 | pF | Package and pin dependent. Temp = 25$^o$C. |
| $C_{OUT}$ | Capacitive Load on Pins as Output | – | 3.5 | 10 | pF | Package and pin dependent. Temp = 25$^o$C. |

*DC Operational Amplifier Specifications*

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ $T_A$ ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ $T_A$ ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

The Operational Amplifier is a component of both the Analog Continuous Time PSoC blocks and the Analog Switched Cap PSoC blocks. The guaranteed specifications are measured in the Analog Continuous Time PSoC block. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 12. 5V DC Operational Amplifier Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $V_{OSOA}$ | Input Offset Voltage (absolute value) | | | | | |
| | Power = Low, Opamp Bias = High | – | 1.6 | 10 | mV | |
| | Power = Medium, Opamp Bias = High | – | 1.3 | 8 | mV | |
| | Power = High, Opamp Bias = High | – | 1.2 | 7.5 | mV | |
| $TCV_{OSOA}$ | Average Input Offset Voltage Drift | – | 7.0 | 35.0 | μV/$^o$C | |
| $I_{EBOA}$ | Input Leakage Current (Port 0 Analog Pins) | – | 20 | – | pA | Gross tested to 1 μA. |
| $C_{INOA}$ | Input Capacitance (Port 0 Analog Pins) | – | 4.5 | 9.5 | pF | Package and pin dependent. Temp = 25$^o$C. |
| $V_{CMOA}$ | Common Mode Voltage Range | 0.0 | – | Vdd | V | The common-mode input voltage range is measured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer. |
| | Common Mode Voltage Range (high power or high opamp bias) | 0.5 | – | Vdd - 0.5 | | |
| $CMRR_{OA}$ | Common Mode Rejection Ratio | | – | – | dB | Specification is applicable at high power. For all other bias modes (except high power, high opamp bias), minimum is 60 dB. |
| | Power = Low | 60 | | | | |
| | Power = Medium | 60 | | | | |
| | Power = High | 60 | | | | |
| $G_{OLOA}$ | Open Loop Gain | | – | – | dB | Specification is applicable at high power. For all other bias modes (except high power, high opamp bias), minimum is 60 dB. |
| | Power = Low | 60 | | | | |
| | Power = Medium | 60 | | | | |
| | Power = High | 80 | | | | |
| $V_{OHIGHOA}$ | High Output Voltage Swing (internal signals) | | | | | |
| | Power = Low | Vdd - 0.2 | – | – | V | |
| | Power = Medium | Vdd - 0.2 | – | – | V | |
| | Power = High | Vdd - 0.5 | – | – | V | |

*DC Low Power Comparator Specifications*

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ $T_A$ ≤ 85°C, 3.0V to 3.6V and -40°C ≤ $T_A$ ≤ 85°C, or 2.4V to 3.0V and -40°C ≤ $T_A$ ≤ 85°C, respectively. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 14.  DC Low Power Comparator Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $V_{REFLPC}$ | Low power comparator (LPC) reference voltage range | 0.2 | – | Vdd - 1 | V | |
| $I_{SLPC}$ | LPC supply current | – | 10 | 40 | μA | |
| $V_{OSLPC}$ | LPC voltage offset | – | 2.5 | 30 | mV | |

*DC Analog Output Buffer Specifications*

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ $T_A$ ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ $T_A$ ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 15.  5V DC Analog Output Buffer Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $V_{OSOB}$ | Input Offset Voltage (Absolute Value) | – | 3 | 12 | mV | |
| $TCV_{OSOB}$ | Average Input Offset Voltage Drift | – | +6 | – | μV/°C | |
| $V_{CMOB}$ | Common-Mode Input Voltage Range | 0.5 | – | Vdd - 1.0 | V | |
| $R_{OUTOB}$ | Output Resistance<br>Power = Low<br>Power = High | <br>–<br>– | <br>1<br>1 | <br>–<br>– | <br>Ω<br>Ω | |
| $V_{OHIGHOB}$ | High Output Voltage Swing (Load = 32 ohms to Vdd/2)<br>Power = Low<br>Power = High | 0.5 x Vdd + 1.3<br>0.5 x Vdd + 1.3 | –<br>– | –<br>– | V<br>V | |
| $V_{OLOWOB}$ | Low Output Voltage Swing (Load = 32 ohms to Vdd/2)<br>Power = Low<br>Power = High | –<br>– | –<br>– | 0.5 x Vdd - 1.3<br>0.5 x Vdd - 1.3 | V<br>V | |
| $I_{SOB}$ | Supply Current Including Bias Cell (No Load)<br>Power = Low<br>Power = High | –<br>– | 1.1<br>2.6 | 5.1<br>8.8 | mA<br>mA | |
| $PSRR_{OB}$ | Supply Voltage Rejection Ratio | 60 | 64 | – | dB | |

*DC Programming Specifications*

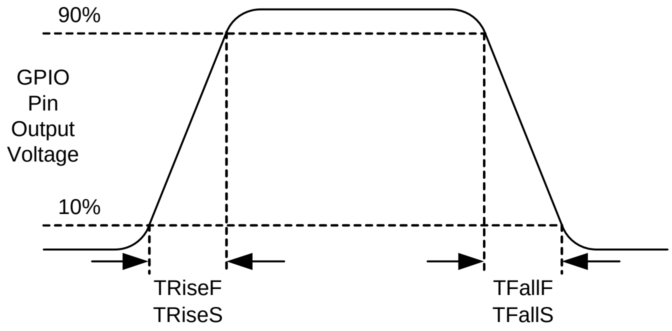
The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ $T_A$ ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ $T_A$ ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 22. DC Programming Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $I_{DDP}$ | Supply Current During Programming or Verify | – | 5 | 25 | mA | |
| $V_{ILP}$ | Input Low Voltage During Programming or Verify | – | – | 0.8 | V | |
| $V_{IHP}$ | Input High Voltage During Programming or Verify | 2.2 | – | – | V | |
| $I_{ILP}$ | Input Current when Applying Vilp to P1[0] or P1[1] During Programming or Verify | – | – | 0.2 | mA | Driving internal pull-down resistor. |
| $I_{IHP}$ | Input Current when Applying Vihp to P1[0] or P1[1] During Programming or Verify | – | – | 1.5 | mA | Driving internal pull-down resistor. |
| $V_{OLV}$ | Output Low Voltage During Programming or Verify | – | – | Vss + 0.75 | V | |
| $V_{OHV}$ | Output High Voltage During Programming or Verify | Vdd - 1.0 | – | Vdd | V | |
| $Flash_{ENPB}$ | Flash Endurance (per block) | 50,000 | – | – | – | Erase/write cycles per block. |
| $Flash_{ENT}$ | Flash Endurance (total)[a] | 1,800,000 | – | – | – | Erase/write cycles. |
| $Flash_{DR}$ | Flash Data Retention | 10 | – | – | Years | |

a. A maximum of 36 x 50,000 block endurance cycles is allowed. This may be balanced between operations on 36x1 blocks of 50,000 maximum cycles each, 36x2 blocks of 25,000 maximum cycles each, or 36x4 blocks of 12,500 maximum cycles each (to limit the total number of cycles to 36x50,000 and that no single block ever sees more than 50,000 cycles).
For the full industrial range, the user must employ a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. Refer to the Flash APIs Application Note AN2015 at http://www.cypress.com under Application Notes for more information.

Figure 14. GPIO Timing Diagram




*AC Operational Amplifier Specifications*

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ $T_A$ ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ $T_A$ ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only. Settling times, slew rates, and gain bandwidth are based on the Analog Continuous Time PSoC block.

Power = High and Opamp Bias = High is not supported at 3.3V.

Table 25. 5V AC Operational Amplifier Specifications

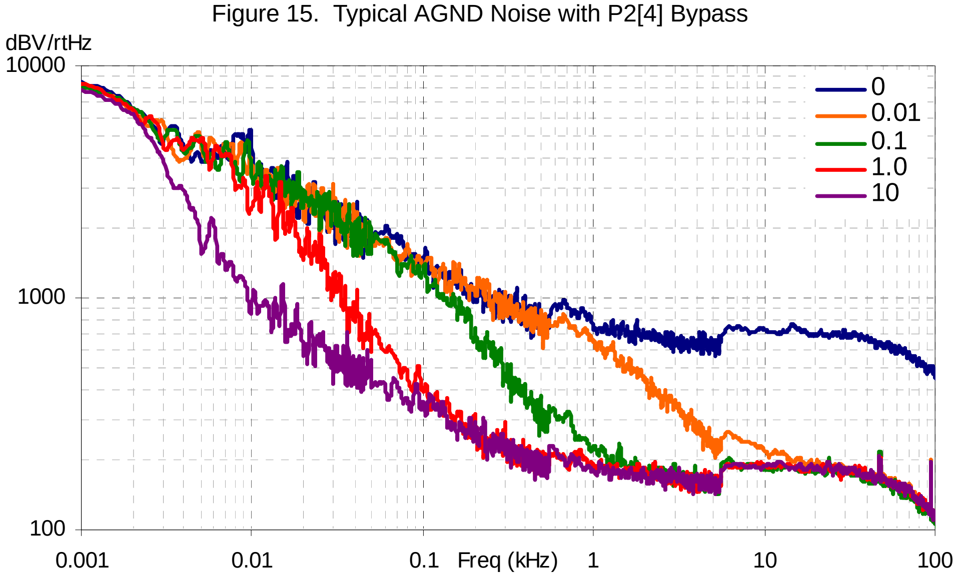
| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $T_{ROA}$ | Rising Settling Time from 80% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain) | | | | | |
| | Power = Low, Opamp Bias = Low | – | – | 3.9 | μs | |
| | Power = Medium, Opamp Bias = High | – | – | 0.72 | μs | |
| | Power = High, Opamp Bias = High | – | – | 0.62 | μs | |
| $T_{SOA}$ | Falling Settling Time from 20% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain) | | | | | |
| | Power = Low, Opamp Bias = Low | – | – | 5.9 | μs | |
| | Power = Medium, Opamp Bias = High | – | – | 0.92 | μs | |
| | Power = High, Opamp Bias = High | – | – | 0.72 | μs | |
| $SR_{ROA}$ | Rising Slew Rate (20% to 80%)(10 pF load, Unity Gain) | | | | | |
| | Power = Low, Opamp Bias = Low | 0.15 | – | – | V/μs | |
| | Power = Medium, Opamp Bias = High | 1.7 | – | – | V/μs | |
| | Power = High, Opamp Bias = High | 6.5 | – | – | V/μs | |
| $SR_{FOA}$ | Falling Slew Rate (20% to 80%)(10 pF load, Unity Gain) | | | | | |
| | Power = Low, Opamp Bias = Low | 0.01 | – | – | V/μs | |
| | Power = Medium, Opamp Bias = High | 0.5 | – | – | V/μs | |
| | Power = High, Opamp Bias = High | 4.0 | – | – | V/μs | |
| $BW_{OA}$ | Gain Bandwidth Product | | | | | |
| | Power = Low, Opamp Bias = Low | 0.75 | – | – | MHz | |
| | Power = Medium, Opamp Bias = High | 3.1 | – | – | MHz | |
| | Power = High, Opamp Bias = High | 5.4 | – | – | MHz | |
| $E_{NOA}$ | Noise at 1 kHz (Power = Medium, Opamp Bias = High) | – | 100 | – | nV/rt-Hz | |

Table 26. 3.3V AC Operational Amplifier Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $T_{ROA}$ | Rising Settling Time from 80% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain) | | | | | |
| | Power = Low, Opamp Bias = Low | – | – | 3.92 | μs | |
| | Power = Low, Opamp Bias = High | – | – | 0.72 | μs | |
| $T_{SOA}$ | Falling Settling Time from 20% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain) | | | | | |
| | Power = Low, Opamp Bias = Low | – | – | 5.41 | μs | |
| | Power = Medium, Opamp Bias = High | – | – | 0.72 | μs | |
| $SR_{ROA}$ | Rising Slew Rate (20% to 80%)(10 pF load, Unity Gain) | | | | | |
| | Power = Low, Opamp Bias = Low | 0.31 | – | – | V/μs | |
| | Power = Medium, Opamp Bias = High | 2.7 | – | – | V/μs | |
| $SR_{FOA}$ | Falling Slew Rate (20% to 80%)(10 pF load, Unity Gain) | | | | | |
| | Power = Low, Opamp Bias = Low | 0.24 | – | – | V/μs | |
| | Power = Medium, Opamp Bias = High | 1.8 | – | – | V/μs | |
| $BW_{OA}$ | Gain Bandwidth Product | | | | | |
| | Power = Low, Opamp Bias = Low | 0.67 | – | – | MHz | |
| | Power = Medium, Opamp Bias = High | 2.8 | – | – | MHz | |
| $E_{NOA}$ | Noise at 1 kHz (Power = Medium, Opamp Bias = High) | – | 100 | – | nV/rt-Hz | |

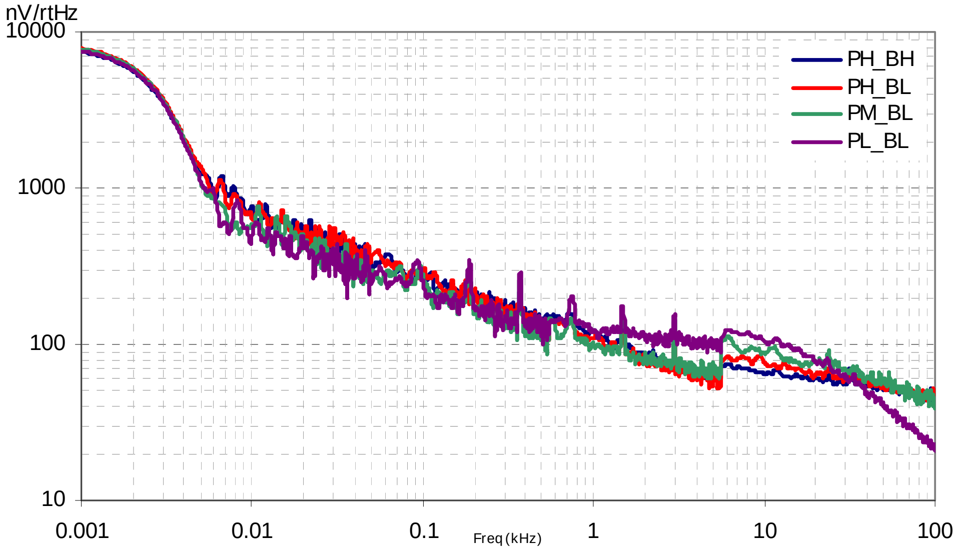
When bypassed by a capacitor on P2[4], the noise of the analog ground signal distributed to each block is reduced by a factor of up to 5 (14 dB). This is at frequencies above the corner frequency defined by the on-chip 8.1k resistance and the external capacitor.

Figure 15. Typical AGND Noise with P2[4] Bypass



At low frequencies, the opamp noise is proportional to 1/f, power independent, and determined by device geometry. At high frequencies, increased power level reduces the noise spectrum level.

Figure 16. Typical Opamp Noise




*AC Low Power Comparator Specifications*

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ $T_A$ ≤ 85°C, 3.0V to 3.6V and -40°C ≤ $T_A$ ≤ 85°C, or 2.4V to 3.0V and -40°C ≤ $T_A$ ≤ 85°C, respectively. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 27. AC Low Power Comparator Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $T_{RLPC}$ | LPC response time | – | – | 50 | µs | ≥ 50 mV overdrive comparator reference set within $V_{REFLPC}$. |



[+] Feedback

### AC External Clock Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ $T_A$ ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ $T_A$ ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 31. 5V AC External Clock Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $F_{OSCEXT}$ | Frequency | 0.093 | – | 24.6 | MHz | |
| – | High Period | 20.6 | – | 5300 | ns | |
| – | Low Period | 20.6 | – | – | ns | |
| – | Power Up IMO to Switch | 150 | – | – | μs | |

Table 32. 3.3V AC External Clock Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $F_{OSCEXT}$ | Frequency with CPU Clock divide by 1[a] | 0.093 | – | 12.3 | MHz | |
| $F_{OSCEXT}$ | Frequency with CPU Clock divide by 2 or greater[b] | 0.186 | – | 24.6 | MHz | |
| – | High Period with CPU Clock divide by 1 | 41.7 | – | 5300 | ns | |
| – | Low Period with CPU Clock divide by 1 | 41.7 | – | – | ns | |
| – | Power Up IMO to Switch | 150 | – | – | μs | |

a. Maximum CPU frequency is 12 MHz at 3.3V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements.

b. If the frequency of the external clock is greater than 12 MHz, the CPU clock divider must be set to 2 or greater. In this case, the CPU clock divider will ensure that the fifty percent duty cycle requirement is met.

### AC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ $T_A$ ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ $T_A$ ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 33. AC Programming Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $T_{RSCLK}$ | Rise Time of SCLK | 1 | – | 20 | ns | |
| $T_{FSCLK}$ | Fall Time of SCLK | 1 | – | 20 | ns | |
| $T_{SSCLK}$ | Data Set up Time to Falling Edge of SCLK | 40 | – | – | ns | |
| $T_{HSCLK}$ | Data Hold Time from Falling Edge of SCLK | 40 | – | – | ns | |
| $F_{SCLK}$ | Frequency of SCLK | 0 | – | 8 | MHz | |
| $T_{ERASEB}$ | Flash Erase Time (Block) | – | 10 | – | ms | |
| $T_{WRITE}$ | Flash Block Write Time | – | 10 | – | ms | |
| $T_{DSCLK}$ | Data Out Delay from Falling Edge of SCLK | – | – | 45 | ns | Vdd > 3.6 |
| $T_{DSCLK3}$ | Data Out Delay from Falling Edge of SCLK | – | – | 50 | ns | 3.0 ≤ Vdd ≤ 3.6 |

*AC I²C Specifications*

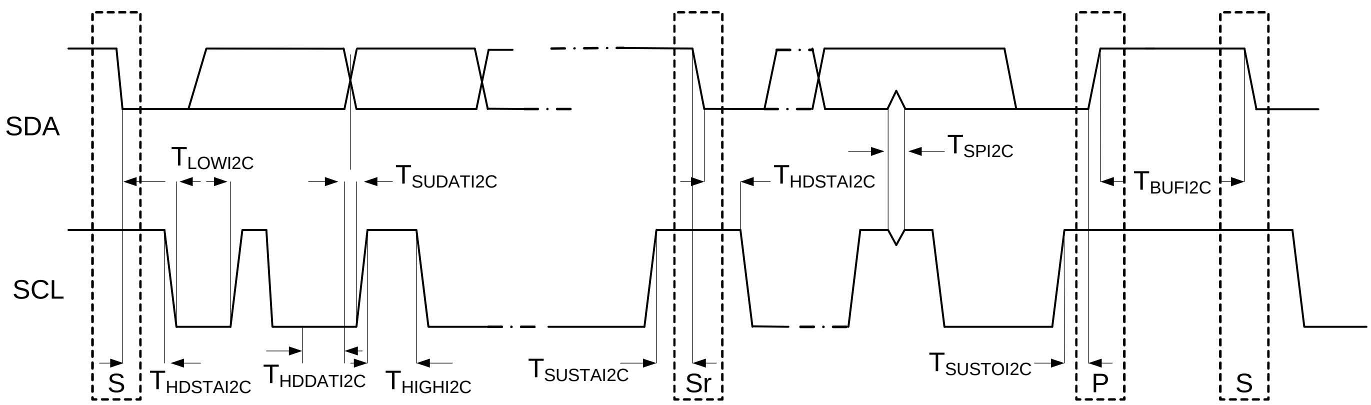
The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ $T_A$ ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ $T_A$ ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 34. AC Characteristics of the I²C SDA and SCL Pins

| Symbol | Description | Standard Mode | | Fast Mode | | Units | Notes |
|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | | |
| $F_{SCLI2C}$ | SCL Clock Frequency | 0 | 100 | 0 | 400 | kHz | |
| $T_{HDSTAI2C}$ | Hold Time (repeated) START Condition. After this period, the first clock pulse is generated. | 4.0 | – | 0.6 | – | µs | |
| $T_{LOWI2C}$ | LOW Period of the SCL Clock | 4.7 | – | 1.3 | – | µs | |
| $T_{HIGHI2C}$ | HIGH Period of the SCL Clock | 4.0 | – | 0.6 | – | µs | |
| $T_{SUSTAI2C}$ | Set-up Time for a Repeated START Condition | 4.7 | – | 0.6 | – | µs | |
| $T_{HDDATI2C}$ | Data Hold Time | 0 | – | 0 | – | µs | |
| $T_{SUDATI2C}$ | Data Set-up Time | 250 | – | 100[a] | – | ns | |
| $T_{SUSTOI2C}$ | Set-up Time for STOP Condition | 4.0 | – | 0.6 | – | µs | |
| $T_{BUFI2C}$ | Bus Free Time Between a STOP and START Condition | 4.7 | – | 1.3 | – | µs | |
| $T_{SPI2C}$ | Pulse Width of spikes are suppressed by the input filter. | – | – | 0 | 50 | ns | |

a. A Fast-Mode I2C-bus device can be used in a Standard-Mode I2C-bus system, but the requirement $t_{SU;DAT}$ ≥ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{rmax} + t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-Mode I2C-bus specification) before the SCL line is released.

Figure 17. Definition for Timing for Fast/Standard Mode on the I²C Bus



## Packaging Information

This section illustrates the packaging specifications for the CY8CLED08 EZ-Color device, along with the thermal impedances for each package and the typical package capacitance on crystal pins.

**Important Note** Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, refer to the document titled *PSoC Emulator Pod Dimensions* at http://www.cypress.com/design/MR10161.

### Packaging Dimensions

Figure 18. 48-Lead (300-Mil) SSOP

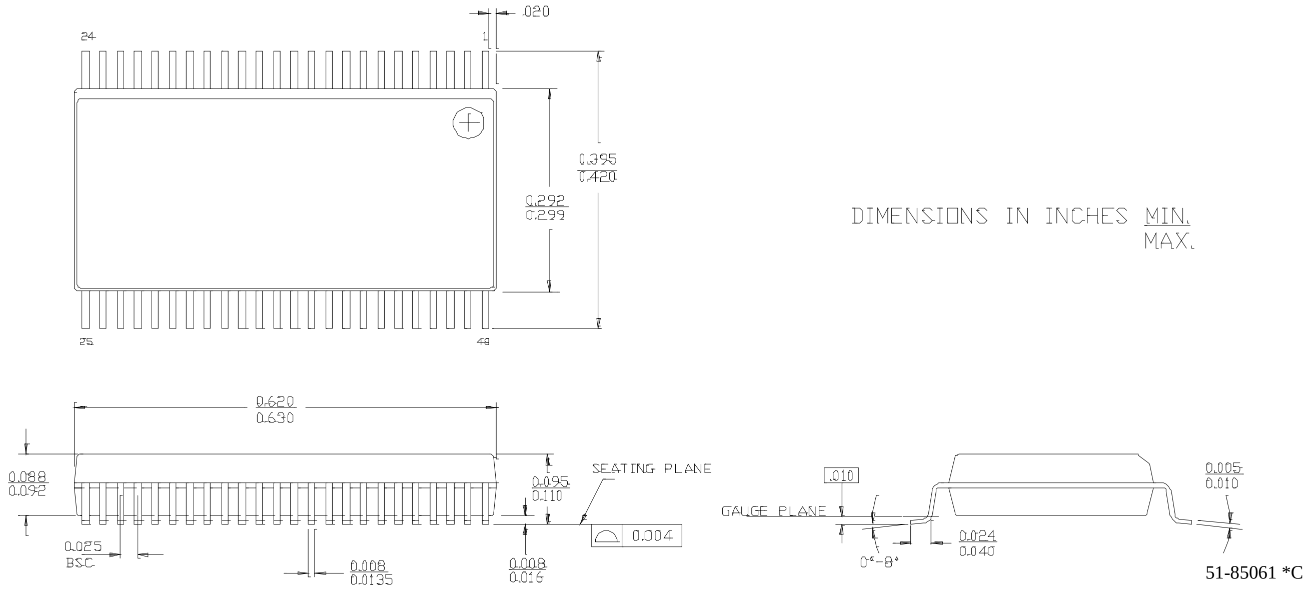
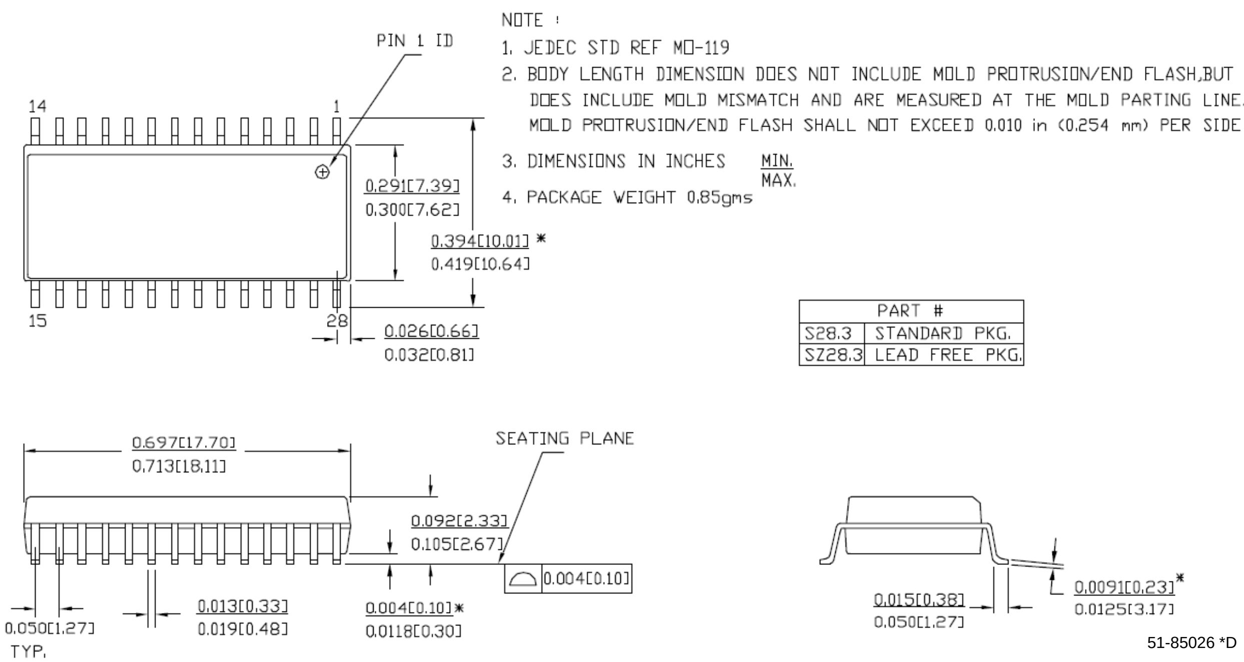


Figure 20. 28-Lead (210-Mil) SSOP




**Important Note** For information on the preferred dimensions for mounting QFN packages, see the following Application Note at http://www.amkor.com/products/notes_papers/MLFAppNote.pdf.

**Important Note** Pinned vias for thermal conduction are not required for the low-power device.

*PSoC Programmer*

Flexible enough to be used on the bench in development, yet suitable for factory programming, PSoC Programmer works either as a standalone programming application or it can operate directly from PSoC Designer or PSoC Express. PSoC Programmer software is compatible with both PSoC ICE-Cube In-Circuit Emulator and PSoC MiniProg. PSoC programmer is available free ofcharge at http://www.cypress.com/psocprogrammer.

*CY3202-C iMAGEcraft C Compiler*

CY3202 is the optional upgrade to PSoC Designer that enables the iMAGEcraft C compiler. It can be purchased from the Cypress Online Store. At http://www.cypress.com, click the Online Store shopping cart icon at the bottom of the web page, and click *PSoC (Programmable System-on-Chip)* to view a current list of available items.

## Evaluation Tools

All evaluation tools can be purchased from the Cypress Online Store.

*CY3261A-RGB EZ-Color RGB Kit*

The CY3261A-RGB board is a preprogrammed HB LED color mix board with seven pre-set colors using the CY8CLED16 EZ-Color HB LED Controller. The board is accompanied by a CD containing the color selector software application, PSoC Express 3.0 Beta 2, PSoC Programmer, and a suite of documents, schematics, and firmware examples. The color selector software application can be installed on a host PC and is used to control the EZ-Color HB LED controller using the included USB cable. The application enables you to select colors via a CIE 1931 chart or by entering coordinates. The kit includes:

- Training Board (CY8CLED16)
- One mini-A to mini-B USB Cable
- PSoC Express CD-ROM
- Design Files and Application Installation CD-ROM

To program and tune this kit via PSoC Express 3.0 you must use a Mini Programmer Unit (CY3217 Kit) and a CY3240-I2CUSB kit.

*CY3210-MiniProg1*

The CY3210-MiniProg1 kit allows a user to program PSoC devices via the MiniProg1 programming unit. The MiniProg is a small, compact prototyping programmer that connects to the PC via a provided USB 2.0 cable. The kit includes:

- MiniProg Programming Unit
- MiniEval Socket Programming and Evaluation Board
- 28-Pin CY8C29466-24PXI PDIP PSoC Device Sample
- 28-Pin CY8C27443-24PXI PDIP PSoC Device Sample
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

*CY3210-PSoCEval1*

The CY3210-PSoCEval1 kit features an evaluation board and the MiniProg1 programming unit. The evaluation board includes an LCD module, potentiometer, LEDs, and plenty of breadboarding space to meet all of your evaluation needs. The kit includes:

- Evaluation Board with LCD Module
- MiniProg Programming Unit
- 28-Pin CY8C29466-24PXI PDIP PSoC Device Sample (2)
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

## Device Programmers

All device programmers can be purchased from the Cypress Online Store.

*CY3216 Modular Programmer*

The CY3216 Modular Programmer kit features a modular programmer and the MiniProg1 programming unit. The modular programmer includes three programming module cards and supports multiple Cypress products. The kit includes:

- Modular Programmer Base
- 3 Programming Module Cards
- MiniProg Programming Unit
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

*CY3207ISSP In-System Serial Programmer (ISSP)*

The CY3207ISSP is a production programmer. It includes protection circuitry and an industrial case that is more robust than the MiniProg in a production-programming environment.
**Note**: CY3207ISSP needs special software and is not compatible with PSoC Programmer. The kit includes:

- CY3207 Programmer Unit
- PSoC ISSP Software CD
- 110 ~ 240V Power Supply, Euro-Plug Adapter
- USB 2.0 Cable