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#### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I <sup>2</sup> C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	24
Program Memory Size	28KB (16K × 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 17x10b; D/A 1x5b, 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f1718-e-so

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



## 3.4 Register Definitions: Status

U-0	U-0	U-0	R-1/q	R-1/q	R/W-0/u	R/W-0/u	R/W-0/u
_	_	_	TO	PD	Z	DC <sup>(1)</sup>	C <sup>(1)</sup>
bit 7						•	bit 0
Legend:							
R = Readabl	e bit	W = Writable	bit	U = Unimplei	mented bit, read	as '0'	
u = Bit is und	changed	x = Bit is unki	nown	-n/n = Value	at POR and BO	R/Value at all c	other Resets
'1' = Bit is se	t	'0' = Bit is cle	ared	q = Value de	pends on condit	ion	
bit 7-5	Unimplemen	ted: Read as '	0'				
bit 4	TO: Time-Ou	TO: Time-Out bit					
	1 = After power-up, CLRWDT instruction or SLEEP instruction						
	0 = A WDT T	ime-out occurr	ed				
bit 3	PD: Power-D	own bit					
	1 = After power-up or by the CLRWDT instruction						
bit 2	<b>Z</b> : Zero bit	<b>Z</b> : Zero bit					
	1 = The resul	t of an arithme	tic or loaic ope	eration is zero			
	0 = The resul	t of an arithme	tic or logic ope	eration is not z	ero		
bit 1	DC: Digit Car	DC: Digit Carry/Digit Borrow bit (ADDWF, ADDLW, SUBLW, SUBWF instructions) <sup>(1)</sup>					
	1 = A carry-out from the 4th low-order bit of the result occurred						
	0 = No carry-out from the 4th low-order bit of the result						
bit 0	C: Carry/Borrow bit <sup>(1)</sup> (ADDWF, ADDLW, SUBLW, SUBWF instructions) <sup>(1)</sup>						
	1 = A carry-o	ut from the Mo	st Significant I	oit of the result	occurred		
	0 = No carry-	out from the M	ost Significant	t bit of the resu	It occurred		
Note 1. E	or Dorrow the ne	larity in royara	od A qubtract	ion in overuter	h by adding the t	wo'o complom	ont of the

### REGISTER 3-1: STATUS: STATUS REGISTER

**Note 1:** For Borrow, the polarity is reversed. A subtraction is executed by adding the two's complement of the second operand.

## TABLE 3-3: PIC16(L)F1718 MEMORY MAP (BANKS 0-7)

	BANK 0		BANK 1		BANK 2		BANK 3		BANK 4		BANK 5		BANK 6		BANK 7
000h		080h		100h		180h		200h		280h		300h		380h	
	Core Registers		Core Registers		Core Registers		Core Registers		Core Registers		Core Registers		Core Registers		Core Registers
	(Table 3-2)		(Table 3-2)		(Table 3-2)		(Table 3-2)		(Table 3-2)		(Table 3-2)		(Table 3-2)		(Table 3-2)
00Bh		08Bh		10Bh		18Bh		20Bh		28Bh		30Bh		38Bh	
00Ch	PORTA	08Ch	TRISA	10Ch	LATA	18Ch	ANSELA	20Ch	WPUA	28Ch	ODCONA	30Ch	SLRCONA	38Ch	INLVLA
00Dh	PORTB	08Dh	TRISB	10Dh	LATB	18Dh	ANSELB	20Dh	WPUB	28Dh	ODCONB	30Dh	SLRCONB	38Dh	INLVLB
00Eh	PORTC	08Eh	TRISC	10Eh	LATC	18Eh	ANSELC	20Eh	WPUC	28Eh	ODCONC	30Eh	SLRCONC	38Eh	INLVLC
00Fh	—	08Fh	—	10Fh	_	18Fh	_	20Fh	—	28Fh	_	30Fh	—	38Fh	—
010h	PORTE	090h	TRISE	110h	—	190h	—	210h	WPUE	290h	—	310h	—	390h	INLVLE
011h	PIR1	091h	PIE1	111h	CM1CON0	191h	PMADRL	211h	SSP1BUF	291h	CCPR1L	311h	—	391h	IOCAP
012h	PIR2	092h	PIE2	112h	CM1CON1	192h	PMADRH	212h	SSP1ADD	292h	CCPR1H	312h	_	392h	IOCAN
013h	PIR3	093h	PIE3	113h	CM2CON0	193h	PMDATL	213h	SSP1MSK	293h	CCP1CON	313h	_	393h	IOCAF
014h	—	094h	—	114h	CM2CON1	194h	PMDATH	214h	SSP1STAT	294h	_	314h	—	394h	IOCBP
015h	TMR0	095h	OPTION_REG	115h	CMOUT	195h	PMCON1	215h	SSP1CON1	295h	_	315h	_	395h	IOCBN
016h	TMR1L	096h	PCON	116h	BORCON	196h	PMCON2	216h	SSP1CON2	296h	_	316h	—	396h	IOCBF
017h	TMR1H	097h	WDTCON	117h	FVRCON	197h	VREGCON <sup>(1)</sup>	217h	SSP1CON3	297h	_	317h	_	397h	IOCCP
018h	T1CON	098h	OSCTUNE	118h	DAC1CON0	198h	—	218h	_	298h	CCPR2L	318h	_	398h	IOCCN
019h	T1GCON	099h	OSCCON	119h	DAC1CON1	199h	RC1REG	219h	_	299h	CCPR2H	319h	—	399h	IOCCF
01Ah	TMR2	09Ah	OSCSTAT	11Ah	DAC2CON0	19Ah	TX1REG	21Ah	_	29Ah	CCP2CON	31Ah	—	39Ah	_
01Bh	PR2	09Bh	ADRESL	11Bh	DAC2CON1	19Bh	SP1BRGL	21Bh	_	29Bh	_	31Bh	—	39Bh	_
01Ch	T2CON	09Ch	ADRESH	11Ch	ZCD1CON	19Ch	SP1BRGH	21Ch	_	29Ch	_	31Ch	_	39Ch	—
01Dh	_	09Dh	ADCON0	11Dh	_	19Dh	RC1STA	21Dh	_	29Dh	—	31Dh	—	39Dh	IOCEP
01Eh	_	09Eh	ADCON1	11Eh	_	19Eh	TX1STA	21Eh	_	29Eh	CCPTMRS	31Eh	—	39Eh	IOCEN
01Fh	—	09Fh	ADCON2	11Fh	_	19Fh	BAUD1CON	21Fh	_	29Fh	_	31Fh	—	39Fh	IOCEF
020h		0A0h		120h		1A0h		220h		2A0h		320h		3A0h	
	General		General		General		General		General		General		General		General
	Purpose		Purpose		Purpose		Purpose		Purpose		Purpose		Purpose		Purpose
	Register		Register		Register		Register		Register		Register		Register		Register
	ou bytes		ou bytes		ou bytes		ou bytes		ou bytes		ou bytes		ou bytes		ou bytes
06Fh		0EFh		16Fh		1EFh		26Fh		2EFh		36Fh		3EFh	
070h		0F0h		170h		1F0h		270h		2F0h		370h		3F0h	
	Common RAM		Accesses		Accesses		Accesses		Accesses		Accesses		Accesses		Accesses
	/011-/F11		/011-/FN		/011-/FN		/011 – / FN		/011-7-11		/011-/FN		/011 – / F11		/011-/FN
07Fh		0FFh		17Fh		1FFh		27Fh		2FFh		37Fh		3FFh	

Legend: = Unimplemented data memory locations, read as '0'.

Note 1: Unimplemented on PIC16LF1717/8/9.

## 3.7.1 TRADITIONAL DATA MEMORY

The traditional data memory is a region from FSR address 0x000 to FSR address 0xFFF. The addresses correspond to the absolute addresses of all SFR, GPR and common registers.





## 6.2.2.1 HFINTOSC

The High-Frequency Internal Oscillator (HFINTOSC) is a factory calibrated 16 MHz internal clock source. The frequency of the HFINTOSC can be altered via software using the OSCTUNE register (Register 6-3).

The output of the HFINTOSC connects to a postscaler and multiplexer (see Figure 6-1). One of multiple frequencies derived from the HFINTOSC can be selected via software using the IRCF<3:0> bits of the OSCCON register. See **Section 6.2.2.7** "Internal Oscillator Clock Switch Timing" for more information.

The HFINTOSC is enabled by:

- Configure the IRCF<3:0> bits of the OSCCON register for the desired HF frequency, and
- FOSC<2:0> = 100, or
- Set the System Clock Source (SCS) bits of the OSCCON register to '1x'

A fast start-up oscillator allows internal circuits to power up and stabilize before switching to HFINTOSC.

The High-Frequency Internal Oscillator Ready bit (HFIOFR) of the OSCSTAT register indicates when the HFINTOSC is running.

The High-Frequency Internal Oscillator Status Locked bit (HFIOFL) of the OSCSTAT register indicates when the HFINTOSC is running within 2% of its final value.

The High-Frequency Internal Oscillator Stable bit (HFIOFS) of the OSCSTAT register indicates when the HFINTOSC is running within 0.5% of its final value.

### 6.2.2.2 MFINTOSC

The Medium Frequency Internal Oscillator (MFINTOSC) is a factory calibrated 500 kHz internal clock source. The frequency of the MFINTOSC can be altered via software using the OSCTUNE register (Register 6-3).

The output of the MFINTOSC connects to a postscaler and multiplexer (see Figure 6-1). One of nine frequencies derived from the MFINTOSC can be selected via software using the IRCF<3:0> bits of the OSCCON register. See **Section 6.2.2.7** "Internal Oscillator Clock Switch Timing" for more information.

The MFINTOSC is enabled by:

- Configure the IRCF<3:0> bits of the OSCCON register for the desired HF frequency, and
- FOSC<2:0> = 100, or
- Set the System Clock Source (SCS) bits of the OSCCON register to '1x'

The Medium Frequency Internal Oscillator Ready bit (MFIOFR) of the OSCSTAT register indicates when the MFINTOSC is running.

## 6.2.2.3 Internal Oscillator Frequency Adjustment

The 500 kHz internal oscillator is factory calibrated. This internal oscillator can be adjusted in software by writing to the OSCTUNE register (Register 6-3). Since the HFINTOSC and MFINTOSC clock sources are derived from the 500 kHz internal oscillator a change in the OSCTUNE register value will apply to both.

The default value of the OSCTUNE register is '0'. The value is a 6-bit two's complement number. A value of 1Fh will provide an adjustment to the maximum frequency. A value of 20h will provide an adjustment to the minimum frequency.

When the OSCTUNE register is modified, the oscillator frequency will begin shifting to the new frequency. Code execution continues during this shift. There is no indication that the shift has occurred.

OSCTUNE does not affect the LFINTOSC frequency. Operation of features that depend on the LFINTOSC clock source frequency, such as the Power-up Timer (PWRT), Watchdog Timer (WDT), Fail-Safe Clock Monitor (FSCM) and peripherals, are *not* affected by the change in frequency.

## 6.2.2.4 LFINTOSC

The Low-Frequency Internal Oscillator (LFINTOSC) is an uncalibrated 31 kHz internal clock source.

The output of the LFINTOSC connects to a multiplexer (see Figure 6-1). Select 31 kHz, via software, using the IRCF<3:0> bits of the OSCCON register. See Section 6.2.2.7 "Internal Oscillator Clock Switch Timing" for more information. The LFINTOSC is also the frequency for the Power-up Timer (PWRT), Watchdog Timer (WDT) and Fail-Safe Clock Monitor (FSCM).

The LFINTOSC is enabled by selecting 31 kHz (IRCF<3:0> bits of the OSCCON register = 000) as the system clock source (SCS bits of the OSCCON register = 1x), or when any of the following are enabled:

- Configure the IRCF<3:0> bits of the OSCCON register for the desired LF frequency, and
- FOSC<2:0> = 100, or
- Set the System Clock Source (SCS) bits of the OSCCON register to '1x'

Peripherals that use the LFINTOSC are:

- Power-up Timer (PWRT)
- Watchdog Timer (WDT)
- Fail-Safe Clock Monitor (FSCM)

The Low-Frequency Internal Oscillator Ready bit (LFIOFR) of the OSCSTAT register indicates when the LFINTOSC is running.

## FIGURE 10-6: FLASH PROGRAM MEMORY WRITE FLOWCHART



## 11.1.4 SLEW RATE CONTROL

The SLRCONA register (Register 11-7) controls the slew rate option for each port pin. Slew rate control is independently selectable for each port pin. When an SLRCONA bit is set, the corresponding port pin drive is slew rate limited. When an SLRCONA bit is cleared, The corresponding port pin drive slews at the maximum rate possible.

## 11.1.5 INPUT THRESHOLD CONTROL

The INLVLA register (Register 11-8) controls the input voltage threshold for each of the available PORTA input pins. A selection between the Schmitt Trigger CMOS or the TTL compatible thresholds is available. The input threshold is important in determining the value of a read of the PORTA register and also the level at which an interrupt-on-change occurs, if that feature is enabled. See Table 34-4: I/O Ports for more information on threshold levels.

**Note:** Changing the input threshold selection should be performed while all peripheral modules are disabled. Changing the threshold level during the time a module is active may inadvertently generate a transition associated with an input pin, regardless of the actual voltage level on that pin.

## 11.1.6 ANALOG CONTROL

The ANSELA register (Register 11-4) is used to configure the Input mode of an I/O pin to analog. Setting the appropriate ANSELA bit high will cause all digital reads on the pin to be read as '0' and allow analog functions on the pin to operate correctly.

The state of the ANSELA bits has no effect on digital output functions. A pin with TRIS clear and ANSEL set will still operate as a digital output, but the Input mode will be analog. This can cause unexpected behavior when executing read-modify-write instructions on the affected port.

Note:	The ANSELA bits default to the Analog
	mode after Reset. To use any pins as
	digital general purpose or peripheral
	inputs, the corresponding ANSEL bits
	must be initialized to '0' by user software.

#### EXAMPLE 11-1: INITIALIZING PORTA

; This code example illustrates						
, IUILIS	; initializing the PORTA register. The					
; other	; other ports are initialized in the same					
; manner.						
BANKSEL	PORTA	;				
CLRF	PORTA	;Init PORTA				
BANKSEL	LATA	;Data Latch				
CLRF	LATA	;				
BANKSEL	ANSELA	;				
CLRF	ANSELA	;digital I/O				
BANKSEL	TRISA	;				
MOVLW	B'00111000'	;Set RA<5:3> as inputs				
MOVWF	TRISA	;and set RA<2:0> as				
		;outputs				

## 11.1.7 PORTA FUNCTIONS AND OUTPUT PRIORITIES

Each PORTA pin is multiplexed with other functions.

Each pin defaults to the PORT latch data after Reset. Other functions are selected with the peripheral pin select logic. See **Section 12.0** "**Peripheral Pin Select (PPS) Module**" for more information.

Analog input functions, such as ADC and comparator inputs are not shown in the peripheral pin select lists. These inputs are active when the I/O pin is set for Analog mode using the ANSELA register. Digital output functions may continue to control the pin when it is in Analog mode.

## **15.4 ADC Acquisition Time**

To ensure accurate temperature measurements, the user must wait at least 200  $\mu$ s after the ADC input multiplexer is connected to the temperature indicator output before the conversion is performed. In addition, the user must wait 200  $\mu$ s between sequential conversions of the temperature indicator output.

TABLE 13-2. SUMIMART OF REGISTERS ASSOCIATED WITH THE TEMPERATURE INDICATO	TABLE 15-2:	SUMMARY OF REGISTERS	ASSOCIATED WITH THE	TEMPERATURE INDICATOR
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Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on page
FVRCON	FVREN	FVRRDY	TSEN	TSRNG	CDFVF	R<1:0>	ADFV	R<1:0>	165

Legend: Shaded cells are unused by the temperature indicator module.



## 22.0 OPERATIONAL AMPLIFIER (OPA) MODULES

The Operational Amplifier (OPA) is a standard three-terminal device requiring external feedback to operate. The OPA module has the following features:

- External connections to I/O ports
- Low leakage inputs
- · Factory Calibrated Input Offset Voltage





## 29.4 Register Definitions: CCP Control

#### U-0 U-0 R/W-0/0 R/W-0/0 R/W-0/0 R/W-0/0 R/W-0/0 R/W-0/0 DCxB<1:0> CCPxM<3:0> \_\_\_\_ bit 7 bit 0 Legend: R = Readable bit W = Writable bit U = Unimplemented bit, read as '0' -n/n = Value at POR and BOR/Value at all other Reset u = Bit is unchanged x = Bit is unknown '1' = Bit is set '0' = Bit is cleared bit 7-6 Unimplemented: Read as '0' bit 5-4 DCxB<1:0>: PWM Duty Cycle Least Significant bits Capture mode: Unused Compare mode: Unused PWM mode: These bits are the two LSbs of the PWM duty cycle. The eight MSbs are found in CCPRxL. bit 3-0 CCPxM<3:0>: CCPx Mode Select bits 11xx = PWM mode 1011 = Compare mode: Auto-conversion Trigger (sets CCPxIF bit), starts ADC conversion if TRIGSEL = CCPx (see Register 21-3) 1010 = Compare mode: generate software interrupt only 1001 = Compare mode: clear output on compare match (set CCPxIF) 1000 = Compare mode: set output on compare match (set CCPxIF) 0111 = Capture mode: every 16th rising edge 0110 = Capture mode: every 4th rising edge 0101 = Capture mode: every rising edge 0100 = Capture mode: every falling edge 0011 = Reserved 0010 = Compare mode: toggle output on match 0001 = Reserved 0000 = Capture/Compare/PWM off (resets CCPx module)

#### **REGISTER 29-1: CCPxCON: CCPx CONTROL REGISTER**

## 30.2 SPI Mode Overview

The Serial Peripheral Interface (SPI) bus is a synchronous serial data communication bus that operates in Full-Duplex mode. Devices communicate in a master/slave environment where the master device initiates the communication. A slave device is controlled through a Chip Select known as Slave Select.

The SPI bus specifies four signal connections:

- Serial Clock (SCK)
- Serial Data Out (SDO)
- Serial Data In (SDI)
- Slave Select (SS)

Figure 30-1 shows the block diagram of the MSSP module when operating in SPI mode.

The SPI bus operates with a single master device and one or more slave devices. When multiple slave devices are used, an independent Slave Select connection is required from the master device to each slave device.

Figure 30-4 shows a typical connection between a master device and multiple slave devices.

The master selects only one slave at a time. Most slave devices have tri-state outputs so their output signal appears disconnected from the bus when they are not selected.

Transmissions involve two shift registers, eight bits in size, one in the master and one in the slave. With either the master or the slave device, data is always shifted out one bit at a time, with the Most Significant bit (MSb) shifted out first. At the same time, a new Least Significant bit (LSb) is shifted into the same register.

Figure 30-5 shows a typical connection between two processors configured as master and slave devices.

Data is shifted out of both shift registers on the programmed clock edge and latched on the opposite edge of the clock.

The master device transmits information out on its SDO output pin which is connected to, and received by, the slave's SDI input pin. The slave device transmits information out on its SDO output pin, which is connected to, and received by, the master's SDI input pin.

To begin communication, the master device first sends out the clock signal. Both the master and the slave devices should be configured for the same clock polarity.

The master device starts a transmission by sending out the MSb from its shift register. The slave device reads this bit from that same line and saves it into the LSb position of its shift register. During each SPI clock cycle, a full-duplex data transmission occurs. This means that while the master device is sending out the MSb from its shift register (on its SDO pin) and the slave device is reading this bit and saving it as the LSb of its shift register, that the slave device is also sending out the MSb from its shift register (on its SDO pin) and the master device is reading this bit and saving it as the LSb of its shift register.

After eight bits have been shifted out, the master and slave have exchanged register values.

If there is more data to exchange, the shift registers are loaded with new data and the process repeats itself.

Whether the data is meaningful or not (dummy data), depends on the application software. This leads to three scenarios for data transmission:

- Master sends useful data and slave sends dummy data.
- Master sends useful data and slave sends useful data.
- Master sends dummy data and slave sends useful data.

Transmissions may involve any number of clock cycles. When there is no more data to be transmitted, the master stops sending the clock signal and it deselects the slave.

Every slave device connected to the bus that has not been selected through its slave select line must disregard the clock and transmission signals and must not transmit out any data of its own.







## 30.5.6 CLOCK STRETCHING

Clock stretching occurs when a device on the bus holds the SCL line low, effectively pausing communication. The slave may stretch the clock to allow more time to handle data or prepare a response for the master device. A master device is not concerned with stretching as anytime it is active on the bus and not transferring data it is stretching. Any stretching done by a slave is invisible to the master software and handled by the hardware that generates SCL.

The CKP bit of the SSP1CON1 register is used to control stretching in software. Any time the CKP bit is cleared, the module will wait for the SCL line to go low and then hold it. Setting CKP will release SCL and allow more communication.

### 30.5.6.1 Normal Clock Stretching

Following an ACK if the R/W bit of SSP1STAT is set, a read request, the slave hardware will clear CKP. This allows the slave time to update SSP1BUF with data to transfer to the master. If the SEN bit of SSP1CON2 is set, the slave hardware will always stretch the clock after the ACK sequence. Once the slave is ready; CKP is set by software and communication resumes.

- Note 1: The BF bit has no effect on if the clock will be stretched or not. This is different than previous versions of the module that would not stretch the clock, clear CKP, if SSP1BUF was read before the 9th falling edge of SCL.
  - 2: Previous versions of the module did not stretch the clock for a transmission if SSP1BUF was loaded before the 9th falling edge of SCL. It is now always cleared for read requests.

## 30.5.6.2 10-Bit Addressing Mode

In 10-bit Addressing mode, when the UA bit is set the clock is always stretched. This is the only time the SCL is stretched without CKP being cleared. SCL is released immediately after a write to SSP1ADD.

Note:	Previous versions of the module did not
	stretch the clock if the second address byte
	did not match.

## 30.5.6.3 Byte NACKing

When AHEN bit of SSP1CON3 is set; CKP is cleared by hardware after the eighth falling edge of SCL for a received matching address byte. When DHEN bit of SSP1CON3 is set; CKP is cleared after the eighth falling edge of SCL for received data.

Stretching after the eighth falling edge of SCL allows the slave to look at the received address or data and decide if it wants to ACK the received data.









## 33.0 INSTRUCTION SET SUMMARY

Each instruction is a 14-bit word containing the operation code (opcode) and all required operands. The opcodes are broken into three broad categories.

- · Byte Oriented
- · Bit Oriented
- Literal and Control

The literal and control category contains the most varied instruction word format.

Table 33-3 lists the instructions recognized by the MPASM  $^{\rm TM}$  assembler.

All instructions are executed within a single instruction cycle, with the following exceptions, which may take two or three cycles:

- Subroutine takes two cycles (CALL, CALLW)
- Returns from interrupts or subroutines take two cycles (RETURN, RETLW, RETFIE)
- Program branching takes two cycles (GOTO, BRA, BRW, BTFSS, BTFSC, DECFSZ, INCSFZ)
- One additional instruction cycle will be used when any instruction references an indirect file register and the file select register is pointing to program memory.

One instruction cycle consists of four oscillator cycles; for an oscillator frequency of 4 MHz, this gives a nominal instruction execution rate of 1 MHz.

All instruction examples use the format '0xhh' to represent a hexadecimal number, where 'h' signifies a hexadecimal digit.

## 33.1 Read-Modify-Write Operations

Any instruction that specifies a file register as part of the instruction performs a Read-Modify-Write (R-M-W) operation. The register is read, the data is modified, and the result is stored according to either the instruction, or the destination designator 'd'. A read operation is performed on a register even if the instruction writes to that register.

TABLE 33-1:	OPCODE FIELD
	DESCRIPTIONS

Field	Description
f	Register file address (0x00 to 0x7F)
W	Working register (accumulator)
b	Bit address within an 8-bit file register
k	Literal field, constant data or label
x	Don't care location (= $0$ or $1$ ). The assembler will generate code with x = $0$ . It is the recommended form of use for compatibility with all Microchip software tools.
d	Destination select; d = 0: store result in W, d = 1: store result in file register f. Default is d = 1.
n	FSR or INDF number. (0-1)
mm	Pre-post increment-decrement mode selection

## TABLE 33-2: ABBREVIATION DESCRIPTIONS

Field	Description
PC	Program Counter
TO	Time-Out bit
С	Carry bit
DC	Digit Carry bit
Z	Zero bit
PD	Power-Down bit

RETFIE	Return from Interrupt
Syntax:	[ <i>label</i> ] RETFIE k
Operands:	None
Operation:	$\begin{array}{l} TOS \to PC, \\ 1 \to GIE \end{array}$
Status Affected:	None
Description:	Return from Interrupt. Stack is POPed and Top-of-Stack (TOS) is loaded in the PC. Interrupts are enabled by setting Global Interrupt Enable bit, GIE (INTCON<7>). This is a 2-cycle instruction.
Words:	1
Cycles:	2
Example:	RETFIE
	After Interrupt PC = TOS GIE = 1

RETURN	Return from Subroutine		
Syntax:	[label] RETURN		
Operands:	None		
Operation:	$TOS \rightarrow PC$		
Status Affected:	None		
Description:	Return from subroutine. The stack is POPed and the top of the stack (TOS) is loaded into the program counter. This is a 2-cycle instruction.		

RETLW	Return with literal in W	RLF Syntax:	Rotate Left f through Carry		
Syntax:	[ <i>label</i> ] RETLW k		[ <i>label</i> ] RLF f,d		
Operands:	$0 \le k \le 255$	Operands:	$0 \le f \le 127$		
Operation:	$k \rightarrow (W);$		$d \in [0,1]$		
	$TOS \rightarrow PC$	Operation:	See description below		
Status Affected:	None	Status Affected:	С		
Description:	The W register is loaded with the 8-bit literal 'k'. The program counter is loaded from the top of the stack (the return address). This is a 2-cycle instruction.	Description:	The contents of register 'f' are rotated one bit to the left through the Carry flag. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is stored back in register 'f'.		
Words:	1		C Register f		
Cycles:	2				
Example:	CALL TABLE;W contains table	Words:	1		
	;offset value	Cycles:	1		
	• ;W now has table value		RLF REG1,0		
TABLE	•		Before Instruction		
	ADDWF PC ; $W = offset$		REG1 = 1110 0110		
	RETLW k1 ;Begin table		C = 0		
	RETLW k2 ;		REG1 = 1110 0110		
	•		W = 1100 1100		
	•		C = 1		
	RETLW kn ; End of table				
	Before Instruction W = 0x07 After Instruction W = value of k8				

## 36.11 Demonstration/Development Boards, Evaluation Kits, and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM<sup>™</sup> and dsPICDEM<sup>™</sup> demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ<sup>®</sup> security ICs, CAN, IrDA<sup>®</sup>, PowerSmart battery management, SEEVAL<sup>®</sup> evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page (www.microchip.com) for the complete list of demonstration, development and evaluation kits.

## 36.12 Third-Party Development Tools

Microchip also offers a great collection of tools from third-party vendors. These tools are carefully selected to offer good value and unique functionality.

- Device Programmers and Gang Programmers from companies, such as SoftLog and CCS
- Software Tools from companies, such as Gimpel and Trace Systems
- Protocol Analyzers from companies, such as Saleae and Total Phase
- Demonstration Boards from companies, such as MikroElektronika, Digilent<sup>®</sup> and Olimex
- Embedded Ethernet Solutions from companies, such as EZ Web Lynx, WIZnet and IPLogika<sup>®</sup>

## 37.2 Package Details

The following sections give the technical details of the packages.

## 28-Lead Skinny Plastic Dual In-Line (SP) – 300 mil Body [SPDIP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	INCHES			
	Dimension Limits	MIN	NOM	MAX
Number of Pins	N	28		
Pitch	е	.100 BSC		
Top to Seating Plane	A	-	-	.200
Molded Package Thickness	A2	.120	.135	.150
Base to Seating Plane	A1	.015	-	-
Shoulder to Shoulder Width	E	.290	.310	.335
Molded Package Width	E1	.240	.285	.295
Overall Length	D	1.345	1.365	1.400
Tip to Seating Plane	L	.110	.130	.150
Lead Thickness	С	.008	.010	.015
Upper Lead Width	b1	.040	.050	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	_	_	.430

#### Notes:

- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. § Significant Characteristic.
- 3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
- 4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-070B