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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I <sup>2</sup> C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	35
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 28x10b; D/A 1x5b, 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	40-UFQFN Exposed Pad
Supplier Device Package	40-UQFN (5x5)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic16lf1717t-i-mv">https://www.e-xfl.com/product-detail/microchip-technology/pic16lf1717t-i-mv</a>

## 5.12 Determining the Cause of a Reset

Upon any Reset, multiple bits in the STATUS and PCON register are updated to indicate the cause of the Reset. Table 5-3 and Table 5-4 show the Reset conditions of these registers.

**TABLE 5-3: RESET STATUS BITS AND THEIR SIGNIFICANCE**

STKOVF	STKUNF	RWD $\overline{T}$	RMCLR	RI	POR	BOR	TO	PD	Condition
0	0	1	1	1	0	x	1	1	Power-on Reset
0	0	1	1	1	0	x	0	x	Illegal, $\overline{TO}$ is set on $\overline{POR}$
0	0	1	1	1	0	x	x	0	Illegal, $\overline{PD}$ is set on $\overline{POR}$
0	0	u	1	1	u	0	1	1	Brown-out Reset
u	u	0	u	u	u	u	0	u	WDT Reset
u	u	u	u	u	u	u	0	0	WDT Wake-up from Sleep
u	u	u	u	u	u	u	1	0	Interrupt Wake-up from Sleep
u	u	u	0	u	u	u	u	u	$\overline{MCLR}$ Reset during normal operation
u	u	u	0	u	u	u	1	0	$\overline{MCLR}$ Reset during Sleep
u	u	u	u	0	u	u	u	u	RESET Instruction Executed
1	u	u	u	u	u	u	u	u	Stack Overflow Reset (STVREN = 1)
u	1	u	u	u	u	u	u	u	Stack Underflow Reset (STVREN = 1)

**TABLE 5-4: RESET CONDITION FOR SPECIAL REGISTERS**

Condition	Program Counter	STATUS Register	PCON Register
Power-on Reset	0000h	---1 1000	00-- 110x
$\overline{MCLR}$ Reset during normal operation	0000h	---u uuuu	uu-- 0uuu
$\overline{MCLR}$ Reset during Sleep	0000h	---1 0uuu	uu-- 0uuu
WDT Reset	0000h	---0 uuuu	uu-- uuuu
WDT Wake-up from Sleep	PC + 1	---0 0uuu	uu-- uuuu
Brown-out Reset	0000h	---1 1uuu	00-- 11u0
Interrupt Wake-up from Sleep	PC + 1 <sup>(1)</sup>	---1 0uuu	uu-- uuuu
RESET Instruction Executed	0000h	---u uuuu	uu-- u0uu
Stack Overflow Reset (STVREN = 1)	0000h	---u uuuu	1u-- uuuu
Stack Underflow Reset (STVREN = 1)	0000h	---u uuuu	u1-- uuuu

**Legend:** u = unchanged, x = unknown, - = unimplemented bit, reads as '0'.

**Note 1:** When the wake-up is due to an interrupt and Global Enable bit (GIE) is set, the return address is pushed on the stack and PC is loaded with the interrupt vector (0004h) after execution of PC + 1.

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## 7.6 Register Definitions: Interrupt Control

**REGISTER 7-1: INTCON: INTERRUPT CONTROL REGISTER**

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R-0/0
GIE	PEIE	TMR0IE	INTE	IOCFIE	TMR0IF	INTF	IOCF <sup>(1)</sup>
bit 7							bit 0

**Legend:**

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

- bit 7      **GIE:** Global Interrupt Enable bit  
1 = Enables all active interrupts  
0 = Disables all interrupts
- bit 6      **PEIE:** Peripheral Interrupt Enable bit  
1 = Enables all active peripheral interrupts  
0 = Disables all peripheral interrupts
- bit 5      **TMR0IE:** Timer0 Overflow Interrupt Enable bit  
1 = Enables the Timer0 interrupt  
0 = Disables the Timer0 interrupt
- bit 4      **INTE:** INT External Interrupt Enable bit  
1 = Enables the INT external interrupt  
0 = Disables the INT external interrupt
- bit 3      **IOCFIE:** Interrupt-on-Change Enable bit  
1 = Enables the interrupt-on-change  
0 = Disables the interrupt-on-change
- bit 2      **TMR0IF:** Timer0 Overflow Interrupt Flag bit  
1 = TMR0 register has overflowed  
0 = TMR0 register did not overflow
- bit 1      **INTF:** INT External Interrupt Flag bit  
1 = The INT external interrupt occurred  
0 = The INT external interrupt did not occur
- bit 0      **IOCF:** Interrupt-on-Change Interrupt Flag bit<sup>(1)</sup>  
1 = When at least one of the interrupt-on-change pins changed state  
0 = None of the interrupt-on-change pins have changed state

**Note 1:** The IOCF Flag bit is read-only and cleared when all the interrupt-on-change flags in the IOCxF registers have been cleared by software.

**Note:** Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit, GIE, of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

## EXAMPLE 10-2: ERASING ONE ROW OF PROGRAM MEMORY

```

; This row erase routine assumes the following:
; 1. A valid address within the erase row is loaded in ADDRHI:ADDRL
; 2. ADDRHI and ADDRL are located in shared data memory 0x70 - 0x7F (common RAM)

      BCF      INTCON,GIE      ; Disable ints so required sequences will execute properly
      BANKSEL PMADRL
      MOVF     ADDRL,W         ; Load lower 8 bits of erase address boundary
      MOVWF    PMADRL
      MOVF     ADDRHI,W        ; Load upper 6 bits of erase address boundary
      MOVWF    PMADRH
      BCF      PMCON1,CFGSR    ; Not configuration space
      BSF      PMCON1,FREER    ; Specify an erase operation
      BSF      PMCON1,WREN     ; Enable writes

      MOVLW    55h             ; Start of required sequence to initiate erase
      MOVWF    PMCON2          ; Write 55h
      MOVLW    0AAh            ;
      MOVWF    PMCON2          ; Write AAh
      BSF      PMCON1,WR       ; Set WR bit to begin erase
      NOP      ; NOP instructions are forced as processor starts
      NOP      ; row erase of program memory.
      ;
      ; The processor stalls until the erase process is complete
      ; after erase processor continues with 3rd instruction

      BCF      PMCON1,WREN     ; Disable writes
      BSF      INTCON,GIE     ; Enable interrupts

```

Required  
Sequence

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## 11.0 I/O PORTS

Each port has six standard registers for its operation. These registers are:

- TRISx registers (data direction)
- PORTx registers (reads the levels on the pins of the device)
- LATx registers (output latch)
- INLVx (input level control)
- ODCONx registers (open-drain)
- SLRCONx registers (slew rate)

Some ports may have one or more of the following additional registers. These registers are:

- ANSELx (analog select)
- WPUx (weak pull-up)

In general, when a peripheral is enabled on a port pin, that pin cannot be used as a general purpose output. However, the pin can still be read.

**TABLE 11-1: PORT AVAILABILITY PER DEVICE**

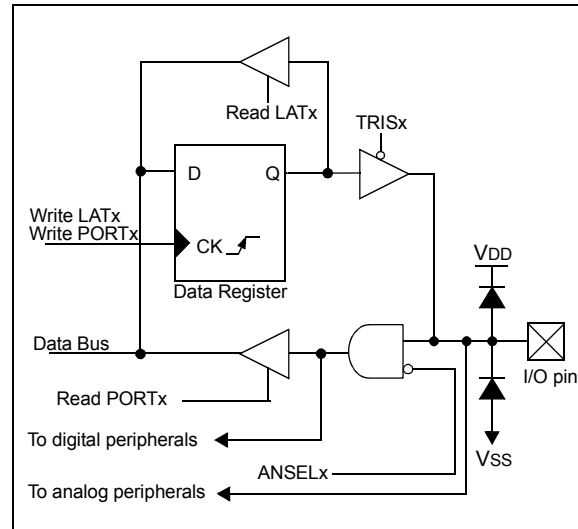
Device	PORTA	PORTB	PORTC	PORTD	PORTE
PIC16(L)F1717	•	•	•	•	•
PIC16(L)F1718	•	•	•		•
PIC16(L)F1719	•	•	•	•	•

The Data Latch (LATx registers) is useful for read-modify-write operations on the value that the I/O pins are driving.

A write operation to the LATx register has the same effect as a write to the corresponding PORTx register. A read of the LATx register reads of the values held in the I/O PORT latches, while a read of the PORTx register reads the actual I/O pin value.

Ports that support analog inputs have an associated ANSELx register. When an ANSEL bit is set, the digital input buffer associated with that bit is disabled. Disabling the input buffer prevents analog signal levels on the pin between a logic high and low from causing excessive current in the logic input circuitry. A simplified model of a generic I/O port, without the interfaces to other peripherals, is shown in Figure 11-1.

**FIGURE 11-1: GENERIC I/O PORT OPERATION**



## 11.1 PORTA Registers

### 11.1.1 DATA REGISTER

PORTA is an 8-bit wide, bidirectional port. The corresponding data direction register is TRISA (Register 11-2). Setting a TRISA bit (= 1) will make the corresponding PORTA pin an input (i.e., disable the output driver). Clearing a TRISA bit (= 0) will make the corresponding PORTA pin an output (i.e., enables output driver and puts the contents of the output latch on the selected pin). Example 11-1 shows how to initialize PORTA.

Reading the PORTA register (Register 11-1) reads the status of the pins, whereas writing to it will write to the PORT latch. All write operations are read-modify-write operations. Therefore, a write to a port implies that the port pins are read, this value is modified and then written to the PORT data latch (LATA).

### 11.1.2 DIRECTION CONTROL

The TRISA register (Register 11-2) controls the PORTA pin output drivers, even when they are being used as analog inputs. The user should ensure the bits in the TRISA register are maintained set when using them as analog inputs. I/O pins configured as analog inputs always read '0'.

### 11.1.3 OPEN-DRAIN CONTROL

The ODCONA register (Register 11-6) controls the open-drain feature of the port. Open-drain operation is independently selected for each pin. When an ODCONA bit is set, the corresponding port output becomes an open-drain driver capable of sinking current only. When an ODCONA bit is cleared, the corresponding port output pin is the standard push-pull drive capable of sourcing and sinking current.

## 12.3 Bidirectional Pins

PPS selections for peripherals with bidirectional signals on a single pin must be made so that the PPS input and PPS output select the same pin. Peripherals that have bidirectional signals include:

- EUSART (synchronous operation)
- MSSP (I<sup>2</sup>C)

**Note:** The I<sup>2</sup>C default input pins are I<sup>2</sup>C and SMBus compatible and are the only pins on the device with this compatibility.

## 12.4 PPS Lock

The PPS includes a mode in which all input and output selections can be locked to prevent inadvertent changes. PPS selections are locked by setting the PPSLOCKED bit of the PPSLOCK register. Setting and clearing this bit requires a special sequence as an extra precaution against inadvertent changes. Examples of setting and clearing the PPSLOCKED bit are shown in Example 12-1.

### EXAMPLE 12-1: PPS LOCK/UNLOCK SEQUENCE

```
; suspend interrupts
    bcf    INTCON,GIE
;   BANKSEL PPSLOCK    ; set bank
; required sequence, next 5 instructions
    movlw  0x55
    movwf  PPSLOCK
    movlw  0xAA
    movwf  PPSLOCK
; Set PPSLOCKED bit to disable writes or
; Clear PPSLOCKED bit to enable writes
    bsf    PPSLOCK,PPSLOCKED
; restore interrupts
    bsf    INTCON,GIE
```

## 12.5 PPS Permanent Lock

The PPS can be permanently locked by setting the PPS1WAY Configuration bit. When this bit is set, the PPSLOCKED bit can only be cleared and set one time after a device Reset. This allows for clearing the PPSLOCKED bit so that the input and output selections can be made during initialization. When the PPSLOCKED bit is set after all selections have been made, it will remain set and cannot be cleared until after the next device Reset event.

## 12.6 Operation During Sleep

PPS input and output selections are unaffected by Sleep.

## 12.7 Effects of a Reset

A device Power-On-Reset (POR) clears all PPS input and output selections to their default values. All other Resets leave the selections unchanged. Default input selections are shown in pin allocation Table 1.

## 13.0 INTERRUPT-ON-CHANGE

All pins on all ports can be configured to operate as Interrupt-on-Change (IOC) pins. An interrupt can be generated by detecting a signal that has either a rising edge or a falling edge. Any individual pin, or combination of pins, can be configured to generate an interrupt. The interrupt-on-change module has the following features:

- Interrupt-on-Change enable (Master Switch)
- Individual pin configuration
- Rising and falling edge detection
- Individual pin interrupt flags

Figure 13-1 is a block diagram of the IOC module.

### 13.1 Enabling the Module

To allow individual pins to generate an interrupt, the IOCIE bit of the INTCON register must be set. If the IOCIE bit is disabled, the edge detection on the pin will still occur, but an interrupt will not be generated.

### 13.2 Individual Pin Configuration

For each pin, a rising edge detector and a falling edge detector are present. To enable a pin to detect a rising edge, the associated bit of the IOCxP register is set. To enable a pin to detect a falling edge, the associated bit of the IOCxN register is set.

A pin can be configured to detect rising and falling edges simultaneously by setting the associated bits in both of the IOCxP and IOCxN registers.

### 13.3 Interrupt Flags

The bits located in the IOCxF registers are status flags that correspond to the interrupt-on-change pins of each port. If an expected edge is detected on an appropriately enabled pin, then the status flag for that pin will be set, and an interrupt will be generated if the IOCIE bit is set. The IOCIF bit of the INTCON register reflects the status of all IOCxF bits.

## 13.4 Clearing Interrupt Flags

The individual status flags, (IOCxF register bits), can be cleared by resetting them to zero. If another edge is detected during this clearing operation, the associated status flag will be set at the end of the sequence, regardless of the value actually being written.

In order to ensure that no detected edge is lost while clearing flags, only AND operations masking out known changed bits should be performed. The following sequence is an example of what should be performed.

### EXAMPLE 13-1: CLEARING INTERRUPT FLAGS (PORTA EXAMPLE)

```
MOVLW    0xff
XORWF    IOCAF, W
ANDWF    IOCAF, F
```

### 13.5 Operation in Sleep

The interrupt-on-change interrupt sequence will wake the device from Sleep mode, if the IOCIE bit is set.

If an edge is detected while in Sleep mode, the affected IOCxF register will be updated prior to the first instruction executed out of Sleep.

## REGISTER 13-4: IOCBP: INTERRUPT-ON-CHANGE PORTB POSITIVE EDGE REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
IOCBP7	IOCBP6	IOCBP5	IOCBP4	IOCBP3	IOCBP2	IOCBP1	IOCBP0
bit 7							bit 0

### Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **IOCBP<7:0>**: Interrupt-on-Change PORTB Positive Edge Enable bits  
 1 = Interrupt-on-Change enabled on the pin for a positive going edge. IOCBFx bit and IOCIF flag will be set upon detecting an edge.  
 0 = Interrupt-on-Change disabled for the associated pin

## REGISTER 13-5: IOCBN: INTERRUPT-ON-CHANGE PORTB NEGATIVE EDGE REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
IOCBN7	IOCBN6	IOCBN5	IOCBN4	IOCBN3	IOCBN2	IOCBN1	IOCBN0
bit 7							bit 0

### Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **IOCBN<7:0>**: Interrupt-on-Change PORTB Negative Edge Enable bits  
 1 = Interrupt-on-Change enabled on the pin for a negative going edge. IOCBFx bit and IOCIF flag will be set upon detecting an edge.  
 0 = Interrupt-on-Change disabled for the associated pin.

## REGISTER 13-6: IOCBF: INTERRUPT-ON-CHANGE PORTB FLAG REGISTER

R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0
IOCBF7	IOCBF6	IOCBF5	IOCBF4	IOCBF3	IOCBF2	IOCBF1	IOCBF0
bit 7							bit 0

### Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	HS - Bit is set in hardware

bit 7-0 **IOCBF<7:0>**: Interrupt-on-Change PORTB Flag bits  
 1 = An enabled change was detected on the associated pin.  
 Set when IOCBPx = 1 and a rising edge was detected on RBx, or when IOCBNx = 1 and a falling edge was detected on RBx.  
 0 = No change was detected, or the user cleared the detected change.



## 19.1.5 CLCx SETUP STEPS

The following steps should be followed when setting up the CLCx:

- Disable CLCx by clearing the LCxEN bit.
- Select desired inputs using CLCxSEL0 through CLCxSEL3 registers (See Table 19-1).
- Clear any associated ANSEL bits.
- Set all TRIS bits associated with inputs.
- Clear all TRIS bits associated with outputs.
- Enable the chosen inputs through the four gates using CLCxGLS0, CLCxGLS1, CLCxGLS2, and CLCxGLS3 registers.
- Select the gate output polarities with the LCxPOLy bits of the CLCxPOL register.
- Select the desired logic function with the LCxMODE<2:0> bits of the CLCxCON register.
- Select the desired polarity of the logic output with the LCxPOL bit of the CLCxPOL register. (This step may be combined with the previous gate output polarity step).
- If driving a device pin, set the desired pin PPS control register and also clear the TRIS bit corresponding to that output.
- If interrupts are desired, configure the following bits:
  - Set the LCxINTP bit in the CLCxCON register for rising event.
  - Set the LCxINTN bit in the CLCxCON register for falling event.
  - Set the CLCxIE bit of the associated PIE registers.
  - Set the GIE and PEIE bits of the INTCON register.
- Enable the CLCx by setting the LCxEN bit of the CLCxCON register.

## 19.2 CLCx Interrupts

An interrupt will be generated upon a change in the output value of the CLCx when the appropriate interrupt enables are set. A rising edge detector and a falling edge detector are present in each CLC for this purpose.

The CLCxIF bit of the associated PIR registers will be set when either edge detector is triggered and its associated enable bit is set. The LCxINTP enables rising edge interrupts and the LCxINTN bit enables falling edge interrupts. Both are located in the CLCxCON register.

To fully enable the interrupt, set the following bits:

- LCxON bit of the CLCxCON register
- CLCxIE bit of the associated PIE registers
- LCxINTP bit of the CLCxCON register (for a rising edge detection)
- LCxINTN bit of the CLCxCON register (for a falling edge detection)
- PEIE and GIE bits of the INTCON register

The CLCxIF bit of the associated PIR registers, must be cleared in software as part of the interrupt service. If another edge is detected while this flag is being cleared, the flag will still be set at the end of the sequence.

## 19.3 Output Mirror Copies

Mirror copies of all LCxCON output bits are contained in the CLCxDATA register. Reading this register reads the outputs of all CLCs simultaneously. This prevents any reading skew introduced by testing or reading the CLCxOUT bits in the individual CLCxCON registers.

## 19.4 Effects of a Reset

The CLCxCON register is cleared to zero as the result of a Reset. All other selection and gating values remain unchanged.

## 19.5 Operation During Sleep

The CLC module operates independently from the system clock and will continue to run during Sleep, provided that the input sources selected remain active.

The HFINTOSC remains active during Sleep when the CLC module is enabled and the HFINTOSC is selected as an input source, regardless of the system clock source selected.

In other words, if the HFINTOSC is simultaneously selected as the system clock and as a CLC input source, when the CLC is enabled, the CPU will go idle during Sleep, but the CLC will continue to operate and the HFINTOSC will remain active.

This will have a direct effect on the Sleep mode current.

**REGISTER 19-11: CLCDATA: CLC DATA OUTPUT**

U-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0
—	—	—	—	MCL4OUT	MLC3OUT	MLC2OUT	MLC1OUT
bit 7				bit 0			

**Legend:**

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
u = Bit is unchanged                  x = Bit is unknown                  -n/n = Value at POR and BOR/Value at all other Resets  
'1' = Bit is set                          '0' = Bit is cleared

bit 7-4              Unimplemented: Read as '0'  
bit 3                MCL4OUT: Mirror copy of LC4OUT bit  
bit 2                MLC3OUT: Mirror copy of LC3OUT bit  
bit 1                MLC2OUT: Mirror copy of LC2OUT bit  
bit 0                MLC1OUT: Mirror copy of LC1OUT bit

**TABLE 19-3: SUMMARY OF REGISTERS ASSOCIATED WITH CLCx**

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Register on Page
ANSELA	—	—	ANSA5	ANSA4	ANSA3	ANSA2	ANSA1	ANSA0	125
ANSELB	—	—	ANSB5	ANSB4	ANSB3	ANSB2	ANSB1	ANSB0	131
ANSELC	ANSC7	ANSC6	ANSC5	ANSC4	ANSC3	ANSC2	—	—	136
ANSELD <sup>(1)</sup>	ANS7	ANS6	ANS5	ANS4	ANS3	ANS2	ANS1	ANS0	141
CLC1CON	LC1EN	—	LC1OUT	LC1INTP	LC1INTN	LC1MODE<2:0>			224
CLC2CON	LC2EN	—	LC2OUT	LC2INTP	LC2INTN	LC2MODE<2:0>			224
CLC3CON	LC3EN	—	LC3OUT	LC3INTP	LC3INTN	LC3MODE<2:0>			224
CLCDATA	—	—	—	—	MCL4OUT	MLC3OUT	MLC2OUT	MLC1OUT	231
CLC1GLS0	LC1G1D4T	LC1G1D4N	LC1G1D3T	LC1G1D3N	LC1G1D2T	LC1G1D2N	LC1G1D1T	LC1G1D1N	227
CLC1GLS1	LC1G2D4T	LC1G2D4N	LC1G2D3T	LC1G2D3N	LC1G2D2T	LC1G2D2N	LC1G2D1T	LC1G2D1N	228
CLC1GLS2	LC1G3D4T	LC1G3D4N	LC1G3D3T	LC1G3D3N	LC1G3D2T	LC1G3D2N	LC1G3D1T	LC1G3D1N	229
CLC1GLS3	LC1G4D4T	LC1G4D4N	LC1G4D3T	LC1G4D3N	LC1G4D2T	LC1G4D2N	LC1G4D1T	LC1G4D1N	230
CLC1POL	LC1POL	—	—	—	LC1G4POL	LC1G3POL	LC1G2POL	LC1G1POL	225
CLC1SEL0	—	—	—	LC1D1S<4:0>					225
CLC1SEL1	—	—	—	LC1D2S<4:0>					226
CLC1SEL2	—	—	—	LC1D3S<4:0>					226
CLC1SEL3	—	—	—	LC1D4S<4:0>					226
CLC2GLS0	LC2G1D4T	LC2G1D4N	LC2G1D3T	LC2G1D3N	LC2G1D2T	LC2G1D2N	LC2G1D1T	LC2G1D1N	227
CLC2GLS1	LC2G2D4T	LC2G2D4N	LC2G2D3T	LC2G2D3N	LC2G2D2T	LC2G2D2N	LC2G2D1T	LC2G2D1N	228
CLC2GLS2	LC2G3D4T	LC2G3D4N	LC2G3D3T	LC2G3D3N	LC2G3D2T	LC2G3D2N	LC2G3D1T	LC2G3D1N	229
CLC2GLS3	LC2G4D4T	LC2G4D4N	LC2G4D3T	LC2G4D3N	LC2G4D2T	LC2G4D2N	LC2G4D1T	LC2G4D1N	230
CLC2POL	LC2POL	—	—	—	LC2G4POL	LC2G3POL	LC2G2POL	LC2G1POL	225
CLC2SEL0	—	—	—	LC2D1S<4:0>					225
CLC2SEL1	—	—	—	LC2D2S<4:0>					226
CLC2SEL2	—	—	—	LC2D3S<4:0>					226

**Legend:** — = unimplemented read as '0'. Shaded cells are not used for CLC module.

**Note 1:** PIC16(L)F1717/9 only.

## 22.3 Register Definitions: Op Amp Control

**REGISTER 22-1: OPAXCON: OPERATIONAL AMPLIFIERS (OPAx) CONTROL REGISTERS**

R/W-0/0	R/W-0/0	U-0	R/W-0/0	U-0	U-0	R/W-0/0	R/W-0/0
OPAxEN	OPAxSP	—	OPAxUG	—	—	OPAxCH<1:0>	
bit 7							bit 0

**Legend:**

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = Value depends on condition

bit 7	<b>OPAxEN:</b> Op Amp Enable bit 1 = Op amp is enabled 0 = Op amp is disabled and consumes no active power
bit 6	<b>OPAxSP:</b> Op Amp Speed/Power Select bit 1 = Op amp operates in high GBWP mode 0 = Reserved. Do not use.
bit 5	<b>Unimplemented:</b> Read as '0'
bit 4	<b>OPAxUG:</b> Op Amp Unity Gain Select bit 1 = OPA output is connected to inverting input. OPAXIN- pin is available for general purpose I/O. 0 = Inverting input is connected to the OPAXIN- pin
bit 3-2	<b>Unimplemented:</b> Read as '0'
bit 1-0	<b>OPAxCH&lt;1:0&gt;:</b> Non-inverting Channel Selection bits 11 = Non-inverting input connects to FVR Butter 2 output 10 = Non-inverting input connects to DAC1_output 01 = Non-inverting input connects to DAC2_output 00 = Non-inverting input connects to OPAXIN+ pin

**TABLE 22-1: SUMMARY OF REGISTERS ASSOCIATED WITH OP AMPS**

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ANSELA	—	—	ANSA5	ANSA4	ANSA3	ANSA2	ANSA1	ANSA0	125
ANSELB	—	—	ANSB5	ANSB4	ANSB3	ANSB2	ANSB1	ANSB0	131
DAC1CON0	DAC1EN	—	DAC1OE1	DAC1OE2	DAC1PSS<1:0>		—	DAC1NSS	260
DAC1CON1	DAC1R<7:0>								260
FVRCON	FVREN	FVRRDY	TSEN	TSRNG	CDAFVR<1:0>		ADFVR<1:0>		165
OPA1CON	OPA1EN	OPA1SP	—	OPA1UG	—	—	OPA1PCH<1:0>		257
OPA2CON	OPA2EN	OPA2SP	—	OPA2UG	—	—	OPA2PCH<1:0>		257
TRISA	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	124
TRISB	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	130

**Legend:** — = unimplemented location, read as '0'. Shaded cells are not used by op amps.

# PIC16(L)F1717/8/9

## 23.6 Register Definitions: DAC Control

### REGISTER 23-1: DAC1CON0: DAC1 CONTROL REGISTER 0

R/W-0/0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	U-0	R/W-0/0
DAC1EN	—	DAC1OE1	DAC1OE2	DAC1PSS<1:0>	—	DAC1NSS	
bit 7							bit 0

#### Legend:

R = Readable bit      W = Writable bit      U = Unimplemented bit, read as '0'  
u = Bit is unchanged      x = Bit is unknown      -n/n = Value at POR and BOR/Value at all other Resets  
'1' = Bit is set      '0' = Bit is cleared

- bit 7      **DAC1EN:** DAC1 Enable bit  
1 = DAC is enabled  
0 = DAC is disabled
- bit 6      **Unimplemented:** Read as '0'
- bit 5      **DAC1OE1:** DAC1 Voltage Output 1 Enable bit  
1 = DAC voltage level is also an output on the DAC1OUT1 pin  
0 = DAC voltage level is disconnected from the DAC1OUT1 pin
- bit 4      **DAC1OE2:** DAC1 Voltage Output 2 Enable bit  
1 = DAC voltage level is also an output on the DAC1OUT2 pin  
0 = DAC voltage level is disconnected from the DAC1OUT2 pin
- bit 3-2      **DAC1PSS<1:0>:** DAC1 Positive Source Select bits  
11 = Reserved, do not use  
10 = FVR Buffer2 output  
01 = VREF+ pin  
00 = VDD
- bit 1      **Unimplemented:** Read as '0'
- bit 0      **DAC1NSS:** DAC1 Negative Source Select bits  
1 = VREF- pin  
0 = VSS

### REGISTER 23-2: DAC1CON1: DAC1 CONTROL REGISTER 1

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
DAC1R<7:0>							
bit 7							bit 0

#### Legend:

R = Readable bit      W = Writable bit      U = Unimplemented bit, read as '0'  
u = Bit is unchanged      x = Bit is unknown      -n/n = Value at POR and BOR/Value at all other Resets  
'1' = Bit is set      '0' = Bit is cleared

- bit 7-0      **DAC1R<7:0>:** DAC1 Voltage Output Select bits

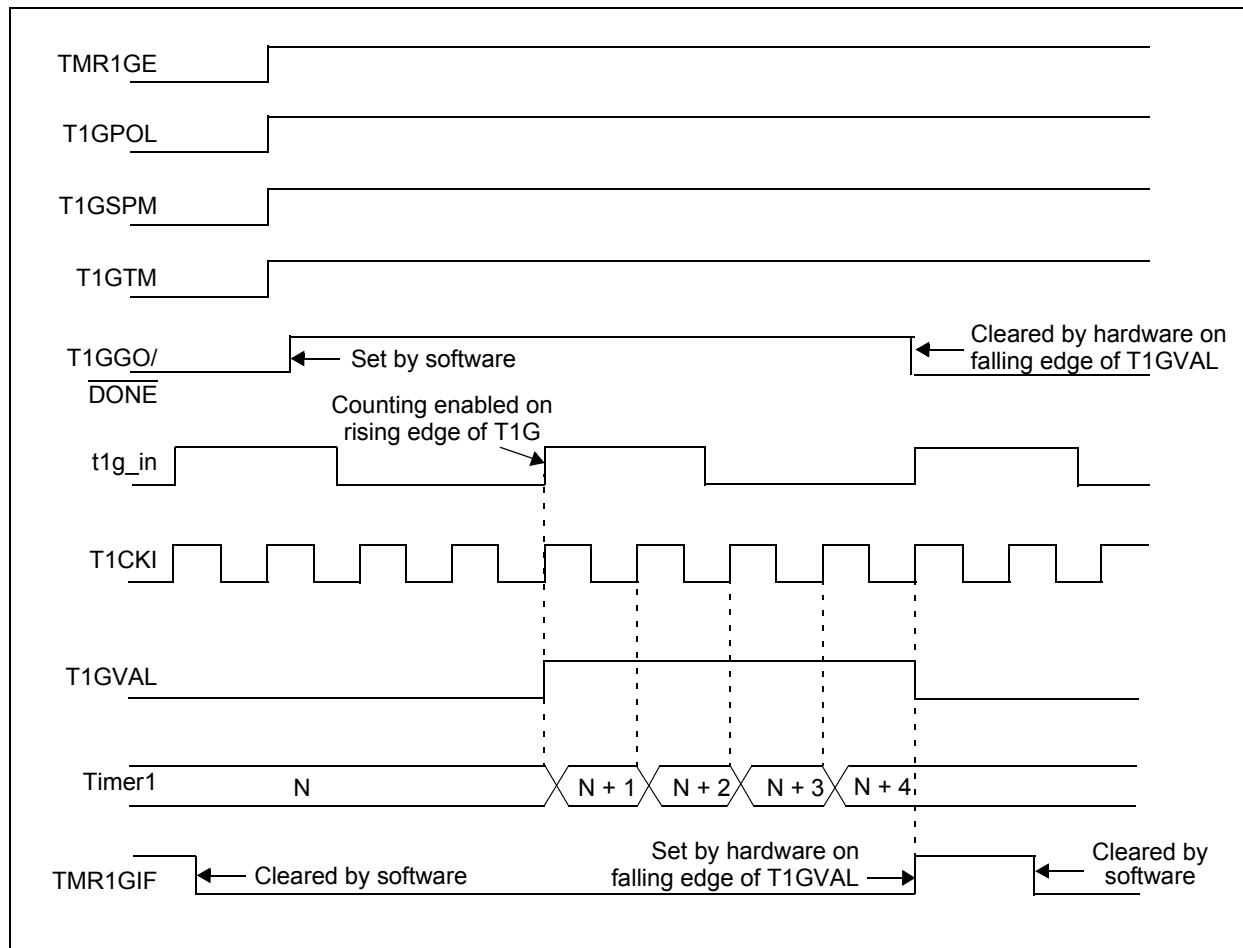
### TABLE 23-1: SUMMARY OF REGISTERS ASSOCIATED WITH THE DAC1 MODULE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on page
DAC1CON0	DAC1EN	—	DAC1OE1	DAC1OE2	DAC1PSS<1:0>	—	DAC1NSS		260
DAC1CON1	DAC1R<7:0>								260

**Legend:** — = Unimplemented location, read as '0'. Shaded cells are not used with the DAC module.

# PIC16(L)F1717/8/9

**FIGURE 27-6: TIMER1 GATE SINGLE-PULSE AND TOGGLE COMBINED MODE**



## 31.1.2.4 Receive Framing Error

Each character in the receive FIFO buffer has a corresponding framing error Status bit. A framing error indicates that a Stop bit was not seen at the expected time. The framing error status is accessed via the FERR bit of the RC1STA register. The FERR bit represents the status of the top unread character in the receive FIFO. Therefore, the FERR bit must be read before reading the RC1REG.

The FERR bit is read-only and only applies to the top unread character in the receive FIFO. A framing error (FERR = 1) does not preclude reception of additional characters. It is not necessary to clear the FERR bit. Reading the next character from the FIFO buffer will advance the FIFO to the next character and the next corresponding framing error.

The FERR bit can be forced clear by clearing the SPEN bit of the RC1STA register which resets the EUSART. Clearing the CREN bit of the RC1STA register does not affect the FERR bit. A framing error by itself does not generate an interrupt.

<b>Note:</b> If all receive characters in the receive FIFO have framing errors, repeated reads of the RC1REG will not clear the FERR bit.
-------------------------------------------------------------------------------------------------------------------------------------------

## 31.1.2.5 Receive Overrun Error

The receive FIFO buffer can hold two characters. An overrun error will be generated if a third character, in its entirety, is received before the FIFO is accessed. When this happens the OERR bit of the RC1STA register is set. The characters already in the FIFO buffer can be read but no additional characters will be received until the error is cleared. The error must be cleared by either clearing the CREN bit of the RC1STA register or by resetting the EUSART by clearing the SPEN bit of the RC1STA register.

## 31.1.2.6 Receiving 9-Bit Characters

The EUSART supports 9-bit character reception. When the RX9 bit of the RC1STA register is set the EUSART will shift nine bits into the RSR for each character received. The RX9D bit of the RC1STA register is the ninth and Most Significant data bit of the top unread character in the receive FIFO. When reading 9-bit data from the receive FIFO buffer, the RX9D data bit must be read before reading the eight Least Significant bits from the RC1REG.

## 31.1.2.7 Address Detection

A special Address Detection mode is available for use when multiple receivers share the same transmission line, such as in RS-485 systems. Address detection is enabled by setting the ADDEN bit of the RC1STA register.

Address detection requires 9-bit character reception. When address detection is enabled, only characters with the ninth data bit set will be transferred to the receive FIFO buffer, thereby setting the RCIF interrupt bit. All other characters will be ignored.

Upon receiving an address character, user software determines if the address matches its own. Upon address match, user software must disable address detection by clearing the ADDEN bit before the next Stop bit occurs. When user software detects the end of the message, determined by the message protocol used, software places the receiver back into the Address Detection mode by setting the ADDEN bit.

# PIC16(L)F1717/8/9

## 31.3 Register Definitions: EUSART Control

### REGISTER 31-1: TX1STA: TRANSMIT STATUS AND CONTROL REGISTER

R/W-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R-1/1	R/W-0/0
CSRC	TX9	TXEN <sup>(1)</sup>	SYNC	SENDB	BRGH	TRMT	TX9D
bit 7							bit 0

#### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

- bit 7      **CSRC:** Clock Source Select bit  
Asynchronous mode:  
Don't care  
Synchronous mode:  
1 = Master mode (clock generated internally from BRG)  
0 = Slave mode (clock from external source)
- bit 6      **TX9:** 9-bit Transmit Enable bit  
1 = Selects 9-bit transmission  
0 = Selects 8-bit transmission
- bit 5      **TXEN:** Transmit Enable bit<sup>(1)</sup>  
1 = Transmit enabled  
0 = Transmit disabled
- bit 4      **SYNC:** EUSART Mode Select bit  
1 = Synchronous mode  
0 = Asynchronous mode
- bit 3      **SENDB:** Send Break Character bit  
Asynchronous mode:  
1 = Send Sync Break on next transmission (cleared by hardware upon completion)  
0 = Sync Break transmission completed  
Synchronous mode:  
Don't care
- bit 2      **BRGH:** High Baud Rate Select bit  
Asynchronous mode:  
1 = High speed  
0 = Low speed  
Synchronous mode:  
Unused in this mode
- bit 1      **TRMT:** Transmit Shift Register Status bit  
1 = TSR empty  
0 = TSR full
- bit 0      **TX9D:** Ninth bit of Transmit Data  
Can be address/data bit or a parity bit.

**Note 1:** SREN/CREN overrides TXEN in Sync mode.

## 31.4.2 AUTO-BAUD OVERFLOW

During the course of automatic baud detection, the ABDOVF bit of the BAUD1CON register will be set if the baud rate counter overflows before the fifth rising edge is detected on the RX pin. The ABDOVF bit indicates that the counter has exceeded the maximum count that can fit in the 16 bits of the SPxBRGH:SPxBRGL register pair. The overflow condition will set the RCIF flag. The counter continues to count until the fifth rising edge is detected on the RX pin. The RCIDL bit will remain false ('0') until the fifth rising edge at which time the RCIDL bit will be set. If the RC1REG is read after the overflow occurs, but before the fifth rising edge, the fifth rising edge will set the RCIF again.

Terminating the auto-baud process early to clear an overflow condition will prevent proper detection of the sync character's fifth rising edge. If any falling edges of the sync character have not yet occurred when the ABDEN bit is cleared, those will be falsely detected as start bits. The following steps are recommended to clear the overflow condition:

1. Read RCREG to clear RCIF.
2. If RCIDL is zero then wait for RCIF and repeat step 1.
3. Clear the ABDOVF bit.

## 31.4.3 AUTO-WAKE-UP ON BREAK

During Sleep mode, all clocks to the EUSART are suspended. Because of this, the Baud Rate Generator is inactive and a proper character reception cannot be performed. The Auto-Wake-up feature allows the controller to wake-up due to activity on the RX/DT line. This feature is available only in Asynchronous mode.

The Auto-Wake-up feature is enabled by setting the WUE bit of the BAUD1CON register. Once set, the normal receive sequence on RX/DT is disabled, and the EUSART remains in an Idle state, monitoring for a wake-up event independent of the CPU mode. A wake-up event consists of a high-to-low transition on the RX/DT line. (This coincides with the start of a Sync Break or a wake-up signal character for the LIN protocol.)

The EUSART module generates an RCIF interrupt coincident with the wake-up event. The interrupt is generated synchronously to the Q clocks in normal CPU operating modes (Figure 31-7), and asynchronously if the device is in Sleep mode (Figure 31-8). The interrupt condition is cleared by reading the RC1REG register.

The WUE bit is automatically cleared by the low-to-high transition on the RX line at the end of the Break. This signals to the user that the Break event is over. At this point, the EUSART module is in Idle mode waiting to receive the next character.

## 31.4.3.1 Special Considerations

### Break Character

To avoid character errors or character fragments during a wake-up event, the wake-up character must be all zeros.

When the wake-up is enabled the function works independent of the low time on the data stream. If the WUE bit is set and a valid non-zero character is received, the low time from the Start bit to the first rising edge will be interpreted as the wake-up event. The remaining bits in the character will be received as a fragmented character and subsequent characters can result in framing or overrun errors.

Therefore, the initial character in the transmission must be all '0's. This must be ten or more bit times, 13-bit times recommended for LIN bus, or any number of bit times for standard RS-232 devices.

### Oscillator Start-up Time

Oscillator start-up time must be considered, especially in applications using oscillators with longer start-up intervals (i.e., LP, XT or HS/PLL mode). The Sync Break (or wake-up signal) character must be of sufficient length, and be followed by a sufficient interval, to allow enough time for the selected oscillator to start and provide proper initialization of the EUSART.

### WUE Bit

The wake-up event causes a receive interrupt by setting the RCIF bit. The WUE bit is cleared in hardware by a rising edge on RX/DT. The interrupt condition is then cleared in software by reading the RC1REG register and discarding its contents.

To ensure that no actual data is lost, check the RCIDL bit to verify that a receive operation is not in process before setting the WUE bit. If a receive operation is not occurring, the WUE bit may then be set just prior to entering the Sleep mode.



## 33.2 Instruction Descriptions

### ADDFSR Add Literal to FSRn

Syntax:	[ <i>label</i> ] ADDFSR FSRn, k
Operands:	$-32 \leq k \leq 31$ $n \in [0, 1]$
Operation:	$FSR(n) + k \rightarrow FSR(n)$
Status Affected:	None
Description:	The signed 6-bit literal 'k' is added to the contents of the FSRnH:FSRnL register pair.  FSRn is limited to the range 0000h-FFFFh. Moving beyond these bounds will cause the FSR to wrap-around.

### ANDLW AND literal with W

Syntax:	[ <i>label</i> ] ANDLW k
Operands:	$0 \leq k \leq 255$
Operation:	$(W) .AND. (k) \rightarrow (W)$
Status Affected:	Z
Description:	The contents of W register are AND'ed with the 8-bit literal 'k'. The result is placed in the W register.

### ADDLW Add literal and W

Syntax:	[ <i>label</i> ] ADDLW k
Operands:	$0 \leq k \leq 255$
Operation:	$(W) + k \rightarrow (W)$
Status Affected:	C, DC, Z
Description:	The contents of the W register are added to the 8-bit literal 'k' and the result is placed in the W register.

### ANDWF AND W with f

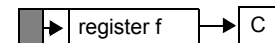
Syntax:	[ <i>label</i> ] ANDWF f,d
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	$(W) .AND. (f) \rightarrow (\text{destination})$
Status Affected:	Z
Description:	AND the W register with register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

### ADDWF Add W and f

Syntax:	[ <i>label</i> ] ADDWF f,d
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	$(W) + (f) \rightarrow (\text{destination})$
Status Affected:	C, DC, Z
Description:	Add the contents of the W register with register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

### ASRF Arithmetic Right Shift

Syntax:	[ <i>label</i> ] ASRF f {,d}
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	$(f<7>) \rightarrow \text{dest}<7>$ $(f<7:1>) \rightarrow \text{dest}<6:0>$ , $(f<0>) \rightarrow C$ ,
Status Affected:	C, Z
Description:	The contents of register 'f' are shifted one bit to the right through the Carry flag. The MSb remains unchanged. If 'd' is '0', the result is placed in W. If 'd' is '1', the result is stored back in register 'f'.



### ADDWFC ADD W and CARRY bit to f

Syntax:	[ <i>label</i> ] ADDWFC f {,d}
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	$(W) + (f) + (C) \rightarrow \text{dest}$
Status Affected:	C, DC, Z
Description:	Add W, the Carry flag and data memory location 'f'. If 'd' is '0', the result is placed in W. If 'd' is '1', the result is placed in data memory location 'f'.

# PIC16(L)F1717/8/9

**TABLE 34-2: SUPPLY CURRENT ( $I_{DD}$ )<sup>(1,2)</sup>**

PIC16LF1717/8/9		Standard Operating Conditions (unless otherwise stated)					
PIC16F1717/8/9							
Param. No.	Device Characteristics	Min.	Typ.†	Max.	Units	Conditions	
						VDD	Note
D009	LDO Regulator	—	75	—	μA	—	High-Power mode, normal operation
		—	15	—	μA	—	Sleep, VREGCON<1> = 0
		—	0.3	—	μA	—	Sleep, VREGCON<1> = 1
D010		—	8	—	μA	1.8	Fosc = 32 kHz, LP Oscillator mode ( <b>Note 4</b> ), -40°C ≤ Ta ≤ +85°C
		—	12	—	μA	3.0	
D010		—	15	—	μA	2.3	Fosc = 32 kHz, LP Oscillator mode ( <b>Note 4, Note 5</b> ), -40°C ≤ Ta ≤ +85°C
		—	17	—	μA	3.0	
		—	21	—	μA	5.0	
D012		—	140	—	μA	1.8	Fosc = 4 MHz, XT Oscillator mode
		—	250	—	μA	3.0	
D012		—	210	—	μA	2.3	Fosc = 4 MHz, XT Oscillator mode ( <b>Note 5</b> )
		—	280	—	μA	3.0	
		—	340	—	μA	5.0	
D014		—	115	—	μA	1.8	Fosc = 4 MHz, External Clock (ECM), Medium Power mode
		—	210	—	μA	3.0	
D014		—	180	—	μA	2.3	Fosc = 4 MHz, External Clock (ECM), Medium Power mode ( <b>Note 5</b> )
		—	240	—	μA	3.0	
		—	300	—	μA	5.0	
D015		—	2.1	—	mA	3.0	Fosc = 32 MHz, External Clock (ECH), High-Power mode
		—	2.5	—	mA	3.6	
D015		—	2.1	—	mA	3.0	Fosc = 32 MHz, External Clock (ECH), High-Power mode ( <b>Note 5</b> )
		—	2.2	—	mA	5.0	

† Data in “Typ” column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

- Note 1:** The test conditions for all  $I_{DD}$  measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD;  $\overline{MCLR}$  = VDD; WDT disabled.
- 2:** The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption.
- 3:** For RC oscillator configurations, current through REXT is not included. The current through the resistor can be extended by the formula  $I_R = V_{DD}/2R_{EXT}$  (mA) with REXT in kΩ.
- 4:** FVR and BOR are disabled.
- 5:** 0.1 μF capacitor on VCAP.
- 6:** 8 MHz clock with 4x PLL enabled.

## 35.0 DC AND AC CHARACTERISTICS GRAPHS AND CHARTS

The graphs and tables provided in this section are for **design guidance** and are **not tested**.

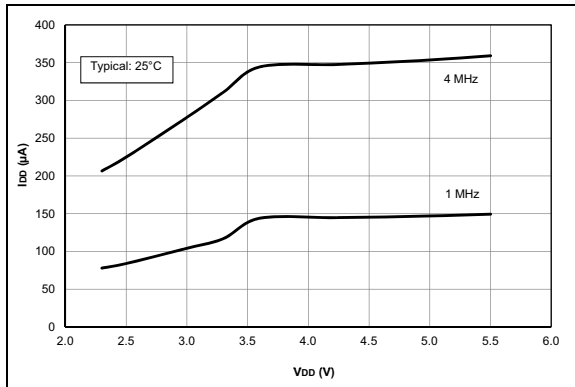
In some graphs or tables, the data presented are **outside specified operating range** (i.e., outside specified  $V_{DD}$  range). This is for **information only** and devices are ensured to operate properly only within the specified range.

Unless otherwise noted, all graphs apply to both the L and LF devices.

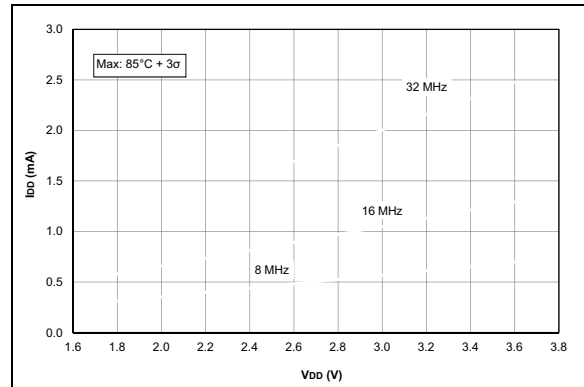
<b>Note:</b>	The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore, outside the warranted range.
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**“Typical” represents the mean of the distribution at 25°C. “Maximum”, “Max.”, “Minimum” or “Min.” represents  $(\text{mean} + 3\sigma)$  or  $(\text{mean} - 3\sigma)$  respectively, where  $\sigma$  is a standard deviation, over each temperature range.**

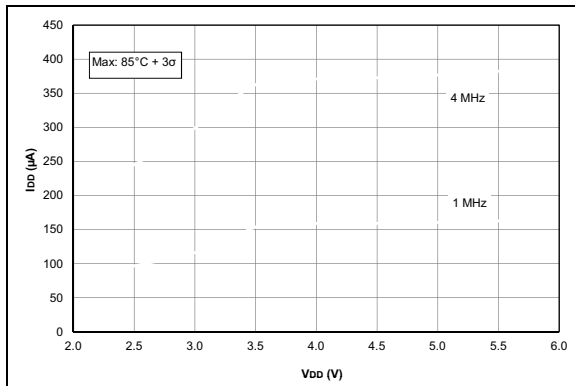
**Note:** Unless otherwise noted,  $V_{IN} = 5V$ ,  $F_{OSC} = 500\text{ kHz}$ ,  $C_{IN} = 0.1\text{ }\mu\text{F}$ ,  $T_A = 25^\circ\text{C}$ .



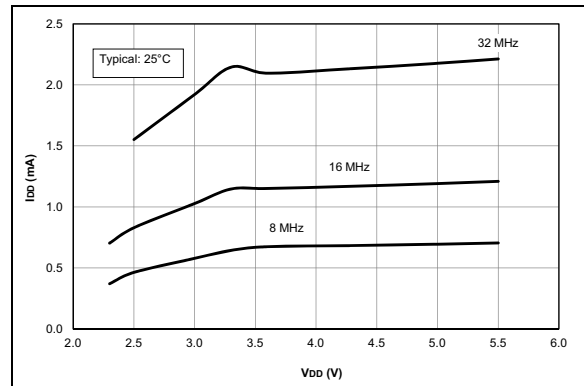
**FIGURE 35-13:**  $I_{DD}$  Typical, EC Oscillator MP Mode, PIC16F1717/8/9 Only.



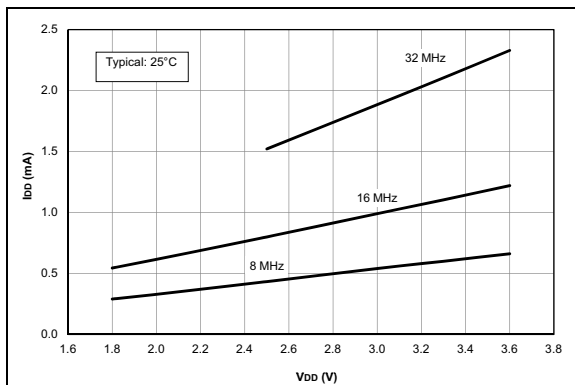
**FIGURE 35-16:**  $I_{DD}$  Maximum, EC Oscillator HP Mode, PIC16LF1717/8/9 Only.



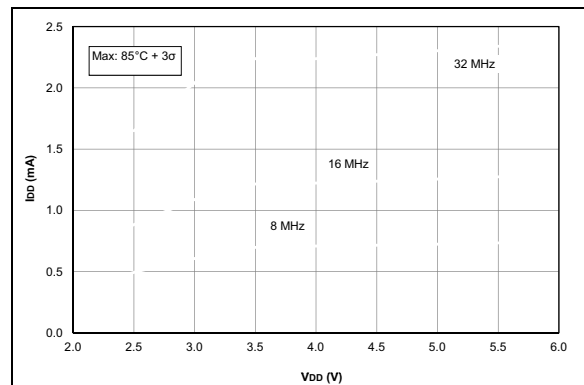
**FIGURE 35-14:**  $I_{DD}$  Maximum, EC Oscillator MP Mode, PIC16F1717/8/9 Only.



**FIGURE 35-17:**  $I_{DD}$  Typical, EC Oscillator HP Mode, PIC16F1717/8/9 Only.



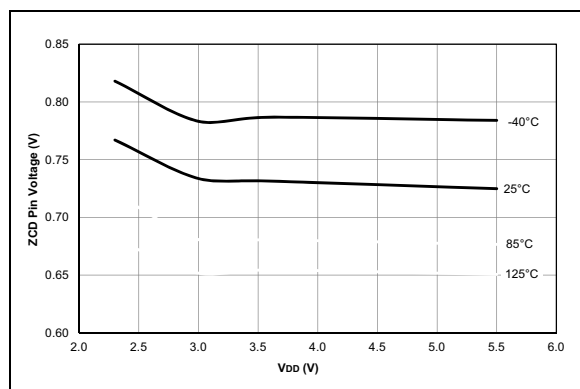
**FIGURE 35-15:**  $I_{DD}$  Typical, EC Oscillator HP Mode, PIC16LF1717/8/9 Only.



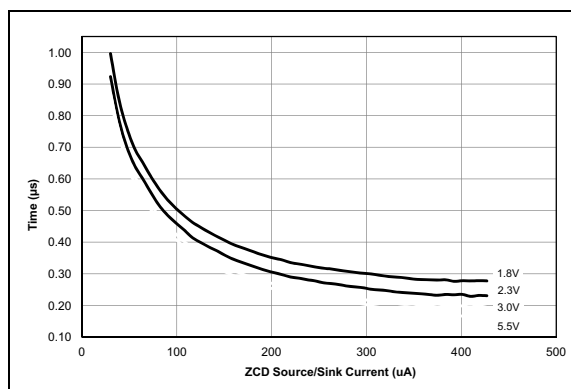
**FIGURE 35-18:**  $I_{DD}$  Maximum, EC Oscillator HP Mode, PIC16F1717/8/9 Only.

# PIC16(L)F1717/8/9

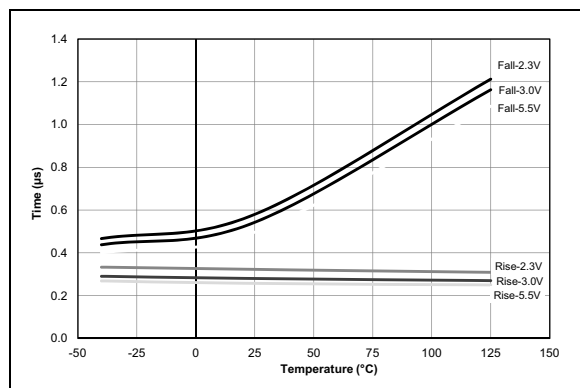
**Note:** Unless otherwise noted,  $V_{IN} = 5V$ ,  $F_{OSC} = 500\text{ kHz}$ ,  $C_{IN} = 0.1\text{ }\mu F$ ,  $T_A = 25^\circ C$ .



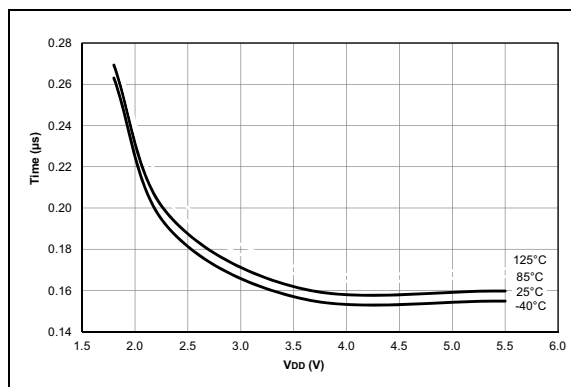
**FIGURE 35-115:** ZCD Pin Voltage, Typical Measured Values



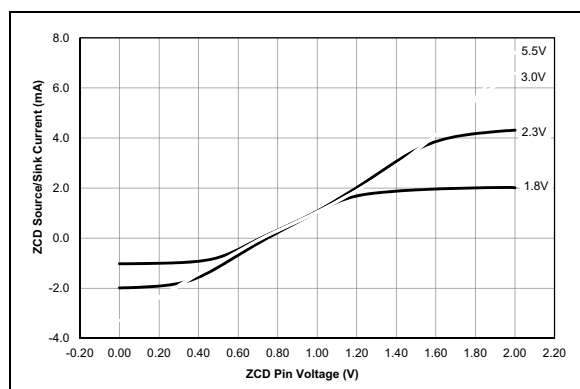
**FIGURE 35-118:** ZCD Pin Response Time Over Current, Typical Measured Values From  $-40^\circ C$  to  $125^\circ C$ .



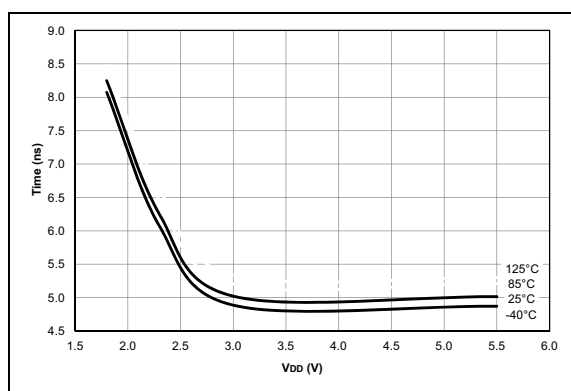
**FIGURE 35-116:** ZCD Response Time Over Voltage, Typical Measured Values.



**FIGURE 35-119:** COG Dead-Band Delay,  $DBR/DBF = 32$ , Typical Measured Values



**FIGURE 35-117:** ZCD Pin Current Over ZCD Pin Voltage, Typical Measured Values From  $-40^\circ C$  to  $125^\circ C$ .



**FIGURE 35-120:** COG Dead-Band  $DBR/DBF$  Delay Per Step, Typical Measured Values.