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Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	24
Program Memory Size	28KB (16K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 17x10b; D/A 1x5b, 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf1718t-i-ss

3.4.5 CORE FUNCTION REGISTERS SUMMARY

The Core Function registers listed in Table 3-11 can be addressed from any Bank.

TABLE 3-11: CORE FUNCTION REGISTERS SUMMARY (1)

Addr.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
Bank 0-31											
x00h or x80h	INDF0	Addressing this location uses contents of FSR0H/FSR0L to address data memory (not a physical register)								xxxx xxxx	uuuu uuuu
x01h or x81h	INDF1	Addressing this location uses contents of FSR1H/FSR1L to address data memory (not a physical register)								xxxx xxxx	uuuu uuuu
x02h or x82h	PCL	Program Counter (PC) Least Significant Byte								0000 0000	0000 0000
x03h or x83h	STATUS	—	—	—	$\overline{TO}$	$\overline{PD}$	Z	DC	C	---1 1000	---q quuu
x04h or x84h	FSR0L	Indirect Data Memory Address 0 Low Pointer								0000 0000	uuuu uuuu
x05h or x85h	FSR0H	Indirect Data Memory Address 0 High Pointer								0000 0000	0000 0000
x06h or x86h	FSR1L	Indirect Data Memory Address 1 Low Pointer								0000 0000	uuuu uuuu
x07h or x87h	FSR1H	Indirect Data Memory Address 1 High Pointer								0000 0000	0000 0000
x08h or x88h	BSR	—	—	—	BSR4	BSR3	BSR2	BSR1	BSR0	---0 0000	---0 0000
x09h or x89h	WREG	Working Register								0000 0000	uuuu uuuu
x0Ah or x8Ah	PCLATH	—	Write Buffer for the upper 7 bits of the Program Counter							-000 0000	-000 0000
x0Bh or x8Bh	INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	0000 0000	0000 0000

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations are unimplemented, read as '0'.

Note 1: These registers can be addressed from any bank.

TABLE 3-12: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Addr.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
Bank 29											
E8Ch — E8Fh	—	Unimplemented								—	—
E90h	RA0PPS	—	—	—	RA0PPS<4:0>					---0 0000	---u uuuu
E91h	RA1PPS	—	—	—	RA1PPS<4:0>					---0 0000	---u uuuu
E92h	RA2PPS	—	—	—	RA2PPS<4:0>					---0 0000	---u uuuu
E93h	RA3PPS	—	—	—	RA3PPS4:0>					---0 0000	---u uuuu
E94h	RA4PPS	—	—	—	RA4PPS<4:0>					---0 0000	---u uuuu
E95h	RA5PPS	—	—	—	RA5PPS<4:0>					---0 0000	---u uuuu
E96h	RA6PPS	—	—	—	RA6PPS<4:0>					---0 0000	---u uuuu
E97h	RA7PPS	—	—	—	RA7PPS<4:0>					---0 0000	---u uuuu
E98h	RB0PPS	—	—	—	RB0PPS<4:0>					---0 0000	---u uuuu
E99h	RB1PPS	—	—	—	RB1PPS<4:0>					---0 0000	---u uuuu
E9Ah	RB2PPS	—	—	—	RB2PPS<4:0>					---0 0000	---u uuuu
E9Bh	RB3PPS	—	—	—	RB3PPS<4:0>					---0 0000	---u uuuu
E9Ch	RB4PPS	—	—	—	RB4PPS<4:0>					---0 0000	---u uuuu
E9Dh	RB5PPS	—	—	—	RB5PPS<4:0>					---0 0000	---u uuuu
E9Eh	RB6PPS	—	—	—	RB6PPS<4:0>					---0 0000	---u uuuu
E9Fh	RB7PPS	—	—	—	RB7PPS<4:0>					---0 0000	---u uuuu
EA0h	RC0PPS	—	—	—	RC0PPS<4:0>					---0 0000	---u uuuu
EA1h	RC1PPS	—	—	—	RC1PPS<4:0>					---0 0000	---u uuuu
EA2h	RC2PPS	—	—	—	RC2PPS<4:0>					---0 0000	---u uuuu
EA3h	RC3PPS	—	—	—	RC3PPS<4:0>					---0 0000	---u uuuu
EA4h	RC4PPS	—	—	—	RC4PPS<4:0>					---0 0000	---u uuuu
EA5h	RC5PPS	—	—	—	RC5PPS<4:0>					---0 0000	---u uuuu
EA6h	RC6PPS	—	—	—	RC6PPS<4:0>					---0 0000	---u uuuu
EA7h	RC7PPS	—	—	—	RC7PPS<4:0>					---0 0000	---u uuuu
EA8h	RD0PPS(1)	—	—	—	RD0PPS<4:0>					---0 0000	---u uuuu
EA9h	RD1PPS(1)	—	—	—	RD1PPS<4:0>					---0 0000	---u uuuu
EAAh	RD2PPS(1)	—	—	—	RD2PPS<4:0>					---0 0000	---u uuuu
EABh	RD3PPS(1)	—	—	—	RD3PPS<4:0>					---0 0000	---u uuuu
EACh	RD4PPS(1)	—	—	—	RD4PPS<4:0>					---0 0000	---u uuuu
EADh	RD5PPS(1)	—	—	—	RD5PPS<4:0>					---0 0000	---u uuuu
EAEh	RD6PPS(1)	—	—	—	RD6PPS<4:0>					---0 0000	---u uuuu
EAFh	RD7PPS(1)	—	—	—	RD7PPS<4:0>					---0 0000	---u uuuu
EB0h	RE0PPS(1)	—	—	—	RE0PPS<4:0>					---0 0000	---u uuuu
EB1h	RE1PPS(1)	—	—	—	RE1PPS<4:0>					---0 0000	---u uuuu
EB2h	RE2PPS(1)	—	—	—	RE2PPS<4:0>					---0 0000	---u uuuu
EB3h — EEFh	—	Unimplemented								—	—

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations are unimplemented, read as '0'.

Note 1: Unimplemented on PIC16(L)F1718.

2: Unimplemented on PIC16LF1717/8/9

FIGURE 6-7: INTERNAL OSCILLATOR SWITCH TIMING

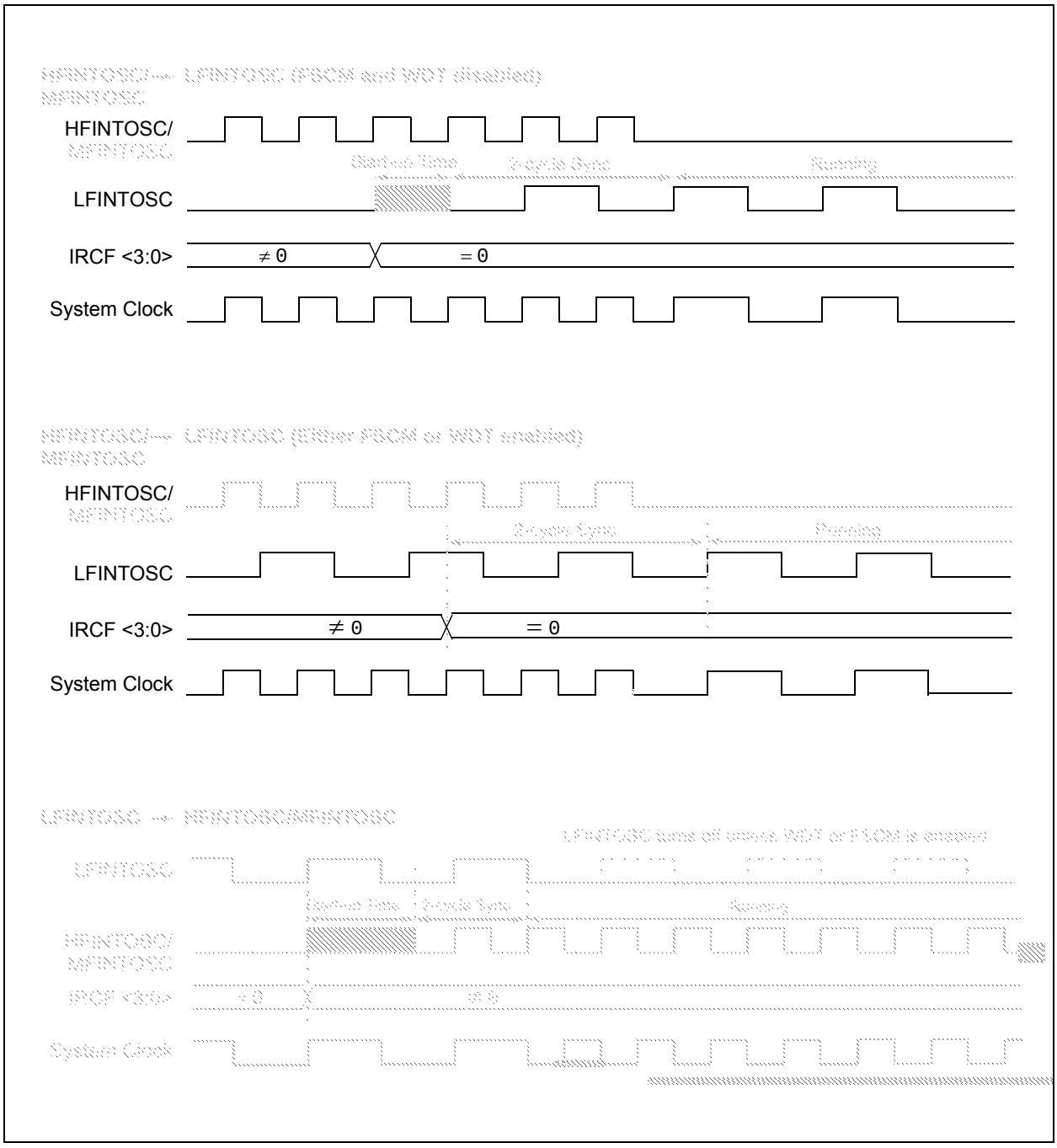
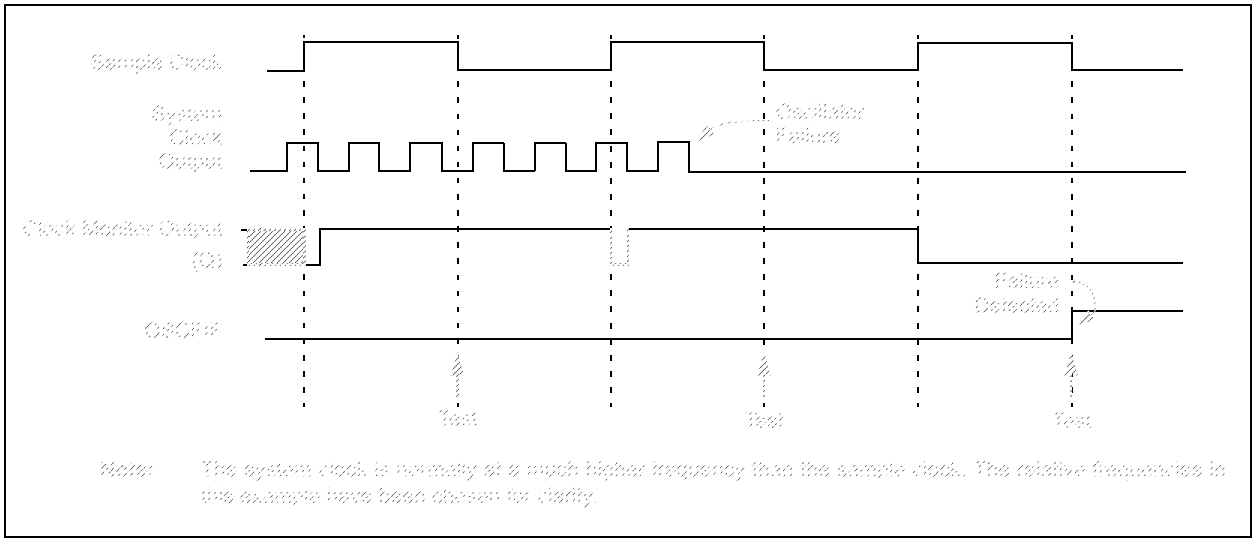


FIGURE 6-10: FSCM TIMING DIAGRAM



Note: The system clock is normally at a much higher frequency than the sample clock. The relative frequencies in this example have been chosen for clarity.

EXAMPLE 10-3: WRITING TO FLASH PROGRAM MEMORY

```
; This write routine assumes the following:
; 1. 64 bytes of data are loaded, starting at the address in DATA_ADDR
; 2. Each word of data to be written is made up of two adjacent bytes in DATA_ADDR,
; stored in little endian format
; 3. A valid starting address (the least significant bits = 00000) is loaded in ADDRH:ADDRL
; 4. ADDRH and ADDRL are located in shared data memory 0x70 - 0x7F (common RAM)
;
        BCF         INTCON,GIE      ; Disable ints so required sequences will execute properly
        BANKSEL     PMADRH          ; Bank 3
        MOVF        ADDRH,W         ; Load initial address
        MOVWF       PMADRH          ;
        MOVF        ADDRL,W         ;
        MOVWF       PMADRL          ;
        MOVLW       LOW DATA_ADDR   ; Load initial data address
        MOVWF       FSR0L           ;
        MOVLW       HIGH DATA_ADDR  ; Load initial data address
        MOVWF       FSR0H           ;
        BCF         PMCON1,CFGS     ; Not configuration space
        BSF         PMCON1,WREN     ; Enable writes
        BSF         PMCON1,LWLO     ; Only Load Write Latches
LOOP
        MOVIW       FSR0++          ; Load first data byte into lower
        MOVWF       PMDATL          ;
        MOVIW       FSR0++          ; Load second data byte into upper
        MOVWF       PMDATH          ;

        MOVF        PMADRL,W        ; Check if lower bits of address are '00000'
        XORLW       0x1F            ; Check if we're on the last of 32 addresses
        ANDLW       0x1F            ;
        BTFSC       STATUS,Z        ; Exit if last of 32 words,
        GOTO        START_WRITE     ;

  Required Sequence
        MOVLW       55h             ; Start of required write sequence:
        MOVWF       PMCON2          ; Write 55h
        MOVLW       0AAh            ;
        MOVWF       PMCON2          ; Write AAh
        BSF         PMCON1,WR       ; Set WR bit to begin write
        NOP                         ; NOP instructions are forced as processor
                                    ; loads program memory write latches
        NOP                         ;

        INCF        PMADRL,F        ; Still loading latches Increment address
        GOTO        LOOP            ; Write next latches

START_WRITE
        BCF         PMCON1,LWLO     ; No more loading latches - Actually start Flash program
                                    ; memory write

  Required Sequence
        MOVLW       55h             ; Start of required write sequence:
        MOVWF       PMCON2          ; Write 55h
        MOVLW       0AAh            ;
        MOVWF       PMCON2          ; Write AAh
        BSF         PMCON1,WR       ; Set WR bit to begin write
        NOP                         ; NOP instructions are forced as processor writes
                                    ; all the program memory write latches simultaneously
        NOP                         ; to program memory.
                                    ; After NOPs, the processor
                                    ; stalls until the self-write process in complete
                                    ; after write processor continues with 3rd instruction
        BCF         PMCON1,WREN     ; Disable writes
        BSF         INTCON,GIE      ; Enable interrupts
```

REGISTER 11-3: LATA: PORTA DATA LATCH REGISTER

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
LATA7	LATA6	LATA5	LATA4	LATA3	LATA2	LATA1	LATA0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **LATA<7:0>:** RA<7:0> Output Latch Value bits(1)

Note 1: Writes to PORTA are actually written to corresponding LATA register. Reads from PORTA register is return of actual I/O pin values.

REGISTER 11-4: ANSELA: PORTA ANALOG SELECT REGISTER

U-0	U-0	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1
—	—	ANSA5	ANSA4	ANSA3	ANSA2	ANSA1	ANSA0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **ANSA<5:0>**: Analog Select between Analog or Digital Function on Pins RA<5:0>, respectively
1 = Analog input. Pin is assigned as analog input(1). Digital input buffer disabled.
0 = Digital I/O. Pin is assigned to port or digital special function.

Note 1: When setting a pin to an analog input, the corresponding TRIS bit must be set to Input mode in order to allow external control of the voltage on the pin.

TABLE 11-4: SUMMARY OF REGISTERS ASSOCIATED WITH PORTB

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ANSELB	—	—	ANSB5	ANSB4	ANSB3	ANSB2	ANSB1	ANSB0	131
INLVLB	INLVLB7	INLVLB6	INLVLB5	INLVLB4	INLVLB3	INLVLB2	INLVLB1	INLVLB0	132
LATB	LATB7	LATB6	LATB5	LATB4	LATB3	LATB2	LATB1	LATB0	130
ODCONB	ODB7	ODB6	ODB5	ODB4	ODB3	ODB2	ODB1	ODB0	132
PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	130
SLRCONB	SLRB7	SLRB6	SLRB5	SLRB4	SLRB3	SLRB2	SLRB1	SLRB0	132
TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	130
WPUB	WPUB7	WPUB6	WPUB5	WPUB4	WPUB3	WPUB2	WPUB1	WPUB0	131

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by PORTB.

12.8 Register Definitions: PPS Input Selection

REGISTER 12-1: xxxPPS: PERIPHERAL xxx INPUT SELECTION

U-0	U-0	U-0	R/W-q/u	R/W-q/u	R/W-q/u	R/W-q/u	R/W-q/u
—	—	—	xxxPPS<4:0>				
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	q = value depends on peripheral

bit 7-5 **Unimplemented:** Read as ‘0’

bit 4-3 **xxxPPS<4:3>:** Peripheral xxx Input PORTx Selection bits
See Table 12-1 for the list of available ports for each peripheral.
11 = Peripheral input is from PORTD (PIC16(L)F1717/9 only)
10 = Peripheral input is from PORTC
01 = Peripheral input is from PORTB
00 = Peripheral input is from PORTA

bit 2-0 **xxxPPS<2:0>:** Peripheral xxx Input PORTx Bit Selection bits
111 = Peripheral input is from PORTx Bit 7 (Rx7)
110 = Peripheral input is from PORTx Bit 6 (Rx6)
101 = Peripheral input is from PORTx Bit 5 (Rx5)
100 = Peripheral input is from PORTx Bit 4 (Rx4)
011 = Peripheral input is from PORTx Bit 3 (Rx3)
010 = Peripheral input is from PORTx Bit 2 (Rx2)
001 = Peripheral input is from PORTx Bit 1 (Rx1)
000 = Peripheral input is from PORTx Bit 0 (Rx0)

TABLE 12-1: AVAILABLE PORTS FOR INPUT BY PERIPHERAL

Peripheral	Register	PIC16(L)F1717/8/9		PIC16(L)F1718	PIC16(L)F1717/9	
		PORTA	PORTB	PORTC	PORTC	PORTD
PIN interrupt	INTPPS	●	●			
Timer0 clock	T0CKIPPS	●	●			
Timer1 clock	T1CKIPPS	●		●	●	
Timer1 gate	T1GPPS		●	●	●	
CCP1	CCP1PPS		●	●	●	
CCP2	CCP2PPS		●	●	●	
COG	COGINPPS		●	●		●
MSSP	SSPCLKPPS		●	●	●	
MSSP	SSPDATPPS		●	●	●	
MSSP	SSPSSPPS	●		●		●
EUSART	RXPPS		●	●	●	
EUSART	CKPPS		●	●	●	
All CLCs	CLCIN0PPS	●		●	●	
All CLCs	CLCIN1PPS	●		●	●	
All CLCs	CLCIN2PPS		●	●		●
All CLCs	CLCIN3PPS		●	●		●
Example: CCP1PPS = 0x0B selects RB3 as the input to CCP1.						

Note: Inputs are not available on all ports. A check in a port column of a peripheral row indicates that the port selection is valid for that peripheral. Unsupported ports will input a ‘0’.

15.4 ADC Acquisition Time

To ensure accurate temperature measurements, the user must wait at least 200 μs after the ADC input multiplexer is connected to the temperature indicator output before the conversion is performed. In addition, the user must wait 200 μs between sequential conversions of the temperature indicator output.

TABLE 15-2: SUMMARY OF REGISTERS ASSOCIATED WITH THE TEMPERATURE INDICATOR

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on page
FVRCON	FVREN	FVRRDY	TSEN	TSRNG	CDFVR<1:0>		ADFVR<1:0>		165

Legend: Shaded cells are unused by the temperature indicator module.

REGISTER 16-2: CMxCON1: COMPARATOR Cx CONTROL REGISTER 1

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
CxINTP	CxINTN	CxPCH<2:0>			CxNCH<2:0>		
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7 **CxINTP:** Comparator Interrupt on Positive Going Edge Enable bits
1 = The CxIF interrupt flag will be set upon a positive going edge of the CxOUT bit
0 = No interrupt flag will be set on a positive going edge of the CxOUT bit

bit 6 **CxINTN:** Comparator Interrupt on Negative Going Edge Enable bits
1 = The CxIF interrupt flag will be set upon a negative going edge of the CxOUT bit
0 = No interrupt flag will be set on a negative going edge of the CxOUT bit

bit 5-3 **CxPCH<2:0>:** Comparator Positive Input Channel Select bits
111 = CxVP connects to AGND
110 = CxVP connects to FVR Buffer 2
101 = CxVP connects to DAC1_output
100 = CxVP connects to DAC2_output
011 = CxVP unconnected, input floating
010 = CxVP unconnected, input floating
001 = CxVP connects to CxIN1+ pin
000 = CxVP connects to CxIN0+ pin

bit 2-0 **CxNCH<2:0>:** Comparator Negative Input Channel Select bits
111 = CxVN connects to AGND
110 = CxVN connects to FVR Buffer 2
101 = CxVN unconnected, input floating
100 = CxVN unconnected, input floating
011 = CxVN connects to CxIN3- pin
010 = CxVN connects to CxIN2- pin
001 = CxVN connects to CxIN1- pin
000 = CxVN connects to CxIN0- pin

REGISTER 18-14: COGxPHR: COG RISING EDGE PHASE DELAY COUNT REGISTER

U-0	U-0	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
—	—	GxPHR<5:0>					
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	q = Value depends on condition

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **GxPHR<5:0>:** Rising Edge Phase Delay Count Value bits
= Number of COGx clock periods to delay rising edge event

REGISTER 18-15: COGxPHF: COG FALLING EDGE PHASE DELAY COUNT REGISTER

U-0	U-0	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
—	—	GxPHF<5:0>					
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	q = Value depends on condition

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **GxPHF<5:0>:** Falling Edge Phase Delay Count Value bits
= Number of COGx clock periods to delay falling edge event

REGISTER 21-3: ADCON2: ADC CONTROL REGISTER 2

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	U-0	U-0	U-0	U-0
TRIGSEL<3:0>(1)				—	—	—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-4 **TRIGSEL<3:0>:** Auto-Conversion Trigger Selection bits(1)

0000 = No auto-conversion trigger selected
0001 = CCP1
0010 = CCP2
0011 = Timer0 – T0_overflow(2)
0100 = Timer1 – T1_overflow(2)
0101 = Timer2 – T2_match
0110 = Comparator C1 – sync_C1OUT
0111 = Comparator C2 – sync_C2OUT
1000 = CLC1 – LC1_out
1001 = CLC2 – LC2_out
1010 = CLC3 – LC3_out
1011 = CLC4 – LC4_out
1100 = Timer4 – T4_match
1101 = Timer6 – T6_match
1110 = Reserved
1111 = Reserved

bit 3-0 **Unimplemented:** Read as '0'

Note 1: This is a rising edge sensitive input for all sources.
2: Signal also sets its corresponding interrupt flag.

REGISTER 21-4: ADRESH: ADC RESULT REGISTER HIGH (ADRESH) ADFM = 0

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
ADRES<9:2>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **ADRES<9:2>**: ADC Result Register bits
Upper eight bits of 10-bit conversion result

25.0 ZERO-CROSS DETECTION (ZCD) MODULE

The ZCD module detects when an A/C signal crosses through the ground potential. The actual zero-crossing threshold is the zero-crossing reference voltage, ZCPINV, which is typically 0.75 V above ground.

The connection to the signal to be detected is through a series current limiting resistor. The module applies a current source or sink to the ZCD pin to maintain a constant voltage on the pin, thereby preventing the pin voltage from forward biasing the ESD protection diodes. When the applied voltage is greater than the reference voltage, the module sinks current. When the applied voltage is less than the reference voltage, the module sources current. The current source and sink action keeps the pin voltage constant over the full range of the applied voltage. The ZCD module is shown in the simplified block diagram Figure 25-2.

The ZCD module is useful when monitoring an AC waveform for, but not limited to, the following purposes:

- A/C period measurement
- Accurate long term time measurement
- Dimmer phase delayed drive
- Low EMI cycle switching

25.1 External Resistor Selection

The ZCD module requires a current limiting resistor in series with the external voltage source. The impedance and rating of this resistor depends on the external source peak voltage. Select a resistor value that will drop all of the peak voltage when the current through the resistor is nominally 300 µA. Refer to Equation 25-1 and Figure 25-1. Make sure that the ZCD I/O pin internal weak pull-up is disabled so it doesn't interfere with the current source and sink.

EQUATION 25-1: EXTERNAL RESISTOR

$$R_{series} = \frac{V_{peak}}{3\times10^{-4}}$$

FIGURE 25-1: EXTERNAL VOLTAGE

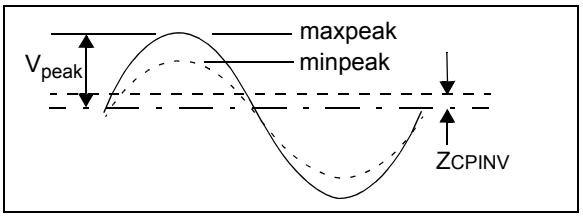


FIGURE 25-2: SIMPLIFIED ZCD BLOCK DIAGRAM

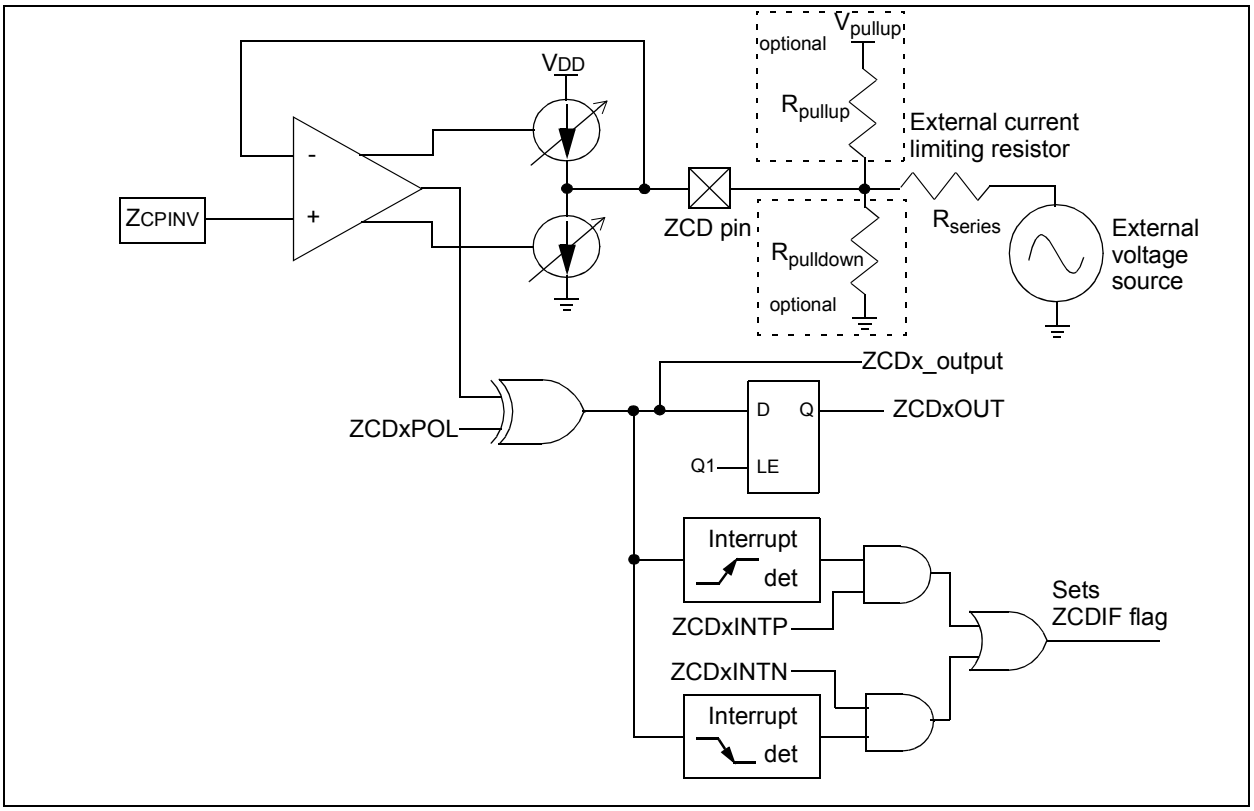


FIGURE 27-3: TIMER1 GATE ENABLE MODE

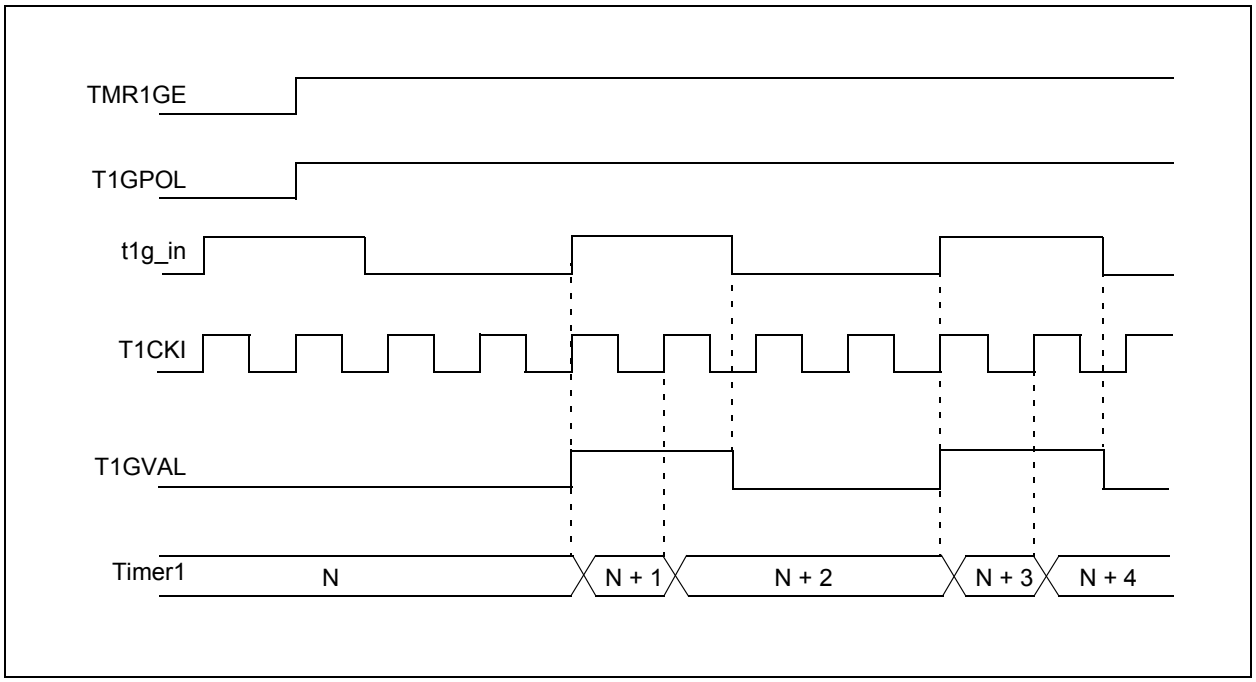
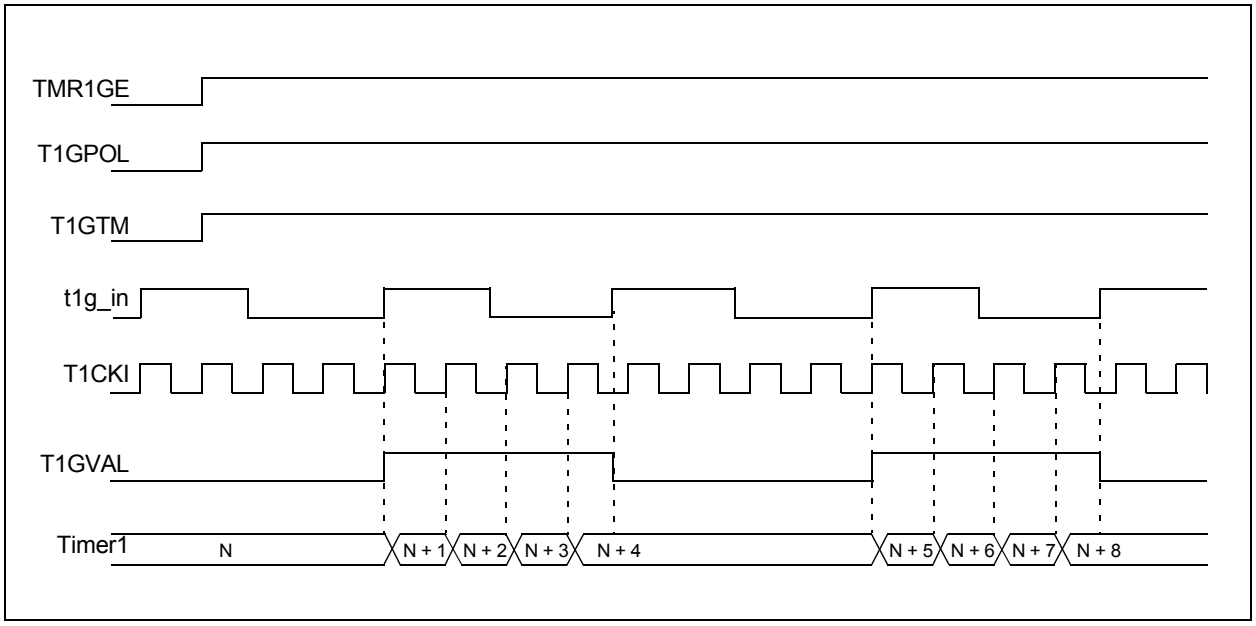


FIGURE 27-4: TIMER1 GATE TOGGLE MODE



30.8 Register Definitions: MSSP Control

REGISTER 30-1: SSP1STAT: SSP STATUS REGISTER

R/W-0/0	R/W-0/0	R-0/0	R-0/0	R-0/0	R-0/0	R-0/0	R-0/0
SMP	CKE	D/$\overline{A}$	P	S	R/$\overline{W}$	UA	BF
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **SMP:** SPI Data Input Sample bit
SPI Master mode:
1 = Input data sampled at end of data output time
0 = Input data sampled at middle of data output time
SPI Slave mode:
SMP must be cleared when SPI is used in Slave mode
In I^2C Master or Slave mode:
1 = Slew rate control disabled for Standard Speed mode (100 kHz and 1 MHz)
0 = Slew rate control enabled for High-Speed mode (400 kHz)

bit 6 **CKE:** SPI Clock Edge Select bit (SPI mode only)
In SPI Master or Slave mode:
1 = Transmit occurs on transition from active to Idle clock state
0 = Transmit occurs on transition from Idle to active clock state
In I^2C™ mode only:
1 = Enable input logic so that thresholds are compliant with SMBus specification
0 = Disable SMBus specific inputs

bit 5 **D/$\overline{A}$:** Data/$\overline{Address}$ bit (I^2C mode only)
1 = Indicates that the last byte received or transmitted was data
0 = Indicates that the last byte received or transmitted was address

bit 4 **P:** Stop bit
(I^2C mode only. This bit is cleared when the MSSP module is disabled, SSPEN is cleared.)
1 = Indicates that a Stop bit has been detected last (this bit is '0' on Reset)
0 = Stop bit was not detected last

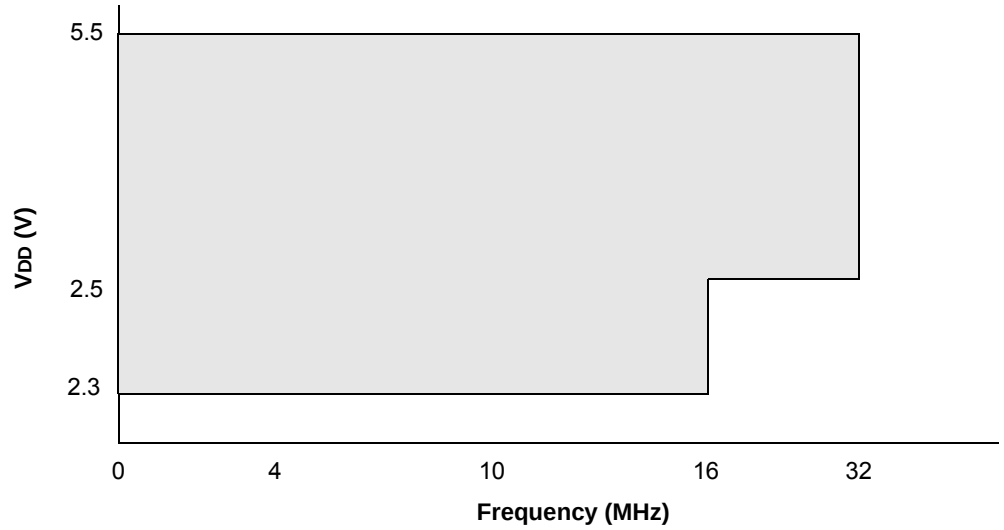
bit 3 **S:** Start bit
(I^2C mode only. This bit is cleared when the MSSP module is disabled, SSPEN is cleared.)
1 = Indicates that a Start bit has been detected last (this bit is '0' on Reset)
0 = Start bit was not detected last

bit 2 **R/$\overline{W}$:** Read/$\overline{Write}$ bit information (I^2C mode only)
This bit holds the R/$\overline{W}$ bit information following the last address match. This bit is only valid from the address match to the next Start bit, Stop bit, or not ACK bit.
In I^2C Slave mode:
1 = Read
0 = Write
In I^2C Master mode:
1 = Transmit is in progress
0 = Transmit is not in progress
OR-ing this bit with SEN, RSEN, PEN, RCEN or ACKEN will indicate if the MSSP is in Idle mode.

bit 1 **UA:** Update Address bit (10-bit I^2C mode only)
1 = Indicates that the user needs to update the address in the SSP1ADD register
0 = Address does not need to be updated

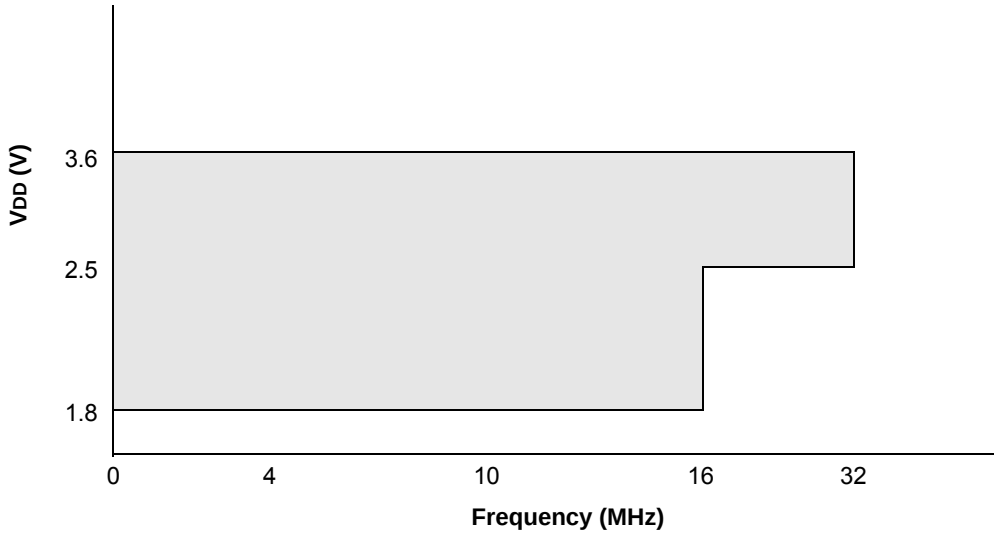
bit 0 **BF:** Buffer Full Status bit
Receive (SPI and I^2C modes):
1 = Receive complete, SSP1BUF is full
0 = Receive not complete, SSP1BUF is empty
Transmit (I^2C mode only):
1 = Data transmit in progress (does not include the $\overline{ACK}$ and Stop bits), SSP1BUF is full
0 = Data transmit complete (does not include the $\overline{ACK}$ and Stop bits), SSP1BUF is empty

FIGURE 34-1: VOLTAGE FREQUENCY GRAPH, -40°C ≤ TA ≤ +125°C, PIC16F1717/8/9 ONLY



Note 1: The shaded region indicates the permissible combinations of voltage and frequency.
2: Refer to Table 34-7 for each Oscillator mode's supported frequencies.

FIGURE 34-2: VOLTAGE FREQUENCY GRAPH, -40°C ≤ TA ≤ +125°C, PIC16LF1717/8/9 ONLY



Note 1: The shaded region indicates the permissible combinations of voltage and frequency.
2: Refer to Table 34-7 for each Oscillator mode's supported frequencies.

TABLE 34-2: SUPPLY CURRENT (I_{DD})(1,2)

PIC16LF1717/8/9		Standard Operating Conditions (unless otherwise stated)					
PIC16F1717/8/9							
Param. No.	Device Characteristics	Min.	Typ.†	Max.	Units	Conditions	
						V_{DD}	Note
D009	LDO Regulator	—	75	—	μA	—	High-Power mode, normal operation
		—	15	—	μA	—	Sleep, VREGCON<1> = 0
		—	0.3	—	μA	—	Sleep, VREGCON<1> = 1
D010		—	8	—	μA	1.8	F_{OSC} = 32 kHz, LP Oscillator mode (**Note 4**), -40°C ≤ T_A ≤ +85°C
		—	12	—	μA	3.0	
D010		—	15	—	μA	2.3	F_{OSC} = 32 kHz, LP Oscillator mode (**Note 4, Note 5**), -40°C ≤ T_A ≤ +85°C
		—	17	—	μA	3.0	
		—	21	—	μA	5.0	
D012		—	140	—	μA	1.8	F_{OSC} = 4 MHz, XT Oscillator mode
		—	250	—	μA	3.0	
D012		—	210	—	μA	2.3	F_{OSC} = 4 MHz, XT Oscillator mode (**Note 5**)
		—	280	—	μA	3.0	
		—	340	—	μA	5.0	
D014		—	115	—	μA	1.8	F_{OSC} = 4 MHz, External Clock (ECM), Medium Power mode
		—	210	—	μA	3.0	
D014		—	180	—	μA	2.3	F_{OSC} = 4 MHz, External Clock (ECM), Medium Power mode (**Note 5**)
		—	240	—	μA	3.0	
		—	300	—	μA	5.0	
D015		—	2.1	—	mA	3.0	F_{OSC} = 32 MHz, External Clock (ECH), High-Power mode
		—	2.5	—	mA	3.6	
D015		—	2.1	—	mA	3.0	F_{OSC} = 32 MHz, External Clock (ECH), High-Power mode (**Note 5**)
		—	2.2	—	mA	5.0	

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The test conditions for all I_{DD} measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to V_{DD}; $\overline{MCLR}$ = V_{DD}; WDT disabled.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption.

3: For RC oscillator configurations, current through R_{EXT} is not included. The current through the resistor can be extended by the formula IR = $V_{DD}/2R_{EXT}$ (mA) with R_{EXT} in kΩ

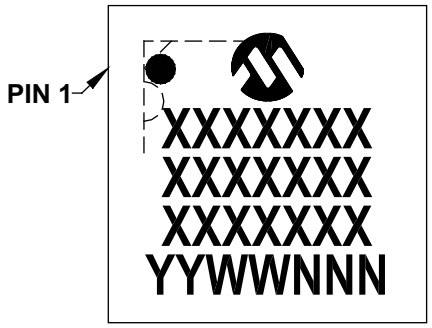
4: FVR and BOR are disabled.

5: 0.1 μF capacitor on V_{CAP}.

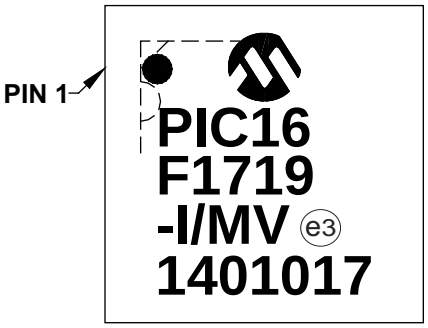
6: 8 MHz clock with 4x PLL enabled.

Package Marking Information (Continued)

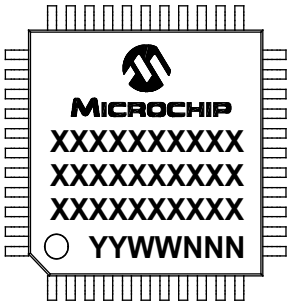
40-Lead UQFN (5x5x0.5 mm)



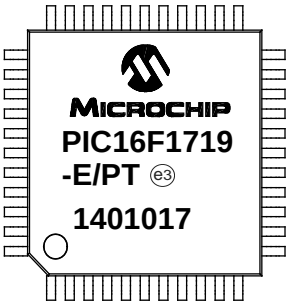
Example



44-Lead TQFP (10x10x1 mm)



Example

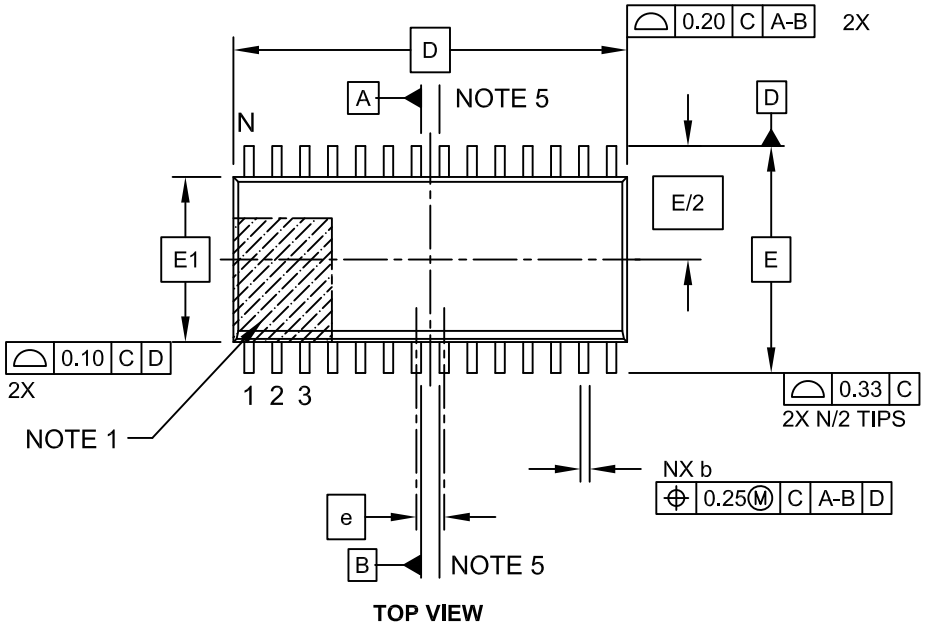


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

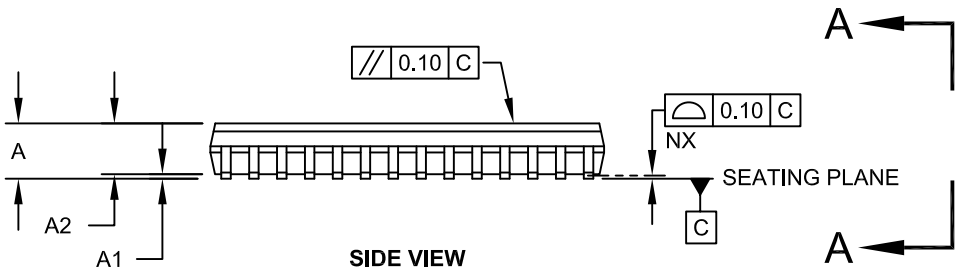
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

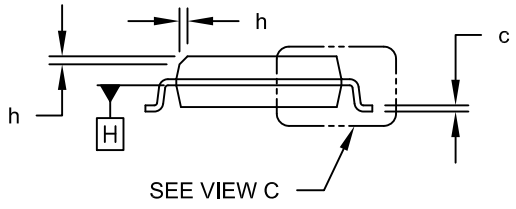
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

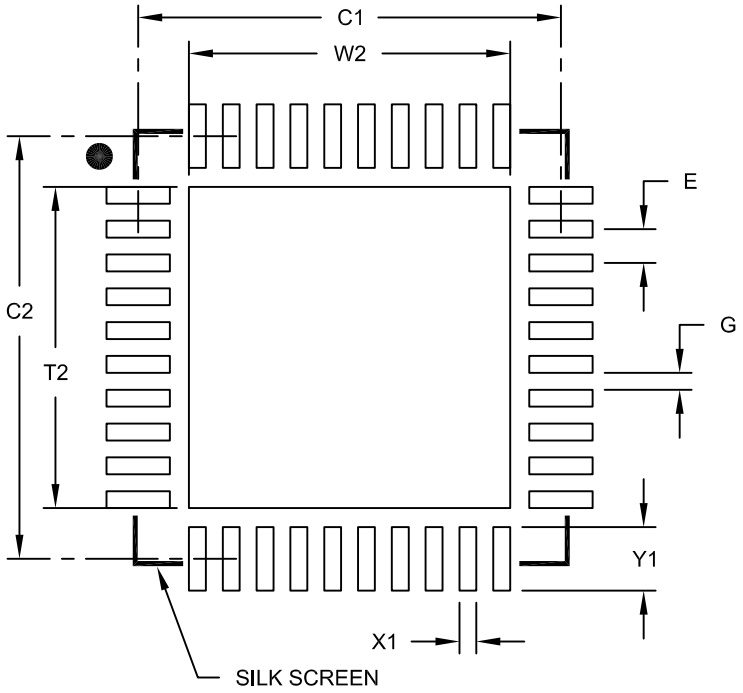


VIEW A-A

Microchip Technology Drawing C04-052C Sheet 1 of 2

40-Lead Plastic Ultra Thin Quad Flat, No Lead Package (MV) - 5x5 mm Body [UQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.40 BSC	
Optional Center Pad Width	W2			3.80
Optional Center Pad Length	T2			3.80
Contact Pad Spacing	C1		5.00	
Contact Pad Spacing	C2		5.00	
Contact Pad Width (X40)	X1			0.20
Contact Pad Length (X40)	Y1			0.75
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2156B