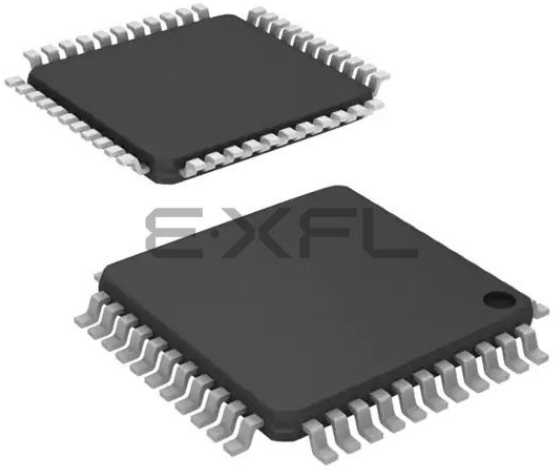

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	35
Program Memory Size	28KB (16K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 28x10b; D/A 1x5b, 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf1719t-i-pt

TABLE 1: 28-PIN ALLOCATION TABLE (PIC16(L)F1718)

I/O(2)	SPDIP,SOIC, SSOP	QFN, UQFN	ADC	Reference	Comparator	Op Amp	DAC	Zero Cross	Timers	CCP	NCO	PWM	COG	MSSP	EUSART	CLC	Interrupt	Pull-up	Basic
RA0	2	27	AN0		C1IN0- C2IN0-											CLCIN0(1)	IOC	Y	
RA1	3	28	AN1		C1IN1- C2IN1-	OPA1OUT										CLCIN1(1)	IOC	Y	
RA2	4	1	AN2	V_{REF}-	C1IN0+ C2IN0+		DAC1OUT1										IOC	Y	
RA3	5	2	AN3	V_{REF}+	C1IN1+												IOC	Y	
RA4	6	3				OPA1IN+			T0CKI(1)								IOC	Y	
RA5	7	4	AN4			OPA1IN-	DAC2OUT1							nSS(1)			IOC	Y	
RA6	10	7															IOC	Y	OSC2 CLKOUT
RA7	9	6															IOC	Y	OSC1 CLKIN
RB0	21	18	AN12		C2IN1+			ZCD					COG1IN(1)				INT(1) IOC	Y	
RB1	22	19	AN10		C1IN3- C2IN3-	OPA2OUT											IOC	Y	
RB2	23	20	AN8			OPA2IN-											IOC	Y	
RB3	24	21	AN9		C1IN2- C2IN2-	OPA2IN+											IOC	Y	
RB4	25	22	AN11														IOC	Y	
RB5	26	23	AN13						T1G(1)								IOC	Y	
RB6	27	24														CLCIN2(1)	IOC	Y	ICSPCLK
RB7	28	25					DAC1OUT2 DAC2OUT2									CLCIN3(1)	IOC	Y	ICSPDAT
RC0	11	8							T1CKI(1) SOSCO								IOC	Y	
RC1	12	9							SOSCI	CCP2(1)							IOC	Y	
RC2	13	10	AN14							CCP1(1)							IOC	Y	
RC3	14	11	AN15											SCL/SCK(1)			IOC	Y	

Note 1: Default peripheral input. Alternate pins can be selected as the peripheral input with the PPS input selection registers.

2: All pin digital outputs default to PORT latch data. Alternate outputs can be selected as the peripheral digital output with the PPS output selection registers.

3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

4: Alternate outputs are excluded from solid shaded areas.

5: Alternate inputs are excluded from dot shaded areas.

TABLE 1-3: PIC16(L)F1717/9 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RC4/AN16/SDI(1)/SDA(1)	RC4	TTL/ST	CMOS	General purpose I/O.
	AN16	AN	—	ADC Channel 16 input.
	SDI	TTL/ST	—	SPI Data input.
	SDA(3)	I^2C	—	I^2C Data input.
RC5/AN17	RC5	TTL/ST	CMOS	General purpose I/O.
	AN17	AN	—	ADC Channel 17 input.
RC6/AN18/CK(1)	RC6	TTL/ST	CMOS	General purpose I/O.
	AN18	AN	—	ADC Channel 18 input.
	CK	TTL/ST		EUSART synchronous clock.
RC7/AN19/RX(1)	RC7	TTL/ST	CMOS	General purpose I/O.
	AN19	AN	—	ADC Channel 19 input.
	RX	TTL/ST	—	EUSART receive.
RDO/AN20	RD0	TTL/ST	CMOS	General purpose I/O.
	AN20	AN	—	ADC Channel 20 input.
RD1/AN21	RD1	TTL/ST	CMOS	General purpose I/O.
	AN21	AN	—	ADC Channel 21 input.
RD2/AN22	RD2	TTL/ST	CMOS	General purpose I/O.
	AN22	AN	—	ADC Channel 22 input.
RD3/AN23	RD3	TTL/ST	CMOS	General purpose I/O.
	AN23	AN	—	ADC Channel 23 input.
RD4/AN24	RD4	TTL/ST	CMOS	General purpose I/O.
	AN24	AN	—	ADC Channel 24 input.
RD5/AN25	RD5	TTL/ST	CMOS	General purpose I/O.
	AN25	AN	—	ADC Channel 25 input.
RD6/AN26	RD6	TTL/ST	CMOS	General purpose I/O.
	AN26	AN	—	ADC Channel 26 input.
RD7/AN27	RD7	TTL/ST	CMOS	General purpose I/O.
	AN27	AN	—	ADC Channel 27 input.
RE0/AN5	RE0	TTL/ST	CMOS	General purpose I/O.
	AN5	AN	—	ADC Channel 5 input.
RE1/AN6	RE1	TTL/ST	CMOS	General purpose I/O.
	AN6	AN	—	ADC Channel 6 input.
RE2/AN7	RE2	TTL/ST	CMOS	General purpose I/O.
	AN7	AN	—	ADC Channel 7 input.
RE3/$\overline{MCLR}$/VPP	RE3	TTL/ST	—	General purpose input.
	$\overline{MCLR}$	ST	—	Master clear input.
	VPP	HV	—	Programming voltage.
VDD	VDD	Power	—	Positive supply.
VSS	VSS	Power	—	Ground reference.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open-Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I^2C = Schmitt Trigger input with I^2C
HV = High Voltage XTAL = Crystal levels

Note 1: Default peripheral input. Alternate pins can be selected as the peripheral input with the PPS input selection registers.

2: All pin digital outputs default to PORT latch data. Alternate outputs can be selected as the peripheral digital output with the PPS output selection registers.

3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

3.4.1 SPECIAL FUNCTION REGISTER

The Special Function Registers are registers used by the application to control the desired operation of peripheral functions in the device. The Special Function Registers occupy the 20 bytes after the core registers of every data memory bank (addresses x0Ch/x8Ch through x1Fh/x9Fh). The registers associated with the operation of the peripherals are described in the appropriate peripheral chapter of this data sheet.

3.4.2 GENERAL PURPOSE RAM

There are up to 80 bytes of GPR in each data memory bank. The GPR occupies the 80 bytes after the SFR registers of selected data memory banks.

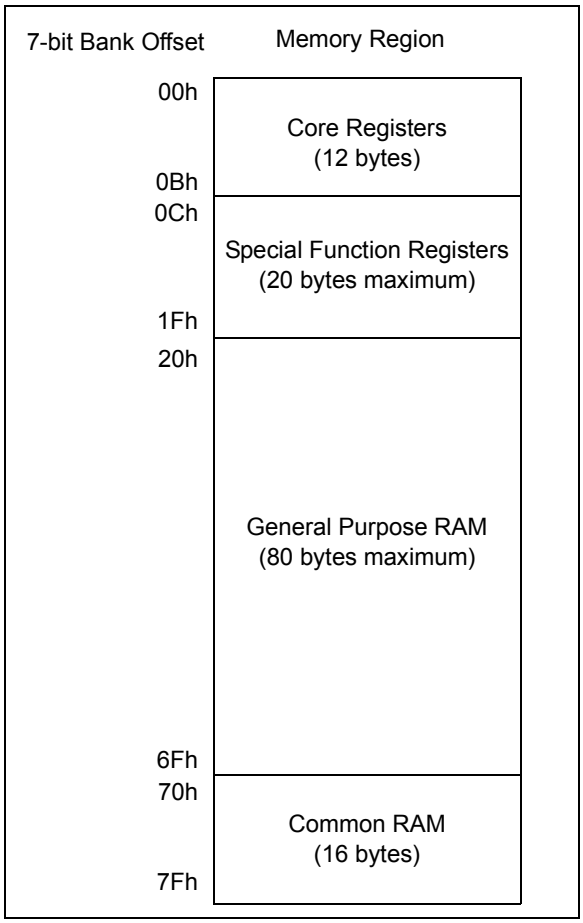
3.4.2.1 Linear Access to GPR

The general purpose RAM can be accessed in a non-banked method via the FSRs. This can simplify access to large memory structures. See **Section 3.7.2 "Linear Data Memory"** for more information.

3.4.3 COMMON RAM

There are 16 bytes of common RAM accessible from all banks.

FIGURE 3-3: BANKED MEMORY PARTITIONING



3.4.4 DEVICE MEMORY MAPS

The memory maps for the device family are as shown in Table 3-3 through Table 3-10.

TABLE 3-8: PIC16(L)F1718/9 MEMORY MAP, BANK 24-31

BANK 24		BANK 25		BANK 26		BANK 27		BANK 28		BANK 29		BANK 30		BANK 31	
C00h	Core Registers (Table 3-2)	C80h	Core Registers (Table 3-2)	D00h	Core Registers (Table 3-2)	D80h	Core Registers (Table 3-2)	E00h	Core Registers (Table 3-2)	E80h	Core Registers (Table 3-2)	F00h	Core Registers (Table 3-2)	F80h	Core Registers (Table 3-2)
C0Bh		C8Bh		D0Bh		D8Bh		E0Bh		E8Bh		F0Bh		F8Bh	
C0Ch	—	C8Ch	—	D0Ch	—	D8Ch	—	E0Ch	See Table 3-9 for register mapping details	E8Ch	See Table 3-9 for register mapping details	F0Ch	See Table 3-9 for register mapping details	F8Ch	See Table 3-10 for register mapping details
C0Dh	—	C8Dh	—	D0Dh	—	D8Dh	—	E0Dh		E8Dh		F0Dh		F8Dh	
C0Eh	—	C8Eh	—	D0Eh	—	D8Eh	—	E0Eh		E8Eh		F0Eh		F8Eh	
C0Fh	—	C8Fh	—	D0Fh	—	D8Fh	—	E0Fh		E8Fh		F0Fh		F8Fh	
C10h	—	C90h	—	D10h	—	D90h	—	E10h		E90h		F10h		F90h	
C11h	—	C91h	—	D11h	—	D91h	—	E11h		E91h		F11h		F91h	
C12h	—	C92h	—	D12h	—	D92h	—	E12h		E92h		F12h		F92h	
C13h	—	C93h	—	D13h	—	D93h	—	E13h		E93h		F13h		F93h	
C14h	—	C94h	—	D14h	—	D94h	—	E14h		E94h		F14h		F94h	
C15h	—	C95h	—	D15h	—	D95h	—	E15h		E95h		F15h		F95h	
C16h	—	C96h	—	D16h	—	D96h	—	E16h		E96h		F16h		F96h	
C17h	—	C97h	—	D17h	—	D97h	—	E17h		E97h		F17h		F97h	
C18h	—	C98h	—	D18h	—	D98h	—	E18h		E98h		F18h		F98h	
C19h	—	C99h	—	D19h	—	D99h	—	E19h		E99h		F19h		F99h	
C1Ah	—	C9Ah	—	D1Ah	—	D9Ah	—	E1Ah		E9Ah		F1Ah		F9Ah	
C1Bh	—	C9Bh	—	D1Bh	—	D9Bh	—	E1Bh		E9Bh		F1Bh		F9Bh	
C1Ch	—	C9Ch	—	D1Ch	—	D9Ch	—	E1Ch		E9Ch		F1Ch		F9Ch	
C1Dh	—	C9Dh	—	D1Dh	—	D9Dh	—	E1Dh		E9Dh		F1Dh		F9Dh	
C1Eh	—	C9Eh	—	D1Eh	—	D9Eh	—	E1Eh		E9Eh		F1Eh		F9Eh	
C1Fh	—	C9Fh	—	D1Fh	—	D9Fh	—	E1Fh		E9Fh		F1Fh		F9Fh	
C20h	General Purpose Register 80 Bytes	CA0h	General Purpose Register 32 Bytes	D20h	Unimplemented Read as '0'	DA0h	Unimplemented Read as '0'	E20h		EA0h		F20h		FA0h	
C6Fh		CBFh		D6Fh		DEFh		E6Fh		EEFh		F6Fh		FEFh	
C70h	Accesses 70h – 7Fh	CC0h	Unimplemented Read as '0'	D70h	Accesses 70h – 7Fh	DF0h	Accesses 70h – 7Fh	E70h	Accesses 70h – 7Fh	EF0h	Accesses 70h – 7Fh	F70h	Accesses 70h – 7Fh	FF0h	Accesses 70h – 7Fh
CFFh		CFFh		D7Fh		DFFh		E7Fh		EFFh		F7Fh		FFFh	

Legend: = Unimplemented data memory locations, read as '0'.

TABLE 3-9: PIC16(L)F1717/8/9 MEMORY MAP, BANK 28-30

	Bank 28		Bank 29		Bank 30
E0Ch	—	E8Ch	—	F0Ch	—
E0Dh	—	E8Dh	—	F0Dh	—
E0Eh	—	E8Eh	—	F0Eh	—
E0Fh	PPSLOCK	E8Fh	—	F0Fh	CLCDATA
E10h	INTPPS	E90h	RA0PPS	F10h	CLC1CON
E11h	T0CKIPPS	E91h	RA1PPS	F11h	CLC1POL
E12h	T1CKIPPS	E92h	RA2PPS	F12h	CLC1SEL0
E13h	T1GPPS	E93h	RA3PPS	F13h	CLC1SEL1
E14h	CCP1PPS	E94h	RA4PPS	F14h	CLC1SEL2
E15h	CCP2PPS	E95h	RA5PPS	F15h	CLC1SEL3
E16h	—	E96h	RA6PPS	F16h	CLC1GLS0
E17h	COGINPPS	E97h	RA7PPS	F17h	CLC1GLS1
E18h	—	E98h	RB0PPS	F18h	CLC1GLS2
E19h	—	E99h	RB1PPS	F19h	CLC1GLS3
E1Ah	—	E9Ah	RB2PPS	F1Ah	CLC2CON
E1Bh	—	E9Bh	RB3PPS	F1Bh	CLC2POL
E1Ch	—	E9Ch	RB4PPS(1)	F1Ch	CLC2SEL0
E1Dh	—	E9Dh	RB5PPS(1)	F1Dh	CLC2SEL1
E1Eh	—	E9Eh	RB6PPS(1)	F1Eh	CLC2SEL2
E1Fh	—	E9Fh	RB7PPS(1)	F1Fh	CLC2SEL3
E20h	SSPCLKPPS	EA0h	RC0PPS	F20h	CLC2GLS0
E21h	SSPDATPPS	EA1h	RC1PPS	F21h	CLC2GLS1
E22h	SSPSSPPS	EA2h	RC2PPS	F22h	CLC2GLS2
E23h	—	EA3h	RC3PPS	F23h	CLC2GLS3
E24h	RXPPS	EA4h	RC4PPS	F24h	CLC3CON
E25h	CKPPS	EA5h	RC5PPS	F25h	CLC3POL
E26h	—	EA6h	RC6PPS	F26h	CLC3SEL0
E27h	—	EA7h	RC7PPS	F27h	CLC3SEL1
E28h	CLCIN0PPS	EA8h	RD0PPS(1)	F28h	CLC3SEL2
E29h	CLCIN1PPS	EA9h	RD1PPS(1)	F29h	CLC3SEL3
E2Ah	CLCIN2PPS	EAAh	RD2PPS(1)	F2Ah	CLC3GLS0
E2Bh	CLCIN3PPS	EABh	RD3PPS(1)	F2Bh	CLC3GLS1
E2Ch	—	EACh	RD4PPS(1)	F2Ch	CLC3GLS2
E2Dh	—	EADh	RD5PPS(1)	F2Dh	CLC3GLS3
E2Eh	—	EAEh	RD6PPS(1)	F2Eh	CLC4CON
E2Fh	—	EAFh	RD7PPS(1)	F2Fh	CLC4POL
E30h	—	EB0h	RE0PPS(1)	F30h	CLC4SEL0
E31h	—	EB1h	RE1PPS(1)	F31h	CLC4SEL1
E32h	—	EB2h	RE2PPS(1)	F32h	CLC4SEL2
E33h	—	EB3h	—	F33h	CLC4SEL3
E34h	—	EB4h	—	F34h	CLC4GLS0
E35h	—	EB5h	—	F35h	CLC4GLS1
E36h	—	EB6h	—	F36h	CLC4GLS2
E37h	—	EB7h	—	F37h	CLC4GLS3
E38h	—	EB8h	—	F38h	—
E39h	—	EB9h	—	F39h	—
E3Ah	—	EBAh	—	F3Ah	—
E3Bh	—	EBBh	—	F3Bh	—
E3Ch	—	EBCh	—	F3Ch	—
E3Dh	—	EBDh	—	F3Dh	—
E3Eh	—	EBEh	—	F3Eh	—
E3Fh	—	EBFh	—	F3Fh	—
E40h	—	EC0h	—	F40h	—
E6Fh		EEFh		F6Fh	

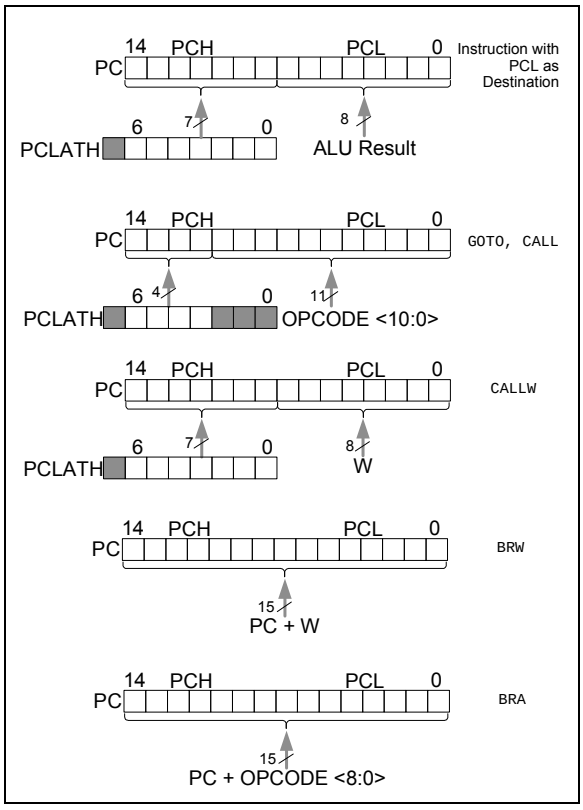
Legend: = Unimplemented data memory locations, read as '0',

Note 1: Only available on PIC16(L)F1717/9 devices.

3.5 PCL and PCLATH

The Program Counter (PC) is 15 bits wide. The low byte comes from the PCL register, which is a readable and writable register. The high byte (PC<14:8>) is not directly readable or writable and comes from PCLATH. On any Reset, the PC is cleared. Figure 3-4 shows the five situations for the loading of the PC.

FIGURE 3-4: LOADING OF PC IN DIFFERENT SITUATIONS



3.5.1 MODIFYING PCL

Executing any instruction with the PCL register as the destination simultaneously causes the Program Counter PC<14:8> bits (PCH) to be replaced by the contents of the PCLATH register. This allows the entire contents of the program counter to be changed by writing the desired upper seven bits to the PCLATH register. When the lower eight bits are written to the PCL register, all 15 bits of the program counter will change to the values contained in the PCLATH register and those being written to the PCL register.

3.5.2 COMPUTED GOTO

A computed GOTO is accomplished by adding an offset to the program counter (ADDWF PCL). When performing a table read using a computed GOTO method, care should be exercised if the table location crosses a PCL memory boundary (each 256-byte block). Refer to Application Note AN556, *"Implementing a Table Read"* (DS00556).

3.5.3 COMPUTED FUNCTION CALLS

A computed function CALL allows programs to maintain tables of functions and provide another way to execute state machines or look-up tables. When performing a table read using a computed function CALL, care should be exercised if the table location crosses a PCL memory boundary (each 256-byte block).

If using the CALL instruction, the PCH<2:0> and PCL registers are loaded with the operand of the CALL instruction. PCH<6:3> is loaded with PCLATH<6:3>.

The CALLW instruction enables computed calls by combining PCLATH and W to form the destination address. A computed CALLW is accomplished by loading the W register with the desired address and executing CALLW. The PCL register is loaded with the value of W and PCH is loaded with PCLATH.

3.5.4 BRANCHING

The branching instructions add an offset to the PC. This allows relocatable code and code that crosses page boundaries. There are two forms of branching, BRW and BRA. The PC will have incremented to fetch the next instruction in both cases. When using either branching instruction, a PCL memory boundary may be crossed.

If using BRW, load the W register with the desired unsigned address and execute BRW. The entire PC will be loaded with the address PC + 1 + W.

If using BRA, the entire PC will be loaded with PC + 1 +, the signed value of the operand of the BRA instruction.

5.0 RESETS

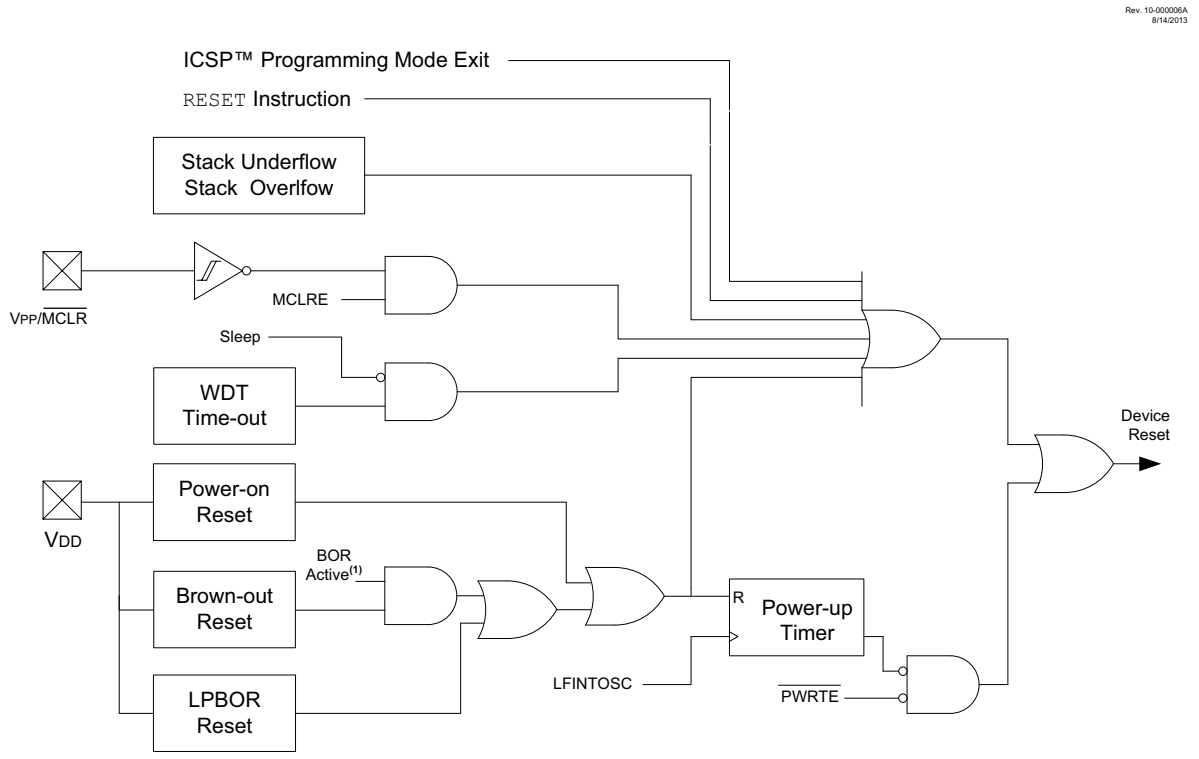
There are multiple ways to reset this device:

- Power-on Reset (POR)
- Brown-out Reset (BOR)
- Low-Power Brown-out Reset (LPBOR)
- MCLR Reset
- WDT Reset
- RESET instruction
- Stack Overflow
- Stack Underflow
- Programming mode exit

To allow VDD to stabilize, an optional Power-up Timer can be enabled to extend the Reset time after a BOR or POR event.

A simplified block diagram of the On-Chip Reset Circuit is shown in Figure 5-1.

FIGURE 5-1: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT



Note 1: See Table 5-1 for BOR active conditions.

6.4 Two-Speed Clock Start-up Mode

Two-Speed Start-up mode provides additional power savings by minimizing the latency between external oscillator start-up and code execution. In applications that make heavy use of the Sleep mode, Two-Speed Start-up will remove the external oscillator start-up time from the time spent awake and can reduce the overall power consumption of the device. This mode allows the application to wake-up from Sleep, perform a few instructions using the INTOSC internal oscillator block as the clock source and go back to Sleep without waiting for the external oscillator to become stable.

Two-Speed Start-up provides benefits when the oscillator module is configured for LP, XT or HS modes. The Oscillator Start-up Timer (OST) is enabled for these modes and must count 1024 oscillations before the oscillator can be used as the system clock source.

If the oscillator module is configured for any mode other than LP, XT or HS mode, then Two-Speed Start-up is disabled. This is because the external clock oscillator does not require any stabilization time after POR or an exit from Sleep.

If the OST count reaches 1024 before the device enters Sleep mode, the OSTS bit of the OSCSTAT register is set and program execution switches to the external oscillator. However, the system may never operate from the external oscillator if the time spent awake is very short.

Note:	Executing a SLEEP instruction will abort the oscillator start-up time and will cause the OSTS bit of the OSCSTAT register to remain clear.

6.4.1 TWO-SPEED START-UP MODE CONFIGURATION

Two-Speed Start-up mode is configured by the following settings:

- IESO (of the Configuration Words) = 1; Internal/External Switchover bit (Two-Speed Start-up mode enabled).
- SCS (of the OSCCON register) = 00.
- FOSC<2:0> bits in the Configuration Words configured for LP, XT or HS mode.

Two-Speed Start-up mode is entered after:

- Power-on Reset (POR) and, if enabled, after Power-up Timer (PWRT) has expired, or
- Wake-up from Sleep.

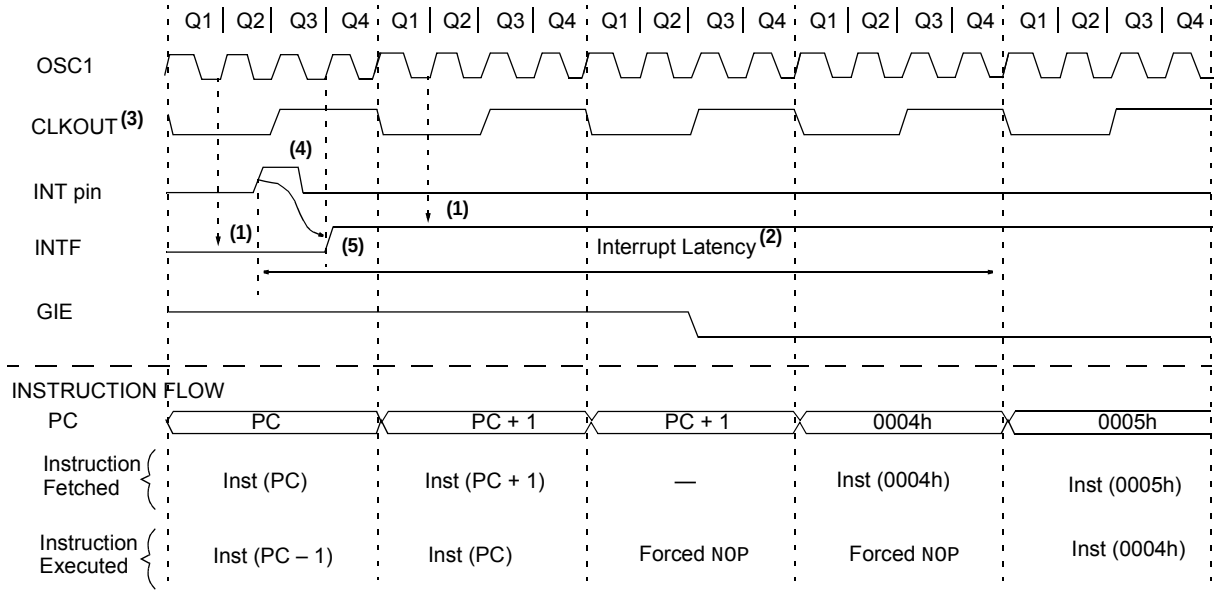
TABLE 6-1: OSCILLATOR SWITCHING DELAYS

Switch From	Switch To	Frequency	Oscillator Delay
Sleep	LFINTOSC(1) MFINTOSC(1) HFINTOSC(1)	31 kHz 31.25 kHz-500 kHz 31.25 kHz-16 MHz	Oscillator Warm-up Delay (TWARM)(2)
Sleep/POR	EC, RC(1)	DC – 32 MHz	2 cycles
LFINTOSC	EC, RC(1)	DC – 32 MHz	1 cycle of each
Sleep/POR	Secondary Oscillator LP, XT, HS(1)	32 kHz-20 MHz	1024 Clock Cycles (OST)
Any clock source	MFINTOSC(1) HFINTOSC(1)	31.25 kHz-500 kHz 31.25 kHz-16 MHz	2 μs (approx.)
Any clock source	LFINTOSC(1)	31 kHz	1 cycle of each
Any clock source	Secondary Oscillator	32 kHz	1024 Clock Cycles (OST)
PLL inactive	PLL active	16-32 MHz	2 ms (approx.)

Note 1: PLL inactive.

2: See **Section 34.0 “Electrical Specifications”**.

FIGURE 7-3: INT PIN INTERRUPT TIMING



Note 1: INTF flag is sampled here (every Q1).

2: Asynchronous interrupt latency = 3-5 TCY. Synchronous latency = 3-4 TCY, where TCY = instruction cycle time. Latency is the same whether Inst (PC) is a single cycle or a 2-cycle instruction.

3: CLKOUT not available in all oscillator modes.

4: For minimum width of INT pulse, refer to AC specifications in **Section 34.0 "Electrical Specifications"**".

5: INTF is enabled to be set any time during the Q4-Q1 cycles.

7.3 Interrupts During Sleep

Some interrupts can be used to wake from Sleep. To wake from Sleep, the peripheral must be able to operate without the system clock. The interrupt source must have the appropriate Interrupt Enable bit(s) set prior to entering Sleep.

On waking from Sleep, if the GIE bit is also set, the processor will branch to the interrupt vector. Otherwise, the processor will continue executing instructions after the SLEEP instruction. The instruction directly after the SLEEP instruction will always be executed before branching to the ISR. Refer to **Section 8.0 "Power-Down Mode (Sleep)"** for more details.

7.4 INT Pin

The INT pin can be used to generate an asynchronous edge-triggered interrupt. This interrupt is enabled by setting the INTE bit of the INTCON register. The INTEDG bit of the OPTION_REG register determines on which edge the interrupt will occur. When the INTEDG bit is set, the rising edge will cause the interrupt. When the INTEDG bit is clear, the falling edge will cause the interrupt. The INTF bit of the INTCON register will be set when a valid edge appears on the INT pin. If the GIE and INTE bits are also set, the processor will redirect program execution to the interrupt vector.

7.5 Automatic Context Saving

Upon entering an interrupt, the return PC address is saved on the stack. Additionally, the following registers are automatically saved in the shadow registers:

- W register
- STATUS register (except for $\overline{TO}$ and $\overline{PD}$)
- BSR register
- FSR registers
- PCLATH register

Upon exiting the Interrupt Service Routine, these registers are automatically restored. Any modifications to these registers during the ISR will be lost. If modifications to any of these registers are desired, the corresponding shadow register should be modified and the value will be restored when exiting the ISR. The shadow registers are available in Bank 31 and are readable and writable. Depending on the user's application, other registers may also need to be saved.

11.4 Register Definitions: PORTB

REGISTER 11-9: PORTB: PORTB REGISTER

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **RB<7:0>**: PORTB General Purpose I/O Pin bits(1)
1 = Port pin is ≥ V_{IH}
0 = Port pin is ≤ V_{IL}

Note 1: Writes to PORTB are actually written to corresponding LATB register. Reads from PORTB register is return of actual I/O pin values.

REGISTER 11-10: TRISB: PORTB TRI-STATE REGISTER

R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1
TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **TRISB<7:0>:** PORTB Tri-State Control bits
1 = PORTB pin configured as an input (tri-stated)
0 = PORTB pin configured as an output

REGISTER 11-11: LATB: PORTB DATA LATCH REGISTER

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
LATB7	LATB6	LATB5	LATB4	LATB3	LATB2	LATB1	LATB0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **LATB<7:0>**: PORTB Output Latch Value bits(1)

Note 1: Writes to PORTB are actually written to corresponding LATB register. Reads from PORTB register is return of actual I/O pin values.

11.6 Register Definitions: PORTC

REGISTER 11-17: PORTC: PORTC REGISTER

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **RC<7:0>**: PORTC General Purpose I/O Pin bits(1)
1 = Port pin is ≥ VIH
0 = Port pin is ≤ VIL

Note 1: Writes to PORTC are actually written to corresponding LATC register. Reads from PORTC register is return of actual I/O pin values.

REGISTER 11-18: TRISC: PORTC TRI-STATE REGISTER

R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1
TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **TRISC<7:0>:** PORTC Tri-State Control bits
1 = PORTC pin configured as an input (tri-stated)
0 = PORTC pin configured as an output

REGISTER 11-19: LATC: PORTC DATA LATCH REGISTER

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
LATC7	LATC6	LATC5	LATC4	LATC3	LATC2	LATC1	LATC0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **LATC<7:0>**: PORTC Output Latch Value bits

FIGURE 23-1: DIGITAL-TO-ANALOG CONVERTER BLOCK DIAGRAM

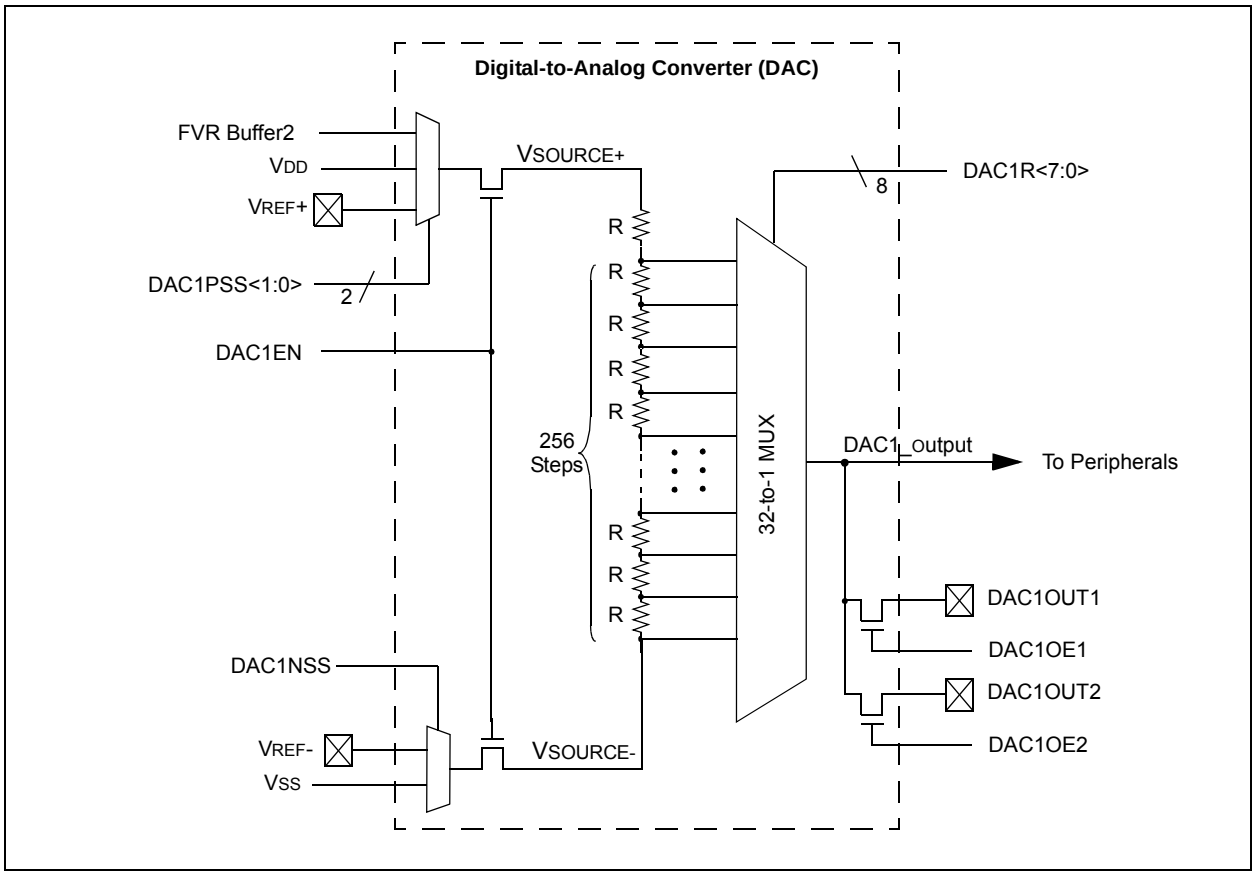
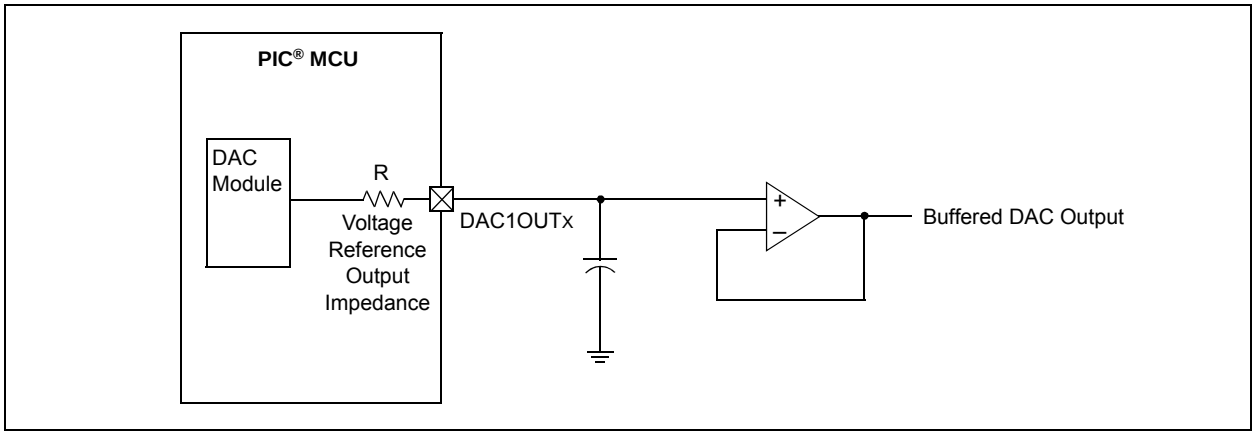


FIGURE 23-2: VOLTAGE REFERENCE OUTPUT BUFFER EXAMPLE



23.4 Operation During Sleep

The DAC continues to function during Sleep. When the device wakes up from Sleep through an interrupt or a Watchdog Timer time-out, the contents of the DAC1CON0 register are not affected. To minimize current consumption in Sleep mode, the voltage reference should be disabled.

23.5 Effects of a Reset

A device Reset affects the following:

- DAC is disabled
- DAC output voltage is removed from the DAC1OUT pin
- The DAC1R<7:0> range select bits are cleared

can be determined from the time difference between the ZCDOUT high and low periods. Note that the time difference, ΔT, is $4*T_{offset}$. The equation for determining the pull-up and pull-down resistor values from the high and low ZCDOUT periods is shown in Equation 25-4. The ZCDOUT signal can be directly observed on a pin by routing the ZCDOUT signal through one of the CLCs.

EQUATION 25-4:

$$R = R_{series}\left(\frac{V_{bias}}{V_{peak}\left(\sin\left(\pi Freq\frac{(\Delta T)}{2}\right)\right)} - 1\right)$$

R is pull-up or pull-down resistor

V_{bias} is V_{pullup} when R is pull-up or V_{DD} when R is pull-down

ΔT is the ZCDOUT high and low period difference

25.6 Handling V_{peak} variations

If the peak amplitude of the external voltage is expected to vary then the series resistor must be selected to keep the ZCD current source and sink below the design maximum range of ± 600 μA for the maximum expected voltage and high enough to be detected accurately at the minimum peak voltage. A general rule of thumb is that the maximum peak voltage can be no more than six times the minimum peak voltage. To ensure that the maximum current does not exceed ± 600 μA and the minimum is at least ± 100 μA compute the series resistance as shown in Equation 25-5. The compensating pull-up for this series resistance can be determined with Equation 25-3 because the pull-up value is independent from the peak voltage.

EQUATION 25-5: SERIES R FOR V RANGE

$$R_{series} = \frac{V_{maxpeak} + V_{minpeak}}{7\times10^{-4}}$$

25.7 Operation During Sleep

The ZCD current sources and interrupts are unaffected by Sleep.

25.8 Effects of a Reset

The ZCD circuit can be configured to default to the active or inactive state on Power-On-Reset (POR). When the ZCDDIS Configuration bit is cleared, the ZCD circuit will be active at POR. When the ZCDDIS Configuration bit is set, the ZCDxEN bit of the ZCDxCON register must be set to enable the ZCD module.

REGISTER 30-3: SSP1CON2: SSP CONTROL REGISTER 2(1)

R/W-0/0	R-0/0	R/W-0/0	R/S/HS-0/0	R/S/HS-0/0	R/S/HS-0/0	R/S/HS-0/0	R/W/HS-0/0
GCEN	ACKSTAT	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	HC = Cleared by hardware S = User set

bit 7 **GCEN:** General Call Enable bit (in I^2C Slave mode only)
1 = Enable interrupt when a general call address (0x00 or 00h) is received in the SSP1SR
0 = General call address disabled

bit 6 **ACKSTAT:** Acknowledge Status bit (in I^2C mode only)
1 = Acknowledge was not received
0 = Acknowledge was received

bit 5 **ACKDT:** Acknowledge Data bit (in I^2C mode only)
In Receive mode:
Value transmitted when the user initiates an Acknowledge sequence at the end of a receive
1 = Not Acknowledge
0 = Acknowledge

bit 4 **ACKEN:** Acknowledge Sequence Enable bit (in I^2C Master mode only)
In Master Receive mode:
1 = Initiate Acknowledge sequence on SDA and SCL pins, and transmit ACKDT data bit. Automatically cleared by hardware.
0 = Acknowledge sequence idle

bit 3 **RCEN:** Receive Enable bit (in I^2C Master mode only)
1 = Enables Receive mode for I^2C
0 = Receive idle

bit 2 **PEN:** Stop Condition Enable bit (in I^2C Master mode only)
SCKMSSP Release Control:
1 = Initiate Stop condition on SDA and SCL pins. Automatically cleared by hardware.
0 = Stop condition Idle

bit 1 **RSEN:** Repeated Start Condition Enable bit (in I^2C Master mode only)
1 = Initiate Repeated Start condition on SDA and SCL pins. Automatically cleared by hardware.
0 = Repeated Start condition Idle

bit 0 **SEN:** Start Condition Enable/Stretch Enable bit
In Master mode:
1 = Initiate Start condition on SDA and SCL pins. Automatically cleared by hardware.
0 = Start condition Idle
In Slave mode:
1 = Clock stretching is enabled for both slave transmit and slave receive (stretch enabled)
0 = Clock stretching is disabled

Note 1: For bits ACKEN, RCEN, PEN, RSEN, SEN: If the I^2C module is not in the Idle mode, this bit may not be set (no spooling) and the SSP1BUF may not be written (or writes to the SSP1BUF are disabled).

31.1.1.5 TSR Status

The TRMT bit of the TX1STA register indicates the status of the TSR register. This is a read-only bit. The TRMT bit is set when the TSR register is empty and is cleared when a character is transferred to the TSR register from the TX1REG. The TRMT bit remains clear until all bits have been shifted out of the TSR register. No interrupt logic is tied to this bit, so the user has to poll this bit to determine the TSR status.

Note:	The TSR register is not mapped in data memory, so it is not available to the user.

31.1.1.6 Transmitting 9-Bit Characters

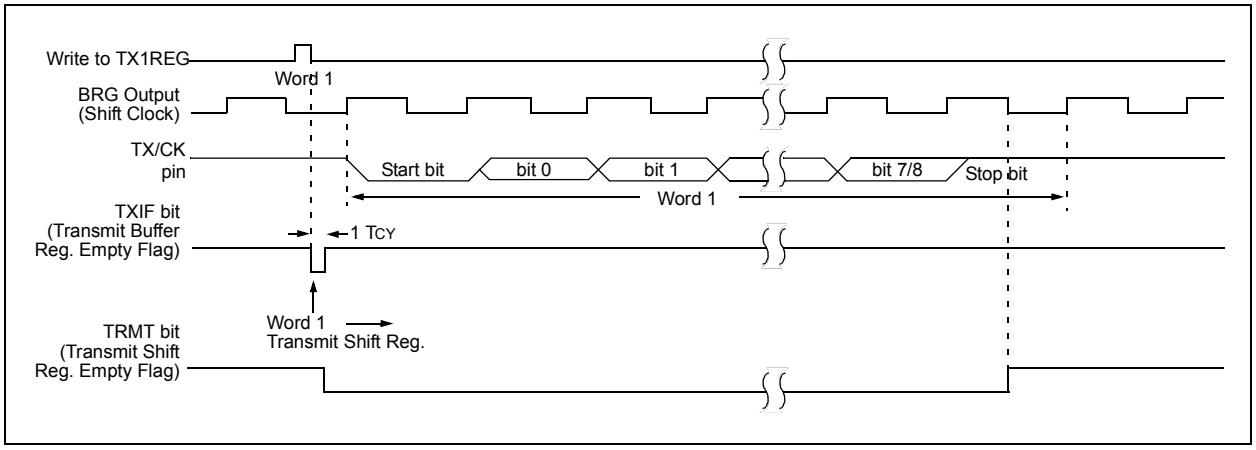
The EUSART supports 9-bit character transmissions. When the TX9 bit of the TX1STA register is set, the EUSART will shift nine bits out for each character transmitted. The TX9D bit of the TX1STA register is the ninth, and Most Significant data bit. When transmitting 9-bit data, the TX9D data bit must be written before writing the eight Least Significant bits into the TX1REG. All nine bits of data will be transferred to the TSR shift register immediately after the TX1REG is written.

A special 9-bit Address mode is available for use with multiple receivers. See **Section 31.1.2.7 "Address Detection"** for more information on the Address mode.

31.1.1.7 Asynchronous Transmission Setup

1. Initialize the SP1BRGH, SP1BRGL register pair and the BRGH and BRG16 bits to achieve the desired baud rate (see **Section 31.4 "EUSART Baud Rate Generator (BRG)"**).
2. Enable the asynchronous serial port by clearing the SYNC bit and setting the SPEN bit.
3. If 9-bit transmission is desired, set the TX9 control bit. A set ninth data bit will indicate that the eight Least Significant data bits are an address when the receiver is set for address detection.
4. Set SCKP bit if inverted transmit is desired.
5. Enable the transmission by setting the TXEN control bit. This will cause the TXIF interrupt bit to be set.
6. If interrupts are desired, set the TXIE interrupt enable bit of the PIE1 register. An interrupt will occur immediately provided that the GIE and PEIE bits of the INTCON register are also set.
7. If 9-bit transmission is selected, the ninth bit should be loaded into the TX9D data bit.
8. Load 8-bit data into the TX1REG register. This will start the transmission.

FIGURE 31-3: ASYNCHRONOUS TRANSMISSION



DECFSZ **Decrement f, Skip if 0**

Syntax:	[*label*] DECFSZ f,d
Operands:	0 ≤ f ≤ 127 d ∈ [0,1]
Operation:	(f) - 1 → (destination); skip if result = 0
Status Affected:	None
Description:	The contents of register 'f' are decremented. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'. If the result is '1', the next instruction is executed. If the result is '0', then a NOP is executed instead, making it a 2-cycle instruction.

GOTO **Unconditional Branch**

Syntax:	[*label*] GOTO k
Operands:	0 ≤ k ≤ 2047
Operation:	k → PC<10:0> PCLATH<6:3> → PC<14:11>
Status Affected:	None
Description:	GOTO is an unconditional branch. The 11-bit immediate value is loaded into PC bits <10:0>. The upper bits of PC are loaded from PCLATH<4:3>. GOTO is a 2-cycle instruction.

INCF **Increment f**

Syntax:	[*label*] INCF f,d
Operands:	0 ≤ f ≤ 127 d ∈ [0,1]
Operation:	(f) + 1 → (destination)
Status Affected:	Z
Description:	The contents of register 'f' are incremented. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.

INCFSZ **Increment f, Skip if 0**

Syntax:	[*label*] INCFSZ f,d
Operands:	0 ≤ f ≤ 127 d ∈ [0,1]
Operation:	(f) + 1 → (destination), skip if result = 0
Status Affected:	None
Description:	The contents of register 'f' are incremented. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'. If the result is '1', the next instruction is executed. If the result is '0', a NOP is executed instead, making it a 2-cycle instruction.

IORLW **Inclusive OR literal with W**

Syntax:	[*label*] IORLW k
Operands:	0 ≤ k ≤ 255
Operation:	(W) .OR. k → (W)
Status Affected:	Z
Description:	The contents of the W register are OR'ed with the 8-bit literal 'k'. The result is placed in the W register.

IORWF **Inclusive OR W with f**

Syntax:	[*label*] IORWF f,d
Operands:	0 ≤ f ≤ 127 d ∈ [0,1]
Operation:	(W) .OR. (f) → (destination)
Status Affected:	Z
Description:	Inclusive OR the W register with register 'f'. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.

SWAPF **Swap Nibbles in f**

Syntax:	[*label*] SWAPF f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	(f<3:0>) → (destination<7:4>), (f<7:4>) → (destination<3:0>)
Status Affected:	None
Description:	The upper and lower nibbles of register 'f' are exchanged. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed in register 'f'.

TRIS **Load TRIS Register with W**

Syntax:	[*label*] TRIS f
Operands:	$5 \le f \le 7$
Operation:	(W) → TRIS register 'f'
Status Affected:	None
Description:	Move data from W register to TRIS register. When 'f' = 5, TRISA is loaded. When 'f' = 6, TRISB is loaded. When 'f' = 7, TRISC is loaded.

XORLW **Exclusive OR literal with W**

Syntax:	[*label*] XORLW k
Operands:	$0 \le k \le 255$
Operation:	(W) .XOR. k → (W)
Status Affected:	Z
Description:	The contents of the W register are XOR'ed with the 8-bit literal 'k'. The result is placed in the W register.

XORWF **Exclusive OR W with f**

Syntax:	[*label*] XORWF f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	(W) .XOR. (f) → (destination)
Status Affected:	Z
Description:	Exclusive OR the contents of the W register with register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

34.0 ELECTRICAL SPECIFICATIONS

34.1 Absolute Maximum Ratings(†)

Ambient temperature under bias ..... -40°C to +125°C
Storage temperature ..... -65°C to +150°C
Voltage on pins with respect to V_{SS}
- on V_{DD} pin
  - PIC16F1717/8/9 ..... -0.3V to +6.5V
  - PIC16LF1717/8/9 ..... -0.3V to +4.0V
- on $\overline{MCLR}$ pin ..... -0.3V to +9.0V
- on all other pins ..... -0.3V to (V_{DD} + 0.3V)

Maximum current
- on V_{SS} pin(1)
  - -40°C ≤ T_A ≤ +85°C ..... 340 mA
  - -40°C ≤ T_A ≤ +125°C ..... 140 mA
- on V_{DD} pin(1) PIC16(L)F1718 only
  - -40°C ≤ T_A ≤ +85°C ..... 250 mA
  - -40°C ≤ T_A ≤ +125°C ..... 85 mA
- on V_{DD} pin(1) PIC16(L)F1717/9 only
  - -40°C ≤ T_A ≤ +85°C ..... 350 mA
  - -40°C ≤ T_A ≤ +125°C ..... 120 mA
- Sunk by any standard I/O pin ..... 50 mA
- Sourced by any standard I/O pin ..... 50 mA
- Sourced by any Op Amp output pin ..... 100 mA

Clamp current, I_K (V_{PIN} < 0 or V_{PIN} > V_{DD}) ..... ±20 mA
Total power dissipation(2) ..... 800 mW

Note 1: Maximum current rating requires even load distribution across I/O pins. Maximum current rating may be limited by the device package power dissipation characterizations, see Table 34-6 to calculate device specifications.

2: Power dissipation is calculated as follows:

$Pdis = V_{DD} * \{Idd - \Sigma Ioh\} + \Sigma\{V_{DD} - Voh) * Ioh\} + \Sigma(Vol * Iol)$.

† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure above maximum rating conditions for extended periods may affect device reliability.

TABLE 34-2: SUPPLY CURRENT (I_{DD})(1,2)

PIC16LF1717/8/9		Standard Operating Conditions (unless otherwise stated)					
PIC16F1717/8/9							
Param. No.	Device Characteristics	Min.	Typ.†	Max.	Units	Conditions	
						V_{DD}	Note
D009	LDO Regulator	—	75	—	μA	—	High-Power mode, normal operation
		—	15	—	μA	—	Sleep, VREGCON<1> = 0
		—	0.3	—	μA	—	Sleep, VREGCON<1> = 1
D010		—	8	—	μA	1.8	F_{OSC} = 32 kHz, LP Oscillator mode (**Note 4**), -40°C ≤ T_A ≤ +85°C
		—	12	—	μA	3.0	
D010		—	15	—	μA	2.3	F_{OSC} = 32 kHz, LP Oscillator mode (**Note 4, Note 5**), -40°C ≤ T_A ≤ +85°C
		—	17	—	μA	3.0	
		—	21	—	μA	5.0	
D012		—	140	—	μA	1.8	F_{OSC} = 4 MHz, XT Oscillator mode
		—	250	—	μA	3.0	
D012		—	210	—	μA	2.3	F_{OSC} = 4 MHz, XT Oscillator mode (**Note 5**)
		—	280	—	μA	3.0	
		—	340	—	μA	5.0	
D014		—	115	—	μA	1.8	F_{OSC} = 4 MHz, External Clock (ECM), Medium Power mode
		—	210	—	μA	3.0	
D014		—	180	—	μA	2.3	F_{OSC} = 4 MHz, External Clock (ECM), Medium Power mode (**Note 5**)
		—	240	—	μA	3.0	
		—	300	—	μA	5.0	
D015		—	2.1	—	mA	3.0	F_{OSC} = 32 MHz, External Clock (ECH), High-Power mode
		—	2.5	—	mA	3.6	
D015		—	2.1	—	mA	3.0	F_{OSC} = 32 MHz, External Clock (ECH), High-Power mode (**Note 5**)
		—	2.2	—	mA	5.0	

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The test conditions for all I_{DD} measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to V_{DD}; $\overline{MCLR}$ = V_{DD}; WDT disabled.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption.

3: For RC oscillator configurations, current through R_{EXT} is not included. The current through the resistor can be extended by the formula IR = $V_{DD}/2R_{EXT}$ (mA) with R_{EXT} in kΩ

4: FVR and BOR are disabled.

5: 0.1 μF capacitor on V_{CAP}.

6: 8 MHz clock with 4x PLL enabled.

FIGURE 34-17: SPI MASTER MODE TIMING (CKE = 0, SMP = 0)

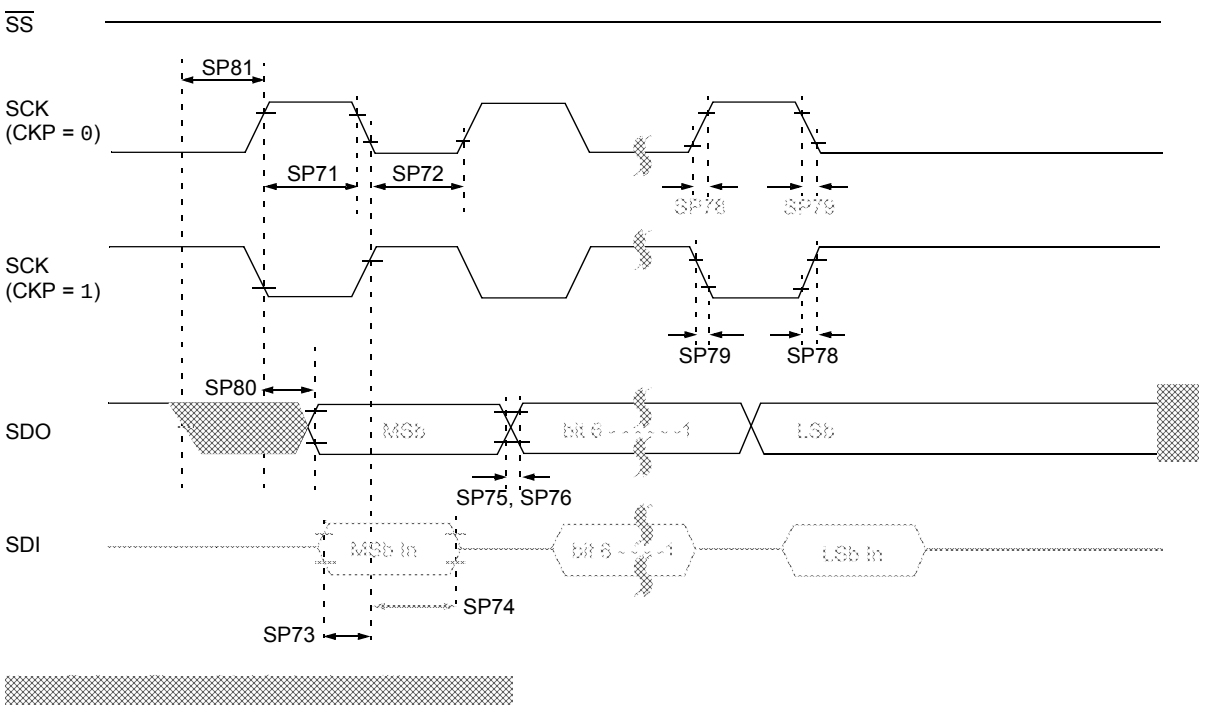
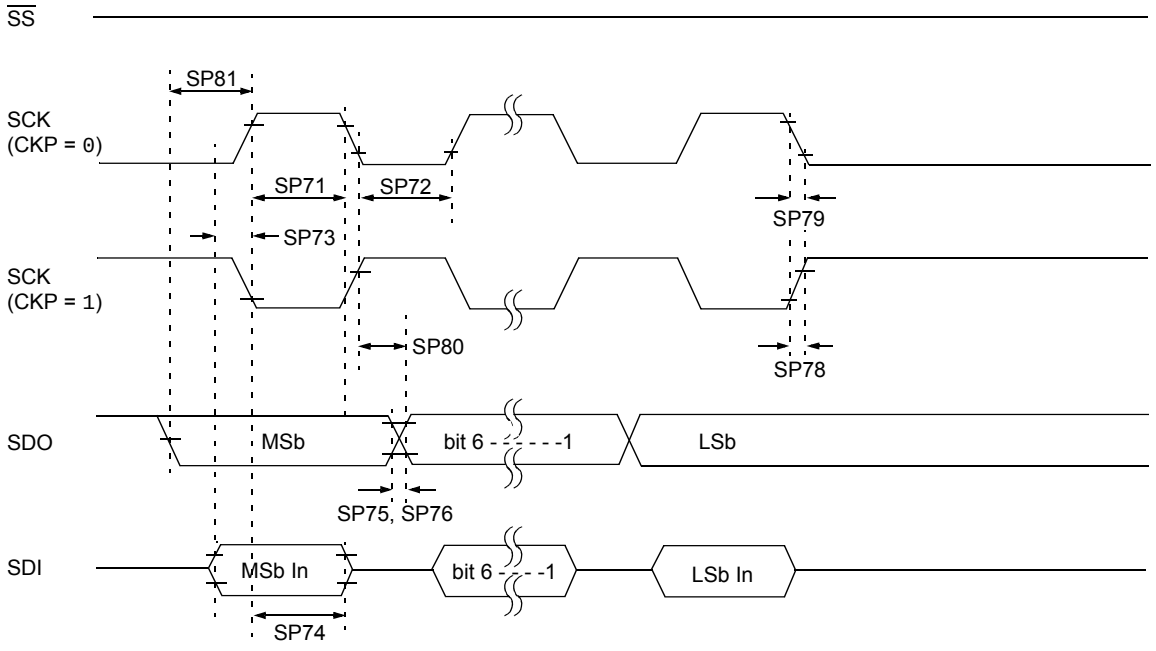


FIGURE 34-18: SPI MASTER MODE TIMING (CKE = 1, SMP = 1)



Note: Refer to Figure 34-4 for load conditions.