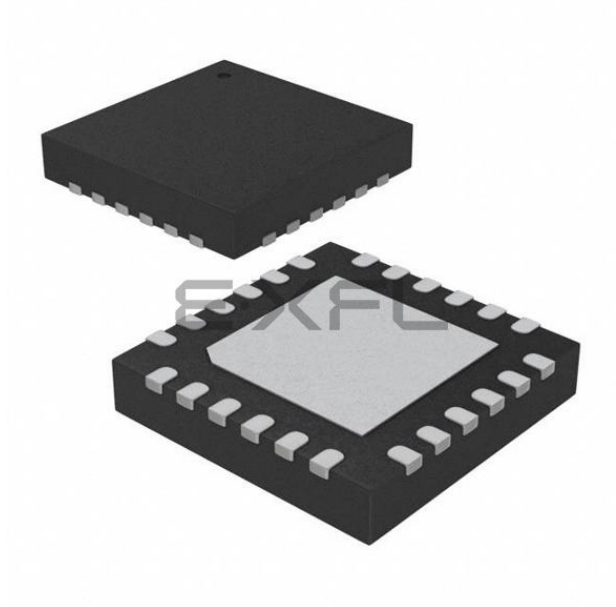

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M23
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	17
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.63V
Data Converters	A/D 5x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	24-VFQFN Exposed Pad
Supplier Device Package	24-VQFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsaml10d14a-mft

Important: SRAM retention is not guaranteed after Power Supply Resets (POR, BOD12 and BOD33).

10.1.4 Boot ROM

SAM L10/L11 devices embed 8 KB of internal ROM mapped at address 0x0200 0000.

Note: Please refer to 14. Boot ROM for more details.

10.2 NVM Rows

SAM L10 and SAM L11 have different Non Volatile Memory (NVM) rows which contain device configuration data that can be used by the system:

Table 10-7. NVM Rows Mapping

NVM Rows	Address
User Row (UROW)	0x00804000
Software Calibration Row	0x00806020
Temperature Log Row	0x00806038
Boot Configuration Row (BOCOR)	0x0080C000

10.2.1 NVM User Row (UROW)

The Non Volatile Memory User Row (UROW) contains device configuration data that are automatically read at device power-on.

This row can be updated using the NVMCTRL peripheral.

When writing to the NVM User Row, the new values are not loaded by the other peripherals on the device until a device reset occurs.

The NVM User Row can be read at the address 0x00804000.

SAM L10 and SAM L11 have different NVM User Row mappings.

Related Links

30. NVMCTRL – Nonvolatile Memory Controller
25. SUPC – Supply Controller
25.8.5 BOD33
26. WDT – Watchdog Timer
26.8.1 CTRLA
26.8.2 CONFIG
26.8.3 EWCTRL

10.2.1.1 SAM L10 User Row

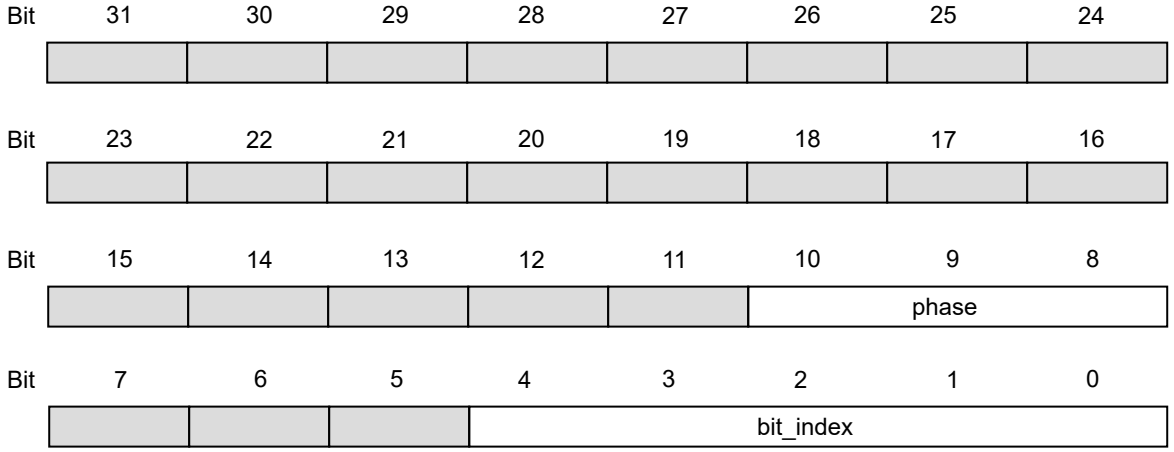
Table 10-8. SAM L10 UROW Bitfields Definition

Bit Pos.	Name	Usage	Factory Setting	Related Peripheral Register
2:0	Reserved	Reserved	Reserved	Reserved
5:3	NSULCK	NVM UnLock Bits	0x7	NVMCTRL.NSULCK

In this mode, the MBIST algorithm is paused when an error is detected. In such a situation, only STATUSA.FAIL is asserted. The state machine waits for user to clear STATUSA.FAIL by writing a '1' in STATUSA.FAIL to resume. Prior to resuming, user can read the DATA and ADDR registers to locate the fault.

4. Locating Faults
   If the test stops with STATUSA.FAIL set, one or more bits failed the test. The test stops at the first detected error. The position of the failing bit can be found by reading the following registers:
   - ADDR: Address of the word containing the failing bit
   - DATA: contains data to identify which bit failed, and during which phase of the test it failed. The DATA register will in this case contains the following bit groups:

Figure 16-6. DATA bits Description When MBIST Operation Returns an Error



- bit_index: contains the bit number of the failing bit
- phase: indicates which phase of the test failed and the cause of the error, as listed in the following table.

Table 16-5. MBIST Operation Phases

Phase	Test actions
0	Write all bits to zero. This phase cannot fail.
1	Read '0', write '1', increment address
2	Read '1', write '0'
3	Read '0', write '1', decrement address
4	Read '1', write '0', decrement address
5	Read '0', write '1'
6	Read '1', write '0', decrement address
7	Read all zeros. bit_index is not used

16.12.25 Component Identification 3

Name: CID3
Offset: 0x1FFC
Reset: 0x000000B1
Property: -

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	PREAMBLEB3[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	1	0	1	1	0	0	0	1

Bits 7:0 – PREAMBLEB3[7:0] Preamble Byte 3
These bits will always return 0x000000B1 when read.

Value	Description
0	The APBC clock for the EVSYS is stopped.
1	The APBC clock for the EVSYS is enabled.

21.6 Functional Description

21.6.1 Principle of Operation

The Reset Controller collects the various Reset sources and generates Reset for the device.

21.6.2 Basic Operation

21.6.2.1 Initialization

After a power-on Reset, the RSTC is enabled and the Reset Cause (RCAUSE) register indicates the POR source.

21.6.2.2 Enabling, Disabling, and Resetting

The RSTC module is always enabled.

21.6.2.3 Reset Causes and Effects

The latest Reset cause is available in RCAUSE register, and can be read during the application boot sequence in order to determine proper action.

These are the groups of Reset sources:

- Power supply Reset: Resets caused by an electrical issue. It covers POR and BODs Resets
- User Reset: Resets caused by the application. It covers external Resets, system Reset requests and watchdog Resets

The following table lists the parts of the device that are reset, depending on the Reset type.

Table 21-1. Effects of the Different Reset Causes

	Power Supply Reset	User Reset	
	POR, BOD33, BOD12	External Reset	WDT Reset, System Reset Request
RTC, OSC32KCTRL, RSTC	Y	N	N
GCLK with WRTLOCK	Y	N	N
Debug logic	Y	Y	N
Others	Y	Y	Y

The external Reset is generated when pulling the $\overline{\text{RESET}}$ pin low.

The POR, BOD12, and BOD33 Reset sources are generated by their corresponding module in the Supply Controller Interface (SUPC).

The WDT Reset is generated by the Watchdog Timer.

The System Reset Request is a Reset generated by the CPU when asserting the SYSRESETREQ bit located in the Reset Control register of the CPU (for details refer to the ARM® Cortex™ Technical Reference Manual on http://www.arm.com).

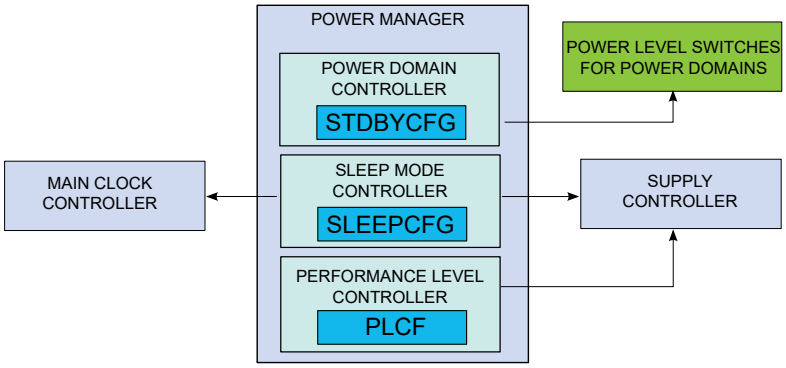
Note: Refer to the Timing Characteristics section of the Electrical Characteristics chapter.

Related Links

26. WDT – Watchdog Timer
25. SUPC – Supply Controller

22.3 Block Diagram

Figure 22-1. PM Block Diagram



22.4 Signal Description

Not applicable.

22.5 Product Dependencies

In order to use this peripheral, other parts of the system must be configured correctly, as described below.

22.5.1 I/O Lines

Not applicable.

22.5.2 Clocks

The PM bus clock (CLK_PM_APB) can be enabled and disabled in the Main Clock module. If this clock is disabled, it can only be re-enabled by a system reset.

22.5.3 DMA

Not applicable.

22.5.4 Interrupts

The interrupt request line is connected to the interrupt controller. Using the PM interrupt requires the interrupt controller to be configured first.

22.5.5 Events

Not applicable.

22.5.6 Debug Operation

When the CPU is halted in debug mode, the PM continues normal operation. If standby sleep mode is requested by the system while in debug mode, the power domains are not turned off. As a consequence, power measurements while in debug mode are not relevant.

If OFF sleep mode is requested by the system while in debug mode, the core domains are kept on, and the debug modules are kept running to allow the debugger to access internal registers. When exiting the OFF mode upon a reset condition, the core domains are reset except the debug logic, allowing users to keep using their current debug session.

22.6.1.2.1 PDSW - Power Domain Switchable

PDSW is the switchable power domain. It contains the Event System, Generic Clock Controller, Main Clock Controller, Oscillator Controller, Non-Volatile Memory Controller, DMA Controller, the Device Service Unit, and the ARM core. PDSW also contains a number of peripherals that allow the device to wake up from an interrupt: SERCOM, Timer, ADC, DAC, OPAMP, CCL, PTC.

22.6.1.2.2 PDAO - Power Domain Always On

PDAO contains all controllers located in the always-on domain. It is powered when in Active, Idle, or Standby mode.

22.6.1.3 Sleep Modes

The device can be set in a sleep mode. In sleep mode, the CPU is stopped and the peripherals are either active or idle, according to the sleep mode depth:

- Idle sleep mode: The CPU is stopped. Synchronous clocks are stopped except when requested. The logic is retained.
- Standby sleep mode: The CPU is stopped as well as the peripherals. The logic is retained, and power domain gating can be used to reduce power consumption further.
- Off sleep mode: The entire device is powered off.

22.6.1.4 Power Domain States and Gating

In Standby sleep mode, the Power Domain Gating technique allows for selecting the state of PDSW power domain automatically (e.g. for executing sleepwalking tasks) or manually:

Active State	The power domain is powered according to the performance level
Retention State	The main voltage supply for the power domain is switched off, while maintaining a secondary low-power supply for sequential cells. The logic context is restored when waking up.

22.6.2 Principle of Operation

In active mode, all clock domains and power domains are active, allowing software execution and peripheral operation. The PM Sleep Mode Controller allows to save power by choosing between different sleep modes depending on application requirements, see 22.6.3.3 Sleep Mode Controller.

The PM Performance Level Controller allows to optimize either for low power consumption or high performance.

The PM Power Domain Controller allows to reduce the power consumption in standby mode even further.

22.6.3 Basic Operation

22.6.3.1 Initialization

After a Power-on Reset (POR), the PM is enabled, the device is in Active mode, the performance level is PL0 (the lowest power consumption) and all the power domains are in active state.

22.6.3.2 Enabling, Disabling and Resetting

The PM is always enabled and can not be reset.

22.6.3.3 Sleep Mode Controller

Sleep mode is entered by executing the Wait For Interrupt instruction (WFI). The Sleep Mode bits in the Sleep Configuration register (SLEEPCFG.SLEEPMODE) select the level of the sleep mode.

Note: A small latency happens between the store instruction and actual writing of the SLEEPCFG register due to bridges. Software must ensure that the SLEEPCFG register reads the desired value before issuing a WFI instruction.

Static Power Domain Gating is a technique that allows to automatically turn off the PDSW power domain supply when not used while keeping PDAO powered up.

- SleepWalking extension to power gating (SleepWalking with dynamic power gating)
  SleepWalking is the capability for a device in Standby Sleep mode, to temporarily wake-up clocks for a peripheral to perform a task without waking-up the CPU. The SleepWalking feature has been expanded to control power gating in addition to clock gating. The power domain PDSW can be automatically controlled (active or retention state) depending on peripheral requirements (PDCFG bit from the STDBYCFG register).

The static and dynamic power gating features are fully transparent for the user.

Table 22-3. Sleep Modes versus Power Domain States Overview

	Power Domain State	
Sleep Mode	**PDSW**	**PDAO**
Active	active	active
Idle	active	active
Standby - At least one peripheral from PDSW with RUNSTDBY = 1 OR PDCFG = 1	active (1)	active
Standby - No peripheral from PDSW with RUNSTDBY = 1	retention	active
Off	off	off

Note:

1. PDSW can be switched automatically in retention mode if the dynamic power gating feature is enabled.

22.6.3.6 Regulators, RAMs, and NVM State in Sleep Mode

By default, in Standby Sleep mode, the RAMs, NVM, and regulators are automatically set in Low-Power mode to reduce power consumption:

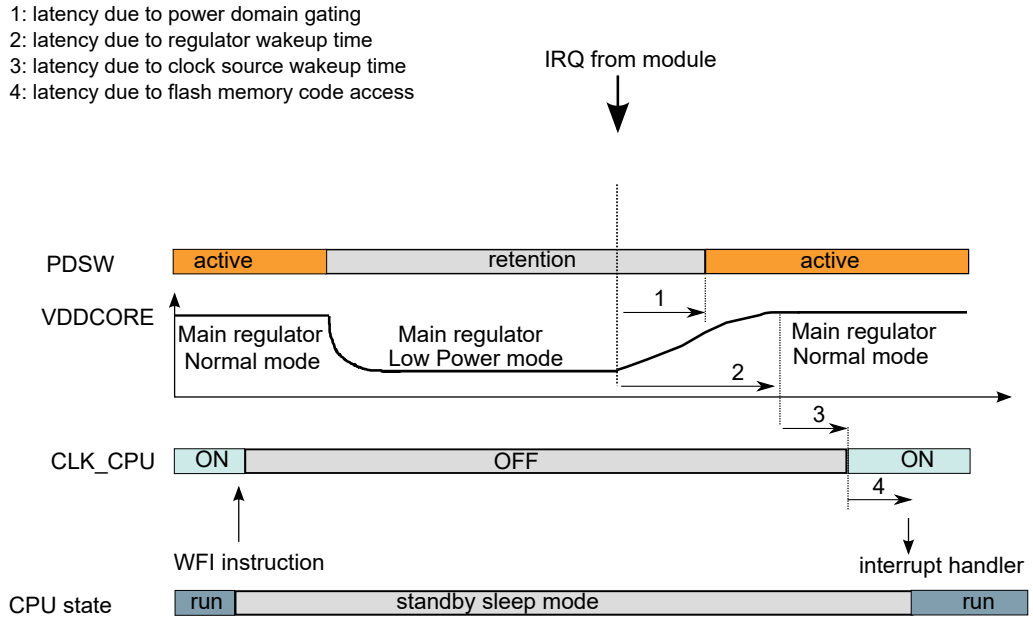
- The RAM is in Low-Power mode if its power domain is in retention or off state.
- Non-Volatile Memory - the NVM is located in the power domain PDSW. By default, the NVM is automatically set in low power mode in these conditions:
  - When the power domain PDSW is in retention or off state.
  - When the device is in Standby Sleep mode and the NVM is not accessed. This behavior can be changed by software by configuring the SLEEPPRM bit group of the CTRLB register in the NVMCTRL peripheral.
  - When the device is in Idle Sleep mode and the NVM is not accessed. This behavior can be changed by software by configuring the SLEEPPRM bit group of the CTRLB register in the NVMCTRL peripheral.
- Regulators: by default, in Standby Sleep mode, the PM analyzes the device activity to use either the main or the low-power voltage regulator to supply the VDDCORE.

GCLK clocks, regulators and RAM are not affected in Idle Sleep mode and will operate as normal.

amount of time for the main regulator to transition to the voltage level corresponding to PL2, causing additional wake-up time.

- Latency due to the CPU clock source wake-up time.
- Latency due to the NVM memory access.
- Latency due to Switchable Power Domain back-bias wake-up time:
  If back-bias is enabled, and the device wakes up from retention, it takes a certain amount of time for the regulator to settle.

Figure 22-5. Total Wake-up Time from Standby Sleep Mode



22.6.5 Standby with Static Power Domain Gating in Details

In Standby Sleep mode, the switchable power domain (PDSW) of a peripheral can remain in active state to perform the peripheral's tasks. This Static Power Domain Gating feature is supported by all peripherals. For some peripherals it must be enabled by writing a Run in Standby bit in the respective Control A register (CTRLA.RUNSTDBY) to '1'. Refer to each peripheral chapter for details.

The following examples illustrate Standby with static Power Domain Gating:

TC0 Standby with Static Power Domain Gating

TC0 peripheral is used in counter operation mode. An interrupt is generated to wake-up the device based on the TC0 peripheral configuration. To make the TC0 peripheral continue to run in Standby Sleep mode, the RUNSTDBY bit is written to '1'.

- Entering Standby mode: As shown in Figure 22-6, PDSW remains active. Refer to 22.6.3.5 Power Domain Controller for details.
- Exiting Standby mode: When conditions are met, the TC0 peripheral generates an interrupt to wake-up the device, and the CPU is able to operate normally and execute the TC0 interrupt handler accordingly.
- Wake-up time:
  - The required time to set PDSW to active state has to be considered for the global wake-up time, refer to 22.6.4.6 Wake-Up Time for details.

22.7 Register Summary

Offset	Name	Bit Pos.								
0x01	SLEEPCFG	7:0						SLEEPMODE[2:0]		
0x02	PLCFG	7:0	PLDIS						PLSEL[1:0]	
0x03	PWCFG	7:0							RAMPSWC[1:0]	
0x04	INTENCLR	7:0								PLRDY
0x05	INTENSET	7:0								PLRDY
0x06	INTFLAG	7:0								PLRDY
0x07	Reserved									
0x08	STDBYCFG	7:0	VREGSMOD[1:0]			DPGPDSW				PDCFG
		15:8				BBIASTR		BBIASHS		

22.8 Register Description

Registers can be 8, 16, or 32 bits wide. Atomic 8-, 16- and 32-bit accesses are supported. In addition, the 8-bit quarters and 16-bit halves of a 32-bit register, and the 8-bit halves of a 16-bit register can be accessed directly.

Some registers are optionally write-protected by the Peripheral Access Controller (PAC). Optional PAC write-protection is denoted by the "PAC Write-Protection" property in each individual register description. For details, refer to 22.5.7 Register Access Protection.

On **SAM L11** devices, this peripheral has different access permissions depending on PAC Security Attribution (Secure or Non-Secure):

- If the peripheral is configured as Non-Secure in the PAC:
  - Secure access and Non-Secure access are granted
- If the peripheral is configured as Secure in the PAC:
  - Secure access is granted
  - Non-Secure access is discarded (Write is ignored, read 0x0) and a PAC error is triggered

Refer to *Peripherals Security Attribution* for more information.

Refer to *Peripherals Security Attribution* for more information.

- Up to 8 channels
  - Enable 8 independent transfers
  - Automatic descriptor fetch for each channel
  - Suspend/resume operation support for each channel
- Flexible arbitration scheme
  - 4 configurable priority levels for each channel
  - Fixed or round-robin priority scheme within each priority level
- From 1 to 256KB data transfer in a single block transfer
- Multiple addressing modes
  - Static
  - Configurable increment scheme
- Optional interrupt generation
  - On block transfer complete
  - On error detection
  - On channel suspend
- 4 event inputs
  - One event input for each of the 4 least significant DMA channels
  - Can be selected to trigger normal transfers, periodic transfers or conditional transfers
  - Can be selected to suspend or resume channel operation
- 4 event outputs
  - One output event for each of the 4 least significant DMA channels
  - Selectable generation on AHB, block, or transaction transfer complete
- Error management supported by write-back function
  - Dedicated Write-Back memory section for each channel to store ongoing descriptor transfer
- CRC polynomial software selectable to
  - CRC-16 (CRC-CCITT)
  - CRC-32 (IEEE® 802.3)

system frequencies, a programmable number of wait states can be used to optimize performance. When changing the AHB bus frequency, the user must ensure that the NVM Controller is configured with the proper number of wait states. Refer to the Electrical Characteristics for the exact number of wait states to be used for a particular frequency range.

30.5.3 Interrupts

The NVM Controller interrupt request line is connected to the interrupt controller. Using the NVMCTRL interrupt requires the interrupt controller to be programmed first.

30.5.4 Events

The NVMCTRL can take the following actions on an input event:

- Write zeroes in one Data FLASH row: Refer to 30.6.7 Tamper Erase for details.
- Write a page in the FLASH or in the Data FLASH: Refer to 30.6.6 Event Automatic Write for details.

The NVMCTRL uses only asynchronous events, so the asynchronous Event System channel path must be configured. By default, the NVMCTRL will detect a rising edge on the incoming event. If the NVMCTRL action must be performed on the falling edge of the incoming event, the event line must be inverted first. This is done by setting the corresponding Event Invert Enable bit in Event Control register (NVMCTRL.AUTOWINV=1).

30.5.5 Debug Operation

When an external debugger forces the CPU into debug mode, the peripheral continues normal operation except that FLASH reads are not cached so that the cache state is not altered by debug tools.

30.5.6 Register Access Protection

All registers with write-access are optionally write-protected by the Peripheral Access Controller (PAC), except the following registers:

- Interrupt Flag Status and Clear register (INTFLAG)
- Status register (STATUS)

Optional write-protection by the Peripheral Access Controller (PAC) is denoted by the "PAC Write-Protection" property in each individual register description.

When TrustZone is supported (**SAM L11** only), all register reads are allowed. Non-secure writes to APB registers are limited as follows. Illegal writes will be ignored.

- Some commands written to CTRLA such as Write/Erase and Lock/Unlock are only permitted to non-secure application and data space.
- Writes to all other registers except CTRLC and INTFLAG are not allowed.

Related Links

15. PAC - Peripheral Access Controller

30.5.7 SAM L11 TrustZone Specific Register Access Protection

The NVMCTRL is a split-secure APB module, all registers are available in the secure alias and only a subset of registers is available in the non-secure alias with limited access.

When NONSEC.WRITE is read zero, all APB write accesses to the non-secure APB alias and all non-secure AHB write accesses to the Page Buffer are discarded. The latter returns a hardfault. Any attempt to change the configuration via the non-secure alias is silently ignored.

Offset	Name	Bit Pos.								
0x01A0	RAM40	7:0	DATA[7:0]							
		15:8	DATA[15:8]							
		23:16	DATA[23:16]							
		31:24	DATA[31:24]							
0x01A4	RAM41	7:0	DATA[7:0]							
		15:8	DATA[15:8]							
		23:16	DATA[23:16]							
		31:24	DATA[31:24]							
0x01A8	RAM42	7:0	DATA[7:0]							
		15:8	DATA[15:8]							
		23:16	DATA[23:16]							
		31:24	DATA[31:24]							
0x01AC	RAM43	7:0	DATA[7:0]							
		15:8	DATA[15:8]							
		23:16	DATA[23:16]							
		31:24	DATA[31:24]							
0x01B0	RAM44	7:0	DATA[7:0]							
		15:8	DATA[15:8]							
		23:16	DATA[23:16]							
		31:24	DATA[31:24]							
0x01B4	RAM45	7:0	DATA[7:0]							
		15:8	DATA[15:8]							
		23:16	DATA[23:16]							
		31:24	DATA[31:24]							
0x01B8	RAM46	7:0	DATA[7:0]							
		15:8	DATA[15:8]							
		23:16	DATA[23:16]							
		31:24	DATA[31:24]							
0x01BC	RAM47	7:0	DATA[7:0]							
		15:8	DATA[15:8]							
		23:16	DATA[23:16]							
		31:24	DATA[31:24]							
0x01C0	RAM48	7:0	DATA[7:0]							
		15:8	DATA[15:8]							
		23:16	DATA[23:16]							
		31:24	DATA[31:24]							
0x01C4	RAM49	7:0	DATA[7:0]							
		15:8	DATA[15:8]							
		23:16	DATA[23:16]							
		31:24	DATA[31:24]							
0x01C8	RAM50	7:0	DATA[7:0]							
		15:8	DATA[15:8]							
		23:16	DATA[23:16]							
		31:24	DATA[31:24]							
0x01CC	RAM51	7:0	DATA[7:0]							
		15:8	DATA[15:8]							

33.7.2 Software Event

Name: SWEVT
Offset: 0x04
Reset: 0x00000000
Property: PAC Write-Protection, Mix-Secure

Important: For **SAM L11 Non-Secure** accesses, write accesses (W*) are allowed only if the security attribution for the corresponding channel (CHANNELx) is set as Non-Secured in the NONSECCHAN register.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	CHANNEL[7:0]							
Access	W/W*/W	W/W*/W	W/W*/W	W/W*/W	W/W*/W	W/W*/W	W/W*/W	W/W*/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – CHANNEL[7:0] Channel x Software Selection
Writing a '0' to this bit has no effect.

Writing a '1' to this bit will trigger a software event for channel x.

These bits always return '0' when read.

Writing '1' to this bit location will clear the MB flag. The transaction will not continue or be terminated until one of the above actions is performed.

Writing '0' to this bit has no effect.

38.7.3.12 Synchronization Busy

Name: SYNCBUSY
Offset: 0x10
Reset: 0x00000000
Property: -

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
		CCx	PER	COUNT	STATUS	CTRLB	ENABLE	SWRST
Access		R	R	R	R	R	R	R
Reset		0	0	0	0	0	0	0

Bit 6 – CCx Compare/Capture Channel x Synchronization Busy
For details on CC channels number, refer to each TC feature list.

This bit is set when the synchronization of CCx between clock domains is started.

This bit is also set when the CCBUFx is written, and cleared on update condition. The bit is automatically cleared when the STATUS.CCBUFx bit is cleared.

Bit 5 – PER PER Synchronization Busy
This bit is cleared when the synchronization of PER between the clock domains is complete.

This bit is set when the synchronization of PER between clock domains is started.

This bit is also set when the PER is written, and cleared on update condition. The bit is automatically cleared when the STATUS.PERBUF bit is cleared.

Bit 4 – COUNT COUNT Synchronization Busy
This bit is cleared when the synchronization of COUNT between the clock domains is complete.

This bit is set when the synchronization of COUNT between clock domains is started.

Bit 3 – STATUS STATUS Synchronization Busy
This bit is cleared when the synchronization of STATUS between the clock domains is complete.

45. PTC - Peripheral Touch Controller

45.1 Overview

The Peripheral Touch Controller (PTC) acquires signals in order to detect touch on capacitive sensors. The external capacitive touch sensor is typically formed on a PCB, and the sensor electrodes are connected to the analog front end of the PTC through the I/O pins in the device. The PTC supports both self- and mutual-capacitance sensors.

In mutual-capacitance mode, sensing is done using capacitive touch matrices in various X-Y configurations, including indium tin oxide (ITO) sensor grids. The PTC requires one pin per X-line and one pin per Y-line.

In self-capacitance mode, the PTC requires only one pin (Y-line) for each touch sensor.

The number of available pins and the assignment of X- and Y-lines is depending on both package type and device configuration. Refer to the Configuration Summary and I/O Multiplexing table for details.

Related Links

1. Configuration Summary

45.2 Features

- Low-power, high-sensitivity, environmentally robust capacitive touch buttons, sliders, and wheels
- Supports wake-up on touch from standby Sleep mode
- Supports mutual capacitance and self-capacitance sensing
  - Mix-and-match mutual-and self-capacitance sensors
- One pin per electrode – no external components
- Load compensating charge sensing
  - Parasitic capacitance compensation and adjustable gain for superior sensitivity
- Zero drift over the temperature and V_{DD} range
  - Auto calibration and recalibration of sensors
- Single-shot and free-running charge measurement
- Hardware noise filtering and noise signal desynchronization for high conducted immunity
- Polarity control, allowing Parallel Acquisition (through the QTouch Library) individually controls the polarity of each line
- Driven Shield Plus for better noise immunity and moisture tolerance
  - Any PTC X/Y line can be used for the driven shield
  - All enabled sensors will be driven at the same potential as the sensor scanned
- Selectable channel change delay allows choosing the settling time on a new channel, as required
- Acquisition-start triggered by command or through auto-triggering feature
- Low CPU utilization through interrupt on acquisition-complete

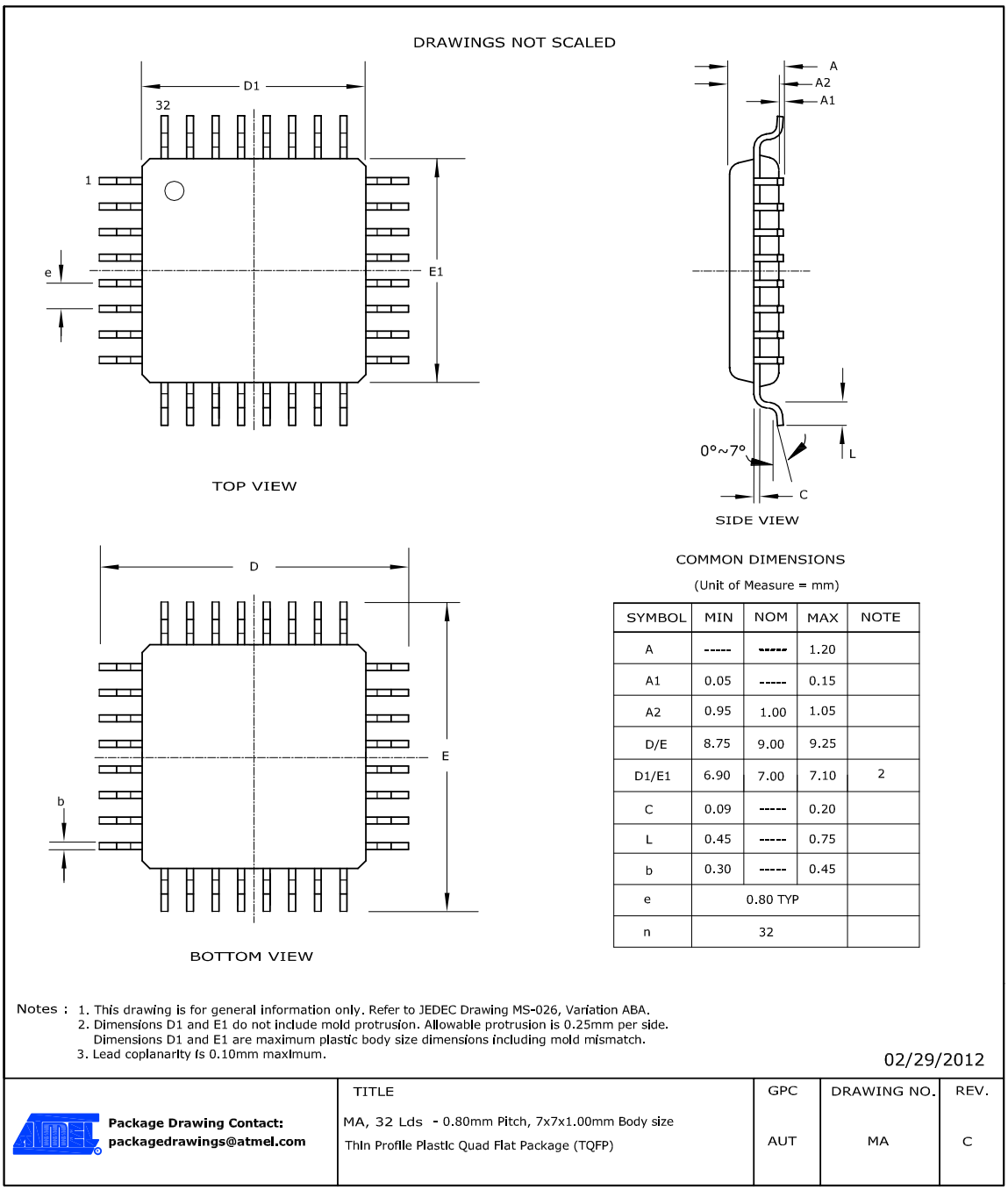
Related Links

1. Configuration Summary

Mode	Conditions	Regulator	PL	CPU Clock	Vcc	Ta	Typ.	Max.	Units
		BUCK	PL0	DFLLUP at 8 MHz	1.8V		28.1	72	
					3.3V		18.5	47	
				OSC 8 MHz	1.8V		32.2	73	
					3.3V		25.3	51	
				OSC 4 MHz	1.8V		38.4	121	
					3.3V		31.9	86	
			PL2	FDPLL96 at 32 MHz	1.8V		41.5	55	
					3.3V		24.6	34	
				DFLLULP at 32 MHz	1.8V		37.1	53	
					3.3V		22.0	32	
IDLE		LDO	PL0	DFLLUP at 8 MHz	1.8V		16.0	81	
					3.3V		16.2	82	
				OSC 8 MHz	1.8V		19.8	82	
					3.3V		22.0	85	
				OSC 4 MHz	1.8V		26.2	152	
					3.3V		29.2	157	
			PL2	FDPLL96 at 32 MHz	1.8V		20.3	54	
					3.3V		20.4	54	
				DFLLULP at 32 MHz	1.8V		14.3	32	
					3.3V		14.4	33	
		BUCK	PL0	DFLLUP at 8 MHz	1.8V		11.1	52	
					3.3V		8.3	35	
				OSC 8 MHz	1.8V		15.5	55	
					3.3V		15.2	40	
				OSC 4 MHz	1.8V		21.3	100	
					3.3V		21.6	73	
			PL2	FDPLL96 at 32 MHz	1.8V		14.9	30	
					3.3V		9.1	19	
				DFLLULP at 32 MHz	1.8V		10.6	24	
					3.3V		6.7	15	

49.2 Package Drawings

49.2.1 32-pin TQFP



COMMON DIMENSIONS

(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	-----	-----	1.20	
A1	0.05	-----	0.15	
A2	0.95	1.00	1.05	
D/E	8.75	9.00	9.25	
D1/E1	6.90	7.00	7.10	2
C	0.09	-----	0.20	
L	0.45	-----	0.75	
b	0.30	-----	0.45	
e	0.80 TYP			
n	32			

Notes : 1. This drawing is for general information only. Refer to JEDEC Drawing MS-026, Variation ABA.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10mm maximum.

02/29/2012

Package Drawing Contact: packagedrawings@atmel.com	TITLE	GPC	DRAWING NO.	REV.
	MA, 32 Lds - 0.80mm Pitch, 7x7x1.00mm Body size Thin Profile Plastic Quad Flat Package (TQFP)	AUT	MA	C

Table 49-1. Device and Package Maximum Weight

100	mg

Table 49-2. Package Characteristics

Moisture Sensitivity Level	MSL3