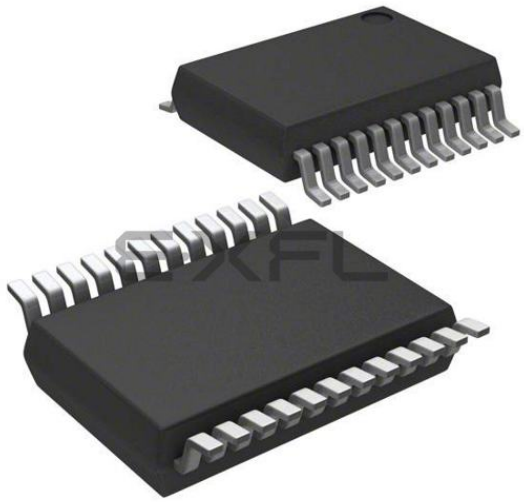

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M23
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	17
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.63V
Data Converters	A/D 5x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	24-SSOP (0.209", 5.30mm Width)
Supplier Device Package	24-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsaml10d15a-yf

Features	Cortex-M23 Configurable Options	SAM L10 Implementation	SAM L11 Implementation
Cross Trigger Interface (CTI)	Present or absent	Absent	Absent
Micro Trace Buffer (MTB)	Present or absent	Absent	Absent
Embedded Trace Macrocell (ETM)	Present or absent	Absent	Absent
JTAGnSW debug protocol	Selects between JTAG or Serial-Wire interfaces for the DAP	Serial-Wire	Serial-Wire
Multi-drop for Serial Wire	Present or absent	Absent	Absent

Note:

1. Refer to Table 11-3 for more information.

For more details, refer to the ARM Cortex-M23 Processor Technical Reference Manual (http://www.arm.com).

11.1.2 Cortex-M23 Core Peripherals

The processor has the following core peripheral:

- System Timer (SysTick)
  - The System Timer is a 24-bit timer clocked by the core frequency.

> **Important:** On SAM L11 devices, there are two System timers, one for Secure state and one for Non-secure state.

- Nested Vectored Interrupt Controller (NVIC)
  - The NVIC is an embedded interrupt controller that supports low latency interrupt processing.

> **Important:** On SAM L11 devices, there are two Vector tables: the Secure Vector table and the Non-Secure Vector table.

- System Control Block (SCB)
  - The System Control Block (SCB) provides system implementation information and system control that includes configuration, control, and reporting of system exceptions
- Memory Protection Unit (MPU)
  - The MPU improves system reliability by defining the memory attributes for different memory regions.

> **Important:** On SAM L11 devices, there are two MPUs: one for the Secure state and one for the Non-secure state. Each MPU can define memory access permissions and attributes independently.

- Security Attribution Unit (SAU)
  - The SAU improves system security by defining security attributes for different regions.

16.12.2 Status A

Name: STATUSA
Offset: 0x0001
Reset: 0x00
Property: PAC Write-Protection

Bit	7	6	5	4	3	2	1	0
			BREXT	PERR	FAIL	BERR	CRSTEXT	DONE
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit 5 – BREXT Boot ROM Phase Extension
Writing a '0' to this bit has no effect.

Writing a '1' to this bit clears the Boot ROM Phase Extension bit.

This bit is set when a debug adapter Cold-Plugging is detected, which extends the Boot ROM phase.

Bit 4 – PERR Protection Error
Writing a '0' to this bit has no effect.

Writing a '1' to this bit clears the Protection Error bit.

This bit is set upon access to:

- A reserved address
- CTRL, ADDR, LENGTH, DATA, CFG from the external address space when DAL<2
- The internal address space with a Non-Secure access (security violation) (SAM L11 only)

Bit 3 – FAIL Failure
Writing a '0' to this bit has no effect.

Writing a '1' to this bit clears the Failure bit.

This bit is set when a DSU operation failure is detected.

Bit 2 – BERR Bus Error
Writing a '0' to this bit has no effect.

Writing a '1' to this bit clears the Bus Error bit.

This bit is set when a bus error is detected.

Bit 1 – CRSTEXT CPU Reset Phase Extension
Writing a '0' to this bit has no effect.

Writing a '1' to this bit clears the CPU Reset Phase Extension bit.

This bit is set when a debug adapter Cold-Plugging is detected, which extends the CPU reset phase.

Bit 0 – DONE Done
Writing a '0' to this bit has no effect.

Writing a '1' to this bit clears the Done bit.

16.12.13 CoreSight ROM Table Entry 0

Name: ENTRY0
Offset: 0x1000
Reset: 0xXXXXX00X
Property: PAC Write-Protection

Bit	31	30	29	28	27	26	25	24
	ADDOFF[19:12]							
Access	R	R	R	R	R	R	R	R
Reset	x	x	x	x	x	x	x	x

Bit	23	22	21	20	19	18	17	16
	ADDOFF[11:4]							
Access	R	R	R	R	R	R	R	R
Reset	x	x	x	x	x	x	x	x

Bit	15	14	13	12	11	10	9	8
	ADDOFF[3:0]							
Access	R	R	R	R				
Reset	x	x	x	x				

Bit	7	6	5	4	3	2	1	0
							FMT	EPRES
Access							R	R
Reset							1	x

Bits 31:12 – ADDOFF[19:0] Address Offset
The base address of the component, relative to the base address of this ROM table.

Bit 1 – FMT Format
Always reads as '1', indicating a 32-bit ROM table.

Bit 0 – EPRES Entry Present
This bit indicates whether an entry is present at this location in the ROM table.

This bit is set at power-up if the device is not protected indicating that the entry is not present.

This bit is cleared at power-up if the device is not protected indicating that the entry is present.

In the data sheet, references to Synchronous Clocks are referring to the CPU and bus clocks (MCLK), while asynchronous clocks are generated by the Generic Clock Controller (GCLK).

17.3 Register Synchronization

17.3.1 Overview

All peripherals are composed of one digital bus interface connected to the APB or AHB bus and running from a corresponding clock in the Main Clock domain, and one peripheral core running from the peripheral Generic Clock (GCLK).

Communication between these clock domains must be synchronized. This mechanism is implemented in hardware, so the synchronization process takes place even if the peripheral generic clock is running from the same clock source and on the same frequency as the bus interface.

All registers in the bus interface are accessible without synchronization.

All registers in the peripheral core are synchronized when written. Some registers in the peripheral core are synchronized when read.

Each individual register description will have the properties "Read-Synchronized" and/or "Write-Synchronized" if a register is synchronized.

As shown in the figure below, each register that requires synchronization has its individual synchronizer and its individual synchronization status bit in the Synchronization Busy register (SYNCBUSY).
Note: For registers requiring both read- and write-synchronization, the corresponding bit in SYNCBUSY is shared.

22.8.6 Interrupt Flag Status and Clear

Name: INTFLAG
Offset: 0x06
Reset: 0x00
Property: –

Bit	7	6	5	4	3	2	1	0
								PLRDY
Access								R/W
Reset								0

Bit 0 – PLRDY Performance Level Ready
This flag is set when the performance level is ready and will generate an interrupt if INTENCLR/SET.PLRDY is '1'.

Writing a '1' to this bit has no effect.

Writing a '1' to this bit clears the Performance Ready interrupt flag.

25.7 Register Summary

Offset	Name	Bit Pos.								
0x00	INTENCLR	7:0						B33SRDY	BOD33DET	BOD33RDY
		15:8					ULPVREFRDY	VCORERDY		VREGRDY
		23:16								
		31:24								
0x04	INTENSET	7:0						B33SRDY	BOD33DET	BOD33RDY
		15:8					ULPVREFRDY	VCORERDY		VREGRDY
		23:16								
		31:24								
0x08	INTFLAG	7:0						B33SRDY	BOD33DET	BOD33RDY
		15:8					ULPVREFRDY	VCORERDY		VREGRDY
		23:16								
		31:24								
0x0C	STATUS	7:0						B33SRDY	BOD33DET	BOD33RDY
		15:8				ULPVREFRDY		VCORERDY		VREGRDY
		23:16								
		31:24								
0x10	BOD33	7:0		RUNSTDBY	STDBYCFG	ACTION[1:0]		HYST	ENABLE	
		15:8	PSEL[3:0]				VREFSEL			ACTCFG
		23:16			LEVEL[5:0]					
		31:24								
0x14 ... 0x17	Reserved									
0x18	VREG	7:0		RUNSTDBY	STDBYPL0			SEL	ENABLE	
		15:8							VREFSEL	LPEFF
		23:16					VSVSTEP[3:0]			
		31:24	VSPER[7:0]							
0x1C	VREF	7:0	ONDEMAND	RUNSTDBY				VREFOE	TSEN	
		15:8								
		23:16					SEL[3:0]			
		31:24								
0x20 ... 0x2B	Reserved									
0x2C	EVCTRL	7:0							BOD33DETEO	
		15:8								
		23:16								
		31:24								

26.8.4 Interrupt Enable Clear

Name: INTENCLR
Offset: 0x04
Reset: 0x00
Property: PAC Write-Protection

This register allows the user to disable an interrupt without doing a read-modify-write operation. Changes in this register will also be reflected in the Interrupt Enable Set (INTENSET) register.

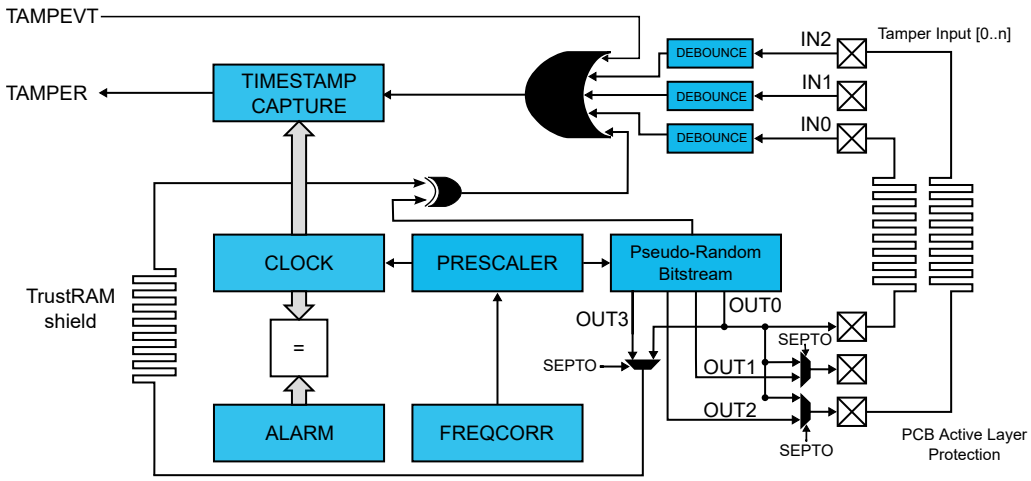
Bit	7	6	5	4	3	2	1	0
								EW
Access								R/W
Reset								0

Bit 0 – EW Early Warning Interrupt Enable
Writing a '0' to this bit has no effect.

Writing a '1' to this bit clears the Early Warning Interrupt Enable bit, which disables the Early Warning interrupt.

Value	Description
0	The Early Warning interrupt is disabled.
1	The Early Warning interrupt is enabled.

Figure 27-4. RTC Block Diagram (Tamper Detection Use Case)



Related Links

27.6.2.3 32-Bit Counter (Mode 0)
27.6.2.4 16-Bit Counter (Mode 1)
27.6.2.5 Clock/Calendar (Mode 2)
27.6.8.4 Tamper Detection

27.4 Signal Description

Table 27-1. Signal Description

Signal	Description	Type
INn [n=0..4]	Tamper Detection Input	Digital input
OUT	Tamper Detection Output	Digital output

One signal can be mapped to one of several pins.

Related Links

4.1 Multiplexed Signals

27.5 Product Dependencies

In order to use this peripheral, other parts of the system must be configured correctly, as described below.

27.5.1 I/O Lines

For more information on I/O configurations, refer to the "RTC Pinout" section.

Related Links: I/O Multiplexing and Considerations

27.5.2 Power Management

The RTC will continue to operate in any sleep mode where the selected source clock is running. The RTC interrupts can be used to wake up the device from sleep modes. Events connected to the event system can trigger other operations in the system without exiting sleep modes. Refer to the *Power Manager* for details on the different sleep modes.

Refer to *Peripherals Security Attribution* for more information.

29.8.13 Pin State

Name: PINSTATE
Offset: 0x38
Reset: 0x00000000
Property: PAC Mix-Secure

Important: For **SAM L11 Non-Secure** accesses, read accesses (R*) are allowed only if the external interrupt x (EXTINTx) is set as Non-Secure in the NONSEC register (NONSEC.EXTINTx bit).

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	PINSTATE[7:0]							
Access	R/R*/R	R/R*/R	R/R*/R	R/R*/R	R/R*/R	R/R*/R	R/R*/R	R/R*/R
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – PINSTATE[7:0] Pin State
These bits return the valid pin state of the debounced external interrupt pin EXTINTx.

30. NVMCTRL – Nonvolatile Memory Controller

30.1 Overview

Non-Volatile Memory (NVM) is a reprogrammable Flash memory that retains program and data storage even with power off. It embeds three separate arrays namely FLASH, Data FLASH and AUX FLASH. The Data FLASH array can be programmed while reading the FLASH array. It is intended to store data while executing from the FLASH without stalling. AUX FLASH stores data needed during the device startup such as calibration and system configuration. The NVM Controller (NVMCTRL) connects to the AHB and APB bus interfaces for system access to the NVM block. The AHB interface is used for reads and writes to the NVM block, while the APB interface is used for commands and configuration.

30.2 Features

- 32-bit AHB interface for reads and writes
- Write-While-Read (WWR) Data Flash
- All NVM Sections are Memory Mapped to the AHB, Including Calibration and System Configuration
- 32-bit APB Interface for Commands and Control
- Programmable Wait States for Read Optimization
- 6 Regions can be Individually Protected or Unprotected
- Additional Protection for Bootloader
- Interface to Power Manager for Power-Down of Flash Blocks in Sleep Modes
- Can Optionally Wake-up on Exit from Sleep or on First Access
- Direct-mapped Cache
- TrustZone Support **(SAM L11)**

Note: A register with property "Enable-Protected" may contain bits that are *not* enable-protected.

Offset	Name	Bit Pos.								
0x54	CHINTENCLR6	7:0							EVD	OVR
0x55	CHINTENSET6	7:0							EVD	OVR
0x56	CHINTFLAG6	7:0							EVD	OVR
0x57	CHSTATUS6	7:0							BUSYCH	RDYUSR
0x58	CHANNEL7	7:0			EVGEN[5:0]					
		15:8	ONDEMAND	RUNSTDBY			EDGSEL[1:0]		PATH[1:0]	
		23:16								
		31:24								
0x5C	CHINTENCLR7	7:0							EVD	OVR
0x5D	CHINTENSET7	7:0							EVD	OVR
0x5E	CHINTFLAG7	7:0							EVD	OVR
0x5F	CHSTATUS7	7:0							BUSYCH	RDYUSR
0x60 ... 0x011F	Reserved									
0x0120	USER0	7:0					CHANNEL[3:0]			
0x0121	USER1	7:0					CHANNEL[3:0]			
0x0122	USER2	7:0					CHANNEL[3:0]			
0x0123	USER3	7:0					CHANNEL[3:0]			
0x0124	USER4	7:0					CHANNEL[3:0]			
0x0125	USER5	7:0					CHANNEL[3:0]			
0x0126	USER6	7:0					CHANNEL[3:0]			
0x0127	USER7	7:0					CHANNEL[3:0]			
0x0128	USER8	7:0					CHANNEL[3:0]			
0x0129	USER9	7:0					CHANNEL[3:0]			
0x012A	USER10	7:0					CHANNEL[3:0]			
0x012B	USER11	7:0					CHANNEL[3:0]			
0x012C	USER12	7:0					CHANNEL[3:0]			
0x012D	USER13	7:0					CHANNEL[3:0]			
0x012E	USER14	7:0					CHANNEL[3:0]			
0x012F	USER15	7:0					CHANNEL[3:0]			
0x0130	USER16	7:0					CHANNEL[3:0]			
0x0131	USER17	7:0					CHANNEL[3:0]			
0x0132	USER18	7:0					CHANNEL[3:0]			
0x0133	USER19	7:0					CHANNEL[3:0]			
0x0134	USER20	7:0					CHANNEL[3:0]			
0x0135	USER21	7:0					CHANNEL[3:0]			
0x0136	USER22	7:0					CHANNEL[3:0]			
0x0137 ... 0x01D3	Reserved									
0x01D4	INTENCLR	7:0								NSCHK
0x01D5	INTENSET	7:0								NSCHK
0x01D6	INTFLAG	7:0								NSCHK
0x01D7	Reserved									
0x01D8	NONSECCHAN	7:0	CHANNELn[7:0]							

33.7.7 Ready Users

Name: READYUSR
Offset: 0x1C
Reset: 0x0000000F
Property: Mix-Secure

Important: For **SAM L11 Non-Secure** accesses, read accesses (R*) are allowed only if the security attribution for the corresponding channel (CHANNELx) is set as Non-Secured in the NONSECCHAN register.

Bit	31	30	29	28	27	26	25	24
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
					READYUSR3	READYUSR2	READYUSR1	READYUSR0
Access	R	R	R	R	R/R*/R	R/R*/R	R/R*/R	R/R*/R
Reset	0	0	0	0	1	1	1	1

Bits 0, 1, 2, 3 – READYUSR Ready User for Channel n
This bit is set when all event users connected to channel n are ready to handle incoming events on channel n.

This bit is cleared when at least one of the event users connected to the channel is not ready.

When the event channel n path is asynchronous, this bit is always read zero.

35.8.8 Interrupt Flag Status and Clear

Name: INTFLAG
Offset: 0x18
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
	ERROR		RXBRK	CTSIC	RXS	RXC	TXC	DRE
Access	R/W		R/W	R/W	R/W	R	R/W	R
Reset	0		0	0	0	0	0	0

Bit 7 – ERROR Error
This flag is cleared by writing '1' to it.

This bit is set when any error is detected. Errors that will set this flag have corresponding status flags in the STATUS register. Errors that will set this flag are COLL, ISF, BUFOVF, FERR, and PERR.Writing '0' to this bit has no effect.

Writing '1' to this bit will clear the flag.

Bit 5 – RXBRK Receive Break
This flag is cleared by writing '1' to it.

This flag is set when auto-baud is enabled (CTRLA.FORM) and a break character is received.

Writing '0' to this bit has no effect.

Writing '1' to this bit will clear the flag.

Bit 4 – CTSIC Clear to Send Input Change
This flag is cleared by writing a '1' to it.

This flag is set when a change is detected on the CTS pin.

Writing '0' to this bit has no effect.

Writing '1' to this bit will clear the flag.

Bit 3 – RXS Receive Start
This flag is cleared by writing '1' to it.

This flag is set when a start condition is detected on the RxD line and start-of-frame detection is enabled (CTRLB.SFDE is '1').

Writing '0' to this bit has no effect.

Writing '1' to this bit will clear the Receive Start interrupt flag.

Bit 2 – RXC Receive Complete
This flag is cleared by reading the Data register (DATA) or by disabling the receiver.

This flag is set when there are unread data in DATA.

Writing '0' to this bit has no effect.

32. PORT - I/O Pin Controller

36.5.2 Power Management

This peripheral can continue to operate in any sleep mode where its source clock is running. The interrupts can wake up the device from sleep modes.

Related Links

22. PM – Power Manager

36.5.3 Clocks

The SERCOM bus clock (CLK_SERCOMx_APB) can be enabled and disabled in the Main Clock Controller. Refer to *Peripheral Clock Masking* for details and default status of this clock.

A generic clock (GCLK_SERCOMx_CORE) is required to clock the SPI. This clock must be configured and enabled in the Generic Clock Controller before using the SPI.

This generic clock is asynchronous to the bus clock (CLK_SERCOMx_APB). Therefore, writes to certain registers will require synchronization to the clock domains.

Related Links

18. GCLK - Generic Clock Controller
19.6.2.6 Peripheral Clock Masking
36.6.6 Synchronization

36.5.4 DMA

The DMA request lines are connected to the DMA Controller (DMAC). In order to use DMA requests with this peripheral the DMAC must be configured first. Refer to *DMAC – Direct Memory Access Controller* for details.

Related Links

28. DMAC – Direct Memory Access Controller

36.5.5 Interrupts

The interrupt request line is connected to the Interrupt Controller. In order to use interrupt requests of this peripheral, the Interrupt Controller (NVIC) must be configured first. Refer to *Nested Vector Interrupt Controller* for details.

36.5.6 Events

Not applicable.

36.5.7 Debug Operation

When the CPU is halted in debug mode, this peripheral will continue normal operation. If the peripheral is configured to require periodical service by the CPU through interrupts or similar, improper operation or data loss may result during debugging. This peripheral can be forced to halt operation during debugging - refer to the Debug Control (DBGCTRL) register for details.

36.5.8 Register Access Protection

Registers with write-access can be write-protected optionally by the peripheral access controller (PAC).

PAC Write-Protection is not available for the following registers:

- Interrupt Flag Clear and Status register (INTFLAG)

36.6.3 Additional Features

36.6.3.1 Address Recognition

When the SPI is configured for slave operation (CTRLA.MODE=0x2) with address recognition (CTRLA.FORM is 0x2), the SERCOM address recognition logic is enabled: the first character in a transaction is checked for an address match.

If there is a match, the Receive Complete Interrupt flag in the Interrupt Flag Status and Clear register (INTFLAG.RXC) is set, the MISO output is enabled, and the transaction is processed. If the device is in sleep mode, an address match can wake up the device in order to process the transaction.

If there is no match, the complete transaction is ignored.

If a 9-bit frame format is selected, only the lower 8 bits of the shift register are checked against the Address register (ADDR).

Preload must be disabled (CTRLB.PLOADEN=0) in order to use this mode.

Related Links

34.6.3.1 Address Match and Mask

36.6.3.2 Preloading of the Slave Shift Register

When starting a transaction, the slave will first transmit the contents of the shift register before loading new data from DATA. The first character sent can be either the reset value of the shift register (if this is the first transmission since the last reset) or the last character in the previous transmission.

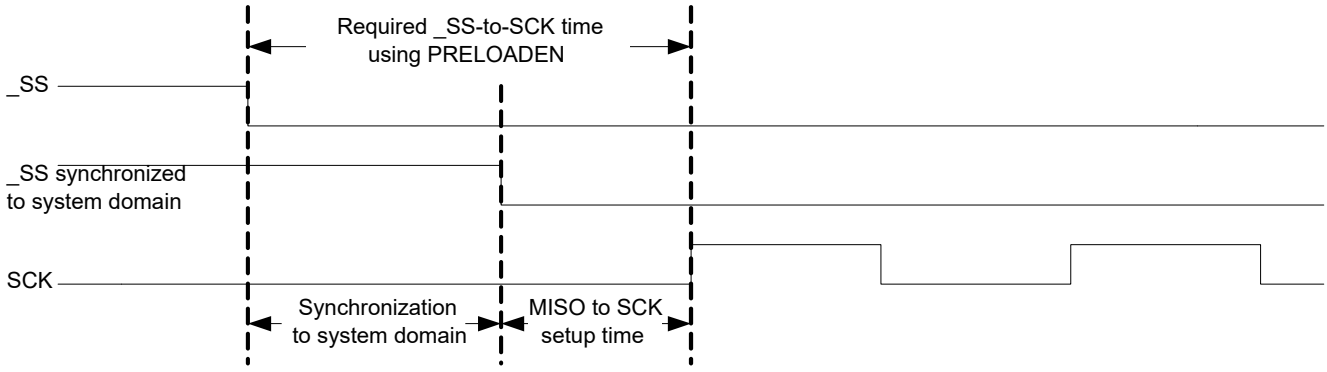
Preloading can be used to preload data into the shift register while $\overline{SS}$ is high: this eliminates sending a dummy character when starting a transaction. If the shift register is not preloaded, the current contents of the shift register will be shifted out.

Only one data character will be preloaded into the shift register while the synchronized $\overline{SS}$ signal is high. If the next character is written to DATA before $\overline{SS}$ is pulled low, the second character will be stored in DATA until transfer begins.

For proper preloading, sufficient time must elapse between $\overline{SS}$ going low and the first SCK sampling edge, as in Timing Using Preloading. See also the *Electrical Characteristics* chapters for timing details.

Preloading is enabled by writing '1' to the Slave Data Preload Enable bit in the CTRLB register (CTRLB.PLOADEN).

Figure 36-4. Timing Using Preloading



36.6.3.3 Master with Several Slaves

Master with multiple slaves in parallel is only available when Master Slave Select Enable (CTRLB.MSSEN) is set to zero and hardware $\overline{SS}$ control is disabled. If the bus consists of several SPI

Value	Description
0	SWRST synchronization is not busy.
1	SWRST synchronization is busy.

Value	Name	Description
0x07	AIN7	ADC AIN7 pin
0x08	AIN8	ADC AIN8 pin
0x09	AIN9	ADC AIN9 pin
0x0A – 0x17	-	Reserved
0x18	TEMP	Temperature Sensor
0x19	BANDGAP	INTREF Voltage Reference
0x1A	SCALEDVDDCORE	1/4 Scaled VDDCORE Supply
0x1B	SCALEDVDDANA	1/4 Scaled VDDANA Supply
0x1C	DAC	DAC Output
0x1D	SCALEDVDDIO	1/4 Scaled VDDIO Supply
0x1E	OPAMP01	OPAMP0 or OPAMP1 output
0x1F	OPAMP2	OPAMP2 output

For Window Mode operation, both comparators in a pair must have the same RUNSTDBY configuration.

When RUNSTDBY is one, any enabled AC interrupt source can wake up the CPU. The AC can also be used during sleep modes where the clock used by the AC is disabled, provided that the AC is still powered (not in shutdown). In this case, the behavior is slightly different and depends on the measurement mode, as listed in Table 42-1.

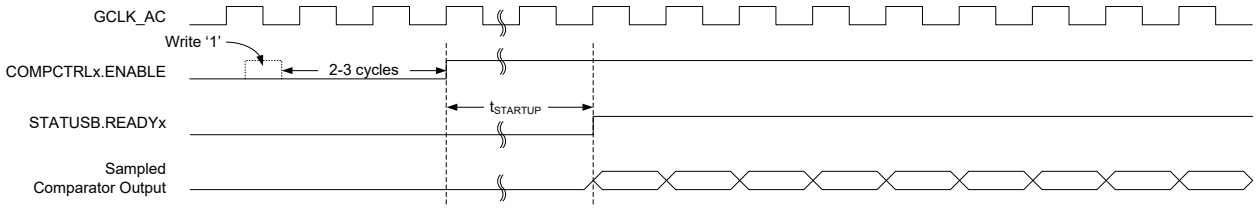
Table 42-1. Sleep Mode Operation

COMPCTRLx.MODE	RUNSTDBY=0	RUNSTDBY=1
0 (Continuous)	COMPx disabled	GCLK_AC stopped, COMPx enabled
1 (Single-shot)	COMPx disabled	GCLK_AC stopped, COMPx enabled only when triggered by an input event

42.6.14.1 Continuous Measurement during Sleep

When a comparator is enabled in continuous measurement mode and GCLK_AC is disabled during sleep, the comparator will remain continuously enabled and will function asynchronously. The current state of the comparator is asynchronously monitored for changes. If an edge matching the interrupt condition is found, GCLK_AC is started to register the interrupt condition and generate events. If the interrupt is enabled in the Interrupt Enable registers (INTENCLR/SET), the AC can wake up the device; otherwise GCLK_AC is disabled until the next edge detection. Filtering is not possible with this configuration.

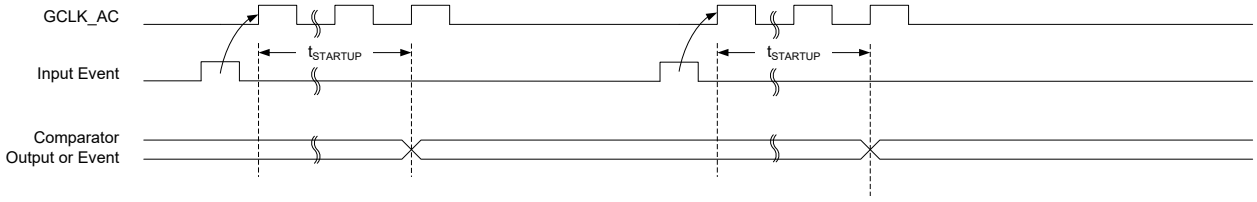
Figure 42-9. Continuous Mode SleepWalking



42.6.14.2 Single-Shot Measurement during Sleep

For low-power operation, event-triggered measurements can be performed during sleep modes. When the event occurs, the Power Manager will start GCLK_AC. The comparator is enabled, and after the start-up time has passed, a comparison is done, with filtering if desired, and the appropriate peripheral events and interrupts are also generated, as shown in Figure 42-10. The comparator and GCLK_AC are then disabled again automatically, unless configured to wake the system from sleep. Filtering is allowed with this configuration.

Figure 42-10. Single-Shot SleepWalking



42.6.15 Synchronization

Due to asynchronicity between the main clock domain and the peripheral clock domains, some registers need to be synchronized when written or read.

The following bits are synchronized when written:

Mode	Conditions	Regulator	PL	CPU Clock	Vcc	Ta	Typ.	Max.	Units
		BUCK	PL0	DFLLUP at 8 MHz	1.8V		28.1	72	
					3.3V		18.5	47	
				OSC 8 MHz	1.8V		32.2	73	
					3.3V		25.3	51	
				OSC 4 MHz	1.8V		38.4	121	
					3.3V		31.9	86	
			PL2	FDPLL96 at 32 MHz	1.8V		41.5	55	
					3.3V		24.6	34	
				DFLLULP at 32 MHz	1.8V		37.1	53	
					3.3V		22.0	32	
IDLE		LDO	PL0	DFLLUP at 8 MHz	1.8V		16.0	81	
					3.3V		16.2	82	
				OSC 8 MHz	1.8V		19.8	82	
					3.3V		22.0	85	
				OSC 4 MHz	1.8V		26.2	152	
					3.3V		29.2	157	
			PL2	FDPLL96 at 32 MHz	1.8V		20.3	54	
					3.3V		20.4	54	
				DFLLULP at 32 MHz	1.8V		14.3	32	
					3.3V		14.4	33	
		BUCK	PL0	DFLLUP at 8 MHz	1.8V		11.1	52	
					3.3V		8.3	35	
				OSC 8 MHz	1.8V		15.5	55	
					3.3V		15.2	40	
				OSC 4 MHz	1.8V		21.3	100	
					3.3V		21.6	73	
			PL2	FDPLL96 at 32 MHz	1.8V		14.9	30	
					3.3V		9.1	19	
				DFLLULP at 32 MHz	1.8V		10.6	24	
					3.3V		6.7	15	