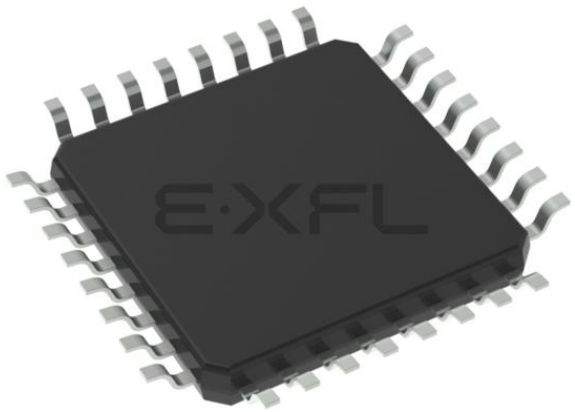

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M23
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	25
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.63V
Data Converters	A/D 10x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	32-TQFP
Supplier Device Package	32-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsaml10e14a-aft

Offset	Bit Pos.	Name					
0x03	31:24	WDT_PER		WDT_ALWAYSON	WDT_ENABLE	WDT_RUNSTDBY	BOD12 Calibration Parameters
0x04	39:32	WDT_EWOFFSET		WDT_WINDOW			
0x05	47:40	Reserved	DXN	RXN	Reserved	BOD33_HYST	WDT_WEN
0x06	55:48	Reserved					
0x07	63:56	Reserved					
0x08	71:64	AS					
0x09	79:72	Reserved	ANSC				
0x0A	87:80	Reserved	DS				
0x0B	95:88	Reserved	RS				
0x0C	103:96	Reserved	URWEN				
0x0D-0xF	127:104	Reserved					
0x10-0x13	159:128	NONSECA					
0x14-0x17	191:160	NONSECB					
0x18-0x1B	223:192	NONSECC					
0x1C-0x1F	255:224	USERCRC					

10.2.2 NVM Software Calibration Area

The NVM Software Calibration Area contains calibration data that can be used by some peripherals, such as the ADC.

Note: Calibration data are determined and written during production test and cannot be written.

The NVM Software Calibration Area can be read at address 0x00806020.

Table 10-12. NVM Software Calibration Bitfields Definition

Bit Position	Name	Description
2:0	ADC LINEARITY	ADC Linearity Calibration. Should be written to CALIB register.
5:3	ADC BIASCAL	ADC Bias Calibration. Should be written to CALIB register.
8:6	DFLLULP Division Factor in PL0	DFLLULP Division Factor in PL0. Should be written to DFLLULPCTRL register.
11:9	DFLLULP Division Factor in PL2	DFLLULP Division Factor in PL2. Should be written to DFLLULPCTRL register.
127:12	Reserved	Reserved

Table 10-13. NVM Software Calibration Row Mapping

Offset	Bit Pos.	Name					
0x00	7:0	DFLLULP Division Factor in PL0	ADC BIASCAL	ADC LINEARITY			
0x01	15:8	Reserved	DFLLULP Division Factor in PL2	DFLLULP Division Factor in PL0			
0x02-0xF	127:16	Reserved					

10.2.3 NVM Temperature Log Row

The NVM Temperature Log Row contains calibration data that are determined and written during production test and cannot be written.

These calibration values are required for calculating the temperature from measuring the temperature sensor in the Supply Controller (SUPC) by the ADC.

  - Countermeasures against side-channel attacks for AES
- Secure Hash Algorithm 2 (SHA-256), compliant with FIPS Pub 180-4
  - Accelerates message schedule and inner compression loop
- Galois Counter Mode (GCM) encryption using AES engine and authentication
  - Accelerates the GF(2128) multiplication for AES-GCM hash function

13.3.3 CRYA APIs

The CRYA APIs which are located in a dedicated Boot ROM area are only accessible from the user application after the Boot ROM has completed. This area is an execute-only area, meaning the CPU cannot do any loads, but can call the APIs. The Boot ROM memory space is a secure area, only the secure application can directly call these APIs.

Table 13-12. CRYA APIs Addresses

CRYA API	Address
AES Encryption	0x02001904
AES Decryption	0x02001908
SHA Process	0x02001900
GCM Process	0x0200190C

13.3.3.1 AES API

The AES software has two function routines to do encryption and decryption on a 128 bit block of input data.

The AES encryption function entry point is located at the Boot ROM address 0x02001904 and the encryption function parameters are:

- Src[in] : a pointer to a 128-bit data block to be encrypted
- Dst[out]: a pointer to 128 bit encrypted data
- Keys[in]: a pointer to 128 bit key
- Length[in]: Number of 32-bit words comprising the Key, 4 for 128 bits key

The AES decryption function entry point is located at the Boot ROM address 0x02001908 and the decryption function parameters are:

- Src[in] : a pointer to a 128-bit data block to be decrypted
- Dst[out]: a pointer to 128 bit decrypted data
- Keys[in]: a pointer to 128 bit key
- Length[in]: Number of 32-bit words comprising the Key, 4 for 128 bits key

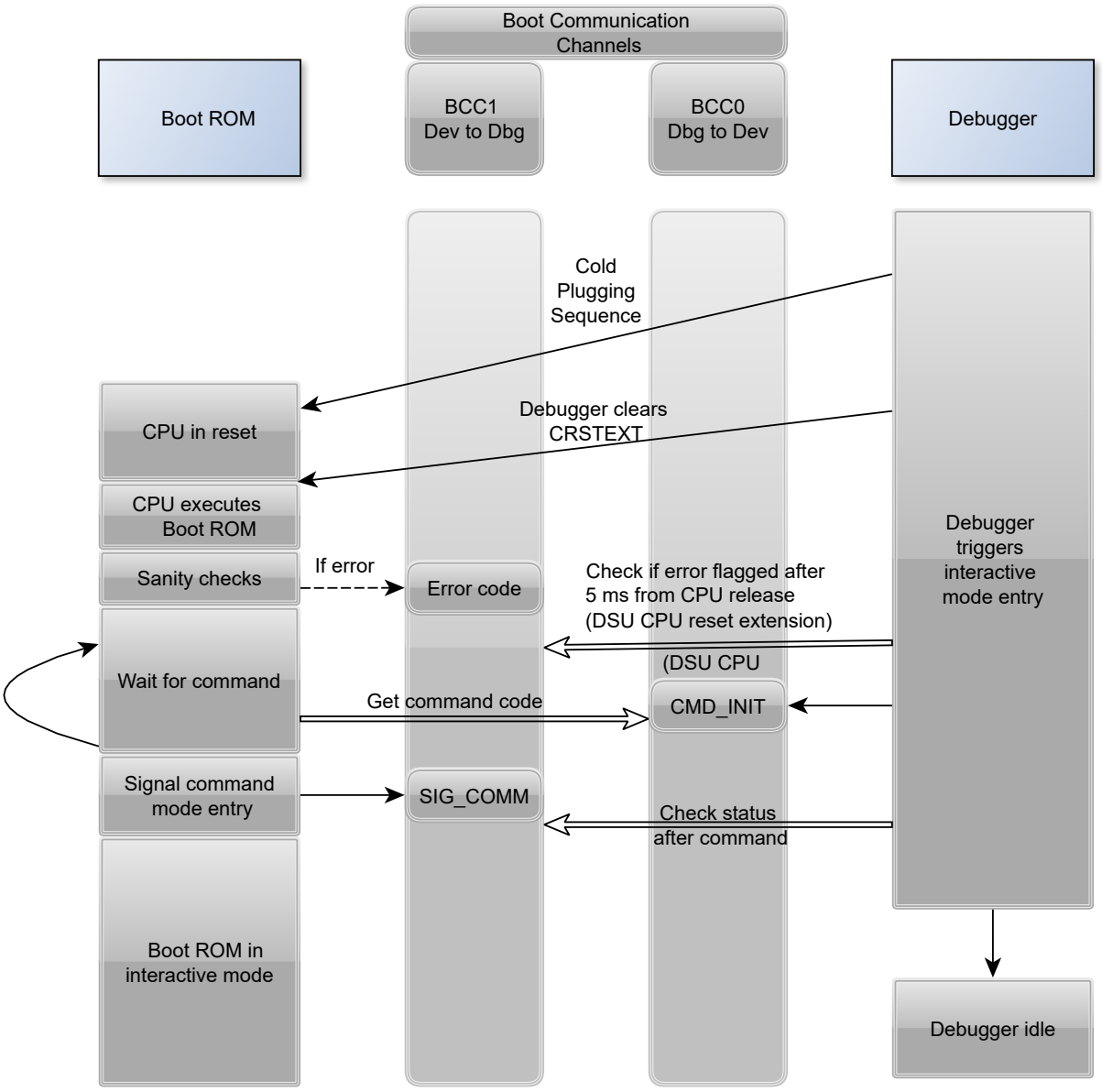
The APIs are:

```
/* Type definition for CRYA AES functions. */
typedef void (*crya_aes_encrypt_t) (const uint8_t *keys, uint32_t key_len, const
uint8_t *src, uint8_t *dst);
typedef void (*crya_aes_decrypt_t) (const uint8_t *keys, uint32_t key_len, const
uint8_t *src, uint8_t *dst);
```

```
/* AES encrypt function
* \param keys[in]: A pointer to 128-bit key
* \param key_len[in]: Number of 32-bit words comprising the key, 4 for 128-bit key
* \param src[in]: A pointer to a 128-bit data block to be encrypted
```

14.4.5.1.1 CMD_INIT

Figure 14-7. CMD_INIT Flow diagram



14.4.5.2 Exit Interactive Mode (CMD_EXIT)

This command allows exiting the Boot Interactive mode.

Exiting the Boot Interactive mode allows to jump to one of the following:

- The Application
- The CPU Park Mode

19.8.6 AHB Mask

Name: AHBMASK
Offset: 0x10
Reset: 0x000001FFF
Property: PAC Write-Protection

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
				TRAM	Reserved	Reserved	Reserved	Reserved
Access				R/W	R/W	R/W	R/W	R/W
Reset				1	1	1	1	1

Bit	7	6	5	4	3	2	1	0
	NVMCTRL	PAC	Reserved	DSU	DMAC	APBC	APBB	APBA
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit 12 – TRAM TRAM AHB Clock Enable

Value	Description
0	The AHB clock for the TRAM is stopped
1	The AHB clock for the TRAM is enabled

Bit 11 – Reserved Must Be Set to 1
Bit 11 must always be set to ‘1’ when programming the AHBMASK register.

Bit 10 – Reserved Must Be Set to 1
Bit 10 must always be set to ‘1’ when programming the AHBMASK register.

Bit 9 – Reserved Must Be Set to 1
Bit 9 must always be set to ‘1’ when programming the AHBMASK register.

Bit 8 – Reserved Must Be Set to 1
Bit 8 must always be set to ‘1’ when programming the AHBMASK register.

Bit 7 – NVMCTRL NVMCTRL AHB Clock Enable

23.8.14 DFLLULP Synchronization Busy

Name: DFLLULPSYNCBUSY
Offset: 0x28
Reset: 0x00000000
Property: -

Bit	31	30	29	28	27	26	25	24
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
					DELAY		ENABLE	
Access	R	R	R	R	R		R	R
Reset	0	0	0	0	0		0	0

Bit 3 – DELAY Delay Register Synchronization Busy
This bit is cleared when the synchronization of DFLLULPDLY is complete.

This bit is set when the synchronization of DFLLULPDLY is started.

Writing this bit has no effect.

Bit 1 – ENABLE Enable Bit Synchronization Busy
This bit is cleared when the synchronization of DFLLULPCTRL.ENABLE is complete.

This bit is set when the synchronization of DFLLULPCTRL.ENABLE is started.

Writing this bit has no effect.

24.5.9 Analog Connections

The external 32.768kHz crystal must be connected between the XIN32 and XOUT32 pins, along with any required load capacitors. For details on recommended oscillator characteristics and capacitor load, refer to the related links.

24.6 Functional Description

24.6.1 Principle of Operation

XOSC32K and OSCULP32K are configured via OSC32KCTRL control registers. Through this interface, the sub-peripherals are enabled, disabled, or have their calibration values updated.

The STATUS register gathers different status signals coming from the sub-peripherals of OSC32KCTRL. The status signals can be used to generate system interrupts, and in some cases wake up the system from standby mode, provided the corresponding interrupt is enabled.

24.6.2 32KHz External Crystal Oscillator (XOSC32K) Operation

The XOSC32K can operate in two different modes:

- External clock, with an external clock signal connected to XIN32
- Crystal oscillator, with an external 32.768kHz crystal connected between XIN32 and XOUT32

At reset, the XOSC32K is disabled, and the XIN32/XOUT32 pins can either be used as General Purpose I/O (GPIO) pins or by other peripherals in the system.

When XOSC32K is enabled, the operating mode determines the GPIO usage. When in crystal oscillator mode, the XIN32 and XOUT32 pins are controlled by the OSC32KCTRL, and GPIO functions are overridden on both pins. When in external clock mode, the only XIN32 pin will be overridden and controlled by the OSC32KCTRL, while the XOUT32 pin can still be used as a GPIO pin.

The XOSC32K is enabled by writing a '1' to the Enable bit in the 32KHz External Crystal Oscillator Control register (XOSC32K.ENABLE=1). The XOSC32K is disabled by writing a '0' to the Enable bit in the 32KHz External Crystal Oscillator Control register (XOSC32K.ENABLE=0).

To enable the XOSC32K as a crystal oscillator, the XTALEN bit in the 32KHz External Crystal Oscillator Control register must be set (XOSC32K.XTALEN=1). If XOSC32K.XTALEN is '0', the external clock input will be enabled.

The XOSC32K 32.768kHz output is enabled by setting the 32KHz Output Enable bit in the 32KHz External Crystal Oscillator Control register (XOSC32K.EN32K=1). The XOSC32K also has a 1.024kHz clock output, which can only be used by the RTC. This clock output is enabled by setting the 1KHz Output Enable bit in the 32KHz External Crystal Oscillator Control register (XOSC32K.EN1K=1).

It is also possible to lock the XOSC32K configuration by setting the Write Lock bit in the 32KHz External Crystal Oscillator Control register (XOSC32K.WRTLOCK=1). If set, the XOSC32K configuration is locked until a Power-On Reset (POR) is detected.

The XOSC32K will behave differently in different sleep modes based on the settings of XOSC32K.RUNSTDBY, XOSC32K.ONDEMAND, and XOSC32K.ENABLE. If XOSC32KCTRL.ENABLE=0, the XOSC32K will be always stopped. For XOS32KCTRL.ENABLE=1, this table is valid:

- Up to 8 channels
  - Enable 8 independent transfers
  - Automatic descriptor fetch for each channel
  - Suspend/resume operation support for each channel
- Flexible arbitration scheme
  - 4 configurable priority levels for each channel
  - Fixed or round-robin priority scheme within each priority level
- From 1 to 256KB data transfer in a single block transfer
- Multiple addressing modes
  - Static
  - Configurable increment scheme
- Optional interrupt generation
  - On block transfer complete
  - On error detection
  - On channel suspend
- 4 event inputs
  - One event input for each of the 4 least significant DMA channels
  - Can be selected to trigger normal transfers, periodic transfers or conditional transfers
  - Can be selected to suspend or resume channel operation
- 4 event outputs
  - One output event for each of the 4 least significant DMA channels
  - Selectable generation on AHB, block, or transaction transfer complete
- Error management supported by write-back function
  - Dedicated Write-Back memory section for each channel to store ongoing descriptor transfer
- CRC polynomial software selectable to
  - CRC-16 (CRC-CCITT)
  - CRC-32 (IEEE® 802.3)

28.8.18 Channel Control A

Name: CHCTRLA
Offset: 0x40
Reset: 0x00
Property: PAC Write-Protection, Enable-Protected

This register affects the DMA channel that is selected in the Channel ID register (CHID.ID).

Bit	7	6	5	4	3	2	1	0
		RUNSTDBY					ENABLE	SWRST
Access	R	R/W	R	R	R	R	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 6 – RUNSTDBY Channel run in standby
This bit is used to keep the DMAC channel running in standby mode.

This bit is not enable-protected.

Value	Description
0	The DMAC channel is halted in standby.
1	The DMAC channel continues to run in standby.

Bit 1 – ENABLE Channel Enable
Writing a '0' to this bit during an ongoing transfer, the bit will not be cleared until the internal data transfer buffer is empty and the DMA transfer is aborted. The internal data transfer buffer will be empty once the ongoing burst transfer is completed.

Writing a '1' to this bit will enable the DMA channel.

This bit is not enable-protected.

Value	Description
0	DMA channel is disabled.
1	DMA channel is enabled.

Bit 0 – SWRST Channel Software Reset
Writing a '0' to this bit has no effect.

Writing a '1' to this bit resets the channel registers to their initial state. The bit can be set when the channel is disabled (ENABLE=0). Writing a '1' to this bit will be ignored as long as ENABLE=1. This bit is automatically cleared when the reset is completed.

Value	Description
0	There is no reset operation ongoing.
1	The reset operation is ongoing.

Debug Access to the bus system can be restricted to allow only accesses to non-secure regions or reject all accesses. See the section on the *NVMCTRL Debugger Access Level* for details.

Note: Refer to the *Mix-Secure Peripherals* section in the *SAM L11 Security Features* chapter for more information.

30.5.8 Analog Connections

Not applicable.

30.6 Functional Description

30.6.1 Principle of Operation

The NVM Controller is a slave on the AHB and APB buses. It responds to commands, read requests and write requests, based on user configuration.

30.6.1.1 Initialization

After power up, the NVM Controller goes through a power-up sequence. During this time, access to the NVM Controller from the AHB bus is halted. Upon power-up completion, the NVM Controller is operational without any need for user configuration.

30.6.2 Memory Organization

Refer to the Physical Memory Map for memory sizes and addresses for each device.

The NVM is organized into rows, where each row contains four pages, as shown in the NVM Row Organization figure. The NVM has a row-erase granularity, while the write granularity is by page. In other words, a single row erase will erase all four pages in the row, while four write operations are used to write the complete row.

Figure 30-2. NVM Row Organization

Row n	Page (n*4) + 3	Page (n*4) + 2	Page (n*4) + 1	Page (n*4) + 0

The NVM block contains the AUX FLASH which contain calibration and system configuration, the FLASH area intended to store code and a separate array dedicated to data storage called Data FLASH that can be modified while the FLASH is read (no bus stall). All these areas are memory mapped. Refer to the NVM Organization figure below for details.

The calibration and auxiliary space contains factory calibration and system configuration information. These spaces can be read from the AHB bus in the same way as the FLASH. Note that Data FLASH requires more cycles to be read. The Data FLASH are can be executable, however this is not recommended as it can weaken an application security and also affect performances.

32.8.7 Data Output Value Set

Name: OUTSET
Offset: 0x18
Reset: 0x00000000
Property: PAC Write-Protection, Mix-Secure

Important: For **SAM L11 Non-Secure** accesses, read and write accesses (RW*) are allowed only if the security attribution for the corresponding I/O pin is set as Non-Secured in the NONSEC register.

This register allows the user to set one or more output I/O pin drive levels high, without doing a read-modify-write operation. Changes in this register will also be reflected in the Data Output Value (OUT), Data Output Value Toggle (OUTTGL) and Data Output Value Clear (OUTCLR) registers.

Tip: The I/O pins are assembled in pin groups (”PORT groups”) with up to 32 pins. Group 0 consists of the PA pins, group 1 is for the PB pins, etc. Each pin group has its own PORT registers, with a 0x80 address spacing. For example, the register address offset for the Data Direction (DIR) register for group 0 (PA00 to PA31) is 0x00, and the register address offset for the DIR register for group 1 (PB00 to PB31) is 0x80.

Bit	31	30	29	28	27	26	25	24
	OUTSET[31:24]							
Access	RW/RW*/RW	RW/RW*/RW	RW/RW*/RW	RW/RW*/RW	RW/RW*/RW	RW/RW*/RW	RW/RW*/RW	RW/RW*/RW
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	OUTSET[23:16]							
Access	RW/RW*/RW	RW/RW*/RW	RW/RW*/RW	RW/RW*/RW	RW/RW*/RW	RW/RW*/RW	RW/RW*/RW	RW/RW*/RW
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	OUTSET[15:8]							
Access	RW/RW*/RW	RW/RW*/RW	RW/RW*/RW	RW/RW*/RW	RW/RW*/RW	RW/RW*/RW	RW/RW*/RW	RW/RW*/RW
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	OUTSET[7:0]							
Access	RW/RW*/RW	RW/RW*/RW	RW/RW*/RW	RW/RW*/RW	RW/RW*/RW	RW/RW*/RW	RW/RW*/RW	RW/RW*/RW
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – OUTSET[31:0] PORT Data Output Value Set
Writing '0' to a bit has no effect.

Writing '1' to CTRLB.TXEN when the USART is enabled will set SYNCBUSY.CTRLB, which will remain set until the transmitter is enabled, and CTRLB.TXEN will read back as '1'.

This bit is not enable-protected.

Value	Description
0	The transmitter is disabled or being enabled.
1	The transmitter is enabled or will be enabled when the USART is enabled.

Bit 13 – PMODE Parity Mode
This bit selects the type of parity used when parity is enabled (CTRLA.FORM is '1'). The transmitter will automatically generate and send the parity of the transmitted data bits within each frame. The receiver will generate a parity value for the incoming data and parity bit, compare it to the parity mode and, if a mismatch is detected, STATUS.PERR will be set.

This bit is not synchronized.

Value	Description
0	Even parity.
1	Odd parity.

Bit 10 – ENC Encoding Format
This bit selects the data encoding format.

This bit is not synchronized.

Value	Description
0	Data is not encoded.
1	Data is IrDA encoded.

Bit 9 – SFDE Start of Frame Detection Enable
This bit controls whether the start-of-frame detector will wake up the device when a start bit is detected on the RxD line.

This bit is not synchronized.

SFDE	INTENSET.RXS	INTENSET.RXC	Description
0	X	X	Start-of-frame detection disabled.
1	0	0	Reserved
1	0	1	Start-of-frame detection enabled. RXC wakes up the device from all sleep modes.
1	1	0	Start-of-frame detection enabled. RXS wakes up the device from all sleep modes.
1	1	1	Start-of-frame detection enabled. Both RXC and RXS wake up the device from all sleep modes.

Bit 8 – COLDEN Collision Detection Enable
This bit enables collision detection.

This bit is not synchronized.

37.8.7 Synchronization Busy

Name: SYNCBUSY
Offset: 0x1C
Reset: 0x00000000
Property: -

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
							ENABLE	SWRST
Access							R	R
Reset							0	0

Bit 1 – ENABLE SERCOM Enable Synchronization Busy
Enabling and disabling the SERCOM (CTRLA.ENABLE) requires synchronization. When written, the SYNCBUSY.ENABLE bit will be set until synchronization is complete.

Value	Description
0	Enable synchronization is not busy.
1	Enable synchronization is busy.

Bit 0 – SWRST Software Reset Synchronization Busy
Resetting the SERCOM (CTRLA.SWRST) requires synchronization. When written, the SYNCBUSY.SWRST bit will be set until synchronization is complete.

Value	Description
0	SWRST synchronization is not busy.
1	SWRST synchronization is busy.

38.7.1.5 Interrupt Enable Clear

Name: INTENCLR
Offset: 0x08
Reset: 0x00
Property: PAC Write-Protection

This register allows the user to disable an interrupt without doing a read-modify-write operation. Changes in this register will also be reflected in the Interrupt Enable Set register (INTENSET).

Bit	7	6	5	4	3	2	1	0
				MCx			ERR	OVF
Access				R/W			R/W	R/W
Reset				0			0	0

Bit 4 – MCx Match or Capture Channel x Interrupt Enable
Writing a '0' to these bits has no effect.

Writing a '1' to MCx will clear the corresponding Match or Capture Channel x Interrupt Enable bit, which disables the Match or Capture Channel x interrupt.

Value	Description
0	The Match or Capture Channel x interrupt is disabled.
1	The Match or Capture Channel x interrupt is enabled.

Bit 1 – ERR Error Interrupt Disable
Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the Error Interrupt Enable bit, which disables the Error interrupt.

Value	Description
0	The Error interrupt is disabled.
1	The Error interrupt is enabled.

Bit 0 – OVF Overflow Interrupt Disable
Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the Overflow Interrupt Enable bit, which disables the Overflow interrupt request.

Value	Description
0	The Overflow interrupt is disabled.
1	The Overflow interrupt is enabled.

38.7.3.17 Channel x Compare Buffer Value, 32-bit Mode

Name: CCBUFx
Offset: 0x30 + x*0x04 [x=0..1]
Reset: 0x00000000
Property: Write-Synchronized

Bit	31	30	29	28	27	26	25	24
	CCBUF[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	CCBUF[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	CCBUF[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CCBUF[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – CCBUF[31:0] Channel x Compare Buffer Value
These bits hold the value of the Channel x Compare Buffer Value. When the buffer valid flag is '1' and double buffering is enabled (CTRLBCLR.LUPD=1), the data from buffer registers will be copied into the corresponding CCx register under UPDATE condition (CTRLBSET.CMD=0x3), including the software update command.

39.8.3 Interrupt Enable Clear

Name: INTENCLR
Offset: 0x08
Reset: 0x00
Property: PAC Write-Protection

This register allows the user to disable an interrupt without doing a read-modify-write operation. Changes in this register will also be reflected in the Interrupt Enable Set (INTENSET) register.

Bit	7	6	5	4	3	2	1	0
								DATARDY
Access								R/W
Reset								0

Bit 0 – DATARDY Data Ready Interrupt Enable
Writing a '1' to this bit will clear the Data Ready Interrupt Enable bit, which disables the corresponding interrupt request.

Value	Description
0	The DATARDY interrupt is disabled.
1	The DATARDY interrupt is enabled.

41.8.8 Sequence Status

Name: SEQSTATUS
Offset: 0x07
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
	SEQBUSY			SEQSTATE[4:0]				
Access	R			R	R	R	R	R
Reset	0			0	0	0	0	0

Bit 7 – SEQBUSY Sequence busy
This bit is set when the sequence start.

This bit is clear when the last conversion in a sequence is done.

Bits 4:0 – SEQSTATE[4:0] Sequence State
These bit fields are the pointer of sequence. This value identifies the last conversion done in the sequence.

Value	Name	Description
0x07	AIN7	ADC AIN7 pin
0x08	AIN8	ADC AIN8 pin
0x09	AIN9	ADC AIN9 pin
0x0A – 0x17	-	Reserved
0x18	TEMP	Temperature Sensor
0x19	BANDGAP	INTREF Voltage Reference
0x1A	SCALEDVDDCORE	1/4 Scaled VDDCORE Supply
0x1B	SCALEDVDDANA	1/4 Scaled VDDANA Supply
0x1C	DAC	DAC Output
0x1D	SCALEDVDDIO	1/4 Scaled VDDIO Supply
0x1E	OPAMP01	OPAMP0 or OPAMP1 output
0x1F	OPAMP2	OPAMP2 output

42.8.4 Interrupt Enable Clear

Name: INTENCLR
Offset: 0x04
Reset: 0x00
Property: PAC Write-Protection

This register allows the user to disable an interrupt without doing a read-modify-write operation. Changes in this register will also be reflected in the Interrupt Enable Set register (INTENSET).

Bit	7	6	5	4	3	2	1	0
				WIN0			COMPx	COMPx
Access				R/W			R/W	R/W
Reset				0			0	0

Bit 4 – WIN0 Window 0 Interrupt Enable
Reading this bit returns the state of the Window 0 interrupt enable.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit disables the Window 0 interrupt.

Value	Description
0	The Window 0 interrupt is disabled.
1	The Window 0 interrupt is enabled.

Bits 1,0 – COMPx Comparator x Interrupt Enable
Reading this bit returns the state of the Comparator x interrupt enable.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit disables the Comparator x interrupt.

Value	Description
0	The Comparator x interrupt is disabled.
1	The Comparator x interrupt is enabled.

Figure 47-2. SPI Timing Requirements in Master Mode

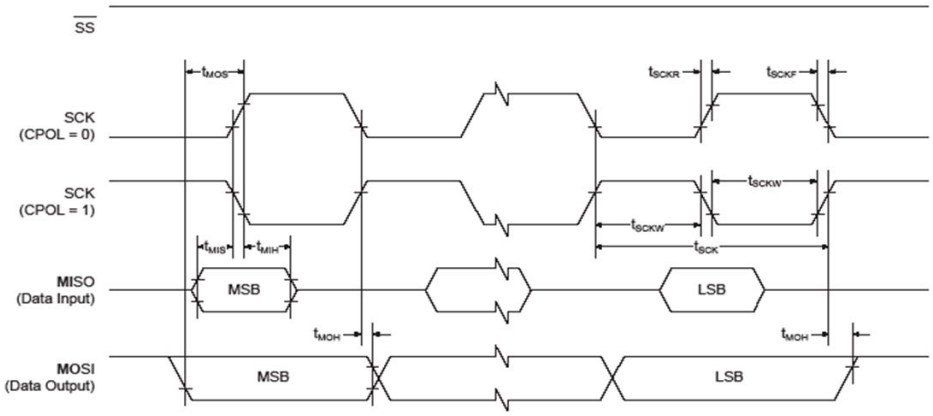
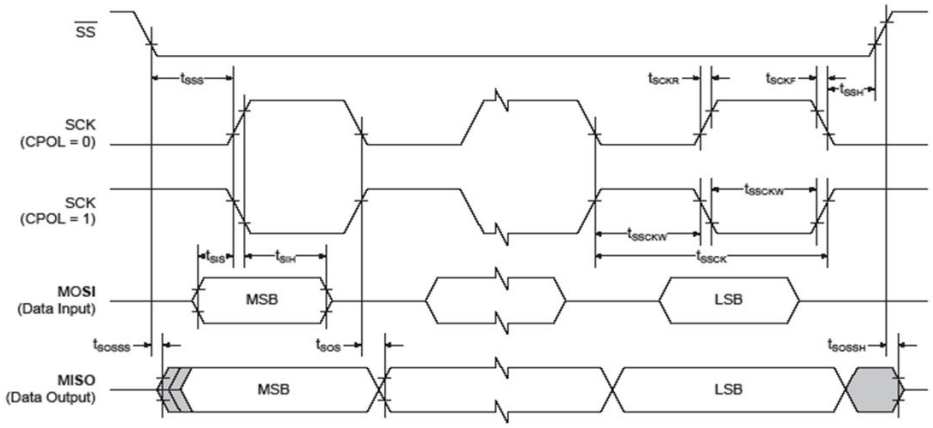


Figure 47-3. SPI Timing Requirements in Slave Mode



Maximum SPI Frequency

- Master mode:
  $f_{SCKmax} = 1/2*(t_{MIS} + t_{valid})$, where t_{valid} is the slave time response to output data after detecting an SCK edge. For a non-volatile memory with t_{valid} = 12 ns Max, $f_{SPCKMax}$ = 3.7 MHz @ VDDIO > 2.7V
- Slave mode:
  $f_{SCKmax} = 1/2*(t_{SOV} + t_{su})$, where t_{su} is the setup time from the master before sampling data. With a perfect master (t_{su}=0), $f_{SPCKMax}$ = 6 MHz @ VDDIO > 2.7V

47.6.2 SERCOM in SPI Mode in PL2

Table 47-27. SPI Timing Characteristics and Requirements (1)

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Units
tSCK	SCK period when tSOV=0 on the slave side	Master	Reception	2*(tMIS +tSLAVE_OUT) (3)	-	-	ns
		Master	Transmission	2*(tMOV +tSLAVE_IN) (4)	-	-	
tSCKW	SCK high/low width	Master		-	0,5*tSCK	-	
tSCKR	SCK rise time(2)	Master		-	0,25*tSCK	-	

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Units
tSCKF	SCK fall time(2)	Master		-	0,25*tSCK	-	
tMIS	MISO setup to SCK	Master, VDD>2,70V		43.8	-	-	
		Master, VDD>1,62V		54.1	-	-	
tMIH	MISO hold after SCK	Master, VDD>2,70V		0	-	-	ns
		Master, VDD>1,62V		0	-	-	
tMOV	MOSI output valid after SCK	Master, VDD>2,70V		-	-	17.5	
		Master, VDD>1,62V		-	-	21.2	
tMOH	MOSI hold after SCK	Master, VDD>2,70V		6.32	-	-	
		Master, VDD>1,62V		6.32	-	-	
tSSCK	Slave SCK Period when tMIS=0 on the master side	Slave	Reception	2*(tSIS +tMASTER_OUT) (5)	-	-	
		Slave	Transmission	2*(tSOV +tMASTER_IN) (6)	-	-	
tSSCKW	SCK high/low width	Slave		-	0,5*tSCK	-	
tSSCKR	SCK rise time(2)	Slave		-	0,25*tSCK	-	
tSSCKF	SCK fall time(2)	Slave		-	0,25*tSCK	-	
tSIS	MOSI setup to SCK	Slave, VDD>2,70V		10.7	-	-	ns
		Slave, VDD>1,62V		11.4	-	-	
tSIH	MOSI hold after SCK	Slave, VDD>2,70V		6.4	-	-	
		Slave, VDD>1,62V		7.1	-	-	
tSSS	SS setup to SCK	Slave	PRELOADEN=1	tSOSS+tEXT_MIS +2*tAPBC (8) (9)	-	-	
			PRELOADEN=0	tSOSS+tEXT_MIS (8)	-	-	
tSSH	SS hold after SCK	Slave		0.5*tSSCK	-	-	
tSOV	MISO output valid after SCK	Slave, VDD>2,70V		-	-	36.1	
		Slave, VDD>1,62V		-	-	46.4	
tSOH	MISO hold after SCK	Slave, VDD>2,70V		13.4	-	-	