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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M23
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	25
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.63V
Data Converters	A/D 10x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-UFQFN Exposed Pad
Supplier Device Package	32-UQFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsaml10e14a-au

        - Standby with Full SRAM Retention (0.5 µA) with 5.3 µs wake-up time
        - Off mode (< 100 nA)
    - Static and dynamic power gating architecture
    - Sleepwalking peripherals
    - Two performance levels
    - Embedded Buck/LDO regulator with on-the-fly selection
- **Security**
    - Up to four tamper pins for static and dynamic intrusion detections
    - Data Flash
        - Optimized for secrets storage
        - Data Scrambling with user-defined key (optional)
        - Rapid Tamper erase on scrambling key and on one user-defined row
        - Silent access for side channel attack resistance
    - TrustRAM
        - Address and Data scrambling with user-defined key
        - Chip-level tamper detection on physical RAM to resist microprobing attacks
        - Rapid Tamper Erase on scrambling key and RAM data
        - Silent access for side channel attack resistance
        - Data remanence prevention
    - Peripherals
        - One True Random Generator (TRNG)
        - AES-128, SHA-256, and GCM cryptography accelerators (optional)
        - Secure pin multiplexing to isolate on dedicated I/O pins a secured communication with external devices from the non-secure application (optional)
    - TrustZone for flexible hardware isolation of memories and peripherals (optional)
        - Up to six regions for the Flash
        - Up to two regions for the Data Flash
        - Up to two regions for the SRAM
        - Individual security attribution for each peripheral, I/O, external interrupt line, and Event System Channel
    - Secure Boot with SHA-based authentication (optional)
    - Up to three debug access levels
    - Up to three Chip Erase commands to erase part of or the entire embedded memories
    - Unique 128-bit serial number
- **Advanced Analog and Touch**
    - One 12-bit 1 Msps Analog-to-Digital Converter (ADC) with up to 10 channels
    - Two Analog Comparators (AC) with window compare function
    - One 10-bit 350 kSPS Digital-to-Analog Converter (DAC) with external and internal outputs
    - Three Operational Amplifiers (OPAMP)
    - One enhanced Peripheral Touch Controller (PTC):
        - Up to 20 self-capacitance channels
        - Up to 100 (10 x 10) mutual-capacitance channels
        - Low-power, high-sensitivity, environmentally robust capacitive touch buttons, sliders, and wheels

Offset	Bit Pos.	Name					
0x03	31:24	WDT_PER		WDT_ALWAYSON	WDT_ENABLE	WDT_RUNSTDBY	BOD12 Calibration Parameters
0x04	39:32	WDT_EWOFFSET		WDT_WINDOW			
0x05	47:40	Reserved	DXN	RXN	Reserved	BOD33_HYST	WDT_WEN
0x06	55:48	Reserved					
0x07	63:56	Reserved					
0x08	71:64	AS					
0x09	79:72	Reserved	ANSC				
0x0A	87:80	Reserved	DS				
0x0B	95:88	Reserved	RS				
0x0C	103:96	Reserved	URWEN				
0x0D-0xF	127:104	Reserved					
0x10-0x13	159:128	NONSECA					
0x14-0x17	191:160	NONSECB					
0x18-0x1B	223:192	NONSECC					
0x1C-0x1F	255:224	USERCRC					

10.2.2 NVM Software Calibration Area

The NVM Software Calibration Area contains calibration data that can be used by some peripherals, such as the ADC.

Note: Calibration data are determined and written during production test and cannot be written.

The NVM Software Calibration Area can be read at address 0x00806020.

Table 10-12. NVM Software Calibration Bitfields Definition

Bit Position	Name	Description
2:0	ADC LINEARITY	ADC Linearity Calibration. Should be written to CALIB register.
5:3	ADC BIASCAL	ADC Bias Calibration. Should be written to CALIB register.
8:6	DFLLULP Division Factor in PL0	DFLLULP Division Factor in PL0. Should be written to DFLLULPCTRL register.
11:9	DFLLULP Division Factor in PL2	DFLLULP Division Factor in PL2. Should be written to DFLLULPCTRL register.
127:12	Reserved	Reserved

Table 10-13. NVM Software Calibration Row Mapping

Offset	Bit Pos.	Name					
0x00	7:0	DFLLULP Division Factor in PL0	ADC BIASCAL	ADC LINEARITY			
0x01	15:8	Reserved	DFLLULP Division Factor in PL2	DFLLULP Division Factor in PL0			
0x02-0xF	127:16	Reserved					

10.2.3 NVM Temperature Log Row

The NVM Temperature Log Row contains calibration data that are determined and written during production test and cannot be written.

These calibration values are required for calculating the temperature from measuring the temperature sensor in the Supply Controller (SUPC) by the ADC.

24.8.9 32KHz Ultra Low-Power Internal Oscillator (OSCULP32K) Control

Name: OSCULP32K
Offset: 0x1C
Reset: 0x0000XX06
Property: PAC Write-Protection

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	WRTLOCK			CALIB[4:0]				
Access	R/W			R/W	R/W	R/W	R/W	R/W
Reset	0			x	x	x	x	x

Bit	7	6	5	4	3	2	1	0
			ULP32KSW					
Access			R/W					
Reset			0					

Bit 15 – WRTLOCK Write Lock
This bit locks the OSCULP32K register for future writes to fix the OSCULP32K configuration.

Value	Description
0	The OSCULP32K configuration is not locked.
1	The OSCULP32K configuration is locked.

Bits 12:8 – CALIB[4:0] Oscillator Calibration
These bits control the oscillator calibration.

These bits are loaded from Flash Calibration at startup.

Bit 5 – ULP32KSW OSCULP32K Clock Switch Enable

Value	Description
0	OSCULP32K is not switched and provided by the ULP32K oscillator.
1	OSCULP32K is switched to be provided by the XOSC32K oscillator.

Bit 8 – VREGRDY Voltage Regulator Ready Interrupt Enable
Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the Voltage Regulator Ready Interrupt Enable bit, which disables the Voltage Regulator Ready interrupt.

Value	Description
0	The Voltage Regulator Ready interrupt is disabled.
1	The Voltage Regulator Ready interrupt is enabled and an interrupt request will be generated when the Voltage Regulator Ready Interrupt Flag is set.

Bit 2 – B33SRDY BOD33 Synchronization Ready Interrupt Enable
Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the BOD33 Synchronization Ready Interrupt Enable bit, which disables the BOD33 Synchronization Ready interrupt.

Value	Description
0	The BOD33 Synchronization Ready interrupt is disabled.
1	The BOD33 Synchronization Ready interrupt is enabled, and an interrupt request will be generated when the BOD33 Synchronization Ready Interrupt flag is set.

Bit 1 – BOD33DET BOD33 Detection Interrupt Enable
Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the BOD33 Detection Interrupt Enable bit, which disables the BOD33 Detection interrupt.

Value	Description
0	The BOD33 Detection interrupt is disabled.
1	The BOD33 Detection interrupt is enabled, and an interrupt request will be generated when the BOD33 Detection Interrupt flag is set.

Bit 0 – BOD33RDY BOD33 Ready Interrupt Enable
Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the BOD33 Ready Interrupt Enable bit, which disables the BOD33 Ready interrupt.

Value	Description
0	The BOD33 Ready interrupt is disabled.
1	The BOD33 Ready interrupt is enabled, and an interrupt request will be generated when the BOD33 Ready Interrupt flag is set.

26.8.6 Interrupt Flag Status and Clear

Name: INTFLAG
Offset: 0x06
Reset: 0x00
Property: N/A

Bit	7	6	5	4	3	2	1	0
								EW
Access								R/W
Reset								0

Bit 0 – EW Early Warning
This flag is cleared by writing a '1' to it.

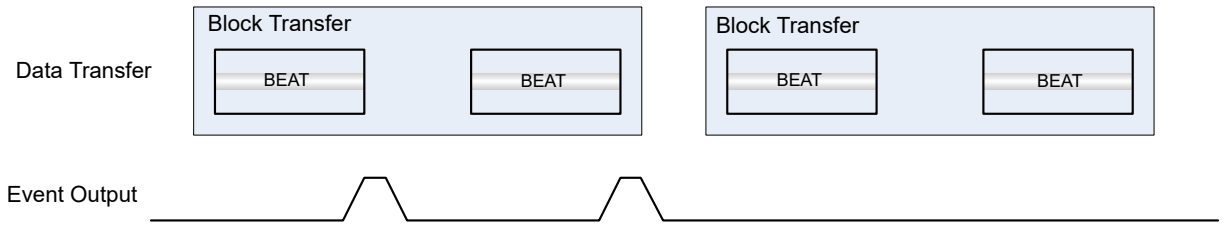
This flag is set when an Early Warning interrupt occurs, as defined by the EWOFFSET bit group in EWCTRL.

Writing a '0' to this bit has no effect.

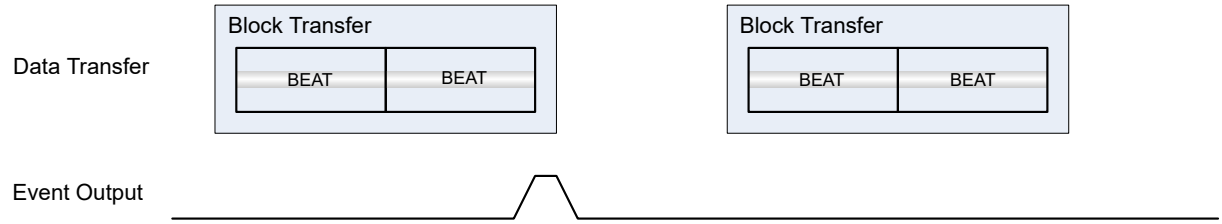
Writing a '1' to this bit clears the Early Warning interrupt flag.

Figure 28-15. Event Output Generation

Beat Event Output



Block Event Output



28.6.3.6 Aborting Transfers

Transfers on any channel can be aborted gracefully by software by disabling the corresponding DMA channel. It is also possible to abort all ongoing or pending transfers by disabling the DMAC.

When a DMA channel disable request or DMAC disable request is detected:

- Ongoing transfers of the active channel will be disabled when the ongoing beat transfer is completed and the write-back memory section is updated. This prevents transfer corruption before the channel is disabled.
- All other enabled channels will be disabled in the next clock cycle.

The corresponding Channel Enable bit in the Channel Control A register is cleared (CHCTRLA.ENABLE=0) when the channel is disabled.

The corresponding DMAC Enable bit in the Control register is cleared (CTRL.DMAENABLE=0) when the entire DMAC module is disabled.

28.6.3.7 CRC Operation

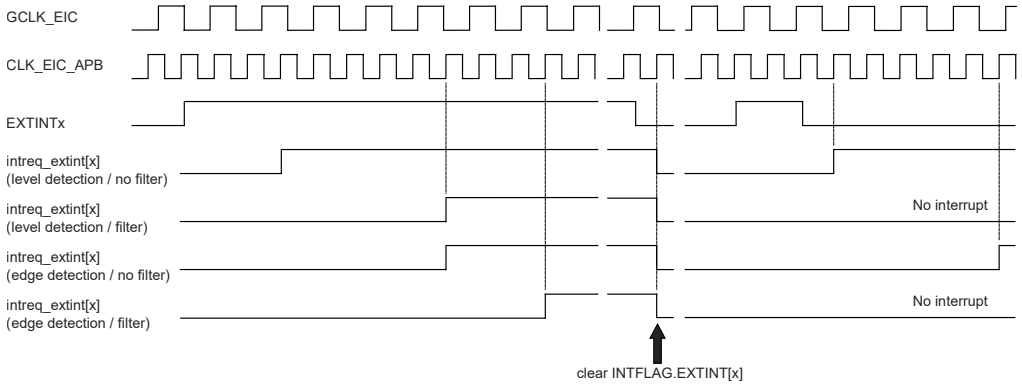
A cyclic redundancy check (CRC) is an error detection technique used to find errors in data. It is commonly used to determine whether the data during a transmission, or data present in data and program memories has been corrupted or not. A CRC takes a data stream or a block of data as input and generates a 16- or 32-bit output that can be appended to the data and used as a checksum.

When the data is received, the device or application repeats the calculation: If the new CRC result does not match the one calculated earlier, the block contains a data error. The application will then detect this and may take a corrective action, such as requesting the data to be sent again or simply not using the incorrect data.

The CRC engine in DMAC supports two commonly used CRC polynomials: CRC-16 (CRC-CCITT) and CRC-32 (IEEE 802.3). Typically, applying CRC-n (CRC-16 or CRC-32) to a data block of arbitrary length will detect any single alteration that is ≤n bits in length, and will detect the fraction 1-2-n of all longer error bursts.

If filtering or synchronous edge detection or debouncing is enabled, the EIC automatically requests GCLK_EIC or CLK_ULP32K to operate. The selection between these two clocks is done by writing the Clock Selection bits in the Control A register (CTRLA.CKSEL). GCLK_EIC must be enabled in the GCLK module. In these modes the external pin is sampled at the EIC clock rate, thus pulses with duration lower than two EIC clock periods may not be properly detected.

Figure 29-2. Interrupt Detection Latency by modes (Rising Edge)



The detection latency depends on the detection mode.

Table 29-2. Detection Latency

Detection mode	Latency (worst case)
Level without filter	Five CLK_EIC_APB periods
Level with filter	Four GCLK_EIC/CLK_ULP32K periods + five CLK_EIC_APB periods
Edge without filter	Four GCLK_EIC/CLK_ULP32K periods + five CLK_EIC_APB periods
Edge with filter	Six GCLK_EIC/CLK_ULP32K periods + five CLK_EIC_APB periods

Related Links

18. GCLK - Generic Clock Controller

29.6.4 Additional Features

29.6.4.1 Non-Maskable Interrupt (NMI)

The non-maskable interrupt pin can also generate an interrupt on edge or level detection, but it is configured with the dedicated NMI Control register (NMICTRL). To select the sense for NMI, write to the NMISENSE bit group in the NMI Control register (NMICTRL.NMISENSE). NMI filtering is enabled by writing a '1' to the NMI Filter Enable bit (NMICTRL.NMIFILTEN).

If edge detection or filtering is required, enable GCLK_EIC or CLK_ULP32K.

NMI detection is enabled only by the NMICTRL.NMISENSE value, and the EIC is not required to be enabled.

When an NMI is detected, the non-maskable interrupt flag in the NMI Flag Status and Clear register is set (NMIFLAG.NMI). NMI interrupt generation is always enabled, and NMIFLAG.NMI generates an interrupt request when set.

29.6.4.2 Asynchronous Edge Detection Mode (No Debouncing)

The EXTINT edge detection can be operated synchronously or asynchronously, selected by the Asynchronous Control Mode bit for external pin x in the External Interrupt Asynchronous Mode register

Value	Description
0	There is no ongoing reset operation.
1	The reset operation is ongoing.

29.8.3 Non-Maskable Interrupt Flag Status and Clear

Name: NMIFLAG
Offset: 0x02
Reset: 0x0000
Property: Mix-Secure

Important: For **SAM L11 Non-Secure** accesses, read and write accesses (RW*) are allowed only if the NMI interrupt is set as Non-Secure in the NONSEC register (NONSEC.NMI bit).

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
								NMI
Access								RW/RW*/RW
Reset								0

Bit 0 – NMI Non-Maskable Interrupt
This flag is cleared by writing a '1' to it.

This flag is set when the NMI pin matches the NMI sense configuration, and will generate an interrupt request.

Writing a '0' to this bit has no effect.

32.8.18 Security Attribution

Name: NONSEC
Offset: 0x6C
Reset: 0x00000000
Property: PAC Write-Protection, Write-Secure

Important: This register is only available for **SAM L11** and has no effect for **SAM L10**.

This register allows the user to configure one or more I/O pins as secured or non-secured.

Tip: The I/O pins are assembled in pin groups (”PORT groups”) with up to 32 pins. Group 0 consists of the PA pins, group 1 is for the PB pins, etc. Each pin group has its own PORT registers, with a 0x80 address spacing. For example, the register address offset for the Data Direction (DIR) register for group 0 (PA00 to PA31) is 0x00, and the register address offset for the DIR register for group 1 (PB00 to PB31) is 0x80.

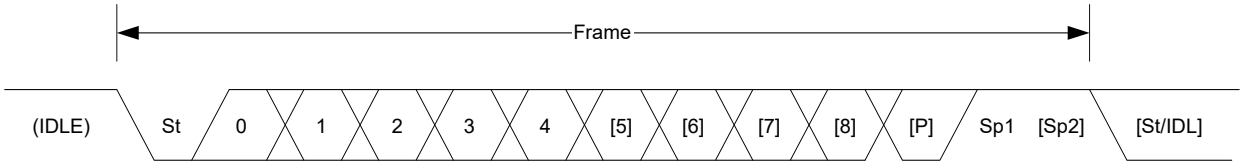
Bit	31	30	29	28	27	26	25	24
	NONSEC[31:24]							
Access	RW/R/RW	RW/R/RW	RW/R/RW	RW/R/RW	RW/R/RW	RW/R/RW	RW/R/RW	RW/R/RW
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	NONSEC[23:16]							
Access	RW/R/RW	RW/R/RW	RW/R/RW	RW/R/RW	RW/R/RW	RW/R/RW	RW/R/RW	RW/R/RW
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	NONSEC[15:8]							
Access	RW/R/RW	RW/R/RW	RW/R/RW	RW/R/RW	RW/R/RW	RW/R/RW	RW/R/RW	RW/R/RW
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	NONSEC[7:0]							
Access	RW/R/RW	RW/R/RW	RW/R/RW	RW/R/RW	RW/R/RW	RW/R/RW	RW/R/RW	RW/R/RW
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – NONSEC[31:0] Port Security Attribution
These bits set the security attribution for the individual I/O pins in the PORT group.

Value	Description
0	The corresponding I/O pin in the PORT group is configured as secured. When module is PAC secured, the configuration for this pin is only available through the secure alias. Attempt

follow immediately, or the communication line can return to the idle (high) state. The figure below illustrates the possible frame formats. Brackets denote optional bits.

Figure 35-2. Frame Formats



St Start bit. Signal is always low.

n, [n] Data bits. 0 to [5..9]

[P] Parity bit. Either odd or even.

Sp, [Sp] Stop bit. Signal is always high.

IDLE No frame is transferred on the communication line. Signal is always high in this state.

35.6.2 Basic Operation

35.6.2.1 Initialization

The following registers are enable-protected, meaning they can only be written when the USART is disabled (CTRL.ENABLE=0):

- Control A register (CTRLA), except the Enable (ENABLE) and Software Reset (SWRST) bits.
- Control B register (CTRLB), except the Receiver Enable (RXEN) and Transmitter Enable (TXEN) bits.
- Baud register (BAUD)

When the USART is enabled or is being enabled (CTRLA.ENABLE=1), any writing attempt to these registers will be discarded. If the peripheral is being disabled, writing to these registers will be executed after disabling is completed. Enable-protection is denoted by the "Enable-Protection" property in the register description.

Before the USART is enabled, it must be configured by these steps:

1. Select either external (0x0) or internal clock (0x1) by writing the Operating Mode value in the CTRLA register (CTRLA.MODE).
2. Select either asynchronous (0) or or synchronous (1) communication mode by writing the Communication Mode bit in the CTRLA register (CTRLA.CMODE).
3. Select pin for receive data by writing the Receive Data Pinout value in the CTRLA register (CTRLA.RXPO).
4. Select pads for the transmitter and external clock by writing the Transmit Data Pinout bit in the CTRLA register (CTRLA.TXPO).
5. Configure the Character Size field in the CTRLB register (CTRLB.CHSIZE) for character size.
6. Set the Data Order bit in the CTRLA register (CTRLA.DORD) to determine MSB- or LSB-first data transmission.
7. To use parity mode:
   7.1. Enable parity mode by writing 0x1 to the Frame Format field in the CTRLA register (CTRLA.FORM).

36.8 Register Description

Registers can be 8, 16, or 32 bits wide. Atomic 8-, 16-, and 32-bit accesses are supported. In addition, the 8-bit quarters and 16-bit halves of a 32-bit register, and the 8-bit halves of a 16-bit register can be accessed directly.

Some registers require synchronization when read and/or written. Synchronization is denoted by the "Read-Synchronized" and/or "Write-Synchronized" property in each individual register description.

Refer to 36.6.6 Synchronization

Some registers are enable-protected, meaning they can only be written when the module is disabled. Enable-protection is denoted by the "Enable-Protected" property in each individual register description.

Optional write-protection by the Peripheral Access Controller (PAC) is denoted by the "PAC Write-Protection" property in each individual register description.

Refer to 36.5.8 Register Access Protection.

On **SAM L11** devices, this peripheral has different access permissions depending on PAC Security Attribution (Secure or Non-Secure):

- If the peripheral is configured as Non-Secure in the PAC:
  - Secure access and Non-Secure access are granted
- If the peripheral is configured as Secure in the PAC:
  - Secure access is granted
  - Non-Secure access is discarded (Write is ignored, read 0x0) and a PAC error is triggered

Refer to *Peripherals Security Attribution* for more information.

36.8.1 Control A

Name: CTRLA
Offset: 0x00
Reset: 0x00000000
Property: PAC Write-Protection, Enable-Protected

Bit	31	30	29	28	27	26	25	24
		DORD	CPOL	CPHA	FORM[3:0]			
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
			DIPO[1:0]				DOPO[1:0]	
Access			R/W	R/W			R/W	R/W
Reset			0	0			0	0

Bit	15	14	13	12	11	10	9	8
								IBON
Access								R/W
Reset								0

Bit	7	6	5	4	3	2	1	0
	RUNSTDBY			MODE[2:0]			ENABLE	SWRST
Access	R/W			R/W	R/W	R/W	R/W	R/W
Reset	0			0	0	0	0	0

Bit 30 – DORD Data Order
This bit selects the data order when a character is shifted out from the shift register.

This bit is not synchronized.

Value	Description
0	MSB is transferred first.
1	LSB is transferred first.

Bit 29 – CPOL Clock Polarity
In combination with the Clock Phase bit (CPHA), this bit determines the SPI transfer mode.

This bit is not synchronized.

Value	Description
0	SCK is low when idle. The leading edge of a clock cycle is a rising edge, while the trailing edge is a falling edge.
1	SCK is high when idle. The leading edge of a clock cycle is a falling edge, while the trailing edge is a rising edge.

Bit 28 – CPHA Clock Phase
In combination with the Clock Polarity bit (CPOL), this bit determines the SPI transfer mode.

37.7 Register Summary - I2C Slave

Offset	Name	Bit Pos.								
0x00	CTRLA	7:0	RUNSTDBY			MODE[2:0]			ENABLE	SWRST
		15:8								
		23:16	SEXTTOEN		SDAHOLD[1:0]					PINOUT
		31:24		LOWTOUT			SCLSM		SPEED[1:0]	
0x04	CTRLB	7:0								
		15:8	AMODE[1:0]					AACKEN	GCMD	SMEN
		23:16						ACKACT	CMD[1:0]	
		31:24								
0x08 ... 0x13	Reserved									
0x14	INTENCLR	7:0	ERROR					DRDY	AMATCH	PREC
0x15	Reserved									
0x16	INTENSET	7:0	ERROR					DRDY	AMATCH	PREC
0x17	Reserved									
0x18	INTFLAG	7:0	ERROR					DRDY	AMATCH	PREC
0x19	Reserved									
0x1A	STATUS	7:0	CLKHOLD	LOWTOUT		SR	DIR	RXNACK	COLL	BUSERR
		15:8					LENERR	HS	SEXTTOUT	
0x1C	SYNCBUSY	7:0							ENABLE	SWRST
		15:8								
		23:16								
		31:24								
0x20 ... 0x23	Reserved									
0x24	ADDR	7:0	ADDR[6:0]							GENCEN
		15:8	TENBITEN					ADDR[9:7]		
		23:16	ADDRMASK[6:0]							
		31:24						ADDRMASK[9:7]		
0x28	DATA	7:0	DATA[7:0]							
		15:8								

37.8 Register Description - I2C Slave

Registers can be 8, 16, or 32 bits wide. Atomic 8-, 16- and 32-bit accesses are supported. In addition, the 8-bit quarters and 16-bit halves of a 32-bit register, and the 8-bit halves of a 16-bit register can be accessed directly.

Some registers are optionally write-protected by the Peripheral Access Controller (PAC). Optional PAC write-protection is denoted by the "PAC Write-Protection" property in each individual register description. For details, refer to 37.5.8 Register Access Protection.

Note that this status will not trigger any interrupt, and should be checked by software to verify that the data were sent correctly. This bit is cleared automatically if responding to an address match with an ACK or a NACK (writing 0x3 to CTRLB.CMD), or INTFLAG.AMATCH is cleared.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the status.

Value	Description
0	No collision detected on last data byte sent.
1	Collision detected on last data byte sent.

Bit 0 – BUSERR Bus Error
The Bus Error bit (STATUS.BUSERR) indicates that an illegal bus condition has occurred on the bus, regardless of bus ownership. An illegal bus condition is detected if a protocol violating start, repeated start or stop is detected on the I2C bus lines. A start condition directly followed by a stop condition is one example of a protocol violation. If a time-out occurs during a frame, this is also considered a protocol violation, and will set STATUS.BUSERR.

This bit is cleared automatically if responding to an address match with an ACK or a NACK (writing 0x3 to CTRLB.CMD) or INTFLAG.AMATCH is cleared.

Writing a '1' to this bit will clear the status.

Writing a '0' to this bit has no effect.

Value	Description
0	No bus error detected.
1	Bus error detected.

41.8.11 Average Control

Name: AVGCTRL
Offset: 0x0C
Reset: 0x00
Property: PAC Write-Protection, Write-Synchronized

Bit	7	6	5	4	3	2	1	0
		ADJRES[2:0]			SAMPLENUM[3:0]			
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bits 6:4 – ADJRES[2:0] Adjusting Result / Division Coefficient
These bits define the division coefficient in 2n steps.

Bits 3:0 – SAMPLENUM[3:0] Number of Samples to be Collected
These bits define how many samples are added together. The result will be available in the Result register (RESULT). Note: if the result width increases, CTRLC.RESSEL must be changed.

Value	Description
0x0	1 sample
0x1	2 samples
0x2	4 samples
0x3	8 samples
0x4	16 samples
0x5	32 samples
0x6	64 samples
0x7	128 samples
0x8	256 samples
0x9	512 samples
0xA	1024 samples
0xB - 0xF	Reserved

42.5.2 Power Management

The AC will continue to operate in any sleep mode where the selected source clock is running. The AC's interrupts can be used to wake up the device from sleep modes. Events connected to the event system can trigger other operations in the system without exiting sleep modes.

Related Links

22. PM – Power Manager

42.5.3 Clocks

The AC bus clock (CLK_AC_APB) can be enabled and disabled in the Main Clock module, MCLK (see *MCLK - Main Clock*, and the default state of CLK_AC_APB can be found in *Peripheral Clock Masking*.

A generic clock (GCLK_AC) is required to clock the AC. This clock must be configured and enabled in the generic clock controller before using the AC. Refer to the Generic Clock Controller chapter for details.

This generic clock is asynchronous to the bus clock (CLK_AC_APB). Due to this asynchronicity, writes to certain registers will require synchronization between the clock domains. Refer to Synchronization for further details.

Related Links

22. PM – Power Manager

42.5.4 DMA

Not applicable.

42.5.5 Interrupts

The interrupt request lines are connected to the interrupt controller. Using the AC interrupts requires the interrupt controller to be configured first. Refer to *Nested Vector Interrupt Controller* for details.

42.5.6 Events

The events are connected to the Event System. Refer to *EVSYS – Event System* for details on how to configure the Event System.

Related Links

33. EVSYS – Event System

42.5.7 Debug Operation

When the CPU is halted in debug mode, the AC will halt normal operation after any on-going comparison is completed. The AC can be forced to continue normal operation during debugging. Refer to DBGCTRL for details. If the AC is configured in a way that requires it to be periodically serviced by the CPU through interrupts or similar, improper operation or data loss may result during debugging.

42.5.8 Register Access Protection

All registers with write-access can be write-protected optionally by the Peripheral Access Controller (PAC), except for the following registers:

- Control B register (CTRLB)
- Interrupt Flag register (INTFLAG)

Optional write-protection by the Peripheral Access Controller (PAC) is denoted by the "PAC Write-Protection" property in each individual register description.

PAC write-protection does not apply to accesses through an external debugger.

44.8.1 Control A

Name: CTRLA
Offset: 0x00
Reset: 0x00
Property: PAC Write-Protection

Bit	7	6	5	4	3	2	1	0
	LPMUX						ENABLE	SWRST
Access	R/W						R/W	R/W
Reset	0						0	0

Bit 7 – LPMUX Low-Power Mux

Value	Description
0	The analog input muxes have low resistance, but consume more power at lower voltages (e.g., are driven by the voltage doubler).
1	The analog input muxes have high resistance, but consume less power at lower voltages (e.g., the voltage doubler is disabled).

Bit 1 – ENABLE Enable

Value	Description
0	The peripheral is disabled.
1	The peripheral is enabled. Each OPAMP must also be enabled individually by the Enable bit in the corresponding OPAMP Control register (OPAMPCTRLx.ENABLE).

Bit 0 – SWRST Software Reset
Writing a '0' to this bit has no effect.

Writing a '1' to this bit resets all registers in the MODULE to their initial state, and the OPAMP will be disabled.

Writing a '1' to CTRLA.SWRST will always take precedence, meaning that all other writes in the same write-operation will be discarded.

Value	Description
0	There is no reset operation ongoing.
1	The reset operation is ongoing.

Note:

1. These values are based on simulation. They are not covered by production test limits or characterization.

Table 47-8. Differential Mode (1)

Symbol	Parameters	Conditions		Measurements			Unit
				Min	Typ	Max	
ENOB	Effective Number of bits	Fadc = 1Msps	Vref=2.0V Vddana=3.0V	9.1	10.2	10.8	bits
			Vref=1.0V Vddana=1.6V to 3.6V	9.0	10.1	10.6	
			Vref=Vddana=1.6V to 3.6V	8.9	9.9	11.0	
			Bandgap Reference, Vddana=1.6V to 3.6V	9.0	9.8	10.6	
TUE	Total Unadjusted Error	without offset and gain compensation	Vref=Vddana=1.6V to 3.6V	-	7	32	LSB
INL	Integral Non Linearity	without offset and gain compensation	Vref=Vddana=1.6V to 3.6V	-	+/-1.9	+/-4.8	
DNL	Differential Non Linearity	without offset and gain compensation	Vref=Vddana=1.6V to 3.6V	-	+0.94/-1	+1.85/-1	
Gain	Gain Error	without gain compensation	Vref=1V Vddana=1.6V to 3.6V	-	+/-0.38	+/-1.9	%
			Vref=3V Vddana=1.6V to 3.6V	-	+/-0.14	+/-0.9	
			Bandgap Reference	-	+/-0.64	+/-5.4	

50. Schematic Checklist

50.1 Introduction

This chapter describes a common checklist which should be used when starting and reviewing the schematics for a SAM L10/L11 design. This chapter illustrates the recommended power supply connections, how to connect external analog references, programmer, debugger, oscillator and crystal.

50.2 Power Supply

The SAM L10/L11 supports a single or dual power supply from 1.62V to 3.63V. The same voltage must be applied to both VDDIO and VDDANA.

The internal voltage regulator has four different modes:

- Linear mode: this mode does not require any external inductor. This is the default mode when CPU and peripherals are running
- Switching mode (Buck): the most efficient mode when the CPU and peripherals are running
- Low Power (LP) mode: This is the default mode used when the device is in Standby mode

Selecting between switching mode and linear mode can be done by software on the fly, but the power supply must be designed according to which mode is to be used.

50.2.1 Power Supply Connections

The following figures shows the recommended power supply connections for Switched/Linear mode and Linear mode only.