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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M23
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	25
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.63V
Data Converters	A/D 10x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	32-TQFP
Supplier Device Package	32-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsaml10e16a-af

10.1.2 Data Flash

SAM L10/L11 devices embed 2 KB of internal Data Flash with Write-While-Read (WWR) capability mapped at address 0x0040 0000.

The Data Flash can be programmed or erased while reading the Flash memory. It is not possible to read the Data Flash while writing or erasing the Flash.
Note: The Data Flash memory can be executable but requires more cycles to be read which may affect system performance.

The Data Flash cannot be cached.

The Data Flash is organized into rows, where each row contains four pages. The Data Flash has a row-erase and a page-write granularity.

Table 10-4. Data Flash Memory Parameters

Device	Memory Size [KB]	Number of Rows	Row size [Bytes]	Number of Pages	Page size [Bytes]
SAM L10/L11	2	8	256	32	64

The Data Flash is divided into one or two regions. Each region has a dedicated lock bit preventing from writing and erasing pages on it. Refer to the NVM Memory Organization figures in the *NVMCTRL* chapter to obtain the definitions of the different regions.

Note: The regions size is configured by the Boot ROM at device startup by reading the NVM Boot Configuration Row (BOCOR).

Table 10-5. Data Flash Lock Regions Parameters

Device	SAM L10	SAM L11
Number of Data FLASH Lock Regions	1	2
Regions Name	Data Flash	Data Flash Secure / Data Flash Non-Secure

10.1.3 SRAM

SAM L10/L11 devices embed 4 KB, 8 KB, or 16 KB of internal SRAM mapped at address 0x2000 0000.

Table 10-6. SRAM Memory Parameters

Device	Memory Size [KB]
SAM L11x16 / SAM L10x16 (1)	16
SAM L11x15 / SAM L10x15 (1)	8
SAM L11x14 (1)	8
SAM L10x14 (1)	4

Note:

1. x = E or D.

SRAM is composed of 4KB sub-blocks which can be retained or not in STANDBY Low-Power mode to optimize power consumption.

By default, all sub-blocks are retained, but it is possible to switch them off using the Power Manager (PM).

SRAM retention is guaranteed for Watchog, External and System Reset resets. However, the two first 2kB of SRAM are reset by the Boot ROM.

Important: The table(s) must be programmed by the programming tool in addition to the application binaries.

14.4.5.6.1 CRC Table format

Table 14-7. CRC Table Fields Description

Description	Header	Start Address (1)	Size in bytes (2)	Expected value (3)
Field	HDR	ADDR	SIZE	REFVAL
Offset	0x0	0x4	0x8	0xC
Value	0x43524349	0x00000000	0x100	0xAABBCCDD

Note 1: ADDR must be a multiple of 4 (Only ADDR[31:2] are used).

Note 2: SIZE must be a multiple of 4 (Only SIZE[31:2] are used).

Note 3: The expected value is the computed CRC32 value of the memory target.

14.4.5.6.2 Requirements

- Each table occupies 16 bytes in memory.
- The table must start at a 16byte aligned address. (i.e. 0xXXXXXXX0)
- The table must be placed in the same memory region as its target memory range. (i.e. a table placed in the Secure APPLICATION region can only target Secure APPLICATION memory addresses).
  Note: There are two exceptions to this rule:
  - For SAM L10: all non-volatile memories are considered as a single region (e.g. a table located in Data Flash can target main array)
  - For SAM L11: ANSC and BNSC regions are considered to belong to the same region as their “parent” region: AS for ANSC and BS for BNSC.

14.4.5.6.3 CRC Command Key

The CRC command (CMD_ CRC) requires an access key (CRCKEY) which is in the NVM BOCOR row at: [0x80C040:0x80C04F]:

BOCOR Offset	Bit Position	Name
0x40-0x4F	639:512	CRCKEY

Just like the ChipErase keys, the key can be set to all 0s to prevent any access to the command.

15.7.10 Peripheral Write Protection Status B

Name: STATUSB
Offset: 0x38
Reset: 0x000000
Property: Mix-Secure

Reading the STATUSB register returns the peripheral write protection status:

Value	Description
0	Peripheral is not write protected.
1	Peripheral is write protected.

Important: For **SAM L11 Non-Secure** accesses, read accesses (R*) are allowed only if the peripheral security attribution for the corresponding peripheral is set as Non-Secured in the NONSECx register.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
				Reserved	DMAC	NVMCTRL	DSU	IDAU
Access				R/R*/R	R/R*/R	R/R*/R	R/R*/R	R/R*/R
Reset				0	0	0	0	0

Bit 4 – Reserved Reserved

Bit 3 – DMAC Peripheral DMAC Write Protection Status

Bit 2 – NVMCTRL Peripheral NVMCTRL Write Protection Status

Bit 1 – DSU Peripheral DSU Write Protection Status

Bit 0 – IDAU Peripheral IDAU Write Protection Status

Once completed, the calculated CRC32 value can be read out of the Data register. The read value must be complemented to match standard CRC32 implementations or kept non-inverted if used as starting point for subsequent CRC32 calculations.

The actual test is started by writing a '1' in the 32-bit Cyclic Redundancy Check bit of the Control register (CTRL.CRC). A running CRC32 operation can be canceled by resetting the module (writing '1' to CTRL.SWRST).

Related Links

30. NVMCTRL – Nonvolatile Memory Controller

16.10.3.2 Interpreting the Results

The user should monitor the Status A register. When the operation is completed, STATUSA.DONE is set. Then the Bus Error bit of the Status A register (STATUSA.BERR) must be read to ensure that no bus error occurred.

16.10.4 Debug Communication Channels

The Debug Communication Channels (DCCO and DCC1) consist of a pair of registers with associated handshake logic, accessible by both CPU and debugger with no security restriction. The registers can be used to exchange data between the CPU and the debugger, during run time as well as in debug mode. This enables the user to build a custom debug protocol using only these registers.

The DCC0 and DCC1 registers are always accessible from the external address space. When the device starts with the cold-plugging procedure, a specific Boot ROM command is needed to exit the Boot ROM main routine.

Important: This command is allowed only when DAL=0x2, otherwise the device must be reset to leave the cold plugging state to let the CPU exit the Boot ROM routine and execute the user code.

Two Debug Communication Channel status bits in the Status B registers (STATUS.DCCDx) indicate whether a new value has been written in DCC0 or DCC1. These bits, DCC0D and DCC1D, are located in the STATUSB registers. They are automatically set on write and cleared on read.

Note: The DCC0 and DCC1 registers are shared with the on-board memory testing logic (MBIST). Accordingly, DCC0 and DCC1 must not be used while performing MBIST operations.

Note: The DCC0 and DCC1 registers are shared with the BCC0 and BCC1 registers therefore mixing DCC and BCC communication is not recommended.

Related Links

30. NVMCTRL – Nonvolatile Memory Controller

16.10.5 Boot Communication Channels

The Boot Communication Channels (BCC0 and BCC1) consist of a pair of registers with associated handshake logic, accessible by both CPU and debugger with no security restriction. The registers are intended to communicate with the CPU while executing the Boot ROM which implements security and failure analysis commands and therefore must not be used for another purpose.

Note: The BCC0 and BCC registers values are not reset except in case of POR or BOD resets.

The low-power regulator starts again and the PDSW power domain is set back to retention state by the PM. During this dynamic SleepWalking period, the CPU is still sleeping.

Exiting standby mode: during the dynamic SleepWalking sequence, if conditions are met, the AC module generates an interrupt to wake up the device.

Related Links

27. RTC – Real-Time Counter
33. EVSYS – Event System

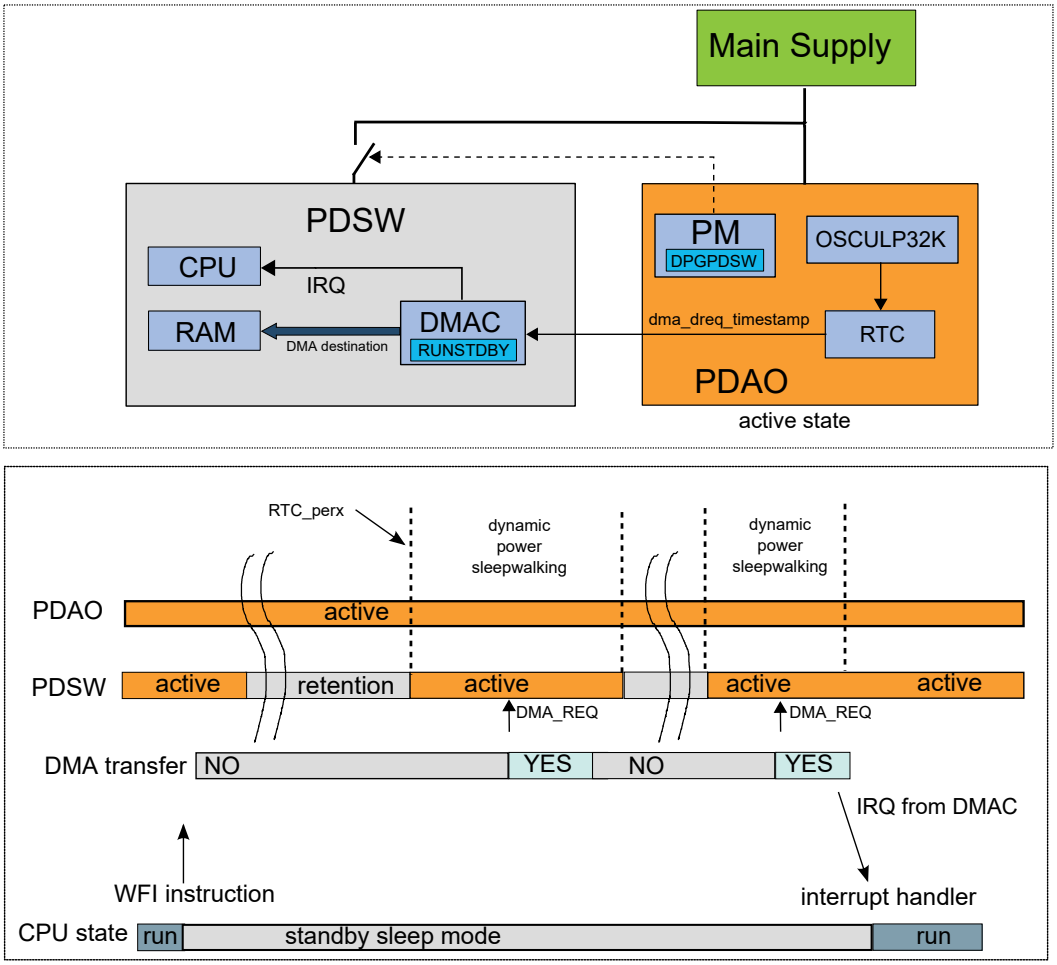
22.6.6.2 Dynamic SleepWalking Based on Peripheral DMA Trigger

To enable this advanced feature, the Dynamic Power Gating for Power Domain SW bit in the Standby Configuration register (STDBYCFG.DPGPDSW) have to be written to '1'.

When in retention state, the power domain PDSW (containing the DMAC) can be automatically set to active state if the PM detects a valid DMA trigger that is coming from a peripheral located in PDAO. A peripheral DMA trigger is valid if the corresponding DMA channel is enabled and its Run in Standby bit (RUNSTDBY) is written to '1'.

This is illustrated in the following example:

Figure 22-9. Dynamic Sleepwalking based on Peripheral DMA Trigger



The Write-Synchronization of the Enable bit is triggered by writing a '1' to the Enable bit of the BOD33 Control register. The Synchronization Ready bit (STATUS.B33SRDY) in the STATUS register will be cleared when the Write-Synchronization starts, and set again when the Write-Synchronization is complete. Writing to the same register while the Write-Synchronization is ongoing (STATUS.B33SRDY is '0') will generate a PAC error without stalling the APB bus.

25.6.7 Low Power VREF in Active Mode

During active functional mode, the brownout detector BOD33 and the main voltage regulator (VREG) can reduce their power consumption by using the low power voltage reference (ULPVREF).

The low power voltage reference is ready and can be selected when ULPVREFRDY bit in STATUS register is high. The ULPVREF Ready (ULPVREFRDY) interrupt can also be used to detect a zero-to-one transition of the STATUS.ULPVREFRDY bit.

Writing the VREF bit in the BOD33 register to '1' selects ULPVREF as voltage reference for the BOD33.

If the chip operated in PL0 ((PM->PLCFG.PLSEL=0) or Performance Level is disabled (PM->PLCFG.PLDIS=1), writing the VREFSEL bit in the VREG register to '1' selects ULPVREF as voltage reference for the main voltage regulator.

CTRLA.ENABLE=0 and check whether the write synchronization has finished, then change the desired bit field value. Enable-protected bits in CTRLA register can be written at the same time as CTRLA.ENABLE is written to '1', but not at the same time as CTRLA.ENABLE is written to '0'.

Enable-protection is denoted by the "Enable-Protected" property in the register description.

The RTC prescaler divides the source clock for the RTC counter.

Note: In Clock/Calendar mode, the prescaler must be configured to provide a 1Hz clock to the counter for correct operation.

The frequency of the RTC clock (CLK_RTC_CNT) is given by the following formula:

$$f_{\mathrm{CLK\_RTC\_CNT}} = \frac{f_{\mathrm{CLK\_RTC\_OSC}}}{2^{\mathrm{PRESCALER}}}$$

The frequency of the oscillator clock, CLK_RTC_OSC, is given by $f_{CLK\_RTC\_OSC}$, and $f_{CLK\_RTC\_CNT}$ is the frequency of the internal prescaled RTC clock, CLK_RTC_CNT.

27.6.2.2 Enabling, Disabling, and Resetting

The RTC is enabled by setting the Enable bit in the Control A register (CTRLA.ENABLE=1). The RTC is disabled by writing CTRLA.ENABLE=0.

The RTC is reset by setting the Software Reset bit in the Control A register (CTRLA.SWRST=1). All registers in the RTC, except DEBUG, will be reset to their initial state, and the RTC will be disabled. The RTC must be disabled before resetting it.

27.6.2.3 32-Bit Counter (Mode 0)

When the RTC Operating Mode bits in the Control A register (CTRLA.MODE) are written to 0x0, the counter operates in 32-bit Counter mode. The block diagram of this mode is shown in Figure 27-1. When the RTC is enabled, the counter will increment on every 0-to-1 transition of CLK_RTC_CNT. The counter will increment until it reaches the top value of 0xFFFFFFFF, and then wrap to 0x00000000. This sets the Overflow Interrupt flag in the Interrupt Flag Status and Clear register (INTFLAG.OVF).

The RTC counter value can be read from or written to the Counter Value register (COUNT) in 32-bit format.

The counter value is continuously compared with the 32-bit Compare register (COMP0). When a compare match occurs, the Compare 0 Interrupt flag in the Interrupt Flag Status and Clear register (INTFLAG.CMP0) is set on the next 0-to-1 transition of CLK_RTC_CNT.

If the Clear on Match bit in the Control A register (CTRLA.MATCHCLR) is '1', the counter is cleared on the next counter cycle when a compare match with COMP0 occurs. This allows the RTC to generate periodic interrupts or events with longer periods than the prescaler events. Note that when CTRLA.MATCHCLR is '1', INTFLAG.CMP0 and INTFLAG.OVF will both be set simultaneously on a compare match with COMP0.

27.6.2.4 16-Bit Counter (Mode 1)

When the RTC Operating Mode bits in the Control A register (CTRLA.MODE) are written to 0x1, the counter operates in 16-bit Counter mode as shown in Figure 27-2. When the RTC is enabled, the counter will increment on every 0-to-1 transition of CLK_RTC_CNT. In 16-bit Counter mode, the 16-bit Period register (PER) holds the maximum value of the counter. The counter will increment until it reaches the PER value, and then wrap to 0x0000. This sets the Overflow Interrupt flag in the Interrupt Flag Status and Clear register (INTFLAG.OVF).

The RTC counter value can be read from or written to the Counter Value register (COUNT) in 16-bit format.

27.12.16 Tamper ID

Name: TAMPID
Offset: 0x68
Reset: 0x00000000

Bit	31	30	29	28	27	26	25	24
	TAMPEVT							
Access	R/W							
Reset	0							

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
					TAMPID3	TAMPID2	TAMPID1	TAMPID0
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit 31 – TAMPEVT Tamper Event Detected
Writing a '0' to this bit has no effect. Writing a '1' to this bit clears the tamper detection bit.

Value	Description
0	A tamper input event has not been detected
1	A tamper input event has been detected

Bits 0, 1, 2, 3 – TAMPID Tamper on Channel n Detected
Writing a '0' to this bit has no effect. Writing a '1' to this bit clears the tamper detection bit.

Value	Description
0	A tamper condition has not been detected on Channel n
1	A tamper condition has been detected on Channel n

28.8.4 CRC Checksum

Name: CRCCHKSUM
Offset: 0x08
Reset: 0x00000000
Property: PAC Write-Protection, Enable-Protected

The CRCCHKSUM represents the 16- or 32-bit checksum value and the generated CRC. The register is reset to zero by default, but it is possible to reset all bits to one by writing the CRCCHKSUM register directly. It is possible to write this register only when the CRC module is disabled. If CRC-32 is selected and the CRC Status Busy flag is cleared (i.e., CRC generation is completed or aborted), the bit reversed (bit 31 is swapped with bit 0, bit 30 with bit 1, etc.) and complemented result will be read from CRCCHKSUM. If CRC-16 is selected or the CRC Status Busy flag is set (i.e., CRC generation is ongoing), CRCCHKSUM will contain the actual content.

Bit	31	30	29	28	27	26	25	24
	CRCCHKSUM[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	CRCCHKSUM[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	CRCCHKSUM[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CRCCHKSUM[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – CRCCHKSUM[31:0] CRC Checksum
These bits store the generated CRC result. The 16 MSB bits are always read zero when CRC-16 is enabled.

- The configuration of secured external interrupts can only be changed in the secure alias. Attempt to change the configuration in non-secure mode is silently ignored. Affected configuration registers are: CTRLA, NMICTRL, NMIFLAG, EVCTRL, INTENCLR, INTENSET, INTFLAG, ASYNCH, CONFIGn, DEBOUNCEN, DPRESCALER.

Note: Refer to the *Mix-Secure Peripherals* section in the SAM L11 *Security Features* chapter for more information.

29.5.10 Analog Connections

Not applicable.

29.6 Functional Description

29.6.1 Principle of Operation

The EIC detects edge or level condition to generate interrupts to the CPU interrupt controller or events to the Event System. Each external interrupt pin (EXTINT) can be filtered using majority vote filtering, clocked by GCLK_EIC or by CLK_ULP32K.

29.6.2 Basic Operation

29.6.2.1 Initialization

The EIC must be initialized in the following order:

1. Enable CLK_EIC_APB
2. If required, configure the NMI by writing the Non-Maskable Interrupt Control register (29.8.2 NMICTRL)
3. Enable GCLK_EIC or CLK_ULP32K when one of the following configuration is selected:
   – the NMI uses edge detection or filtering.
   – one EXTINT uses filtering.
   – one EXTINT uses synchronous edge detection.
   – one EXTINT uses debouncing.

   GCLK_EIC is used when a frequency higher than 32KHz is required for filtering.

   CLK_ULP32K is recommended when power consumption is the priority. For CLK_ULP32K write a '1' to the Clock Selection bit in the Control A register (CTRLA.CKSEL).
4. Configure the EIC input sense and filtering by writing the Configuration n register (CONFIG).
5. Optionally, enable the asynchronous mode.
6. Optionally, enable the debouncer mode.
7. Enable the EIC by writing a ‘1’ to CTRLA.ENABLE.

The following bits are enable-protected, meaning that it can only be written when the EIC is disabled (CTRLA.ENABLE=0):

- Clock Selection bit in Control A register (CTRLA.CKSEL)

The following registers are enable-protected:

- Event Control register (29.8.5 EVCTRL)
- Configuration n register (CONFIG).
- External Interrupt Asynchronous Mode register (29.8.9 ASYNCH)

30.8.1 Control A

Name: CTRLA
Offset: 0x00
Reset: 0x0000
Property: PAC Write-Protection, Write-Mix-Secure

Important: For **SAM L11 Non-Secure** accesses, write accesses (W*) are allowed only if Non-Secure Write is set in the NONSEC register.

Bit	15	14	13	12	11	10	9	8
	CMDEX[7:0]							
Access	W/W*/W	W/W*/W	W/W*/W	W/W*/W	W/W*/W	W/W*/W	W/W*/W	W/W*/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
		CMD[6:0]						
Access		W/W/W	W/W/W	W/W/W	W/W/W	W/W/W	W/W/W	W/W/W
Reset		0	0	0	0	0	0	0

Bits 15:8 – CMDEX[7:0] Command Execution
When this bit group is written to the key value 0xA5, the command written to CMD will be executed. If a value different from the key value is tried, the write will not be performed and the key error interrupt (INTFLAG.KEYE) will be set. PROGE is set if a previously written command is not completed yet or in case of bad conditions.

The key value must be written at the same time as CMD. If a command is issued through the APB bus on the same cycle as an AHB bus access, the AHB bus access will be given priority. The command will then be executed when the NVM block and the AHB bus are idle.

STATUS.READY must be '1' when the command has issued.

Note: The NVM Address bit field in the Address register (ADDR.ADDR) is driving the hardware (8-bit) address to the NVM when a command is executed using CMDEX.

Bits 6:0 – CMD[6:0] Command
These bits define the command to be executed when the CMDEX key is written.

Important: For **SAM L11**, only ER, WP, PBC, SDAL0 commands are available from the non-secure alias. Non-secure ER, WP, PBC are processed only if ADDR points to a non secure address, otherwise a PROGE error is issued.

Each pin may be secured or non-secured, with secured pins only accessible by secure accesses.

Device-specific configurations may cause some lines (and the corresponding Pxy pin) not to be implemented.

32.5.2 Power Management

During Reset, all PORT lines are configured as inputs with input buffers, output buffers and pull disabled.

The PORT peripheral will continue operating in any sleep mode where its source clock is running.

32.5.3 Clocks

The PORT bus clock (CLK_PORT_APB) can be enabled and disabled in the Main Clock module, and the default state of CLK_PORT_APB can be found in the *Peripheral Clock Masking* section in *MCLK – Main Clock*.

The PORT requires an APB clock, which may be divided from the CPU main clock and allows the CPU to access the registers of PORT through the high-speed matrix and the AHB/APB bridge.

The priority of IOBUS accesses is higher than APB accesses. One clock cycle latency can be observed on the APB access in case of concurrent PORT accesses.

Related Links

19. MCLK – Main Clock

32.5.4 DMA

Not applicable.

32.5.5 Interrupts

Not applicable.

32.5.6 Events

The events of this peripheral are connected to the Event System.

Related Links

33. EVSYS – Event System

32.5.7 Debug Operation

When the CPU is halted in debug mode, this peripheral will continue normal operation.

32.5.8 Register Access Protection

All registers with write-access can be optionally write-protected by the Peripheral Access Controller (PAC).

Note: Optional write-protection is indicated by the "PAC Write-Protection" property in the register description.

Write-protection does not apply for accesses through an external debugger.

Related Links

15. PAC - Peripheral Access Controller

32.5.9 Analog Connections

Analog functions are connected directly between the analog blocks and the I/O pads using analog buses. However, selecting an analog peripheral function for a given pin will disable the corresponding digital features of the pad.

33.7.20 Event User Security Attribution Check

Name: NSCHKUSERm
Offset: 0x01F0 + m*0x04 [m=0..1]
Reset: 0x00000000
Property: PAC Write-Protection

This register allows the user to select one or more event users to check their security attribution as non-secured.

Important: This register is only available for **SAM L11** and has no effect for **SAM L10**.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
		USERn[22:16]						
Access		RW/RW/RW	RW/RW/RW	RW/RW/RW	RW/RW/RW	RW/RW/RW	RW/RW/RW	RW/RW/RW
Reset		0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	USERn[15:8]							
Access	RW/RW/RW	RW/RW/RW	RW/RW/RW	RW/RW/RW	RW/RW/RW	RW/RW/RW	RW/RW/RW	RW/RW/RW
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	USERn[7:0]							
Access	RW/RW/RW	RW/RW/RW	RW/RW/RW	RW/RW/RW	RW/RW/RW	RW/RW/RW	RW/RW/RW	RW/RW/RW
Reset	0	0	0	0	0	0	0	0

Bits 22:0 – USERn[22:0] Event User n Selection [n=22..0]
These bits selects the individual event users for security attribution check. If any event user selected in NSCHKUSER has the corresponding bit in NONSECUSER set to the opposite value, then the NSCHK interrupt flag will be set.

Value	Description
0	0-to-1 transition will be detected on corresponding NONSECUSER bit.
1	1-to-0 transition will be detected on corresponding NONSECUSER bit.

36.8 Register Description

Registers can be 8, 16, or 32 bits wide. Atomic 8-, 16-, and 32-bit accesses are supported. In addition, the 8-bit quarters and 16-bit halves of a 32-bit register, and the 8-bit halves of a 16-bit register can be accessed directly.

Some registers require synchronization when read and/or written. Synchronization is denoted by the "Read-Synchronized" and/or "Write-Synchronized" property in each individual register description.

Refer to 36.6.6 Synchronization

Some registers are enable-protected, meaning they can only be written when the module is disabled. Enable-protection is denoted by the "Enable-Protected" property in each individual register description.

Optional write-protection by the Peripheral Access Controller (PAC) is denoted by the "PAC Write-Protection" property in each individual register description.

Refer to 36.5.8 Register Access Protection.

On **SAM L11** devices, this peripheral has different access permissions depending on PAC Security Attribution (Secure or Non-Secure):

- If the peripheral is configured as Non-Secure in the PAC:
  - Secure access and Non-Secure access are granted
- If the peripheral is configured as Secure in the PAC:
  - Secure access is granted
  - Non-Secure access is discarded (Write is ignored, read 0x0) and a PAC error is triggered

Refer to *Peripherals Security Attribution* for more information.

Case 1: Address packet accepted – Read flag set

The STATUS.DIR bit is ‘1’, indicating an I2C master read operation. The SCL line is forced low, stretching the bus clock. If an ACK is sent, I2C slave hardware will set the Data Ready bit in the Interrupt Flag register (INTFLAG.DRDY), indicating data are needed for transmit. If a NACK is sent, the I2C slave will wait for a new start condition and address match.

Typically, software will immediately acknowledge the address packet by sending an ACK/NACK bit. The I2C slave Command bit field in the Control B register (CTRLB.CMD) can be written to '0x3' for both read and write operations as the command execution is dependent on the STATUS.DIR bit. Writing ‘1’ to INTFLAG.AMATCH will also cause an ACK/NACK to be sent corresponding to the CTRLB.ACKACT bit.

Case 2: Address packet accepted – Write flag set

The STATUS.DIR bit is cleared, indicating an I2C master write operation. The SCL line is forced low, stretching the bus clock. If an ACK is sent, the I2C slave will wait for data to be received. Data, repeated start or stop can be received.

If a NACK is sent, the I2C slave will wait for a new start condition and address match. Typically, software will immediately acknowledge the address packet by sending an ACK/NACK. The I2C slave command CTRLB.CMD = 3 can be used for both read and write operation as the command execution is dependent on STATUS.DIR.

Writing ‘1’ to INTFLAG.AMATCH will also cause an ACK/NACK to be sent corresponding to the CTRLB.ACKACT bit.

37.6.2.5.2 Receiving Address Packets (SCLSM=1)

When SCLSM=1, the I2C slave will stretch the SCL line only after an ACK, see Slave Behavioral Diagram (SCLSM=1). When the I2C slave is properly configured, it will wait for a start condition to be detected.

When a start condition is detected, the successive address packet will be received and checked by the address match logic.

If the received address is not a match, the packet will be rejected and the I2C slave will wait for a new start condition.

If the address matches, the acknowledge action as configured by the Acknowledge Action bit Control B register (CTRLB.ACKACT) will be sent and the Address Match bit in the Interrupt Flag register (INTFLAG.AMATCH) is set. SCL will be stretched until the I2C slave clears INTFLAG.AMATCH. As the I2C slave holds the clock by forcing SCL low, the software is given unlimited time to respond to the address.

The direction of a transaction is determined by reading the Read/Write Direction bit in the Status register (STATUS.DIR). This bit will be updated only when a valid address packet is received.

If the Transmit Collision bit in the Status register (STATUS.COLL) is set, the last packet addressed to the I2C slave had a packet collision. A collision causes the SDA and SCL lines to be released without any notification to software. The next AMATCH interrupt is, therefore, the first indication of the previous packet’s collision. Collisions are intended to follow the SMBus Address Resolution Protocol (*ARP*).

After the address packet has been received from the I2C master, INTFLAG.AMATCH be set to ‘1’ to clear it.

37.6.2.5.3 Receiving and Transmitting Data Packets

After the I2C slave has received an address packet, it will respond according to the direction either by waiting for the data packet to be received or by starting to send a data packet by writing to DATA.DATA.

Table 37-2. Module Request for SERCOM I²C Master

Condition	Request		
	DMA	Interrupt	Event
Data needed for transmit (TX) (Master transmit mode)	Yes (request cleared when data is written)		NA
Data needed for transmit (RX) (Master transmit mode)	Yes (request cleared when data is read)		
Master on Bus (MB)		Yes	
Stop received (SB)		Yes	
Error (ERROR)		Yes	

37.6.4.1 DMA Operation

Smart mode must be enabled for DMA operation in the Control B register by writing CTRLB.SMEN=1.

37.6.4.1.1 Slave DMA

When using the I²C slave with DMA, an address match will cause the address interrupt flag (INTFLAG.ADDRMATCH) to be raised. After the interrupt has been serviced, data transfer will be performed through DMA.

The I²C slave generates the following requests:

- Write data received (RX): The request is set when master write data is received. The request is cleared when DATA is read.
- Read data needed for transmit (TX): The request is set when data is needed for a master read operation. The request is cleared when DATA is written.

37.6.4.1.2 Master DMA

When using the I²C master with DMA, the ADDR register must be written with the desired address (ADDR.ADDR), transaction length (ADDR.LEN), and transaction length enable (ADDR.LENEN). When ADDR.LENEN is written to 1 along with ADDR.ADDR, ADDR.LEN determines the number of data bytes in the transaction from 0 to 255. DMA is then used to transfer ADDR.LEN bytes followed by an automatically generated NACK (for master reads) and a STOP.

If a NACK is received by the slave for a master write transaction before ADDR.LEN bytes, a STOP will be automatically generated and the length error (STATUS.LENERR) will be raised along with the INTFLAG.ERROR interrupt.

The I²C master generates the following requests:

- Read data received (RX): The request is set when master read data is received. The request is cleared when DATA is read.
- Write data needed for transmit (TX): The request is set when data is needed for a master write operation. The request is cleared when DATA is written.

38. TC – Timer/Counter

38.1 Overview

There are up to three TC peripheral instances.

Each TC consists of a counter, a prescaler, compare/capture channels and control logic. The counter can be set to count events, or clock pulses. The counter, together with the compare/capture channels, can be configured to timestamp input events or IO pin edges, allowing for capturing of frequency and/or pulse width.

A TC can also perform waveform generation, such as frequency generation and pulse-width modulation.

38.2 Features

- Selectable configuration
  - 8-, 16- or 32-bit TC operation, with compare/capture channels
- 2 compare/capture channels (CC) with:
  - Double buffered timer period setting (in 8-bit mode only)
  - Double buffered compare channel
- Waveform generation
  - Frequency generation
  - Single-slope pulse-width modulation
- Input capture
  - Event / IO pin edge capture
  - Frequency capture
  - Pulse-width capture
  - Time-stamp capture
- One input event
- Interrupts/output events on:
  - Counter overflow/underflow
  - Compare match or capture
- Internal prescaler
- DMA support

Name	Description
	or the Compare Channel 0 (CC0) register value depending on the waveform generator mode in 38.6.2.6.1 Waveform Output Operations.
ZERO	The counter is ZERO when it contains all zeroes
MAX	The counter reaches MAX when it contains all ones
UPDATE	The timer/counter signals an update when it reaches ZERO or TOP, depending on the direction settings.
Timer	The timer/counter clock control is handled by an internal source
Counter	The clock control is handled externally (e.g. counting external events)
CC	For compare operations, the CC are referred to as “compare channels” For capture operations, the CC are referred to as “capture channels.”

Each TC instance has up to two compare/capture channels (CC0 and CC1).

The counter in the TC can either count events from the Event System, or clock ticks of the GCLK_TCx clock, which may be divided by the prescaler.

The counter value is passed to the CCx where it can be either compared to user-defined values or captured.

The CCx registers are using buffer registers (CCBUFx) for optimized timing. Each buffer register has a buffer valid (BUFV) flag that indicates when the buffer contains a new value.

The Counter register (COUNT) and the Compare and Capture registers with buffers (CCx and CCBUFx) can be configured as 8-, 16- or 32-bit registers, with according MAX values. Mode settings (CTRLA.MODE) determine the maximum range of the Counter register.

In 8-bit mode, a Period Value (PER) register and its Period Buffer Value (PERBUF) register are also available. The counter range and the operating frequency determine the maximum time resolution achievable with the TC peripheral.

The TC can be set to count up or down. Under normal operation, the counter value is continuously compared to the TOP or ZERO value to determine whether the counter has reached that value. On a comparison match the TC can request DMA transactions, or generate interrupts or events for the Event System.

In compare operation, the counter value is continuously compared to the values in the CCx registers. In case of a match the TC can request DMA transactions, or generate interrupts or events for the Event System. In waveform generator mode, these comparisons are used to set the waveform period or pulse width.

Capture operation can be enabled to perform input signal period and pulse width measurements, or to capture selectable edges from an IO pin or internal event from Event System.

38.6.2 Basic Operation

38.6.2.1 Initialization

The following registers are enable-protected, meaning that they can only be written when the TC is disabled (CTRLA.ENABLE =0):

Value	OPAMPx	Name	Description
0x2	x=0	REFERENCE	REFERENCE[DAC/REFBUF]
	x=1	OA0OUT	OPAMP0 output
	x=2	OA1OUT	OPAMP1 output
0x3	x=0,1,2	GND	
0x4	x=0,1	RG_CONN	
	x=2	Reserved	

Bit 9 – RES1EN Resistor 1 Enable

Value	Description
0	R1 disconnected from RES1MUX.
1	R1 connected to RES1MUX.

Bit 8 – RES2OUT Resistor ladder To Output

Value	Description
0	Swith open.
1	Switch closed.

Bit 7 – ONDEMAND On Demand Control
The On Demand operation mode allows the OPAMPx to be enabled or disabled, depending on other peripheral requests.

Value	Description
0	The OPAMPx is always on, if enabled.
1	The OPAMPx is enabled when a peripheral is requesting the OPAMPx to be used as an input. The OPAMPx is disabled if no peripheral is requesting it as an input.

Bit 6 – RUNSTDBY Run in Standby
This bit controls how the OPAMPx behaves during standby sleep mode:

Value	Description
0	The OPAMPx is disabled in standby sleep mode.
1	The OPAMPx is not stopped in standby sleep mode. If OPAMPCTRLx.ONDEMAND=1, the OPAMPx will be running when a peripheral is requesting it as an input. If OPAMPCTRLx.ONDEMAND=0, OPAMPx will always be running in standby sleep mode.

Bit 5 – RES2VCC Resistor ladder To VCC

Value	Description
0	Swith open.
1	Switch closed.

Bits 4:3 – BIAS[1:0] Bias Selection
These bits are used to select the bias mode.

Sleep Mode	Condition	Typ	Unit
	L11 with BOOTOPT=0	4.1	
	L10 or L11 with BOOTOPT=1, BS = 0x40	210	
	L10 or L11 with BOOTOPT=1, BS = 0x80	410	
	L10 or L11 with BOOTOPT=2, BS = 0x40	210	
	L10 or L11 with BOOTOPT=2, BS = 0x80	410	

Note:

1. These values are based on simulation. They are not covered by production test limits or characterization.

46.9 I/O Pin Characteristics

There are two different pin types with three different speeds: Normal and High Sink(2).

The Drive Strength bit is located in the Pin Configuration register of the PORT (PORT.PINCFG.DRVSTR).

Table 46-11. I/O Pins Common Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IL}	Input low-level voltage	V_{DD}=1.62V-2.7V	-	-	0.25*V_{DD}	V
		V_{DD}=2.7V-3.63V	-	-	0.3*V_{DD}	
V_{IH}	Input high-level voltage	V_{DD}=1.62V-2.7V	0.7*V_{DD}	-	-	
		V_{DD}=2.7V-3.63V	0.55*V_{DD}	-	-	
V_{OL}	Output low-level voltage	V_{DD}>1.62V, I_{OL} max	-	0.1*V_{DD}	0.2*V_{DD}	
V_{OH}	Output high-level voltage	V_{DD}>1.62V, I_{OH} max	0.75*V_{DD}	0.85*V_{DD}	-	
R_{PULL}	Pull-up - Pull-down resistance		20	40	63	kΩ
I_{LEAK}	Input leakage current	Pull-up resistors disabled	-1	±0.015	1	µA

Table 46-12. I/O Pins Maximum Output Current

Symbol	Parameter	Conditions	Normal Pins	High Sink Pins(2)	Normal Pins	High Sink Pins(2)	Units
			DRVSTR=0		DRVSTR=1		
I_{OL}	Maximum Output low-level current	V_{DD}=1.62V-3V	1	2	2	4	mA
		V_{DD}=3V-3.63V	2.5	6	6	12	
I_{OH}	Maximum Output high-level current	V_{DD}=1.62V-3V	0.7	1.5	1.5	3	
		V_{DD}=3V-3.63V	2	5	5	10	