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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M23
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	25
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.63V
Data Converters	A/D 10x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-UFQFN Exposed Pad
Supplier Device Package	32-UQFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsaml10e16a-au

        - Hardware noise filtering and noise signal desynchronization for high conducted immunity
        - Driven Shield Plus for better noise immunity and moisture tolerance
        - Parallel Acquisition through Polarity control
        - Supports wake-up on touch from Standby Sleep mode

- **Communication Interfaces**
    - Up to three Serial Communication Interfaces (SERCOM) that can operate as:
        - USART with full-duplex and single-wire half-duplex configuration
        - I^2C up to 3.4 Mbit/s (High-Speed mode) on one instance and up to 1 Mbit/s (Fast-mode Plus) on the second instance
        - Serial Peripheral Interface (SPI)
        - ISO7816 on one instance
        - RS-485 on one instance
        - LIN Slave on one instance

- **Timers/Output Compare/Input Capture**
    - Three 16-bit Timers/Counters (TC), each configurable as:
        - One 16-bit TC with two compare/capture channels
        - One 8-bit TC with two compare/capture channels
        - One 32-bit TC with two compare/capture channels, by using two TCs
    - 32-bit Real-Time Counter (RTC) with clock/calendar functions
    - Watchdog Timer (WDT) with Window mode

- **Input/Output (I/O)**
    - Up to 25 programmable I/O lines
    - Eight external interrupts (EIC)
    - One non-maskable interrupt (NMI)
    - One Configurable Custom Logic (CCL) that supports:
        - Combinatorial logic functions, such as AND, NAND, OR, and NOR
        - Sequential logic functions, such as Flip-Flop and Latches

- **Qualification and Class-B Support**
    - AEC-Q100 REVH (Grade 1 [-40ºC to +125ºC]) (planned)
    - Class-B safety library, IEC 60730 (future)

- **Debugger Development Support**
    - Two-pin Serial Wire Debug (SWD) programming and debugging interface

- **Packages**

Type	VQFN		TQFP	SSOP	WLCSP(1)
Pin Count	24	32	32	24	32
I/O Pins (up to)	17	25	25	17	25
Contact/Lead Pitch	0.5 mm	0.5 mm	0.8 mm	0.65 mm	0.4 mm
Dimensions	4x4x0.9 mm	5x5x1 mm	7x7x1.2 mm	8.2x5.3x2.0 mm	2.79x2.79x0.482 mm

Note:

1. Contact local sales for availability.

Table 4-7. Secure Pin Multiplexing on SERCOM Pins

Pin Name	Secure Pin Multiplexing Pad Name
PA16	SERCOM1/PAD[0]
PA17	SERCOM1/PAD[1]
PA18	SERCOM1/PAD[2]
PA19	SERCOM1/PAD[3]

4.5 General Purpose I/O (GPIO) Clusters

Table 4-8. GPIO Clusters

Package	Cluster	GPIO	Supply Pins Connected to the Cluster
32-pin	1	PA00 PA01 PA02 PA03 PA04 PA05 PA06 PA07	V_{DDANA}/GNDANA
	2	PA08 PA09 PA10 PA11 PA14 PA15 PA16 PA17 PA18 PA19 PA22 PA23 PA24 PA25 PA27 PA30 PA31	V_{DDIO}/GND
24-pin	1	PA00 PA01 PA02 PA03 PA04 PA05	V_{DDANA}/GND
	2	PA08 PA14 PA15 PA16 PA17 PA18 PA19 PA22 PA23 PA30 PA31	V_{DDIO}/GND

6.3 Power-On Reset and Brown-Out Detectors

The SAM L10/L11 embed three features to monitor, warn and reset the device:

- A Power-on Reset (POR) on V_{DD} (VDDANA and VDDIO):
  - Monitoring is always activated, including during device startup or during any sleep modes.
  - Having V_{DD} below a fixed threshold voltage will reset the whole device.

  Note: Refer to 46.11.2 Power-On Reset (POR) Characteristics for the rising and falling threshold voltages.
- A Brown-out Detector (BOD33) on V_{DD} (VDDANA and VDDIO):
  - The BOD33 can monitor VDD continuously (continuous mode) or periodically (sampled mode) with a programmable sample frequency in active mode as in any sleep modes.
  - A programmable threshold loaded from the NVM User Row is used to trigger an interrupt and/or reset the whole device.
- A Brown-out Detector (BOD12) on VDDCORE.
  Note: BOD12 is calibrated in production and its calibration parameters are stored in the NVM User Row. These data must not be changed to ensure correct device behavior.

6.4 Voltage Regulator

The embedded voltage regulator is used to provide VDDCORE to the device.

The SAM L10/L11 Voltage Regulator has three modes:

- Linear (LDO) mode: The default mode after reset.
- Switching (BUCK) mode: The most power efficient mode when the CPU and peripherals are running (Active mode).
  Note: In Active mode, the voltage regulator can be selected on the fly between LDO (low-dropout) type regulator and Buck converter using the Supply Controller (SUPC)
- Low-Power mode (LPVREG): The default mode, used when the device is in Standby Sleep mode.

6.5 Typical Powering Schematic

The SAM L10/L11 requires a single supply from 1.62V to 3.63V.

The following figures show the recommended power supply connections for two voltage regulators use cases:

- LDO mode only
- LDO/BUCK modes
  Note: By default the LDO voltage regulator is enabled after any reset. Switching to BUCK mode is then required to benefit from its power efficiency.

Note: Some OPAMP Outputs (OAxOUT) can be connected directly to specific Analog Comparator or ADC Inputs (AINx) if they share the same pad: as an example, OA0OUT can be connected to the Analog Comparator AIN3 or ADC AIN5 input (PA07 pin).

7.1 Reference Voltages

Some analog peripherals require a reference voltage for proper operation.

Apart from external voltages (that is, V_{DDANA} or V_{REFx}), the device has a DETREF module that provides two different internal voltage references:

- BANDGAP: A stable voltage reference, fixed at 1.1V.
- INTREF: A variable voltage reference, configured by the Voltage References System Control register in the Supply Controller (SUPC.VREF).

The respective reference voltage source must be selected within each dedicated analog peripheral register:

- ADC: Reference Control register (ADC.REFCTRL)
- DAC: Reference Selection bits in the Control B register (DAC.CTRLB.REFSEL)
  Note: AC has a fixed reference voltage to BANDGAP value.

7.2 Analog On Demand Feature

The Analog On Demand feature allows the ADC and the AC analog peripherals to automatically enable the OPAMPx only when it is needed, thereby allowing a reduction in power consumption. It also allows the ADC analog block to be powered-off when a conversion is completed.
Note: The Analog On Demand is independent from the On Demand Clock request feature, which is used by peripherals to automatically request a source clock which was previously stopped.

OPAMP case
The Analog On Demand feature of the OPAMPx is activated by writing a '1' to the OPAMP.OPAMPCTRLx.ONDEMAND bit.

In that case, the OPAMPx is automatically enabled when the ADC or the AC requests it (as an input) and is automatically disabled when no more requests are coming from these peripherals.

⚠ CAUTION The Analog On Demand feature is not fully supported on cascaded OPAMPs. If several OPAMPs are cascaded together, only the OPAMPx that is connected to the ADC or AC can be enabled/disabled automatically. Upstream OPAMPs will not benefit from this feature.

In Standby Sleep mode, the Analog On Demand feature is still supported if OPAMP.OPAMPCTRLx.RUNSTDBY=1.

If OPAMP.OPAMPCTRLx.RUNSTDBY=0, the OPAMPx will be disabled entering this Sleep mode.

ADC case
For the ADC peripheral, Analog On Demand feature is enabled by writing the ADC.CTRLA.ONDEMAND bit to '1'.

When this feature is activated, the analog block is powered-off when the conversion is complete.

In Sleep mode, when an ADC start request is detected, the analog block is powered-on again and the ADC starts a new conversion after the start-up time delay.

Bit 5 – OSC32KCTRL Interrupt Flag for OSC32KCTRL

Bit 4 – OSCCTRL Interrupt Flag for OSCCTRL

Bit 3 – RSTC Interrupt Flag for RSTC

Bit 2 – MCLK Interrupt Flag for MCLK

Bit 1 – PM Interrupt Flag for PM

Bit 0 – PAC Interrupt Flag for PAC

16.12.23 Component Identification 1

Name: CID1
Offset: 0x1FF4
Reset: 0x00000010
Property: -

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	CCLASS[3:0]				PREAMBLE[3:0]			
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	1	0	0	0	0

Bits 7:4 – CCLASS[3:0] Component Class
These bits will always return 0x1 when read indicating that this ARM CoreSight component is ROM table (refer to the ARM Debug Interface v5 Architecture Specification at http://www.arm.com).

Bits 3:0 – PREAMBLE[3:0] Preamble
These bits will always return 0x00 when read.

19.8.9 APBC Mask

Name: APBCMASK
Offset: 0x1C
Reset: 0x00001FFF for 32-pin packages / 0x00001FF7 for 24-pin packages
Property: PAC Write-Protection

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
				OPAMP	CCL	TRNG	PTC	DAC
Access				R/W	R	R	R	R
Reset				1	1	1	1	1

Bit	7	6	5	4	3	2	1	0
	ADC	TC2	TC1	TC0	SERCOM2	SERCOM1	SERCOM0	EVSYS
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit 12 – OPAMP OPAMP APBC Clock Enable

Value	Description
0	The APBC clock for the OPAMP is stopped.
1	The APBC clock for the OPAMP is enabled.

Bit 11 – CCL CCL APBC Mask Clock Enable

Value	Description
0	The APBC clock for the CCL is stopped.
1	The APBC clock for the CCL is enabled.

Bit 10 – TRNG TRNG APBC Mask Clock Enable

Value	Description
0	The APBC clock for the TRNG is stopped.
1	The APBC clock for the TRNG is enabled.

Bit 9 – PTC PTC APBC Mask Clock Enable

Value	Description
0	The APBC clock for the PTC is stopped.
1	The APBC clock for the PTC is enabled.

26.8.8 Clear

Name: CLEAR
Offset: 0x0C
Reset: 0x00
Property: Write-Synchronized

Bit	7	6	5	4	3	2	1	0
	CLEAR[7:0]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – CLEAR[7:0] Watchdog Clear
In Normal mode, writing 0xA5 to this register during the watchdog time-out period will clear the Watchdog Timer and the watchdog time-out period is restarted.

In Window mode, any writing attempt to this register before the time-out period started (i.e., during TO_{WDTW}) will issue an immediate system Reset. Writing 0xA5 during the time-out period TO_{WDT} will clear the Watchdog Timer and the complete time-out sequence (first TO_{WDTW} then TO_{WDT}) is restarted.

In both modes, writing any other value than 0xA5 will issue an immediate system Reset.

The counter value is continuously compared with the 16-bit Compare registers (COMPn, n=0..1). When a compare match occurs, the Compare n Interrupt flag in the Interrupt Flag Status and Clear register (INTFLAG.CMPn, n=0..1) is set on the next 0-to-1 transition of CLK_RTC_CNT.

27.6.2.5 Clock/Calendar (Mode 2)

When the RTC Operating Mode bits in the Control A register (CTRLA.MODE) are written to 0x2, the counter operates in Clock/Calendar mode, as shown in Figure 27-3. When the RTC is enabled, the counter will increment on every 0-to-1 transition of CLK_RTC_CNT. The selected clock source and RTC prescaler must be configured to provide a 1Hz clock to the counter for correct operation in this mode.

The time and date can be read from or written to the Clock Value register (CLOCK) in a 32-bit time/date format. Time is represented as:

- Seconds
- Minutes
- Hours

Hours can be represented in either 12- or 24-hour format, selected by the Clock Representation bit in the Control A register (CTRLA.CLKREP). This bit can be changed only while the RTC is disabled.

The date is represented in this form:

- Day as the numeric day of the month (starting at 1)
- Month as the numeric month of the year (1 = January, 2 = February, etc.)
- Year as a value from 0x00 to 0x3F. This value must be added to a user-defined reference year. The reference year must be a leap year (2016, 2020 etc). Example: the year value 0x2D, added to a reference year 2016, represents the year 2061.

The RTC will increment until it reaches the top value of 23:59:59 December 31 of year value 0x3F, and then wrap to 00:00:00 January 1 of year value 0x00. This will set the Overflow Interrupt flag in the Interrupt Flag Status and Clear registers (INTFLAG.OVF).

The clock value is continuously compared with the 32-bit Alarm register (ALARM0). When an alarm match occurs, the Alarm 0 Interrupt flag in the Interrupt Flag Status and Clear registers (INTFLAG.ALARM0) is set on the next 0-to-1 transition of CLK_RTC_CNT. E.g. For a 1Hz clock counter, it means the Alarm 0 Interrupt flag is set with a delay of 1s after the occurrence of alarm match.

A valid alarm match depends on the setting of the Alarm Mask Selection bits in the Alarm 0 Mask register (MASK0.SEL). These bits determine which time/date fields of the clock and alarm values are valid for comparison and which are ignored.

If the Clear on Match bit in the Control A register (CTRLA.MATCHCLR) is set, the counter is cleared on the next counter cycle when an alarm match with ALARM0 occurs. This allows the RTC to generate periodic interrupts or events with longer periods than it would be possible with the prescaler events only (see 27.6.8.1 Periodic Intervals).
Note: When CTRLA.MATCHCLR is 1, INTFLAG.ALARM0 and INTFLAG.OVF will both be set simultaneously on an alarm match with ALARM0.

27.6.3 DMA Operation

The RTC generates the following DMA request:

- Tamper (TAMPER): The request is set on capture of the timestamp. The request is cleared when the Timestamp register is read.

27.12.13 General Purpose n

Name: GP
Offset: 0x40 + n*0x04 [n=0..1]
Reset: 0x00000000
Property: -

Bit	31	30	29	28	27	26	25	24
	GP[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

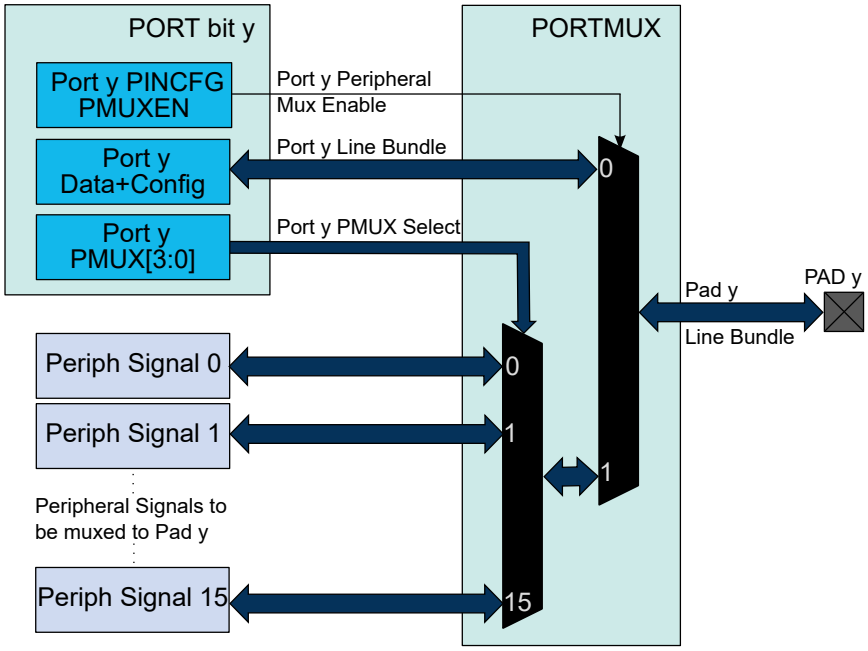
Bit	23	22	21	20	19	18	17	16
	GP[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	GP[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	GP[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – GP[31:0] General Purpose
These bits are for user-defined general purpose use, see 27.6.8.3 General Purpose Registers.

Figure 32-3. Overview of the peripheral functions multiplexing



The I/O pins of the device are controlled by PORT peripheral registers. Each port pin has a corresponding bit in the Data Direction (DIR) and Data Output Value (OUT) registers to enable that pin as an output and to define the output state.

The direction of each pin in a PORT group is configured by the DIR register. If a bit in DIR is set to '1', the corresponding pin is configured as an output pin. If a bit in DIR is set to '0', the corresponding pin is configured as an input pin.

When the direction is set as output, the corresponding bit in the OUT register will set the level of the pin. If bit y in OUT is written to '1', pin y is driven HIGH. If bit y in OUT is written to '0', pin y is driven LOW. Pin configuration can be set by Pin Configuration (PINCFGy) registers, with y=00, 01, ..31 representing the bit position.

The Data Input Value (IN) is set as the input value of a port pin with resynchronization to the PORT clock. To reduce power consumption, these input synchronizers are clocked only when system requires reading the input value. The value of the pin can always be read, whether the pin is configured as input or output. If the Input Enable bit in the Pin Configuration registers (PINCFGy.INEN) is '0', the input value will not be sampled.

In PORT, the Peripheral Multiplexer Enable bit in the PINCFGy register (PINCFGy.PMUXEN) can be written to '1' to enable the connection between peripheral functions and individual I/O pins. The Peripheral Multiplexing n (PMUXn) registers select the peripheral function for the corresponding pin. This will override the connection between the PORT and that I/O pin, and connect the selected peripheral signal to the particular I/O pin instead of the PORT line bundle.

The security attribution of each pin in a PORT group is configured by the NONSEC register. If a bit in the NONSEC register is set to '0', the corresponding pin is configured as a secured pin and can only be handled by secure accesses. If a bit in the NONSEC register is set to '1', the corresponding pin is configured as a non-secured pin. Only secure accesses are allowed to write to the NONSEC register.

32.8.10 Control

Name: CTRL
Offset: 0x24
Reset: 0x00000000
Property: PAC Write-Protection, Secure

Tip: The I/O pins are assembled in pin groups (”PORT groups”) with up to 32 pins. Group 0 consists of the PA pins, group 1 is for the PB pins, etc. Each pin group has its own PORT registers, with a 0x80 address spacing. For example, the register address offset for the Data Direction (DIR) register for group 0 (PA00 to PA31) is 0x00, and the register address offset for the DIR register for group 1 (PB00 to PB31) is 0x80.

Bit	31	30	29	28	27	26	25	24
	SAMPLING[31:24]							
Access	RW/-/RW	RW/-/RW	RW/-/RW	RW/-/RW	RW/-/RW	RW/-/RW	RW/-/RW	RW/-/RW
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SAMPLING[23:16]							
Access	RW/-/RW	RW/-/RW	RW/-/RW	RW/-/RW	RW/-/RW	RW/-/RW	RW/-/RW	RW/-/RW
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SAMPLING[15:8]							
Access	RW/-/RW	RW/-/RW	RW/-/RW	RW/-/RW	RW/-/RW	RW/-/RW	RW/-/RW	RW/-/RW
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SAMPLING[7:0]							
Access	RW/-/RW	RW/-/RW	RW/-/RW	RW/-/RW	RW/-/RW	RW/-/RW	RW/-/RW	RW/-/RW
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – SAMPLING[31:0] Input Sampling Mode
Configures the input sampling functionality of the I/O pin input samplers, for pins configured as inputs via the Data Direction register (DIR).

The input samplers are enabled and disabled in sub-groups of eight. Thus if any pins within a byte request continuous sampling, all pins in that eight pin sub-group will be continuously sampled.

Value	Description
0	The I/O pin input synchronizer is disabled.
1	The I/O pin input synchronizer is enabled.

33. EVSYS – Event System

33.1 Overview

The Event System (EVSYS) allows autonomous, low-latency and configurable communication between peripherals.

Several peripherals can be configured to generate and/or respond to signals known as events. The exact condition to generate an event, or the action taken upon receiving an event, is specific to each peripheral. Peripherals that respond to events are called event users. Peripherals that generate events are called event generators. A peripheral can have one or more event generators and can have one or more event users. Channels and event users can be defined as secured or non-secured, where secured channels or event users can only be handled by secure code.

Communication is made without CPU intervention and without consuming system resources such as bus or RAM bandwidth. This reduces the load on the CPU and other system resources, compared to a traditional interrupt-based system.

33.2 Features

- 8 configurable event channels:
  - All channels can be connected to any event generator
  - All channels provide a pure asynchronous path
  - 4 channels (CHANNEL0 to CHANNEL3) provide a resynchronized or synchronous path using their dedicated generic clock (GCLK_EVSYS_CHANNEL_n)
- 49 event generators.
- 23 event users.
- Configurable edge detector.
- Peripherals can be event generators, event users, or both.
- SleepWalking and interrupt for operation in sleep modes.
- Software event generation.
- Each event user can choose which channel to respond to.
- Optional Static or Round-Robin interrupt priority arbitration.
- Each channel and each event user can be configured as secured or non-secured (**SAM L11**).

35.8.13 DBGCTRL

35.5.8 Register Access Protection

Registers with write-access can be write-protected optionally by the peripheral access controller (PAC).

PAC Write-Protection is not available for the following registers:

- Interrupt Flag Clear and Status register (INTFLAG)
- Status register (STATUS)
- Data register (DATA)

Optional PAC Write-Protection is denoted by the "PAC Write-Protection" property in each individual register description.

Write-protection does not apply to accesses through an external debugger.

Related Links

15. PAC - Peripheral Access Controller

35.5.9 SAM L11 TrustZone Specific Register Access Protection

On **SAM L11** devices, this peripheral has different access permissions depending on PAC Security Attribution (Secure or Non-Secure):

- If the peripheral is configured as Non-Secure in the PAC:
  - Secure access and Non-Secure access are granted
- If the peripheral is configured as Secure in the PAC:
  - Secure access is granted
  - Non-Secure access is discarded (Write is ignored, read 0x0) and a PAC error is triggered

Refer to *Peripherals Security Attribution* for more information.

35.5.10 Analog Connections

Not applicable.

35.6 Functional Description

35.6.1 Principle of Operation

The USART uses the following lines for data transfer:

- RxD for receiving
- TxD for transmitting
- XCK for the transmission clock in synchronous operation

USART data transfer is frame based. A serial frame consists of:

- 1 start bit
- From 5 to 9 data bits (MSB or LSB first)
- No, even or odd parity bit
- 1 or 2 stop bits

A frame starts with the start bit followed by one character of data bits. If enabled, the parity bit is inserted after the data bits and before the first stop bit. After the stop bit(s) of a frame, either the next frame can

35.6.2.6 Data Reception

The receiver accepts data when a valid start bit is detected. Each bit following the start bit will be sampled according to the baud rate or XCK clock, and shifted into the receive shift register until the first stop bit of a frame is received. The second stop bit will be ignored by the receiver.

When the first stop bit is received and a complete serial frame is present in the receive shift register, the contents of the shift register will be moved into the two-level or four-level receive buffer. Then, the Receive Complete interrupt flag in the Interrupt Flag Status and Clear register (INTFLAG.RXC) will be set, and the optional interrupt will be generated.

The received data can be read from the DATA register when the Receive Complete interrupt flag is set.

35.6.2.6.1 Disabling the Receiver

Writing '0' to the Receiver Enable bit in the CTRLB register (CTRLB.RXEN) will disable the receiver, flush the two-level or four-level receive buffer, and data from ongoing receptions will be lost.

35.6.2.6.2 Error Bits

The USART receiver has three error bits in the Status (STATUS) register: Frame Error (FERR), Buffer Overflow (BUFOVF), and Parity Error (PERR). Once an error happens, the corresponding error bit will be set until it is cleared by writing ‘1’ to it. These bits are also cleared automatically when the receiver is disabled.

There are two methods for buffer overflow notification, selected by the Immediate Buffer Overflow Notification bit in the Control A register (CTRLA.IBON):

When CTRLA.IBON=1, STATUS.BUFOVF is raised immediately upon buffer overflow. Software can then empty the receive FIFO by reading RxDATA, until the receiver complete interrupt flag (INTFLAG.RXC) is cleared.

When CTRLA.IBON=0, the buffer overflow condition is attending data through the receive FIFO. After the received data is read, STATUS.BUFOVF will be set along with INTFLAG.RXC.

35.6.2.6.3 Asynchronous Data Reception

The USART includes a clock recovery and data recovery unit for handling asynchronous data reception.

The clock recovery logic can synchronize the incoming asynchronous serial frames at the RxD pin to the internally generated baud-rate clock.

The data recovery logic samples and applies a low-pass filter to each incoming bit, thereby improving the noise immunity of the receiver.

35.6.2.6.4 Asynchronous Operational Range

The operational range of the asynchronous reception depends on the accuracy of the internal baud-rate clock, the rate of the incoming frames, and the frame size (in number of bits). In addition, the operational range of the receiver is depending on the difference between the received bit rate and the internally generated baud rate. If the baud rate of an external transmitter is too high or too low compared to the internally generated baud rate, the receiver will not be able to synchronize the frames to the start bit.

There are two possible sources for a mismatch in baud rate: First, the reference clock will always have some minor instability. Second, the baud-rate generator cannot always do an exact division of the reference clock frequency to get the baud rate desired. In this case, the BAUD register value should be set to give the lowest possible error. Refer to *Clock Generation – Baud-Rate Generator* for details.

Recommended maximum receiver baud-rate errors for various character sizes are shown in the table below.

37.10.5 Interrupt Enable Set

Name: INTENSET
Offset: 0x16
Reset: 0x00
Property: PAC Write-Protection

This register allows the user to enable an interrupt without doing a read-modify-write operation. Changes in this register will also be reflected in the Interrupt Enable Clear register (INTENCLR).

Bit	7	6	5	4	3	2	1	0
	ERROR						SB	MB
Access	R/W						R/W	R/W
Reset	0						0	0

Bit 7 – ERROR Error Interrupt Enable
Writing '0' to this bit has no effect.

Writing '1' to this bit will set the Error Interrupt Enable bit, which enables the Error interrupt.

Value	Description
0	Error interrupt is disabled.
1	Error interrupt is enabled.

Bit 1 – SB Slave on Bus Interrupt Enable
Writing '0' to this bit has no effect.

Writing '1' to this bit will set the Slave on Bus Interrupt Enable bit, which enables the Slave on Bus interrupt.

Value	Description
0	The Slave on Bus interrupt is disabled.
1	The Slave on Bus interrupt is enabled.

Bit 0 – MB Master on Bus Interrupt Enable
Writing '0' to this bit has no effect.

Writing '1' to this bit will set the Master on Bus Interrupt Enable bit, which enables the Master on Bus interrupt.

Value	Description
0	The Master on Bus interrupt is disabled.
1	The Master on Bus interrupt is enabled.

- Control A register (CTRLA), except the Enable (ENABLE) and Software Reset (SWRST) bits
- Drive Control register (DRVCTRL)
- Wave register (WAVE)
- Event Control register (EVCTRL)

Writing to Enable-Protected bits and setting the CTRLA.ENABLE bit can be performed in a single 32-bit access of the CTRLA register. Writing to Enable-Protected bits and clearing the CTRLA.ENABLE bit cannot be performed in a single 32-bit access.

Before enabling the TC, the peripheral must be configured by the following steps:

1. Enable the TC bus clock (CLK_TCx_APB).
2. Select 8-, 16- or 32-bit counter mode via the TC Mode bit group in the Control A register (CTRLA.MODE). The default mode is 16-bit.
3. Select one wave generation operation in the Waveform Generation Operation bit group in the WAVE register (WAVE.WAVEGEN).
4. If desired, the GCLK_TCx clock can be prescaled via the Prescaler bit group in the Control A register (CTRLA.PRESCALER).
   – If the prescaler is used, select a prescaler synchronization operation via the Prescaler and Counter Synchronization bit group in the Control A register (CTRLA.PRESYNC).
5. If desired, select one-shot operation by writing a '1' to the One-Shot bit in the Control B Set register (CTRLBSET.ONESHOT).
6. If desired, configure the counting direction 'down' (starting from the TOP value) by writing a '1' to the Counter Direction bit in the Control B register (CTRLBSET.DIR).
7. For capture operation, enable the individual channels to capture in the Capture Channel x Enable bit group in the Control A register (CTRLA.CAPTEN).
8. If desired, enable inversion of the waveform output or IO pin input signal for individual channels via the Invert Enable bit group in the Drive Control register (DRVCTRL.INVEN).

38.6.2.2 Enabling, Disabling, and Resetting

The TC is enabled by writing a '1' to the Enable bit in the Control A register (CTRLA.ENABLE). The TC is disbled by writing a zero to CTRLA.ENABLE.

The TC is reset by writing a '1' to the Software Reset bit in the Control A register (CTRLA.SWRST). All registers in the TC, except DBGCTRL, will be reset to their initial state. Refer to the CTRLA register for details.

The TC should be disabled before the TC is reset in order to avoid undefined behavior.

38.6.2.3 Prescaler Selection

The GCLK_TCx is fed into the internal prescaler.

The prescaler consists of a counter that counts up to the selected prescaler value, whereupon the output of the prescaler toggles.

If the prescaler value is higher than one, the counter update condition can be optionally executed on the next GCLK_TCx clock pulse or the next prescaled clock pulse. For further details, refer to Prescaler (CTRLA.PRESCALER) and Counter Synchronization (CTRLA.PRESYNC) description.

Prescaler outputs from 1 to 1/1024 are available. For a complete list of available prescaler outputs, see the register description for the Prescaler bit group in the Control A register (CTRLA.PRESCALER).

Note: When counting events, the prescaler is bypassed.

The joint stream of prescaler ticks and event action ticks is called CLK_TC_CNT.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Units
		Master, VDD>1,62V		0	-	-	
tMOV	MOSI output valid after SCK	Master, VDD>2,70V		-	-	34.5	ns
		Master, VDD>1,62V		-	-	38.6	
tMOH	MOSI hold after SCK	Master, VDD>2,70V		9.7	-	-	
		Master, VDD>1,62V		9.7	-	-	
tSSCK	Slave SCK Period when tMIS=0 on the master side	Slave	Reception	2*(tSIS +tMASTER_OUT) (5)	-	-	
		Slave	Transmission	2*(tSOV +tMASTER_IN) (6)	-	-	
tSSCKW	SCK high/low width	Slave		-	0,5*tSCK	-	
tSSCKR	SCK rise time(2)	Slave		-	0,25*tSCK	-	
tSSCKF	SCK fall time(2)	Slave		-	0,25*tSCK	-	
tSIS	MOSI setup to SCK	Slave, VDD>2,70V		25.6	-	-	ns
		Slave, VDD>1,62V		26.2	-	-	
tSIH	MOSI hold after SCK	Slave, VDD>2,70V		13.2	-	-	
		Slave, VDD>1,62V		13.9	-	-	
tSSS	SS setup to SCK	Slave	PRELOADEN=1	tSOSS+tEXT_MIS +2*tAPBC (8) (9)	-	-	
			PRELOADEN=0	tSOSS+tEXT_MIS (8)	-	-	
tSSH	SS hold after SCK	Slave		0.5*tSSCK	-	-	
tSOV	MISO output valid after SCK	Slave, VDD>2,70V		-	-	69	
		Slave, VDD>1,62V		-	-	78.4	
tSOH	MISO hold after SCK	Slave, VDD>2,70V		20.2	-	-	
		Slave, VDD>1,62V		20.2	-	-	
tSOSS	MISO setup after SS low	Slave, VDD>2,70V		-	-	1* tSCK	
		Slave, VDD>1,62V		-	-	1* tSCK	

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Units
		VREF= INT1V	VDD = 1.62V	+/-0,4	+/-0,7	+/-4.2	
			VDD = 3.63V	+/-0,4	+/-0,8	+/-6	
DNL	Differential non-linearity	VREF= Ext 1.0V	VDD = 1.62V	+/-0,1	+/-0,3	+/-2	LSB
			VDD = 3.63V	+/-0,1	+/-0,3	+/-1.5	
		VREF= VDDANA	VDD = 1.62V	+/-0,1	+-0,2	+/-3.0	
			VDD = 3.63V	+/-0,1	+/-0,2	+/-1.6	
		VREF= INT1V	VDD = 1.62V	+/-0,3	+/-0,6	+/-4.3	
			VDD = 3.63V	+/-0,3	+/-0,8	+/-7	
	Gain error	VREF= Ext 1.0V		-	+/-4	+/-16	mV
		VREF= VDDANA		-	+/-12	+/-60	mV
		VREF= INT1V		-	+/-1	+/-23	mV
	Offset error	VREF= Ext 1.0V		-	+/-1	+/-13	mV
		VREF= VDDANA		-	+/-2.5	+/-32	mV
		VREF= INT1V		-	+/-1.5	+/-30	mV

Note:

1. All values measured using a conversion rate of 350ksps.

47.4.4 Analog Comparator Characteristics

Table 47-13. Electrical and Timing (1)

Symbol	Parameters	Conditions	Min.	Typ	Max.	Unit
PNIVR	Positive and Negative input range voltage		0	-	V_{DDANA}	V
ICMR	Input common mode range		0	-	V_{DDANA}-0.1	V
Off	Offset	COMPCTRLn.SPEED=0x0	-70	-4.5/+1.5	70	mV
		COMPCTRLn.SPEED=0x1	-55	-4.5/+1.5	55	
		COMPCTRLn.SPEED=0x2	-48	-4.5/+1.5	48	
		COMPCTRLn.SPEED=0x3	-42	-4.5/+1.5	42	
V_{Hys}	Hysteresis	COMPCTRLn.HYST=0x0	10	45	79	mV
		COMPCTRLn.HYST=0x1	22	70	115	
		COMPCTRLn.HYST=0x2	37	90	138	
		COMPCTRLn.HYST=0x3	49	105	159	

50.5 Unused or Unconnected Pins

For unused pins the default state of the pins will give the lowest current leakage. Thus there is no need to do any configuration of the unused pins in order to lower the power consumption.

50.6 Clocks and Crystal Oscillators

The SAM L10/L11 can be run from internal or external clock sources, or a mix of internal and external sources. An example of usage can be to use the internal 16MHz oscillator as source for the system clock and an external 32.768kHz watch crystal as clock source for the Real-Time counter (RTC).

50.6.1 External Clock Source

Figure 50-6. External Clock Source Schematic

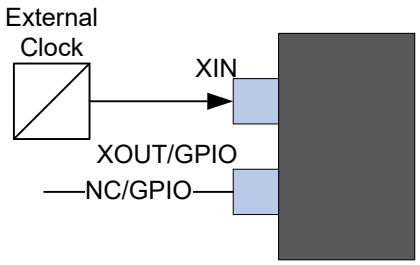
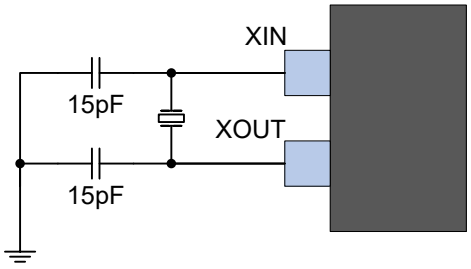


Table 50-4. External Clock Source Connections

Signal Name	Recommended Pin Connection	Description
XIN	XIN is used as input for an external clock signal	Input for inverting oscillator pin
XOUT/GPIO	Can be left unconnected or used as normal GPIO	NC/GPIO

50.6.2 Crystal Oscillator

Figure 50-7. Crystal Oscillator Schematic



The crystal should be located as close to the device as possible. Long signal lines may cause too high load to operate the crystal, and cause crosstalk to other parts of the system.

Table 50-5. Crystal Oscillator Checklist

Signal Name	Recommended Pin Connection	Description
XIN	Load capacitor 15pF(1)(2)	External crystal between 0.4 to 32MHz
XOUT	Load capacitor 15pF(1)(2)	