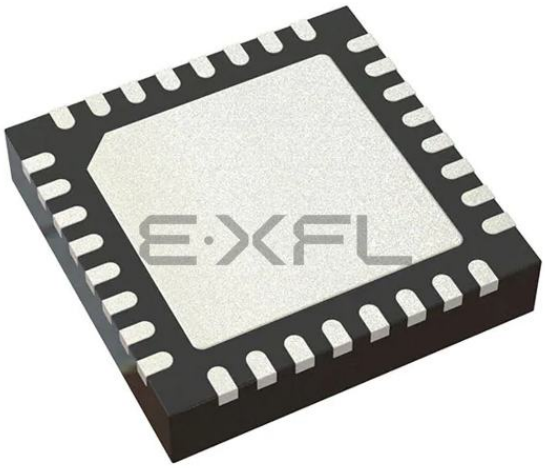

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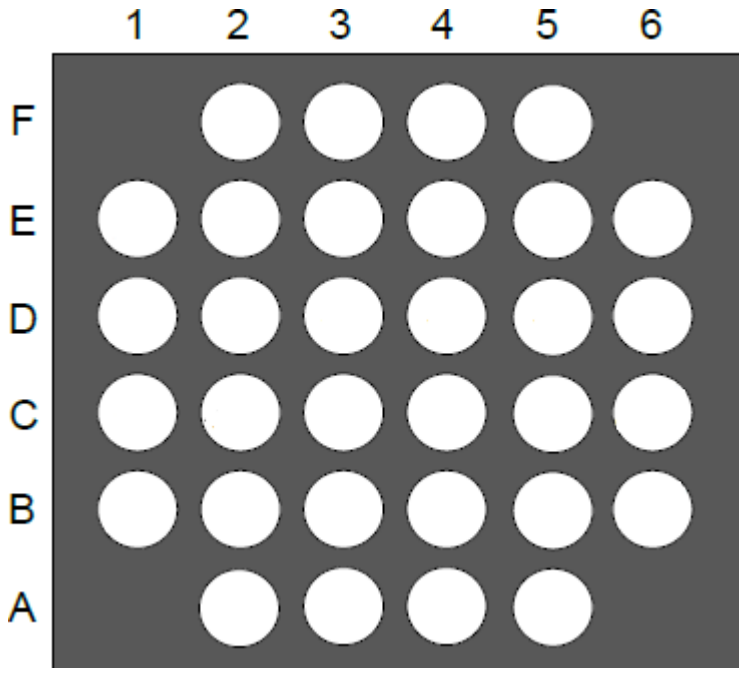
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M23
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	25
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.63V
Data Converters	A/D 10x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VFQFN Exposed Pad
Supplier Device Package	32-VQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsaml10e16a-mu

Feature	SAM L10 Family	SAM L11 Family
CRC	Yes	Yes
Debug Access Levels (DAL)	2	3

Figure 4-4. SAM L10/L11 32-pin WLCSP Pinout



4.1 Multiplexed Signals

Each pin is controlled by the I/O Pin Controller (PORT) as a general purpose I/O and alternatively can be assigned to one of the peripheral functions: A, B, C, D, E, G, H, or I.

The following table describes the peripheral signals multiplexed to the PORT I/O pins.

The column “Reset State” indicates the reset state of the line with mnemonics:

- "I/O" or "Function" indicates whether the I/O pin resets in I/O mode or in peripheral function mode.
- “I” / ”O” / "Hi-Z" indicates whether the I/O is configured as an input, output or is tri-stated.
- “PU” / “PD” indicates whether pullup, pulldown or nothing is enabled.

Table 4-1. Pinout Multiplexing

Pin				Pin Name	Supply	A	B(1)						C(2)(3)	D(2)(3)	E	G	H	I	Reset State
SSOP24	VQFN24	WLCSP32	TQFP32 / VQFN32			EIC	REF	ADC	AC	PTC	DAC	OPAMP	SERCOM	SERCOM ALTERNATIVE	TC	RTC/ Debug	AC/ GCLK	CCL	
5	2	A2	1	PA00 / XIN32	VDDANA	EXTINT[0]				XY[0]		OA1NEG		SERCOM1/ PAD[0]	TC2/ WO[0]				I/O, Hi-Z
6	3	A3	2	PA01 / XOUT32	VDDANA	EXTINT[1]				XY[1]		OA1POS		SERCOM1/ PAD[1]	TC2/ WO[1]				I/O, Hi-Z
7	4	A4	3	PA02	VDDANA	EXTINT[2]		AIN[0]		XY[2]	VOUT	OA0NEG		SERCOM0/ PAD[2]					I/O, Hi-Z
8	5	B3	4	PA03	VDDANA	EXTINT[3]	VREFA	AIN[1]		XY[3]		OA2NEG		SERCOM0/ PAD[3]					I/O, Hi-Z
9	6	B4	5	PA04	VDDANA	EXTINT[4]	VREFB	AIN[2]	AIN[0]			OA2OUT		SERCOM0/ PAD[0]	TC0/ WO[0]			IN[0]	I/O, Hi-Z
10	7	A5	6	PA05	VDDANA	EXTINT[5]		AIN[3]	AIN[1]	XY[4]		OA2POS		SERCOM0/ PAD[1]	TC0/ WO[1]			IN[1]	I/O, Hi-Z

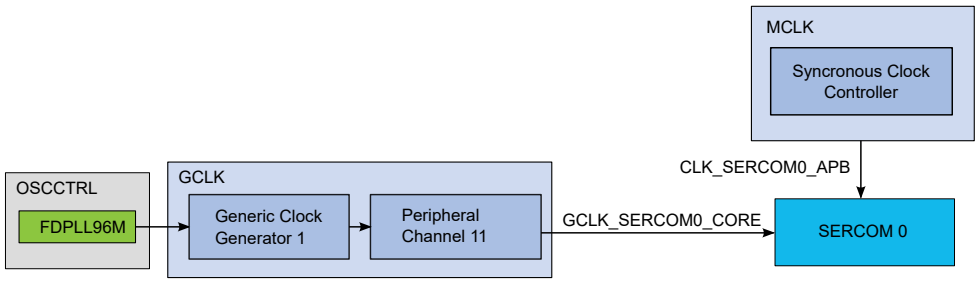
Bit 0 – IDAU Peripheral IDAU Non-Secure
The IDAU Peripheral is always secured.

Generic Clock 0 serves as the clock source for the FDPLL96M clock input (when multiplying another clock source).

- *Main Clock Controller (MCLK)*
  - The MCLK generates and controls the synchronous clocks on the system. This includes the CPU, bus clocks (APB, AHB) as well as the synchronous (to the CPU) user interfaces of the peripherals. It contains clock masks that can turn on/off the user interface of a peripheral as well as prescalers for the CPU and bus clocks.

The figure below illustrates an example, where SERCOM0 is clocked by the FDPLL96M in Open Loop mode. The FDPLL96M is enabled, the Generic Clock Generator 1 uses the FDPLL96M as its clock source and feeds into Peripheral Channel 11. The Generic Clock 10, also called GCLK_SERCOM0_CORE, is connected to SERCOM0. The SERCOM0 interface, clocked by CLK_SERCOM0_APB, has been unmasked in the APBC Mask register in the MCLK.

Figure 17-2. Example of SERCOM Clock



To customize the clock distribution, refer to these registers and bit fields:

- The source oscillator for a generic clock generator 'n' is selected by writing to the Source bit field in the Generator Control n register (GCLK.GENCTRLn.SRC).
- A Peripheral Channel m can be configured to use a specific Generic Clock Generator by writing to the Generic Clock Generator bit field in the respective Peripheral Channel m register (GCLK.PCHCTRLm.GEN)
- The Peripheral Channel number, *m*, is fixed for a given peripheral. See the Mapping table in the description of GCLK.PCHCTRLm.
- The AHB clocks are enabled and disabled by writing to the respective bit in the AHB Mask register (MCLK.AHBMASK).
- The APB clocks are enabled and disabled by writing to the respective bit in the APB x Mask registers (MCLK.APBxMASK).

17.2 Synchronous and Asynchronous Clocks

As the CPU and the peripherals can be in different clock domains, that is, they are clocked from different clock sources and with different clock speeds, some peripheral accesses by the CPU need to be synchronized. In this case the peripheral includes a Synchronization Busy (SYNCBUSY) register that can be used to check if a sync operation is in progress.

For a general description, see 17.3 Register Synchronization. Some peripherals have specific properties described in their individual “Synchronization” sub-sections.

22. PM – Power Manager

19.5.3 Clocks

The MCLK bus clock (CLK_MCLK_APB) can be enabled and disabled in the Main Clock module, and the default state of CLK_MCLK_APB can be found in the Peripheral Clock Masking section. If this clock is disabled, it can only be re-enabled by a reset.

The Generic Clock GCLK_MAIN or the DFLLULP Clock CLK_DFLLULP is required to generate the Main Clocks. GCLK_MAIN is configured in the Generic Clock Controller, and can be re-configured by the user if needed. CLK_DFLLULP is configured in the Oscillators Controller (OSCCTRL).

Related Links

18. GCLK - Generic Clock Controller

19.6.2.6 Peripheral Clock Masking

19.5.3.1 Main Clock

The main clock CLK_MAIN is the common source for the synchronous clocks. This is fed into the common 8-bit prescaler that is used to generate synchronous clocks to the CPU, AHBx, and APBx modules.

19.5.3.2 CPU Clock

The CPU clock (CLK_CPU) is routed to the CPU. Halting the CPU clock inhibits the CPU from executing instructions.

19.5.3.3 APBx and AHBx Clock

The APBx clocks (CLK_APBx) and the AHBx clocks (CLK_AHBx) are the root clock source used by modules requiring a clock on the APBx and the AHBx bus. These clocks are always synchronous to the CPU clock, and can run even when the CPU clock is turned off in sleep mode. A clock gater is inserted after the common APB clock to gate any APBx clock of a module on APBx bus, as well as the AHBx clock.

19.5.3.4 Clock Domains

The device has these synchronous clock domains:

- CPU synchronous clock domain (CPU Clock Domain). Frequency is f_{CPU}.

See also the related links for the clock domain partitioning.

Related Links

19.6.2.6 Peripheral Clock Masking

19.5.4 DMA

Not applicable.

19.5.5 Interrupts

The interrupt request line is connected to the Interrupt Controller. Using the MCLK interrupt requires the Interrupt Controller to be configured first.

19.5.6 Events

Not applicable.

19.8.4 Interrupt Flag Status and Clear

Name: INTFLAG
Offset: 0x03
Reset: 0x01
Property: –

Bit	7	6	5	4	3	2	1	0
								CKRDY
Access								R/W
Reset								1

Bit 0 – CKRDY Clock Ready
This flag is cleared by writing a '1' to the flag.

This flag is set when the synchronous CPU, APBx, and AHBx clocks have frequencies as indicated in the CLKCFG registers and will generate an interrupt if INTENCLR/SET.CKRDY is '1'.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit clears the Clock Ready interrupt flag.

20.8.7 Status

Name: STATUS
Offset: 0x0B
Reset: 0x00
Property: –

Bit	7	6	5	4	3	2	1	0
							OVF	BUSY
Access							R/W	R
Reset							0	0

Bit 1 – OVF Sticky Count Value Overflow
This bit is cleared by writing a '1' to it.

This bit is set when an overflow condition occurs to the value counter.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the OVF status.

Bit 0 – BUSY FREQM Status

Value	Description
0	No ongoing frequency measurement.
1	Frequency measurement is ongoing.

22.6.1.2.1 PDSW - Power Domain Switchable

PDSW is the switchable power domain. It contains the Event System, Generic Clock Controller, Main Clock Controller, Oscillator Controller, Non-Volatile Memory Controller, DMA Controller, the Device Service Unit, and the ARM core. PDSW also contains a number of peripherals that allow the device to wake up from an interrupt: SERCOM, Timer, ADC, DAC, OPAMP, CCL, PTC.

22.6.1.2.2 PDAO - Power Domain Always On

PDAO contains all controllers located in the always-on domain. It is powered when in Active, Idle, or Standby mode.

22.6.1.3 Sleep Modes

The device can be set in a sleep mode. In sleep mode, the CPU is stopped and the peripherals are either active or idle, according to the sleep mode depth:

- Idle sleep mode: The CPU is stopped. Synchronous clocks are stopped except when requested. The logic is retained.
- Standby sleep mode: The CPU is stopped as well as the peripherals. The logic is retained, and power domain gating can be used to reduce power consumption further.
- Off sleep mode: The entire device is powered off.

22.6.1.4 Power Domain States and Gating

In Standby sleep mode, the Power Domain Gating technique allows for selecting the state of PDSW power domain automatically (e.g. for executing sleepwalking tasks) or manually:

Active State	The power domain is powered according to the performance level
Retention State	The main voltage supply for the power domain is switched off, while maintaining a secondary low-power supply for sequential cells. The logic context is restored when waking up.

22.6.2 Principle of Operation

In active mode, all clock domains and power domains are active, allowing software execution and peripheral operation. The PM Sleep Mode Controller allows to save power by choosing between different sleep modes depending on application requirements, see 22.6.3.3 Sleep Mode Controller.

The PM Performance Level Controller allows to optimize either for low power consumption or high performance.

The PM Power Domain Controller allows to reduce the power consumption in standby mode even further.

22.6.3 Basic Operation

22.6.3.1 Initialization

After a Power-on Reset (POR), the PM is enabled, the device is in Active mode, the performance level is PL0 (the lowest power consumption) and all the power domains are in active state.

22.6.3.2 Enabling, Disabling and Resetting

The PM is always enabled and can not be reset.

22.6.3.3 Sleep Mode Controller

Sleep mode is entered by executing the Wait For Interrupt instruction (WFI). The Sleep Mode bits in the Sleep Configuration register (SLEEPCFG.SLEEPMODE) select the level of the sleep mode.

Note: A small latency happens between the store instruction and actual writing of the SLEEPCFG register due to bridges. Software must ensure that the SLEEPCFG register reads the desired value before issuing a WFI instruction.

26.8.6 Interrupt Flag Status and Clear

Name: INTFLAG
Offset: 0x06
Reset: 0x00
Property: N/A

Bit	7	6	5	4	3	2	1	0
								EW
Access								R/W
Reset								0

Bit 0 – EW Early Warning
This flag is cleared by writing a '1' to it.

This flag is set when an Early Warning interrupt occurs, as defined by the EWOFFSET bit group in EWCTRL.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit clears the Early Warning interrupt flag.

27.8.15 Tamper ID

Name: TAMPID
Offset: 0x68
Reset: 0x00000000

Bit	31	30	29	28	27	26	25	24
	TAMPEVT							
Access	R/W							
Reset	0							

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
					TAMPID3	TAMPID2	TAMPID1	TAMPID0
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit 31 – TAMPEVT Tamper Event Detected
Writing a '0' to this bit has no effect. Writing a '1' to this bit clears the tamper detection bit.

Value	Description
0	A tamper input event has not been detected
1	A tamper input event has been detected

Bits 0, 1, 2, 3 – TAMPID Tamper on Channel n Detected
Writing a '0' to this bit has no effect. Writing a '1' to this bit clears the tamper detection bit.

Value	Description
0	A tamper condition has not been detected on Channel n
1	A tamper condition has been detected on Channel n

27.12.17 Tamper Control B

Name: TAMPCTRLB
Offset: 0x6C
Reset: 0x00000000
Property: PAC Write-Protection, Enable-Protected

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
					ALSI3	ALSI2	ALSI1	ALSI0
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bits 0, 1, 2, 3 – ALSI Active Layer Internal Select n

Value	Description
0	Active layer Protection is monitoring the RTC signal using INn and OUTn tamper pins
1	Active layer Protection is monitoring the RTC signal on the TrustRAM shield

28.8.2 CRC Control

Name: CRCCTRL
Offset: 0x02
Reset: 0x0000
Property: PAC Write-Protection, Enable-Protected

Bit	15	14	13	12	11	10	9	8
			CRCSRC[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
					CRCPOLY[1:0]		CRCBEATSIZE[1:0]	
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bits 13:8 – CRCSRC[5:0] CRC Input Source
These bits select the input source for generating the CRC, as shown in the table below. The selected source is locked until either the CRC generation is completed or the CRC module is disabled. This means the CRCSRC cannot be modified when the CRC operation is ongoing. The lock is signaled by the CRCBUSY status bit. CRC generation complete is generated and signaled from the selected source when used with the DMA channel.

Value	Name	Description
0x00	NOACT	No action
0x01	IO	I/O interface
0x02-0x1F	-	Reserved
0x20	CHN	DMA channel 0
0x21	CHN	DMA channel 1
0x22	CHN	DMA channel 2
0x23	CHN	DMA channel 3
0x24	CHN	DMA channel 4
0x25	CHN	DMA channel 5
0x26	CHN	DMA channel 6
0x27	CHN	DMA channel 7
0x28	CHN	DMA channel 8
0x29	CHN	DMA channel 9
0x2A	CHN	DMA channel 10
0x2B	CHN	DMA channel 11
0x2C	CHN	DMA channel 12
0x2D	CHN	DMA channel 13
0x2E	CHN	DMA channel 14
0x2F	CHN	DMA channel 15
0x30	CHN	DMA channel 16
0x31	CHN	DMA channel 17
0x32	CHN	DMA channel 18

28.8.6 Debug Control

Name: DBGCTRL
Offset: 0x0D
Reset: 0x00
Property: PAC Write-Protection

Bit	7	6	5	4	3	2	1	0
								DBGRUN
Access								R/W
Reset								0

Bit 0 – DBGRUN Debug Run
This bit is not reset by a software reset.

This bit controls the functionality when the CPU is halted by an external debugger.

Value	Description
0	The DMAC is halted when the CPU is halted by an external debugger.
1	The DMAC continues normal operation when the CPU is halted by an external debugger.

28.10.2 Block Transfer Count

Name: BTCNT
Offset: 0x02
Property: -

The BTCNT register offset is relative to (BASEADDR or WRBADDR) + Channel Number * 0x10

Bit	15	14	13	12	11	10	9	8
	BTCNT[15:8]							
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	BTCNT[7:0]							
Access								
Reset								

Bits 15:0 – BTCNT[15:0] Block Transfer Count
This bit group holds the 16-bit block transfer count.

During a transfer, the internal counter value is decremented by one after each beat transfer. The internal counter is written to the corresponding write-back memory section for the DMA channel when the DMA channel loses priority, is suspended or gets disabled. The DMA channel can be disabled by a complete transfer, a transfer error or by software.

30.8.14 Security Control

Name: SECCTRL
Offset: 0x34
Reset: 'x' initially determined from NVM User Row after Reset
Property: PAC Write-Protection, Secure

Bit	31	30	29	28	27	26	25	24
	KEY[7:0]							
Access	W/-/W	W/-/W	W/-/W	W/-/W	W/-/W	W/-/W	W/-/W	W/-/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
						TEROW[2:0]		
Access						RW/-/RW	RW/-/RW	RW/-/RW
Reset						0	0	0

Bit	7	6	5	4	3	2	1	0
		DXN			DSCEN	SILACC		TAMPEEN
Access		R/-/R			RW/-/RW	RW/-/RW		RW/-/RW
Reset		x			0	0		0

Bits 31:24 – KEY[7:0] Write Key
When this bit group is written to the key value 0xA5, the write will be performed. If a value different from the key value is tried, the write will be discarded and INTFLAG.KEYE set.

Bits 10:8 – TEROW[2:0] Tamper Erase Row
Row address of the row in data space to be erased on RTC tamper event.

Bit 6 – DXN Data eXecute Never
This bit field is only available for SAM L11 and has no effect for SAM L10.

Value	Description
0	Execution out of Data Flash is authorized.
1	Execution out of Data Flash is not authorized.

Bit 3 – DSCEN Data Scramble Enable

Important: This bitfield is only available for **SAM L11** and has no effect for **SAM L10**.

36.8.6 Interrupt Flag Status and Clear

Name: INTFLAG
Offset: 0x18
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
	ERROR				SSL	RXC	TXC	DRE
Access	R/W				R/W	R	R/W	R
Reset	0				0	0	0	0

Bit 7 – ERROR Error
This flag is cleared by writing '1' to it.

This bit is set when any error is detected. Errors that will set this flag have corresponding status flags in the STATUS register. The BUFOVF error will set this interrupt flag.

Writing '0' to this bit has no effect.

Writing '1' to this bit will clear the flag.

Bit 3 – SSL Slave Select Low
This flag is cleared by writing '1' to it.

This bit is set when a high to low transition is detected on the _SS pin in slave mode and Slave Select Low Detect (CTRLB.SSDE) is enabled.

Writing '0' to this bit has no effect.

Writing '1' to this bit will clear the flag.

Bit 2 – RXC Receive Complete
This flag is cleared by reading the Data (DATA) register or by disabling the receiver.

This flag is set when there are unread data in the receive buffer. If address matching is enabled, the first data received in a transaction will be an address.

Writing '0' to this bit has no effect.

Writing '1' to this bit has no effect.

Bit 1 – TXC Transmit Complete
This flag is cleared by writing '1' to it or by writing new data to DATA.

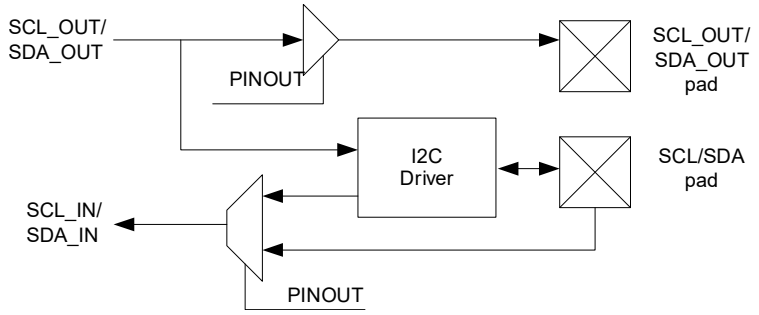
In master mode, this flag is set when the data have been shifted out and there are no new data in DATA.

In slave mode, this flag is set when the _SS pin is pulled high. If address matching is enabled, this flag is only set if the transaction was initiated with an address match.

Writing '0' to this bit has no effect.

Writing '1' to this bit will clear the flag.

Figure 37-14. I²C Pad Interface



37.6.3.4 Quick Command

Setting the Quick Command Enable bit in the Control B register (CTRLB.QCEN) enables quick command. When quick command is enabled, the corresponding interrupt flag (INTFLAG.SB or INTFLAG.MB) is set immediately after the slave acknowledges the address. At this point, the software can either issue a stop command or a repeated start by writing CTRLB.CMD or ADDR.ADDR.

37.6.4 DMA, Interrupts and Events

Each interrupt source has its own interrupt flag. The interrupt flag in the Interrupt Flag Status and Clear register (INTFLAG) will be set when the interrupt condition is meet. Each interrupt can be individually enabled by writing '1' to the corresponding bit in the Interrupt Enable Set register (INTENSET), and disabled by writing '1' to the corresponding bit in the Interrupt Enable Clear register (INTENCLR). An interrupt request is generated when the interrupt flag is set and the corresponding interrupt is enabled. The interrupt request is active until the interrupt flag is cleared, the interrupt is disabled or the I²C is reset. See the 37.8.5 INTFLAG (Slave) or 37.10.6 INTFLAG (Master) register for details on how to clear interrupt flags.

Table 37-1. Module Request for SERCOM I²C Slave

Condition	Request		
	DMA	Interrupt	Event
Data needed for transmit (TX) (Slave transmit mode)	Yes (request cleared when data is written)		NA
Data received (RX) (Slave receive mode)	Yes (request cleared when data is read)		
Data Ready (DRDY)		Yes	
Address Match (AMATCH)		Yes	
Stop received (PREC)		Yes	
Error (ERROR)		Yes	

Value	Name	Description
0x0	OFF	Event action disabled
0x1	RETRIGGER	Start, restart or retrigger TC on event
0x2	COUNT	Count on event
0x3	START	Start TC on event
0x4	STAMP	Time stamp capture
0x5	PPW	Period captured in CC0, pulse width in CC1
0x6	PWP	Period captured in CC1, pulse width in CC0
0x7	PW	Pulse width capture

43.8.7 Status

Name: STATUS
Offset: 0x07
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
								READY
Access								R
Reset								0

Bit 0 – READY DAC Ready

Value	Description
0	DAC is not ready for conversion.
1	Startup time has elapsed, DAC is ready for conversion.

Abbreviation	Description
GPIO	General Purpose Input/Output
I^2C	Inter-Integrated Circuit
IF	Interrupt Flag
INT	Interrupt
MBIST	Memory Built-In Self-Test
MEM-AP	Memory Access Port
MTB	Micro Trace Buffer
NMI	Non-maskable Interrupt
NVIC	Nested Vector Interrupt Controller
NVM	Nonvolatile Memory
NVMCTRL	Nonvolatile Memory Controller
OPAMP	Operation Amplifier
OSC	Oscillator
PAC	Peripheral Access Controller
PC	Program Counter
PER	Period
PM	Power Manager
POR	Power-on Reset
PORT	I/O Pin Controller
PTC	Peripheral Touch Controller
PWM	Pulse-Width Modulation
RAM	Random-Access Memory
REF	Reference
RTC	Real-Time Counter
RX	Receiver/Receive
SEEP	SmartEEPROM Page
SERCOM	Serial Communication Interface
SMBus	System Management Bus
SP	Stack Pointer
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
SUPC	Supply Controller