What is "Embedded - Microcontrollers"?

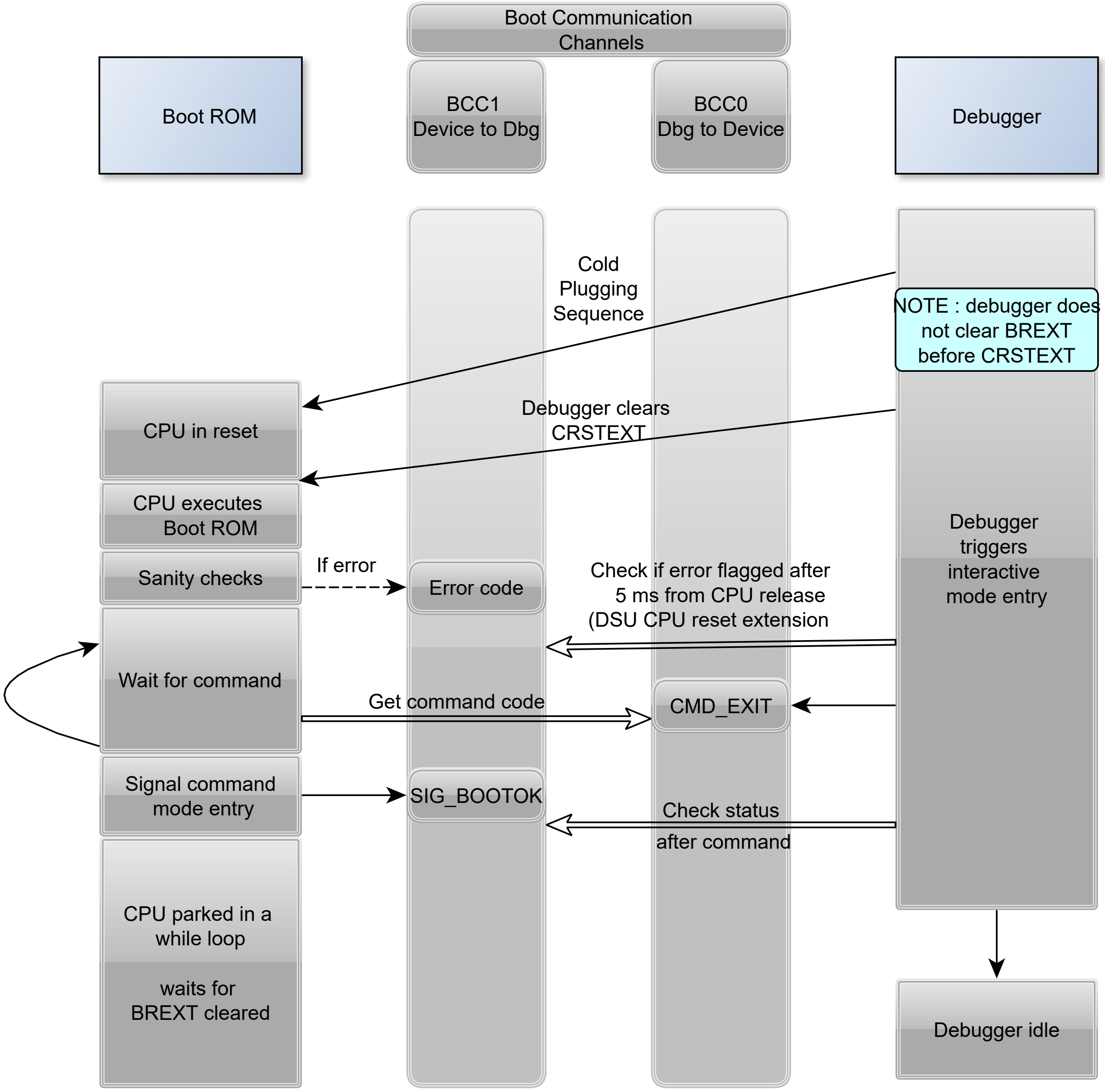
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M23
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	25
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.63V
Data Converters	A/D 10x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VFQFN Exposed Pad
Supplier Device Package	32-VQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsaml10e16a-mut

Pin				Pin Name	Supply	A	B[1]						C[2][3]	D[2][3]	E	G	H	I	Reset State
SSOP24	VQFN24	WLCSP32	TQFP32 / VQFN32			EIC	REF	ADC	AC	PTC	DAC	OPAMP	SERCOM	SERCOM ALTERNATIVE	TC	RTC/ Debug	AC/ GCLK	CCL	
		C4	7	PA06	VDDANA	EXTINT[6]		AIN[4]	AIN[2]	XY[5]		OA0POS		SERCOM0/PAD[2]	TC1/WO[0]			IN[2]	I/O, Hi-Z
		B5	8	PA07	VDDANA	EXTINT[7]		AIN[5]	AIN[3]			OA0OUT		SERCOM0/PAD[3]	TC1/WO[1]			OUT[0]	I/O, Hi-Z
11	8	B6	9	VDDANA															-
12	9	C6	10	GNDANA															-
13	10	D4	11	PA08	VDDIO	NMI		AIN[6]		XY[6]			SERCOM1/PAD[0]	SERCOM2/PAD[0]		RTC/IN[0]		IN[3]	I/O, Hi-Z
		D6	12	PA09	VDDIO	EXTINT[0]		AIN[7]		XY[7]			SERCOM1/PAD[1]	SERCOM2/PAD[1]		RTC/IN[1]		IN[4]	I/O, Hi-Z
		C5	13	PA10	VDDIO	EXTINT[1]		AIN[8]		XY[8]			SERCOM1/PAD[2]	SERCOM2/PAD[2]			GCLK_IO[4]	IN[5]	I/O, Hi-Z
		D5	14	PA11	VDDIO	EXTINT[2]		AIN[9]		XY[9]			SERCOM1/PAD[3]	SERCOM2/PAD[3]			GCLK_IO[3]	OUT[1]	I/O, Hi-Z
14	11	E6	15	PA14 / XOSC	VDDIO	EXTINT[3]				XY[10]			SERCOM2/PAD[2]	SERCOM0/PAD[2]	TC0/WO[0]		GCLK_IO[0]		I/O, Hi-Z
15	12	E5	16	PA15 / XOUT	VDDIO	EXTINT[4]				XY[11]			SERCOM2/PAD[3]	SERCOM0/PAD[3]	TC0/WO[1]		GCLK_IO[1]		I/O, Hi-Z
16	13	D3	17	PA16[4]	VDDIO	EXTINT[5]				XY[12]			SERCOM1/PAD[0]	SERCOM0/PAD[0]		RTC/IN[2]	GCLK_IO[2]	IN[0]	I/O, Hi-Z
17	14	F5	18	PA17[4]	VDDIO	EXTINT[6]				XY[13]			SERCOM1/PAD[1]	SERCOM0/PAD[1]		RTC/IN[3]	GCLK_IO[3]	IN[1]	I/O, Hi-Z
18	15	E4	19	PA18	VDDIO	EXTINT[7]				XY[14]			SERCOM1/PAD[2]	SERCOM0/PAD[2]	TC2/WO[0]	RTC/OUT[0]	AC/CMP[0]	IN[2]	I/O, Hi-Z
19	16	E3	20	PA19	VDDIO	EXTINT[0]				XY[15]			SERCOM1/PAD[3]	SERCOM0/PAD[3]	TC2/WO[1]	RTC/OUT[1]	AC/CMP[1]	OUT[0]	I/O, Hi-Z
20	17	F4	21	PA22[4]	VDDIO	EXTINT[1]				XY[16]			SERCOM0/PAD[0]	SERCOM2/PAD[0]	TC0/WO[0]	RTC/OUT[2]	GCLK_IO[2]		I/O, Hi-Z
21	18	F3	22	PA23[4]	VDDIO	EXTINT[2]				XY[17]			SERCOM0/PAD[1]	SERCOM2/PAD[1]	TC0/WO[1]	RTC/OUT[3]	GCLK_IO[1]		I/O, Hi-Z
		F2	23	PA24	VDDIO	EXTINT[3]							SERCOM0/PAD[2]	SERCOM2/PAD[2]	TC1/WO[0]				I/O, Hi-Z
		E2	24	PA25	VDDIO	EXTINT[4]							SERCOM0/PAD[3]	SERCOM2/PAD[3]	TC1/WO[1]				I/O, Hi-Z
		D2	25	PA27	VDDIO	EXTINT[5]											GCLK_IO[0]		I/O, Hi-Z
22	19	C2	26	$\overline{\text{RESET}}$	VDDIO														I, PU
23	20	E1	27	VDDCORE															-
24	21	D1	28	GND															-
1	22	C1	29	VDDOUT															-
2	23	B1	30	VDDIO															-

Figure 14-9. CMD_EXIT to Park mode flow diagram


Boot Communication Channels
Boot ROM
BCC1 Device to Dbg
BCC0 Dbg to Device
Debugger
Cold Plugging Sequence
NOTE : debugger does not clear BREXT before CRSTEXT
CPU in reset
Debugger clears CRSTEXT
CPU executes Boot ROM
Sanity checks
If error
Error code
Check if error flagged after 5 ms from CPU release (DSU CPU reset extension
Debugger triggers interactive mode entry
Wait for command
Get command code
CMD_EXIT
Signal command mode entry
SIG_BOOTOK
Check status after command
CPU parked in a while loop
waits for BREXT cleared
Debugger idle

14.4.5.3 System Reset Request (CMD_RESET)

This command allows resetting the system using a system reset request. Since the reset is executed immediately after receiving the command, no reply is sent to the debugger.

After reset, the CPU executes the Boot ROM code from the beginning

14.4.5.4 Chip Erase (CMD_CHIPERASE) - SAM L10 only

CMD_CHIPERASE command erases the entire device except BOOT area, and reverts to Debug Access Level 2.

15.6 Register Summary

Important:
For **SAM L11**, the PAC register map is automatically duplicated in a Secure and Non-Secure alias:

- The Non-Secure alias is at the peripheral base address
- The Secure alias is located at the peripheral base address + 0x200

Refer to *Mix-Secure Peripherals* for more information on register access rights

Offset	Name	Bit Pos.								
0x00	WRCTRL	7:0	PERID[7:0]							
		15:8	PERID[15:8]							
		23:16	KEY[7:0]							
		31:24								
0x04	EVCTRL	7:0								ERREO
0x05 ... 0x07	Reserved									
0x08	INTENCLR	7:0								ERR
0x09	INTENSET	7:0								ERR
0x0A ... 0x0F	Reserved									
0x10	INTFLAGAHB	7:0	BROM	HSRAMDSU	HSRAMDMAC	HSRAMCPU	HPB2	HPB1	HPB0	FLASH
		15:8								
		23:16								
		31:24								
0x14	INTFLAGA	7:0	GCLK	SUPC	OSC32KCTRL	OSCCTRL	RSTC	MCLK	PM	PAC
		15:8			AC	PORT	FREQM	EIC	RTC	WDT
		23:16								
		31:24								
0x18	INTFLAGB	7:0				Reserved	DMAC	NVMCTRL	DSU	IDAU
		15:8								
		23:16								
		31:24								
0x1C	INTFLAGC	7:0	ADC	TC2	TC1	TC0	SERCOM2	SERCOM1	SERCOM0	EVSYS
		15:8			TRAM	OPAMP	CCL	TRNG	PTC	DAC
		23:16								
		31:24								
0x20 ... 0x33	Reserved									

16.12.10 Configuration

Name: CFG
Offset: 0x001C
Reset: 0x0000000
Property: PAC Write-Protection

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
Access								
Reset								
Bit	7	6	5	4	3	2	1	0
					DCCDMALEVEL[1:0]		LQOS[1:0]	
Access					RW	RW	RW	RW
Reset					0	0	0	2

Bits 3:2 – DCCDMALEVEL[1:0] DMA TriggerLevel
0x0X: DCC1 trigger is the image of STATUSB.DCC1D, this signals to the DMA that a data is available for read, this is the correct configuration for a channel that reads DCC1.

0x1X: DCC1 trigger is the image of STATUSB.DCC1D inverted, this signals to the DMA that DCC1 is ready for write, this is the correct configuration for a channel that writes DCC1

0xX0: DCC0 trigger is the image of STATUSB.DCC0D, this signals to the DMA that a data is available for read, this is the correct configuration for a channel that reads DCC0.

0xX1: DCC0 trigger is the image of STATUSB.DCC0D inverted, this signals to the DMA that DCC0 is ready for write, this is the correct configuration for a channel that writes DCC0

Bits 1:0 – LQOS[1:0] Latency Quality Of Service
Defines the latency quality of service required when accessing the RAM:

0: Background Transfers

1: Bandwidth Sensitive

2: Latency sensitive

3: Latency critical

20.5.2 Power Management

The FREQM will continue to operate in idle sleep mode where the selected source clock is running. The FREQM's interrupts can be used to wake up the device from idle sleep mode. Refer to the Power Manager chapter for details on the different sleep modes.

Related Links

22. PM – Power Manager

20.5.3 Clocks

The clock for the FREQM bus interface (CLK_APB_FREQM) is enabled and disabled by the Main Clock Controller, the default state of CLK_APB_FREQM can be found in Peripheral Clock Masking.

Two generic clocks are used by the FREQM: Reference Clock (GCLK_FREQM_REF) and Measurement Clock (GCLK_FREQM_MSR).

GCLK_FREQM_REF is required to clock the internal reference timer, which acts as the frequency reference.

GCLK_FREQM_MSR is required to clock a ripple counter for frequency measurement. These clocks must be configured and enabled in the generic clock controller before using the FREQM.

Related Links

19. MCLK – Main Clock

19.6.2.6 Peripheral Clock Masking

18. GCLK - Generic Clock Controller

20.5.4 DMA

Not applicable.

20.5.5 Interrupts

The interrupt request line is connected to the interrupt controller. Using FREQM interrupt requires the interrupt controller to be configured first.

20.5.6 Events

Not applicable

20.5.7 Debug Operation

When the CPU is halted in debug mode the FREQM continues its normal operation. The FREQM cannot be halted when the CPU is halted in debug mode. If the FREQM is configured in a way that requires it to be periodically serviced by the CPU, improper operation or data loss may result during debugging.

20.5.8 Register Access Protection

All registers with write-access can be write-protected optionally by the Peripheral Access Controller (PAC), except the following registers:

- Control B register (CTRLB)
- Interrupt Flag Status and Clear register (INTFLAG)
- Status register (STATUS)

Optional write-protection by the Peripheral Access Controller (PAC) is denoted by the "PAC Write-Protection" property in each individual register description.

Write-protection does not apply to accesses through an external debugger.

23.8.15 DPLL Control A

Name: DPLLCTRLA
Offset: 0x2C
Reset: 0x80
Property: PAC Write-Protection

Bit	7	6	5	4	3	2	1	0
	ONDEMAND	RUNSTDBY					ENABLE	
Access	R/W	R/W					R/W	
Reset	1	0					0	

Bit 7 – ONDEMAND On Demand Clock Activation
The On Demand operation mode allows the DPLL to be enabled or disabled depending on peripheral clock requests.

If the ONDEMAND bit has been previously written to '1', the DPLL will only be running when requested by a peripheral. If there is no peripheral requesting the DPLL's clock source, the DPLL will be in a disabled state.

If On Demand is disabled the DPLL will always be running when enabled.

In standby sleep mode, the On Demand operation is still active.

Value	Description
0	The DPLL is always on, if enabled.
1	The DPLL is enabled when a peripheral is requesting the DPLL to be used as a clock source. The DPLL is disabled if no peripheral is requesting the clock source.

Bit 6 – RUNSTDBY Run in Standby
This bit controls how the DPLL behaves during standby sleep mode:

Value	Description
0	The DPLL is disabled in standby sleep mode if no peripheral requests the clock.
1	The DPLL is not stopped in standby sleep mode. If ONDEMAND=1, the DPLL will be running when a peripheral is requesting the clock. If ONDEMAND=0, the clock source will always be running in standby sleep mode.

Bit 1 – ENABLE DPLL Enable, Write-Synchronized (ENABLE)
The software operation of enabling or disabling the DPLL takes a few clock cycles, so the DPLLSYNCBUSY.ENABLE status bit indicates when the DPLL is successfully enabled or disabled.

Value	Description
0	The DPLL is disabled.
1	The DPLL is enabled.

Offset	Name	Bit Pos.								
		31:24	GP[31:24]							
0x44	GP1	7:0	GP[7:0]							
		15:8	GP[15:8]							
		23:16	GP[23:16]							
		31:24	GP[31:24]							
0x48 ... 0x5F	Reserved									
0x60	TAMPCTRL	7:0	IN3ACT[1:0]		IN2ACT[1:0]		IN1ACT[1:0]		IN0ACT[1:0]	
		15:8								
		23:16					TAMLVL3	TAMLVL2	TAMLVL1	TAMLVL0
		31:24					DEBNC3	DEBNC2	DEBNC1	DEBNC0
0x64	TIMESTAMP	7:0	COUNT[7:0]							
		15:8	COUNT[15:8]							
		23:16								
		31:24								
0x68	TAMPID	7:0					TAMPID3	TAMPID2	TAMPID1	TAMPID0
		15:8								
		23:16								
		31:24	TAMPEVT							
0x6C	TAMPCTRLB	7:0					ALSI3	ALSI2	ALSI1	ALSI0
		15:8								
		23:16								
		31:24								

27.10 Register Description - Mode 1 - 16-Bit Counter

This Register Description section is valid if the RTC is in COUNT16 mode (CTRLA.MODE=1).

Registers can be 8, 16, or 32 bits wide. Atomic 8-, 16-, and 32-bit accesses are supported. In addition, the 8-bit quarters and 16-bit halves of a 32-bit register, and the 8-bit halves of a 16-bit register can be accessed directly.

Some registers require synchronization when read and/or written. Synchronization is denoted by the "Read-Synchronized" and/or "Write-Synchronized" property in each individual register description.

Optional write-protection by the Peripheral Access Controller (PAC) is denoted by the "PAC Write-Protection" property in each individual register description.

Some registers are enable-protected, meaning they can only be written when the module is disabled. Enable-protection is denoted by the "Enable-Protected" property in each individual register description.

On **SAM L11** devices, this peripheral has different access permissions depending on PAC Security Attribution (Secure or Non-Secure):

- If the peripheral is configured as Non-Secure in the PAC:
  - Secure access and Non-Secure access are granted
- If the peripheral is configured as Secure in the PAC:
  - Secure access is granted
  - Non-Secure access is discarded (Write is ignored, read 0x0) and a PAC error is triggered

27.12.2 Control B in Clock/Calendar mode (CTRLA.MODE=2)

Name: CTRLB
Offset: 0x2
Reset: 0x0000
Property: PAC Write-Protection, Enable-Protected

Bit	15	14	13	12	11	10	9	8
	SEPTO	ACTF[2:0]				DEBF[2:0]		
Access	R/W	R/W	R/W	R/W		R/W	R/W	R/W
Reset	0	0	0	0		0	0	0

Bit	7	6	5	4	3	2	1	0
	DMAEN	RTCOUT	DEBASYNC	DEBMAJ				GP0EN
Access	R/W	R/W	R/W	R/W				R/W
Reset	0	0	0	0				0

Bit 15 – SEPTO Separate Tamper Outputs

Value	Description
0	IN[n] is compared tp OUT[0] (backward-compatible).
1	IN[n] is compared tp OUT[n].

Bits 14:12 – ACTF[2:0] Active Layer Frequency
These bits define the prescaling factor for the RTC clock output (OUT) used during active layer protection in terms of the CLK_RTC.

Value	Name	Description
0x0	DIV2	CLK_RTC_OUT = CLK_RTC / 2
0x1	DIV4	CLK_RTC_OUT = CLK_RTC / 4
0x2	DIV8	CLK_RTC_OUT = CLK_RTC / 8
0x3	DIV16	CLK_RTC_OUT = CLK_RTC / 16
0x4	DIV32	CLK_RTC_OUT = CLK_RTC / 32
0x5	DIV64	CLK_RTC_OUT = CLK_RTC / 64
0x6	DIV128	CLK_RTC_OUT = CLK_RTC / 128
0x7	DIV256	CLK_RTC_OUT = CLK_RTC / 256

Bits 10:8 – DEBF[2:0] Debounce Frequency
These bits define the prescaling factor for the input debouncers in terms of the CLK_RTC.

Value	Name	Description
0x0	DIV2	CLK_RTC_DEB = CLK_RTC / 2
0x1	DIV4	CLK_RTC_DEB = CLK_RTC / 4
0x2	DIV8	CLK_RTC_DEB = CLK_RTC / 8
0x3	DIV16	CLK_RTC_DEB = CLK_RTC / 16
0x4	DIV32	CLK_RTC_DEB = CLK_RTC / 32
0x5	DIV64	CLK_RTC_DEB = CLK_RTC / 64
0x6	DIV128	CLK_RTC_DEB = CLK_RTC / 128
0x7	DIV256	CLK_RTC_DEB = CLK_RTC / 256

Offset	Name	Bit Pos.								
		31:24								
0x30	ACTIVE	7:0					LVLEXx	LVLEXx	LVLEXx	LVLEXx
		15:8	ABUSY			ID[4:0]				
		23:16	BTCNT[7:0]							
		31:24	BTCNT[15:8]							
0x34	BASEADDR	7:0	BASEADDR[7:0]							
		15:8			BASEADDR[13:8]					
		23:16								
		31:24								
0x38	WRBADDR	7:0	WRBADDR[7:0]							
		15:8			WRBADDR[13:8]					
		23:16								
		31:24								
0x3C ... 0x3E	Reserved									
0x3F	CHID	7:0					ID[3:0]			
0x40	CHCTRLA	7:0		RUNSTDBY					ENABLE	SWRST
0x41 ... 0x43	Reserved									
0x44	CHCTRLB	7:0		LVL[1:0]		EVOE	EVIE	EVACT[2:0]		
		15:8				TRIGSRC[4:0]				
		23:16	TRIGACT[1:0]							
		31:24							CMD[1:0]	
0x48 ... 0x4B	Reserved									
0x4C	CHINTENCLR	7:0						SUSP	TCMPL	TERR
0x4D	CHINTENSET	7:0						SUSP	TCMPL	TERR
0x4E	CHINTFLAG	7:0						SUSP	TCMPL	TERR
0x4F	CHSTATUS	7:0						FERR	BUSY	PEND

28.8 Register Description

Registers can be 8, 16, or 32 bits wide. Atomic 8-, 16- and 32-bit accesses are supported. In addition, the 8-bit quarters and 16-bit halves of a 32-bit register, and the 8-bit halves of a 16-bit register can be accessed directly.

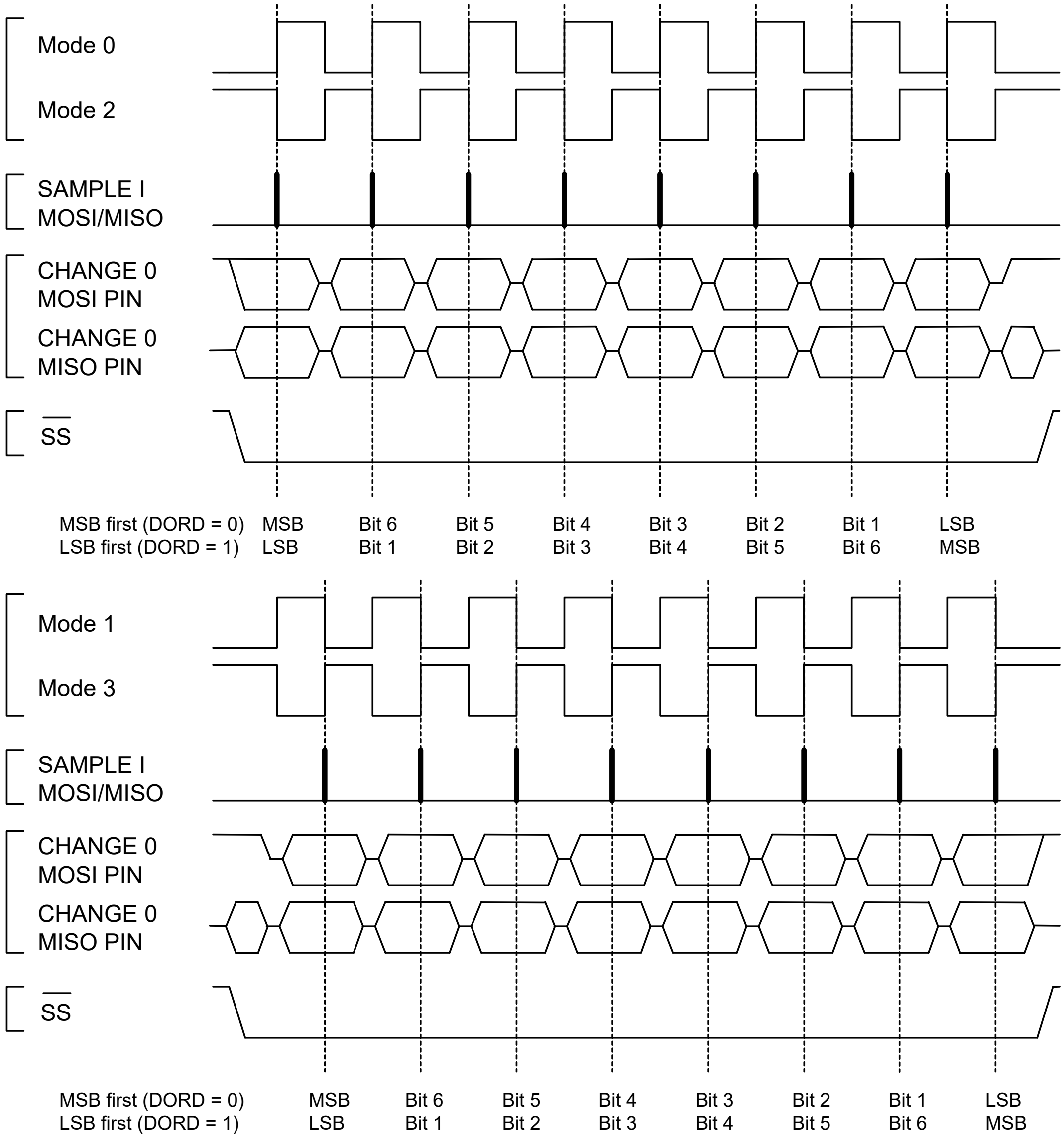
Some registers are optionally write-protected by the Peripheral Access Controller (PAC). Optional PAC write-protection is denoted by the "PAC Write-Protection" property in each individual register description. For details, refer to 28.5.8 Register Access Protection.

Some registers are enable-protected, meaning they can only be written when the peripheral is disabled. Enable-protection is denoted by the "Enable-Protected" property in each individual register description.

On **SAM L11** devices, this peripheral has different access permissions depending on PAC Security Attribution (Secure or Non-Secure):

Offset	Name	Bit Pos.								
		23:16	DATA[23:16]							
		31:24	DATA[31:24]							
0x0118	RAM6	7:0	DATA[7:0]							
		15:8	DATA[15:8]							
		23:16	DATA[23:16]							
		31:24	DATA[31:24]							
0x011C	RAM7	7:0	DATA[7:0]							
		15:8	DATA[15:8]							
		23:16	DATA[23:16]							
		31:24	DATA[31:24]							
0x0120	RAM8	7:0	DATA[7:0]							
		15:8	DATA[15:8]							
		23:16	DATA[23:16]							
		31:24	DATA[31:24]							
0x0124	RAM9	7:0	DATA[7:0]							
		15:8	DATA[15:8]							
		23:16	DATA[23:16]							
		31:24	DATA[31:24]							
0x0128	RAM10	7:0	DATA[7:0]							
		15:8	DATA[15:8]							
		23:16	DATA[23:16]							
		31:24	DATA[31:24]							
0x012C	RAM11	7:0	DATA[7:0]							
		15:8	DATA[15:8]							
		23:16	DATA[23:16]							
		31:24	DATA[31:24]							
0x0130	RAM12	7:0	DATA[7:0]							
		15:8	DATA[15:8]							
		23:16	DATA[23:16]							
		31:24	DATA[31:24]							
0x0134	RAM13	7:0	DATA[7:0]							
		15:8	DATA[15:8]							
		23:16	DATA[23:16]							
		31:24	DATA[31:24]							
0x0138	RAM14	7:0	DATA[7:0]							
		15:8	DATA[15:8]							
		23:16	DATA[23:16]							
		31:24	DATA[31:24]							
0x013C	RAM15	7:0	DATA[7:0]							
		15:8	DATA[15:8]							
		23:16	DATA[23:16]							
		31:24	DATA[31:24]							
0x0140	RAM16	7:0	DATA[7:0]							
		15:8	DATA[15:8]							
		23:16	DATA[23:16]							
		31:24	DATA[31:24]							

Figure 36-3. SPI Transfer Modes


Mode 0
Mode 2
SAMPLE I
MOSI/MISO
CHANGE 0
MOSI PIN
CHANGE 0
MISO PIN
SS
MSB first (DORD = 0) MSB Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 Bit 1 LSB
LSB first (DORD = 1) LSB Bit 1 Bit 2 Bit 3 Bit 4 Bit 5 Bit 6 MSB
Mode 1
Mode 3
SAMPLE I
MOSI/MISO
CHANGE 0
MOSI PIN
CHANGE 0
MISO PIN
SS
MSB first (DORD = 0) MSB Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 Bit 1 LSB
LSB first (DORD = 1) LSB Bit 1 Bit 2 Bit 3 Bit 4 Bit 5 Bit 6 MSB

36.6.2.6 Transferring Data

36.6.2.6.1 Master

In master mode (CTRLA.MODE=0x3), when Master Slave Enable Select (CTRLB.MSSEN) is ‘1’, hardware will control the $\overline{\text{SS}}$ line.

When Master Slave Select Enable (CTRLB.MSSEN) is '0', the $\overline{\text{SS}}$ line must be configured as an output. $\overline{\text{SS}}$ can be assigned to any general purpose I/O pin. When the SPI is ready for a data transaction, software must pull the $\overline{\text{SS}}$ line low.

When writing a character to the Data register (DATA), the character will be transferred to the shift register. Once the content of TxDATA has been transferred to the shift register, the Data Register Empty flag in the Interrupt Flag Status and Clear register (INTFLAG.DRE) will be set. And a new character can be written to DATA.

Each time one character is shifted out from the master, another character will be shifted in from the slave simultaneously. If the receiver is enabled (CTRLA.RXEN=1), the contents of the shift register will be

36.8.3 Baud Rate

Name: BAUD
Offset: 0x0C
Reset: 0x00
Property: PAC Write-Protection, Enable-Protected

Bit	7	6	5	4	3	2	1	0
	BAUD[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – BAUD[7:0] Baud Register
These bits control the clock generation, as described in the *SERCOM Clock Generation – Baud-Rate Generator*.

Related Links

34.6.2.3 Clock Generation – Baud-Rate Generator

34.6.2.3.1 Asynchronous Arithmetic Mode BAUD Value Selection

Bit 0 – DRE Data Register Empty Interrupt Enable
Writing '0' to this bit has no effect.

Writing '1' to this bit will set the Data Register Empty Interrupt Enable bit, which enables the Data Register Empty interrupt.

Value	Description
0	Data Register Empty interrupt is disabled.
1	Data Register Empty interrupt is enabled.

36.8.10 Data

Name: DATA
Offset: 0x28
Reset: 0x0000
Property: –

Bit	15	14	13	12	11	10	9	8
								DATA[8:8]
Access								R/W
Reset								0

Bit	7	6	5	4	3	2	1	0
	DATA[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 8:0 – DATA[8:0] Data
Reading these bits will return the contents of the receive data buffer. The register should be read only when the Receive Complete Interrupt Flag bit in the Interrupt Flag Status and Clear register (INTFLAG.RXC) is set.

Writing these bits will write the transmit data buffer. This register should be written only when the Data Register Empty Interrupt Flag bit in the Interrupt Flag Status and Clear register (INTFLAG.DRE) is set.

38.7.1.14 Period Value, 8-bit Mode

Name: PER
Offset: 0x1B
Reset: 0xFF
Property: Write-Synchronized

Bit	7	6	5	4	3	2	1	0
	PER[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	1

Bits 7:0 – PER[7:0] Period Value
These bits hold the value of the Period Buffer register PERBUF. The value is copied to PER register on UPDATE condition.

This bit has no effect when input capture operation is enabled.

Value	Description
0	The CCBUFx and PERBUF buffer registers value are copied into CCx and PER registers on hardware update condition.
1	The CCBUFx and PERBUF buffer registers value are not copied into CCx and PER registers on hardware update condition.

Bit 0 – DIR Counter Direction
This bit is used to change the direction of the counter.

Writing a '0' to this bit has no effect

Writing a '1' to this bit will clear the bit and make the counter count up.

Value	Description
0	The timer/counter is counting up (incrementing).
1	The timer/counter is counting down (decrementing).

42.8.13 Synchronization Busy

Name: SYNCBUSY
Offset: 0x20
Reset: 0x00000000
Property: Read-Only

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
				COMPCTRLx	COMPCTRLx	WINCTRL	ENABLE	SWRST
Access				R	R	R	R	R
Reset				0	0	0	0	0

Bits 4,3 – COMPCTRLx COMPCTRLx Synchronization Busy
This bit is cleared when the synchronization of the COMPCTRLx register between the clock domains is complete.

This bit is set when the synchronization of the COMPCTRLx register between clock domains is started.

Bit 2 – WINCTRL WINCTRL Synchronization Busy
This bit is cleared when the synchronization of the WINCTRL register between the clock domains is complete.

This bit is set when the synchronization of the WINCTRL register between clock domains is started.

Bit 1 – ENABLE Enable Synchronization Busy
This bit is cleared when the synchronization of the CTRLA.ENABLE bit between the clock domains is complete.

This bit is set when the synchronization of the CTRLA.ENABLE bit between clock domains is started.

Bit 0 – SWRST Software Reset Synchronization Busy
This bit is cleared when the synchronization of the CTRLA.SWRST bit between the clock domains is complete.

This bit is set when the synchronization of the CTRLA.SWRST bit between clock domains is started.

44. OPAMP – Operational Amplifier Controller

44.1 Overview

The Operational Amplifier (OPAMP) Controller configures and controls three low power, general purpose operational amplifiers offering a high degree of flexibility and rail-to-rail inputs.

Most common inverting or non-inverting programmable gain and hysteresis configurations can be selected by software - no external components are required for these configurations.

The OPAMPs can be cascaded for both standalone mode and built-in configurations.

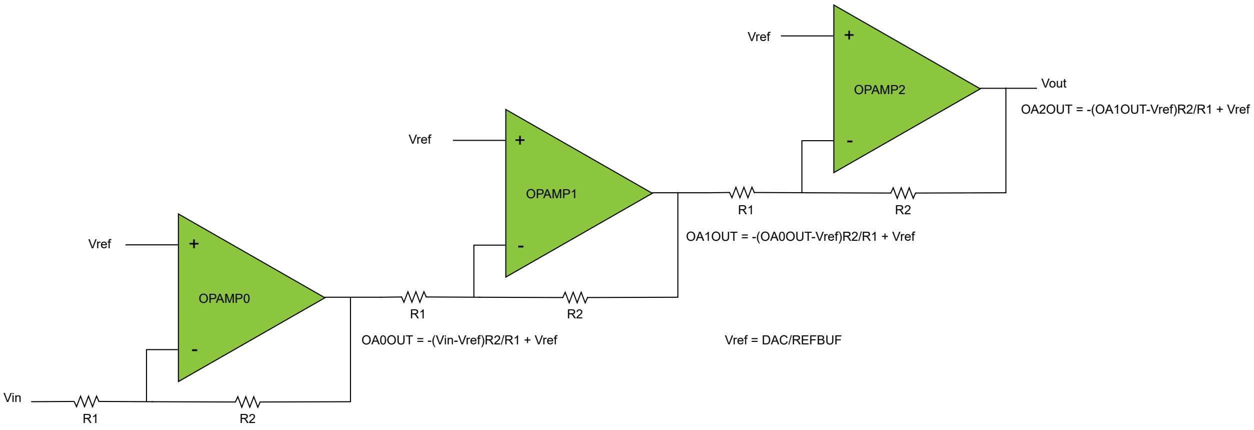
Each OPAMP can be used as a standalone amplifier. External pins are available for filter configurations or other applications. A reference can be generated from the DAC to be used as selectable reference for inverting PGA (programmable gain amplifier) or instrumentation amplifier. Each OPAMP can be used as buffer or PGA for the ADC or an AC. The OPAMP offset voltage can be compensated when it is used in combination with the ADC.

Four modes are available to select the trade-off between speed and power consumption to best fit the application requirements and optimize the power consumption.

44.2 Features

- Three individually configurable low power OPAMPs
- Rail-to-rail inputs
- Configurable resistor ladders for internal feedback
- Selectable configurations
  - Standalone OPAMP with flexible inputs
  - Unity gain amplifier
  - Non-inverting / inverting Programmable Gain Amplifier (PGA)
  - Cascaded PGAs
  - Instrumentation amplifier
  - Comparator with programmable hysteresis
- OPAMP output:
  - On I/O pins
  - As input for AC or ADC
- Flexible input selection:
  - I/O pins
  - DAC
  - Ground
- Low power options:
  - Selectable voltage doubler and propagation delay versus current consumption
  - On demand start-up for ADC and AC operations
- Offset/Gain measurement for calibration when used with the ADC

Figure 44-5. Cascaded Inverting PGA


Vref
+
OPAMP2
-
Vout
OA2OUT = -(OA1OUT-Vref)R2/R1 + Vref
Vref
+
OPAMP1
-
R1
R2
OA1OUT = -(OA0OUT-Vref)R2/R1 + Vref
Vref
+
OPAMP0
-
R1
R2
OA0OUT = -(Vin-Vref)R2/R1 + Vref
Vref = DAC/REFBUF
Vin
R1
R2

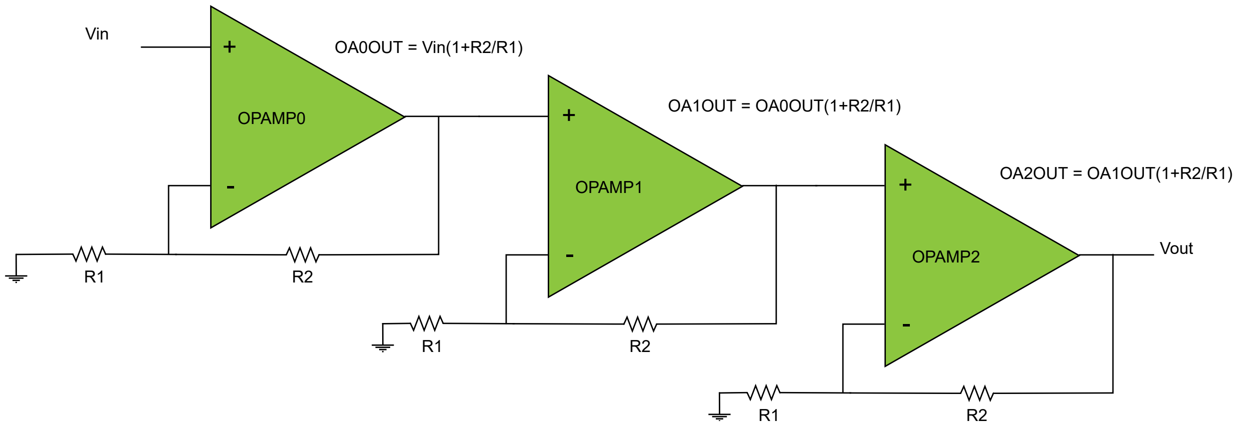
44.6.10.5 Cascaded Non-Inverting PGA

The OPAMPs can be configured as three cascaded, non-inverting PGAs using these settings in OPAMPCTRLx:

Table 44-6. Cascaded Non-Inverting PGA (Exemple: R1=4R, R2=12R)

	MUXPOS	MUXNEG	RES1MUX	POTMUX	RES2VCC	RES2OUT	RES1EN	ANAOUT
OPAMP0	0000	001	011	100	0	1	1	0
OPAMP1	0100	001	011	100	0	1	1	0
OPAMP2	0100	001	011	100	0	1	1	0

Figure 44-6. Cascaded Non-Inverting PGA



44.6.10.6 Two OPAMPs Differential Amplifier

In this mode, OPAMP0 can be coupled with OPAMP1 or OPAMP1 with OPAMP2 in order to amplify a differential signal.

To configure OPAMP0 and OPAMP1 as differential amplifier, the OPAMPCTRLx register can be configured as follows:

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Units
		Master, VDD>1,62V		0	-	-	
tMOV	MOSI output valid after SCK	Master, VDD>2,70V		-	-	34.5	ns
		Master, VDD>1,62V		-	-	38.6	
tMOH	MOSI hold after SCK	Master, VDD>2,70V		9.7	-	-	
		Master, VDD>1,62V		9.7	-	-	
tSSCK	Slave SCK Period when tMIS=0 on the master side	Slave	Reception	2*(tSIS +tMASTER_OUT) (5)	-	-	
		Slave	Transmission	2*(tSOV +tMASTER_IN) (6)	-	-	
tSSCKW	SCK high/low width	Slave		-	0,5*tSCK	-	
tSSCKR	SCK rise time(2)	Slave		-	0,25*tSCK	-	
tSSCKF	SCK fall time(2)	Slave		-	0,25*tSCK	-	
tSIS	MOSI setup to SCK	Slave, VDD>2,70V		25.6	-	-	ns
		Slave, VDD>1,62V		26.2	-	-	
tSIH	MOSI hold after SCK	Slave, VDD>2,70V		13.2	-	-	
		Slave, VDD>1,62V		13.9	-	-	
tSSS	SS setup to SCK	Slave	PRELOADEN=1	tSOSS+tEXT_MIS +2*tAPBC (8) (9)	-	-	
			PRELOADEN=0	tSOSS+tEXT_MIS (8)	-	-	
tSSH	SS hold after SCK	Slave		0.5*tSSCK	-	-	
tSOV	MISO output valid after SCK	Slave, VDD>2,70V		-	-	69	
		Slave, VDD>1,62V		-	-	78.4	
tSOH	MISO hold after SCK	Slave, VDD>2,70V		20.2	-	-	
		Slave, VDD>1,62V		20.2	-	-	
tSOSS	MISO setup after SS low	Slave, VDD>2,70V		-	-	1* tSCK	
		Slave, VDD>1,62V		-	-	1* tSCK	