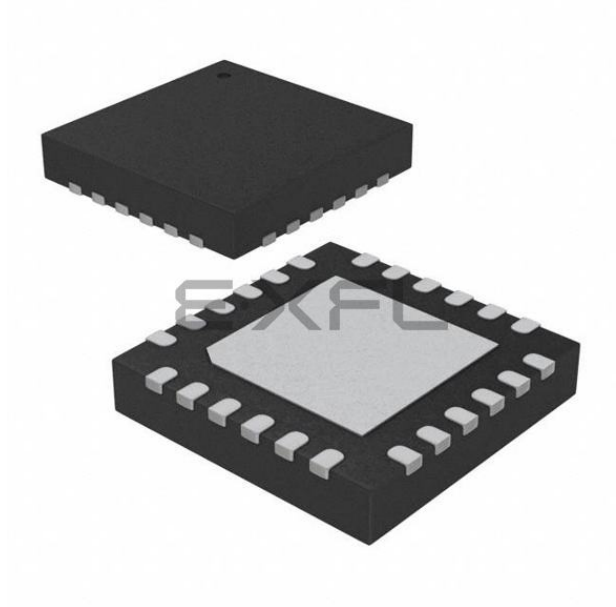

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M23 |
| Core Size | 32-Bit Single-Core |
| Speed | 32MHz |
| Connectivity | I²C, LINbus, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, POR, PWM, WDT |
| Number of I/O | 17 |
| Program Memory Size | 16KB (16K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 2K x 8 |
| RAM Size | 8K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.62V ~ 3.63V |
| Data Converters | A/D 5x12b; D/A 1x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 24-VFQFN Exposed Pad |
| Supplier Device Package | 24-VQFN (4x4) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/atsaml11d14a-mft |

The NVM Temperature Log Row can be read at address 0x00806038.

**Table 10-14. Temperature Log Row Bitfields Definition**

| Bit Position | Name | Description |
|---|---|---|
| 7:0 | ROOM_TEMP_VAL_INT | Integer part of room temperature in °C |
| 11:8 | ROOM_TEMP_VAL_DEC | Decimal part of room temperature |
| 19:12 | HOT_TEMP_VAL_INT | Integer part of hot temperature in °C |
| 23:20 | HOT_TEMP_VAL_DEC | Decimal part of hot temperature |
| 31:24 | ROOM_INT1V_VAL | 2's complement of the internal 1V reference drift at room temperature (versus a 1.0 centered value) |
| 39:32 | HOT_INT1V_VAL | 2's complement of the internal 1V reference drift at hot temperature (versus a 1.0 centered value) |
| 51:40 | ROOM_ADC_VAL | Temperature sensor 12bit ADC conversion at room temperature |
| 63:52 | HOT_ADC_VAL | Temperature sensor 12bit ADC conversion at hot temperature |

**Important:** Hot temperature corresponds to the max operating temperature +/- 5%, so 85°C +/- 5% (package grade 'U') or 125°C +/- 5% (package grade 'F').

**Table 10-15. Temperature Log Row Mapping**

| Offset | Bit Pos. | Name | |
|---|---|---|---|
| 0x00 | 7:0 | ROOM_TEMP_VAL_INT | |
| 0x01 | 15:8 | HOT_TEMP_VAL_INT | ROOM_TEMP_VAL_DEC |
| 0x02 | 23:16 | HOT_TEMP_VAL_DEC | HOT_TEMP_VAL_INT |
| 0x03 | 31:24 | ROOM_INT1V_VAL | |
| 0x04 | 39:32 | HOT_INT1V_VAL | |
| 0x05 | 47:40 | ROOM_ADC_VAL | |
| 0x06 | 55:48 | HOT_ADC_VAL | ROOM_ADC_VAL |
| 0x07 | 63:56 | HOT_ADC_VAL | |

### 10.2.4 NVM Boot Configuration Row (BOCOR)

The Non-Volatile Memory Boot Configuration Row (BOCOR) contains device configuration data that are automatically read by the Boot ROM program at device startup.

This row can be updated using the NVMCTRL peripheral.

When writing to the NVM Boot Configuration Row, the new values are not loaded by the other peripherals on the device until a device reset occurs.

The NVM Boot Configuration Row can be read at address 0x0080C000.

SAM L10 and SAM L11 have different NVM Boot Configuration Row mappings.

#### 10.2.4.1 SAM L10 Boot Configuration Row

**Table 10-16. SAM L10 BOCOR Bitfields Definition**

| Bit Pos. | Name | Usage | Factory Setting | Related Peripheral Register |
|---|---|---|---|---|
| 31:0 | Reserved | Reserved | Reserved | Reserved |
| 39:32 | BOOTPROT | Boot Protection size = BOOTPROT*0x100 | 0x00 | Boot ROM |

- URWEN
- NONSECA, NONSECB, NONSECC

USERCRC is the CRC of the NVM User row area which starts from 0x00804008 and finish at 0x0080401B (bit 64 to bit 223):

**Table 14-2. SAM L11 UROW Area Computed in USERCRC**

| Offset | Bit Pos. | Name | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| 0x08 | 71:64 | AS | | | | | | | |
| 0x09 | 79:72 | Reserved | | | | | ANSC | | |
| 0x0A | 87:80 | Reserved | | | | | | DS | |
| 0x0B | 95:88 | Reserved | | | RS | | | | |
| 0x0C | 103:96 | Reserved | | | | | | | URWEN |
| 0x0D-0xF | 127:104 | Reserved | | | | | | | |
| 0x10-0x13 | 159:128 | NONSECA | | | | | | | |
| 0x14-0x17 | 191:160 | NONSECB | | | | | | | |
| 0x18-0x1B | 223:192 | NONSECC | | | | | | | |

#### 14.4.2.1.2 Boot Configuration Row CRC (BOCORCRC)

BOCORCRC allows to check the following fuses parameters integrity:

- BS, BNSC
- BOOTOPT
- BOOTPROT, BCWEN, BCREN

BOCORCRC is the CRC of the NVM Boot Configuration row area, which starts from 0x0080C000 and finish at 0x00800C007 (bit 0 to bit 63).

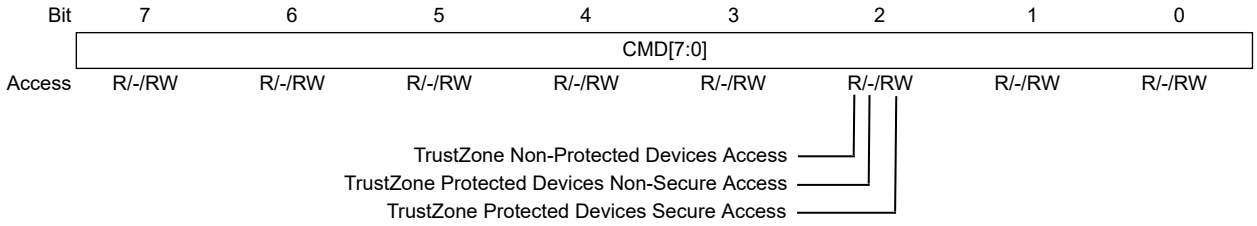
**Table 14-3. SAM L11 BOCOR Area Computed in BOCORCRC**

| Offset | Bit Pos. | Name | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| 0x00 | 7:0 | Reserved | | | | | | | |
| 0x01 | 15:8 | BS | | | | | | | |
| 0x02 | 23:16 | Reserved | | | | | BNSC | | |
| 0x03 | 31:24 | BOOTOPT | | | | | | | |
| 0x04 | 39:32 | BOOTPROT | | | | | | | |
| 0x05 | 47:40 | Reserved | | | | | | | |
| 0x06 | 55:48 | Reserved | | | | | | BCREN | BCWEN |
| 0x07 | 63:56 | Reserved | | | | | | | |

If one of the checks fails, the Boot ROM will report the error to the DSU peripheral and will enter the Boot Interactive mode:

- This will allow, if a debugger is connected, to put the device in the highest debug access level mode (DAL = 2) by issuing a Chip Erase command . Once in that mode, it is possible for a programming tool to reprogram the NVM Rows.
- When the check fails and no debugger is connected, the part will reset and restart the check sequence again.

**Note:** Boot Interactive mode is described later in this chapter.


Bit
7
6
5
4
3
2
1
0
CMD[7:0]
Access
R/-/RW
R/-/RW
R/-/RW
R/-/RW
R/-/RW
R/-/RW
R/-/RW
R/-/RW
TrustZone Non-Protected Devices Access
TrustZone Protected Devices Non-Secure Access
TrustZone Protected Devices Secure Access

### 16.12.16 CoreSight ROM Table Memory Type

**Name:** MEMTYPE
**Offset:** 0x1FCC
**Reset:** 0x0000000x
**Property:** -

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Access | | | | | | | | |
| Reset | | | | | | | | |

| Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Access | | | | | | | | |
| Reset | | | | | | | | |

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Access | | | | | | | | |
| Reset | | | | | | | | |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | SMEMP |
| Access | | | | | | | | R |
| Reset | | | | | | | | x |

**Bit 0 – SMEMP** System Memory Present
This bit indicates whether system memory is present on the bus that connects to the ROM table.

This bit is set at power-up if the device is not protected, indicating that the system memory is accessible from a debug adapter.

This bit is cleared at power-up if the device is protected, indicating that the system memory is not accessible from a debug adapter.

If the Output Enable bit in the Generator Control register is set (GENCTRLn.OE = 1) and the generator is enabled (GENCTRLn.GENEN=1), the Generator requests its clock source and the GCLK_GEN clock is output to an I/O pin.
**Note:** The I/O pin (GCLK/IO[n]) must first be configured as output by writing the corresponding PORT registers.

If GENCTRLn.OE is 0, the according I/O pin is set to an Output Off Value, which is selected by GENCTRLn.OOV: If GENCTRLn.OOV is '0', the output clock will be low. If this bit is '1', the output clock will be high.

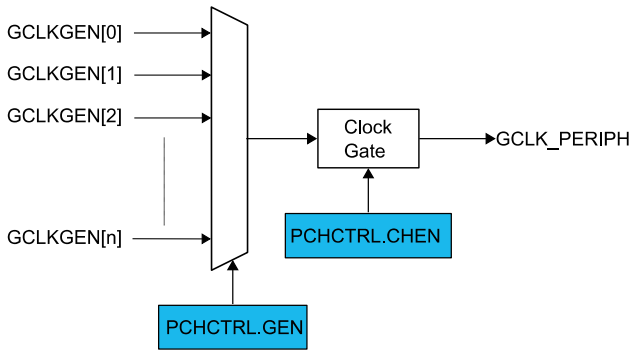
In Standby mode, if the clock is output (GENCTRLn.OE=1), the clock on the I/O pin is frozen to the OOV value if the Run In Standby bit of the Generic Control register (GENCTRLn.RUNSTDBY) is zero.
**Note:** With GENCTRLn.OE=1 and RUNSTDBY=0, entering the Standby mode can take longer due to a clock source dependent delay between turning off Power Domain PDSW. The maximum delay can be equal to the clock source period multiplied by the division factor.

If GENCTRLn.RUNSTDBY is '1', the GCLKGEN clock is kept running and output to the I/O pin.

**Related Links**
22.6.3.5 Power Domain Controller

### 18.6.3 Peripheral Clock

**Figure 18-4. Peripheral Clock**




#### 18.6.3.1 Enabling a Peripheral Clock

Before a Peripheral Clock is enabled, one of the Generators must be enabled (GENCTRLn.GENEN) and selected as source for the Peripheral Channel by setting the Generator Selection bits in the Peripheral Channel Control register (PCHCTRL.GEN). Any available Generator can be selected as clock source for each Peripheral Channel.

When a Generator has been selected, the peripheral clock is enabled by setting the Channel Enable bit in the Peripheral Channel Control register, PCHCTRLm.CHEN = 1. The PCHCTRLm.CHEN bit must be synchronized to the generic clock domain. PCHCTRLm.CHEN will continue to read as its previous state until the synchronization is complete.

#### 18.6.3.2 Disabling a Peripheral Clock

A Peripheral Clock is disabled by writing PCHCTRLm.CHEN=0. The PCHCTRLm.CHEN bit must be synchronized to the Generic Clock domain. PCHCTRLm.CHEN will stay in its previous state until the synchronization is complete. The Peripheral Clock is gated when disabled.

**Related Links**
18.8.4 PCHCTRLm

## 22.7 Register Summary

| Offset | Name | Bit Pos. | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x01 | SLEEPCFG | 7:0 | | | | | | SLEEPMODE[2:0] | | |
| 0x02 | PLCFG | 7:0 | PLDIS | | | | | | PLSEL[1:0] | |
| 0x03 | PWCFG | 7:0 | | | | | | | RAMPSWC[1:0] | |
| 0x04 | INTENCLR | 7:0 | | | | | | | | PLRDY |
| 0x05 | INTENSET | 7:0 | | | | | | | | PLRDY |
| 0x06 | INTFLAG | 7:0 | | | | | | | | PLRDY |
| 0x07 | Reserved | | | | | | | | | |
| 0x08 | STDBYCFG | 7:0 | VREGSMOD[1:0] | | | DPGPDSW | | | | PDCFG |
| | | 15:8 | | | | BBIASTR | | BBIASHS | | |

## 22.8 Register Description

Registers can be 8, 16, or 32 bits wide. Atomic 8-, 16- and 32-bit accesses are supported. In addition, the 8-bit quarters and 16-bit halves of a 32-bit register, and the 8-bit halves of a 16-bit register can be accessed directly.

Some registers are optionally write-protected by the Peripheral Access Controller (PAC). Optional PAC write-protection is denoted by the "PAC Write-Protection" property in each individual register description. For details, refer to 22.5.7 Register Access Protection.

On **SAM L11** devices, this peripheral has different access permissions depending on PAC Security Attribution (Secure or Non-Secure):

- If the peripheral is configured as Non-Secure in the PAC:
  - Secure access and Non-Secure access are granted
- If the peripheral is configured as Secure in the PAC:
  - Secure access is granted
  - Non-Secure access is discarded (Write is ignored, read 0x0) and a PAC error is triggered

Refer to *Peripherals Security Attribution* for more information.

#### 25.6.3.4 1.2V Brown-Out Detector (BOD12)

The BOD12 is calibrated in production and its calibration configuration is stored in the NVM User Row. This configuration must not be changed to assure the correct behavior of the BOD12. The BOD12 generates a reset when 1.2V crosses below the preset brown-out level. The BOD12 is always disabled in Standby Sleep mode.

#### 25.6.3.5 Continuous Mode

Continuous mode is the default mode for BOD33.

The BOD33 is continuously monitoring the VDD supply voltage if it is enabled (BOD33.ENABLE=1) and if the BOD33 Configuration bit in the BOD33 register is cleared (BOD33.ACTCFG=0 for active mode, BOD33.STDBYCFG=0 for standby mode).

#### 25.6.3.6 Sampling Mode

The Sampling Mode is a low-power mode where the BOD33 is being repeatedly enabled on a sampling clock's ticks. The BOD33 will monitor the supply voltage for a short period of time and then go to a low-power disabled state until the next sampling clock tick.

Sampling mode is enabled in Active mode for BOD33 by writing the ACTCFG bit (BOD33.ACTCFG=1). Sampling mode is enabled in Standby mode by writing to the STDBYCFG bit (BOD33.STBYCFG=1). The frequency of the clock ticks ($F_{clksampling}$) is controlled by the Prescaler Select bit groups in the BOD33 register (BOD33.PSEL).

$$F_{clksampling} = \frac{F_{clkprescaler}}{2^{(\mathrm{PSEL}+1)}}$$

The prescaler signal ($F_{clkprescaler}$) is a 1KHz clock, output by the 32KHz Ultra Low Power Oscillator OSCULP32K.

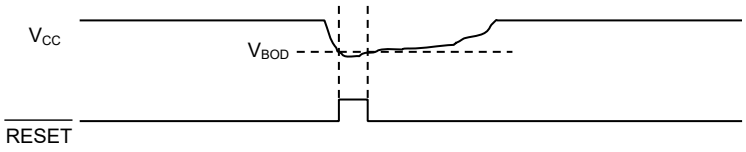
As the sampling clock is different from the APB clock domain, synchronization among the clocks is necessary. See also 25.6.6 Synchronization.

#### 25.6.3.7 Hysteresis

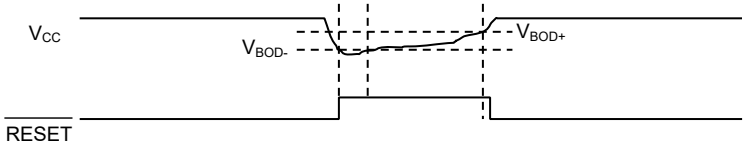
A hysteresis on the trigger threshold of a BOD will reduce the sensitivity to ripples on the monitored voltage: instead of switching $\overline{\text{RESET}}$ at each crossing of $V_{BOD}$, the thresholds for switching $\overline{\text{RESET}}$ on and off are separated ($V_{BOD-}$ and $V_{BOD+}$, respectively).

**Figure 25-2. BOD Hysteresis Principle**

Hysteresis OFF:




Hysteresis ON:




Enabling the BOD33 hysteresis by writing the Hysteresis bit in the BOD33 register (BOD33.HYST) to '1' will add hysteresis to the BOD33 threshold level.

### 27.10.17 Tamper Control B

**Name:** TAMPCTRLB
**Offset:** 0x6C
**Reset:** 0x00000000
**Property:** PAC Write-Protection, Enable-Protected

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Access | | | | | | | | |
| Reset | | | | | | | | |

| Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Access | | | | | | | | |
| Reset | | | | | | | | |

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Access | | | | | | | | |
| Reset | | | | | | | | |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | | | | | ALSI3 | ALSI2 | ALSI1 | ALSI0 |
| Access | | | | | R/W | R/W | R/W | R/W |
| Reset | | | | | 0 | 0 | 0 | 0 |

**Bits 0, 1, 2, 3 – ALSI** Active Layer Internal Select n

| Value | Description |
|---|---|
| 0 | Active layer Protection is monitoring the RTC signal using INn and OUTn tamper pins |
| 1 | Active layer Protection is monitoring the RTC signal on the TrustRAM shield |

### 28.8.1 Control

**Name:** CTRL
**Offset:** 0x00
**Reset:** 0x00X0
**Property:** PAC Write-Protection, Enable-Protected

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| | | | | | LVLENx3 | LVLENx2 | LVLENx1 | LVLENx0 |
| Access | | | | | R/W | R/W | R/W | R/W |
| Reset | | | | | 0 | 0 | 0 | 0 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | | | | | | CRCENABLE | DMAENABLE | SWRST |
| Access | | | | | | R/W | R/W | R/W |
| Reset | | | | | | 0 | 0 | 0 |

**Bits 8, 9, 10, 11 – LVLENx** Priority Level x Enable
When this bit is set, all requests with the corresponding level will be fed into the arbiter block. When cleared, all requests with the corresponding level will be ignored.

For details on arbitration schemes, refer to the Arbitration section.

These bits are not enable-protected.

| Value | Description |
|---|---|
| 0 | Transfer requests for Priority level x will not be handled. |
| 1 | Transfer requests for Priority level x will be handled. |

**Bit 2 – CRCENABLE** CRC Enable
Writing a '0' to this bit will disable the CRC calculation when the CRC Status Busy flag is cleared (CRCSTATUS. CRCBUSY). The bit is zero when the CRC is disabled.

Writing a '1' to this bit will enable the CRC calculation.

| Value | Description |
|---|---|
| 0 | The CRC calculation is disabled. |
| 1 | The CRC calculation is enabled. |

**Bit 1 – DMAENABLE** DMA Enable
Setting this bit will enable the DMA module.

Writing a '0' to this bit will disable the DMA module. When writing a '0' during an ongoing transfer, the bit will not be cleared until the internal data transfer buffer is empty and the DMA transfer is aborted. The internal data transfer buffer will be empty once the ongoing burst transfer is completed.

This bit is not enable-protected.

| Value | Description |
|---|---|
| 0 | The peripheral is disabled. |
| 1 | The peripheral is enabled. |

- External interrupt pins (EXTINTx). See 29.6.2 Basic Operation.
- Non-maskable interrupt pin (NMI). See 29.6.4 Additional Features.
- Non-secure check interrupt pin (NSCHK). See 29.8.8 INTFLAG

Each interrupt source has an associated interrupt flag. The interrupt flag in the Interrupt Flag Status and Clear register (INTFLAG) is set when an interrupt condition occurs (NMIFLAG for NMI). Each interrupt, except NMI, can be individually enabled by setting the corresponding bit in the Interrupt Enable Set register (INTENSET=1), and disabled by setting the corresponding bit in the Interrupt Enable Clear register (INTENCLR=1).

An interrupt request is generated when the interrupt flag is set and the corresponding interrupt is enabled. The interrupt request remains active until the interrupt flag is cleared, the interrupt is disabled, or the EIC is reset. See the INTFLAG register for details on how to clear interrupt flags. The EIC has at least one common interrupt request line for all the interrupt sources, and one interrupt request line for the NMI. The user must read the INTFLAG (or NMIFLAG) register to determine which interrupt condition is present.

**Note:** Interrupts must be globally enabled for interrupt requests to be generated.

### 29.6.7 Events

The EIC can generate the following output events:

- External event from pin (EXTINTx).

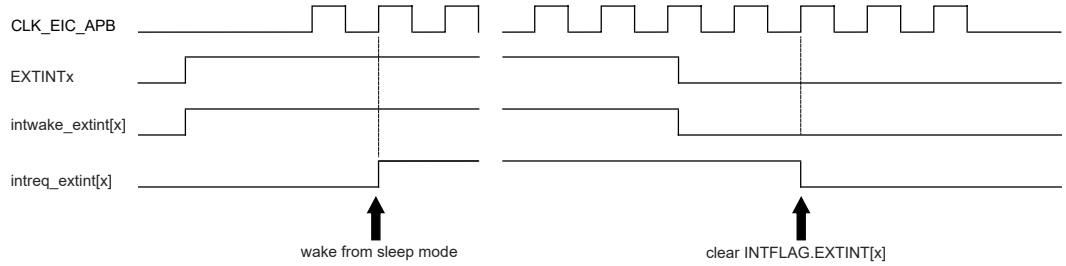
Setting an Event Output Control register (EVCTRL.EXTINTEO) enables the corresponding output event. Clearing this bit disables the corresponding output event. Refer to *Event System* for details on configuring the Event System.

When the condition on pin EXTINTx matches the configuration in the CONFIGn register, the corresponding event is generated, if enabled.

### 29.6.8 Sleep Mode Operation

In sleep modes, an EXTINTx pin can wake up the device if the corresponding condition matches the configuration in the CONFIG register, and the corresponding bit in the Interrupt Enable Set register (29.8.7 INTENSET) is written to '1'.

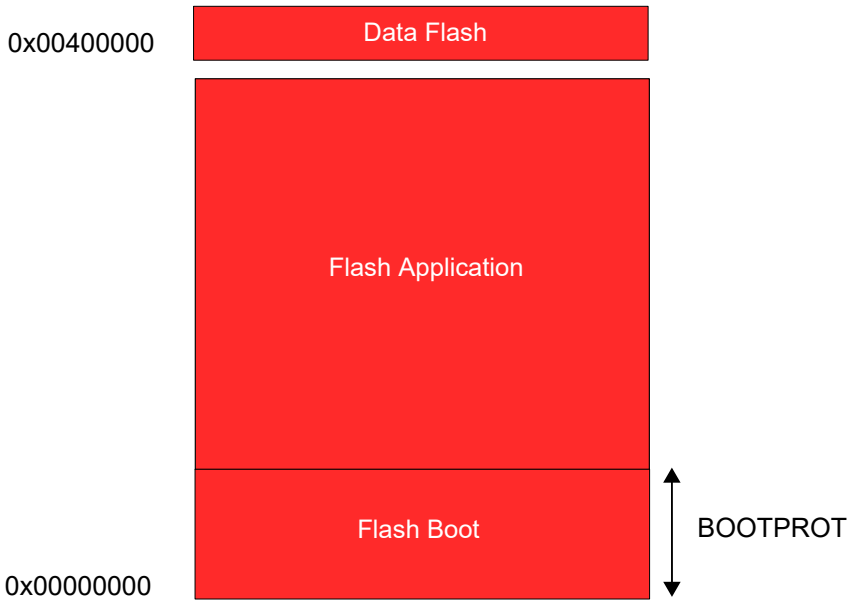
**Figure 29-5. Wake-up Operation Example (High-Level Detection, No Filter, Interrupt Enable Set)**




### 29.6.9 SAM L11 Secure Access Rights

Non-secure write to CTRLA register or DPRESCALER register is prohibited. Non-secure read to CTRLA or DPRESCALER register or SYNCBUSY register will return zero with no error resulting. Non-secure write to a bit of EVCTRL, ASYNCH, DEBOUNCEN, INTENCLR, INTENSET, INTFLAG and CONFIG registers is prohibited if the related bit of NONSEC.EXTINT is zero. Non-secure write to NMICTRL and NMIFLAG registers is prohibited if NONSECNMI.NMI is zero. Bits relating to secure EXTINT read as zero in non-secure mode with no error resulting.

**Figure 30-3. NVM Memory Organization**




The lower rows in the FLASH can be allocated as a boot loader section by using the BOOTPROT fuses.

The boot loader section size is defined by the BOOTPROT fuses expressed in number of rows.

**Important:** Refer to the Boot ROM section to get Chip Erase commands effects for this specific BOOT area.

### 30.6.3 Region Unlock Bits

The NVMCTRL has the ability to lock regions defined in the NVM Memory Organization figures.

When a region is locked all modify (i.e. write or erase) commands directed to these regions are discarded. When such an operation occurs a LOCKE error is reported in the INTFLAG register and can generate an interruption.

To lock or unlock a region, write a one to the bitfield corresponding to the selected regions in the SULCK and NSULCK registers with the correct key. Writes to these registers are silently discarded when the key is not correct. Writing these registers with the correct key will temporarily lock/unlock the corresponding regions. The new setting will stay in effect until the next Reset, or until the setting is changed again while writing SULCK and NSULCK. The current status of the lock can be determined by reading the SULCK and NSULCK registers. To change the default lock/unlock setting for a region, the user row of the AUX FLASH must be written using the Write Page command. Writing to the AUX FLASH user row will take effect after the next Reset. Therefore, a boot of the device is needed for changes in the lock/unlock setting to take effect. Refer to the Physical Memory Map for calibration and auxiliary space address mapping.

### 30.6.4 Command and Data Interface

The NVM Controller is addressable from the APB bus, while the NVM main address space is addressable from the AHB bus. Read and automatic page write operations are performed by addressing the FLASH, Data FLASH and AUX FLASH spaces directly, while other operations such as manual page writes and row erases must be performed by issuing commands through the NVM Controller.

and can reside in program or data memory. To use this feature, the row must be previously erased and the page buffer must contain the desired data to be written.

As the Page Buffer is lost when the NVM enters low power mode (refer to 30.5.1 Power Management ) cannot be used if the device enters STANDBY mode or if the NVM uses power reduction modes.

The cache coherency is not ensured after an Event Automatic Write in a FLASH page. The FLASH region is cacheable, it is the user responsability to clear the cache after such an action. Note that the Data FLASH is not subject to cache coherency issues since it is not cacheble.

### 30.6.7 Tamper Erase

Tamper Erase ensures rapid overwrite on tamper of a Data FLASH row selected by SECCTRL.TEROW.

When a RTC tamper event occur while tamper erase is enabled (SECCTRL.TAMPEEN=1):

- the Tamper Erase row in data space addressed by SECCTRL.TEROW is written to zero.

This is performed using a special overwrite mechanism in the NVM block that overwrites the complete row with zero. The RTC must be configured to generate the tamper erase event.

**Note:** Data Flash endurance is affected by the tamper erase feature. Refer to the "NVM Reliability Characteristics" from Electrical Characteristics chapter.

### 30.6.8 Silent Access

When enabled (SECCTRL.SILACC=1), Silent accesses are performed when accessing one Data Flash row selected by SECCTRL.TEROW. The physical and logical size of the TEROW is divided by two to store each word of Data and its complement to reduce Data Flash reading noise.

When Silent Access is enabled, data in the selected Tamper Erase ROW must be accessed using following address mapping:

**TEROW_base_address**

| W31 | W30 | W29 | … | W3 | W2 | W1 | W0 | Page |
|---|---|---|---|---|---|---|---|---|
| Data | Data | Data | Data | Data | Data | Data | Data | page0 |
| Data | Data | Data | Data | Data | Data | Data | Data | page1 |
| reserved | reserved | reserved | reserved | reserved | reserved | reserved | reserved | page2 |
| reserved | reserved | reserved | reserved | reserved | reserved | reserved | reserved | page3 |

**TEROW_base_address + ROW size**

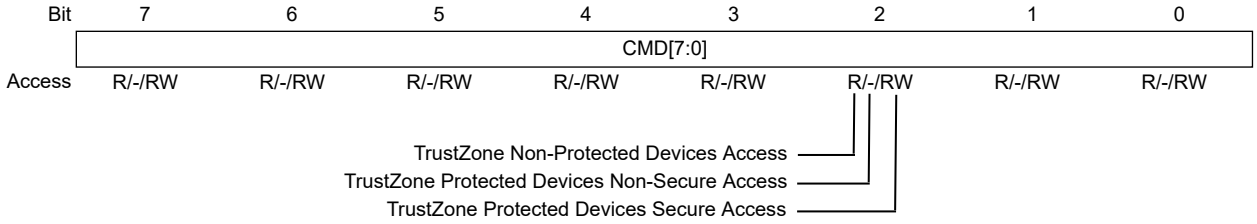
All accesses to Reserved area are discarded and generate a bus error.

Note that the physical TEROW mapping in Data Flash is the following:

**TEROW_physical_base_address**

| W31 | W30 | W29 | … | W3 | W2 | W1 | W0 | Page |
|---|---|---|---|---|---|---|---|---|
| CompData | Data | CompData | Data | CompData | Data | CompData | Data | page0 |
| CompData | Data | CompData | Data | CompData | Data | CompData | Data | page1 |

On SAM L11 devices, the Mix-Secure peripheral has different types of registers (Non-Secure, Secure, Write-Secure, Mix-Secure, and Write-Mix-Secure) with different access permissions for each bitfield. Refer to *Mix-Secure Peripherals* for more details. In the following register descriptions, the access permissions are specified as shown in the following figure.



### 30.8.9 Address

**Name:** ADDR
**Offset:** 0x1C
**Reset:** 0x00000000
**Property:** PAC Write-Protection, Secure

ADDR drives the hardware address to the NVM when a command is executed using CMDEX. This is a Byte aligned address. This register is automatically updated upon AHB writes to the page buffer.

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | |
| Access | | | | | | | | |
| Reset | | | | | | | | |

| Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| | ARRAY[1:0] | | | | | | | |
| Access | RW/-/RW | RW/-/RW | | | | | | |
| Reset | 0 | 0 | | | | | | |

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| | AOFFSET[15:8] | | | | | | | |
| Access | RW/-/RW | RW/-/RW | RW/-/RW | RW/-/RW | RW/-/RW | RW/-/RW | RW/-/RW | RW/-/RW |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | AOFFSET[7:0] | | | | | | | |
| Access | RW/-/RW | RW/-/RW | RW/-/RW | RW/-/RW | RW/-/RW | RW/-/RW | RW/-/RW | RW/-/RW |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Bits 23:22 – ARRAY[1:0]** Array Select

| Value | Description |
|---|---|
| 00 | Flash |
| 01 | Data Flash |
| 10 | NVM Rows |

**Bits 15:0 – AOFFSET[15:0]** Array Offset
Address offset

### 38.7.2.3 Control B Set

**Name:** CTRLBSET
**Offset:** 0x05
**Reset:** 0x00
**Property:** PAC Write-Protection, Read-synchronized, Write-Synchronized

This register allows the user to set bits in the CTRLB register without doing a read-modify-write operation. Changes in this register will also be reflected in the Control B Clear register (CTRLBCLR).

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | CMD[2:0] | | | | | ONESHOT | LUPD | DIR |
| Access | R/W | R/W | R/W | | | R/W | R/W | R/W |
| Reset | 0 | 0 | 0 | | | 0 | 0 | 0 |

**Bits 7:5 – CMD[2:0]** Command
These bits are used for software control of the TC. The commands are executed on the next prescaled GCLK_TC clock cycle. When a command has been executed, the CMD bit group will be read back as zero.

Writing 0x0 to these bits has no effect.

Writing a value different from 0x0 to these bits will issue a command for execution.

| Value | Name | Description |
|---|---|---|
| 0x0 | NONE | No action |
| 0x1 | RETRIGGER | Force a start, restart or retrigger |
| 0x2 | STOP | Force a stop |
| 0x3 | UPDATE | Force update of double buffered registers |
| 0x4 | READSYNC | Force a read synchronization of COUNT |

**Bit 2 – ONESHOT** One-Shot on Counter
This bit controls one-shot operation of the TC.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will enable one-shot operation.

| Value | Description |
|---|---|
| 0 | The TC will wrap around and continue counting on an overflow/underflow condition. |
| 1 | The TC will wrap around and stop on the next underflow/overflow condition. |

**Bit 1 – LUPD** Lock Update
This bit controls the update operation of the TC buffered registers.

When CTRLB.LUPD is set, no any update of the registers with value of its buffered register is performed on hardware UPDATE condition. Locking the update ensures that all buffer registers are valid before an hardware update is performed. After all the buffer registers are loaded correctly, the buffered registers can be unlocked.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will set the LUPD bit.

This bit has no effect when input capture operation is enabled.

| Value | Description |
|---|---|
| 0 | The CCBUFx and PERBUF buffer registers value are copied into CCx and PER registers on hardware update condition. |
| 1 | The CCBUFx and PERBUF buffer registers value are not copied into CCx and PER registers on hardware update condition. |

**Bit 0 – DIR** Counter Direction
This bit is used to change the direction of the counter.

Writing a '0' to this bit has no effect

Writing a '1' to this bit will clear the bit and make the counter count up.

| Value | Description |
|---|---|
| 0 | The timer/counter is counting up (incrementing). |
| 1 | The timer/counter is counting down (decrementing). |

### 41.8.2 Control B

**Name:** CTRLB
**Offset:** 0x01
**Reset:** 0x00
**Property:** PAC Write-Protection, Enable-Protected

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | | | | | | PRESCALER[2:0] | | |
| Access | | | | | | R/W | R/W | R/W |
| Reset | | | | | | 0 | 0 | 0 |

**Bits 2:0 – PRESCALER[2:0]** Prescaler Configuration
This field defines the ADC clock relative to the peripheral clock.

| Value | Name | Description |
|---|---|---|
| 0x0 | DIV2 | Peripheral clock divided by 2 |
| 0x1 | DIV4 | Peripheral clock divided by 4 |
| 0x2 | DIV8 | Peripheral clock divided by 8 |
| 0x3 | DIV16 | Peripheral clock divided by 16 |
| 0x4 | DIV32 | Peripheral clock divided by 32 |
| 0x5 | DIV64 | Peripheral clock divided by 64 |
| 0x6 | DIV128 | Peripheral clock divided by 128 |
| 0x7 | DIV256 | Peripheral clock divided by 256 |

1. For this Flash technology, a maximum number of 8 consecutive writes is allowed per row. Once this number is reached, a row erase is mandatory.

**Table 46-41. Flash Erase and Programming Current**

| Symbol | Parameter | Typ. | Units |
|---|---|---|---|
| $IDD_{NVM}$ | Maximum current (peak) during whole programming or erase operation | 10 | mA |

**Table 46-42. NVM Reliability Characteristics**

| Symbol | Parameter | Conditions | Min. | Typ. | Units |
|---|---|---|---|---|---|
| $Ret_{NVM25k}$ | Retention after up to 25k | Average ambient 55°C | 10 | 50 | Years |
| $Ret_{NVM2.5k}$ | Retention after up to 2.5k | Average ambient 55°C | 20 | 100 | Years |
| $Ret_{NVM100}$ | Retention after up to 100 | Average ambient 55°C | 25 | >100 | Years |
| $Cyc_{NVM}$ | Cycling Endurance(1) | -40°C < Ta < 85°C<br>-40°C < Ta < 125°C | 25K | 100K | Cycles |
| | Cycling Endurance using Tamper Erase(1) | | 50 | 100 | Cycles |

**Note:** 1. An endurance cycle is a write and an erase operation.

## 46.13 Oscillators Characteristics

### 46.13.1 Crystal Oscillator (XOSC) Characteristics

**Digital Clock Characteristics**

The following table describes the characteristics for the oscillator when a digital clock is applied on XIN.

**Table 46-43. Digital Clock Characteristics**

| Symbol | Parameter | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $F_{XIN}$ | XIN clock frequency | - | - | 24 | MHz |
| $DC_{XIN}$(1) | XIN clock duty cycle | 40 | 50 | 60 | % |

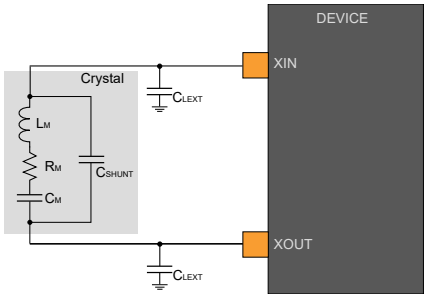
**Note:**

1. These values are based on simulation. They are not covered by production test limits or characterization.

**Crystal Oscillator Characteristics**

The following Table describes the characteristics for the oscillator when a crystal is connected between XIN and XOUT.

**Figure 46-3. Oscillator Connection**




The user must choose a crystal oscillator where the crystal load capacitance $C_L$ is within the range given in the Table. The exact value of $C_L$ can be found in the crystal data sheet. The capacitance of the external capacitors ($C_{LEXT}$) can then be computed as follows:

$C_{LEXT} = 2(C_L - C_{PARA} - C_{PCB} - C_{SHUNT})$

Where:

- $C_{PARA}$ is the internal load capacitor parasitic between XIN and XOUT ($C_{PARA} = (C_{XIN} * C_{XOUT})/(C_{XIN} + C_{XOUT})$)
- $C_{PCB}$ is the capacitance of the PCB
- $C_{SHUNT}$ is the shunt capacity of the crystal.

**Table 46-44. Multi Crystal Oscillator Electrical Characteristics**

| Symbol | Parameter | Conditions | Min. | Typ. | Max | Units |
|---|---|---|---|---|---|---|
| Fout | Crystal oscillator frequency | | 0.4 | - | 32 | MHz |
| ESR(2) | Crystal Equivalent Series Resistance - SF = 3 | F = 0,4MHz - CL=100 pF XOSC,GAIN=0 | - | - | 5.6K | Ω |
| | | F = 2MHz - CL=20 pF XOSC,GAIN=0, Cshunt=3.3pF | - | - | 330 | |
| | | F = 4MHz - CL=20 pF XOSC,GAIN=1, Cshunt=2.5pF | - | - | 240 | |
| | | F = 8MHz - CL=20 pF XOSC,GAIN=2, Cshunt=5.5pF | - | - | 105 | |
| | | F = 16MHz - CL=20 pF XOSC,GAIN=3, Cshunt=4pF | - | - | 60 | |
| | | F = 32MHz - CL=20 pF XOSC,GAIN=4, Cshunt=3.9pF | - | - | 55 | |
| Cxin(2) | Parasitic load capacitor | | - | 6.7 | - | pF |
| Cxout(2) | | | - | 4.2 | - | pF |
| Tstart(2) | Startup time | F = 2MHz - CL=20 pF XOSC,GAIN=0, Cshunt=3.3pF | - | 15.6K | 81.6K | Cycles |
| | | F = 4MHz - CL=20 pF XOSC,GAIN=1, Cshunt=2.5pF | - | 6.3K | 25.2K | |