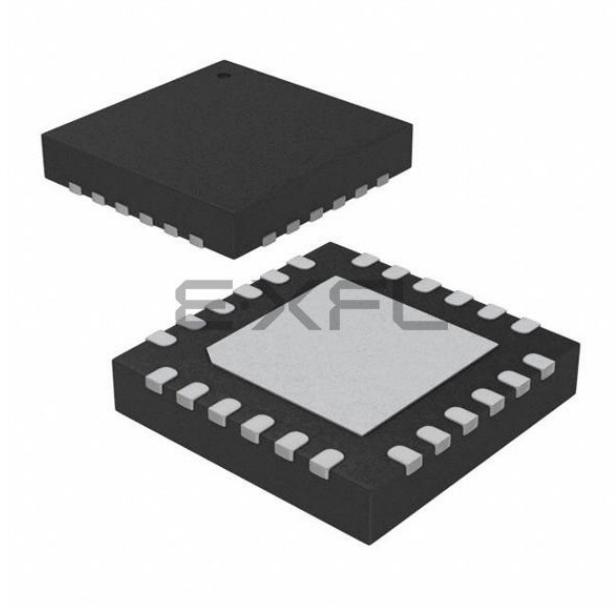

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M23
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	17
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.63V
Data Converters	A/D 5x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	24-VFQFN Exposed Pad
Supplier Device Package	24-VQFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsaml11d16a-mft

7. Analog Peripherals Considerations

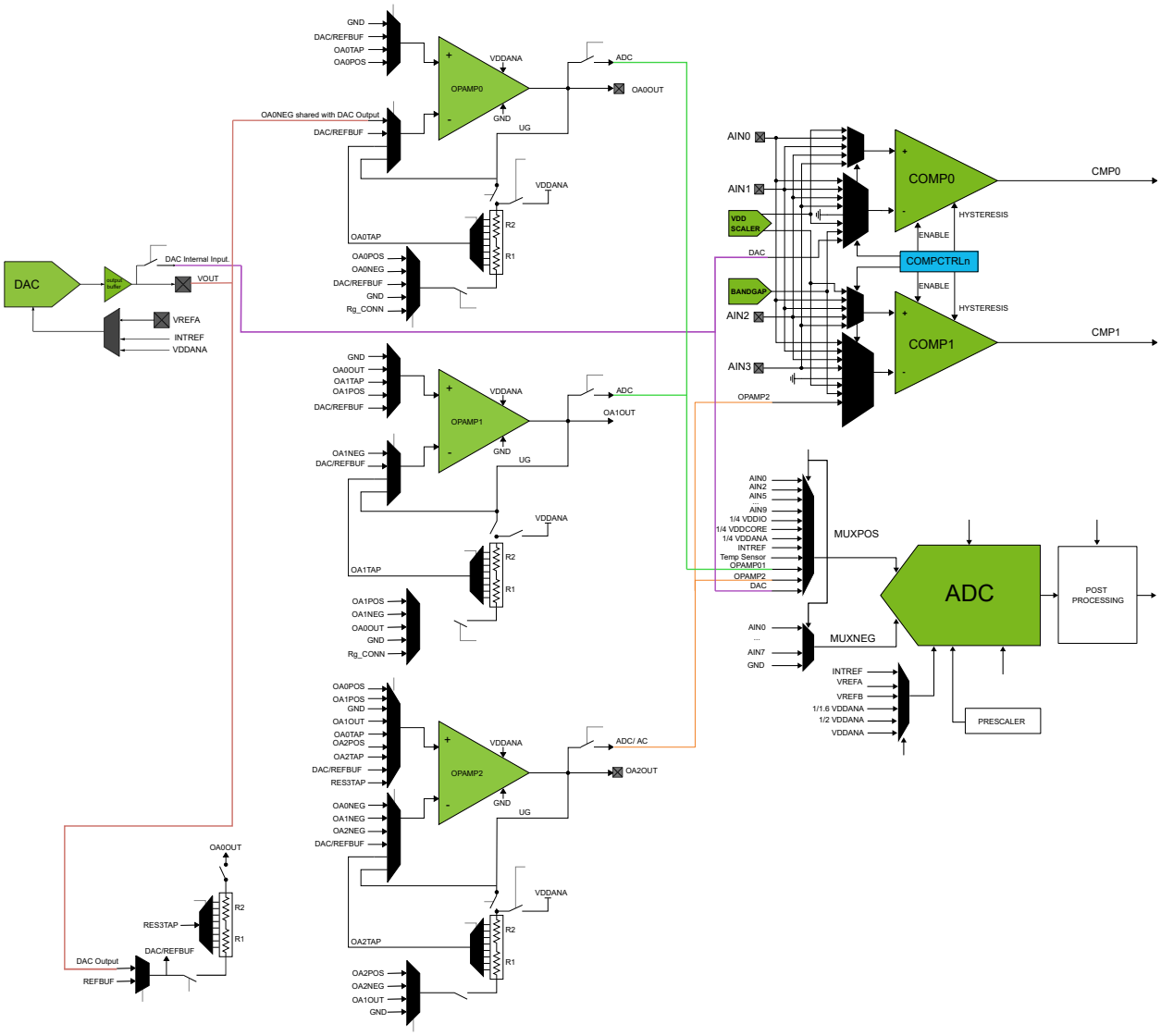
This chapter provides a global view of the analog system, which is composed of the following analog peripherals: AC, ADC, DAC, OPAMP.

The analog peripherals can be connected to each other as illustrated in the following block diagram.

Important:
When an analog peripheral is enabled, each analog output of the peripheral will be prevented from using the alternative functions of the output pads. This is also true even when the peripheral is used for internal purposes.

Analog inputs do not interfere with alternate pad functions.

Figure 7-1. Analog Signal Components Interconnections



Bit Pos.	Name	Usage	Factory Setting	Related Peripheral Register
6	Reserved	Reserved	Reserved	Reserved
12:7	BOD33 Level	BOD33 threshold level at power-on	0x6	SUPC.BOD33
13	BOD33 Disable	BOD33 Disable at power-on	0x0	SUPC.BOD33
15:14	BOD33 Action	BOD33 Action at power-on	0x1	SUPC.BOD33
24:16	BOD12 Calibration Parameters	**DO NOT CHANGE(1)**	**0x08F**	Reserved
25	WDT_RUNSTDBY	WDT Runstdby at power-on	0x0	WDT.CTRLA
26	WDT_ENABLE	WDT Enable at power-on	0x0	WDT.CTRLA
27	WDT_ALWAYSON	WDT Always-On at power-on	0x0	WDT.CTRLA
31:28	WDT_PER	WDT Period at power-on	0xB	WDT.CONFIG
35:32	WDT_WINDOW	WDT Window mode time-out at power-on	0xB	WDT.CONFIG
39:36	WDT_EWOFFSET	WDT Early Warning Interrupt Time Offset at power-on	0xB	WDT.EWCTRL
40	WDT_WEN	WDT Timer Window Mode Enable at power-on	0x0	WDT.CTRLA
41	BOD33_HYST	BOD33 Hysteresis configuration at power-on	0x0	SUPC.BOD33
255:42	Reserved	Reserved	Reserved	Reserved

⚠ CAUTION

1. BOD12 is calibrated in production and its calibration parameters must not be changed to ensure the correct device behavior.

Table 10-9. SAM L10 UROW Mapping

Offset	Bit Pos.	Name							
0x00	7:0	BOD33 Level	-	NSULCK			Reserved		
0x01	15:8	BOD33 Action		BOD33 Disable	BOD33 Level				
0x02	23:16	BOD12 Calibration Parameters							
0x03	31:24	WDT_PER				WDT_ALWAYSON	WDT_ENABLE	WDT_RUNSTDBY	BOD12 Calibration Parameters
0x04	39:32	WDT_EWOFFSET				WDT_WINDOW			
0x05	47:40	Reserved						BOD33_HYST	WDT_WEN
0x06-0x1F	255:48	Reserved							

10.2.1.2 SAM L11 User Row

Table 10-10. SAM L11 UROW Bitfields Definition

Bit Pos.	Name	Usage	Factory Setting	Related Peripheral Register
2:0	SULCK	NVM Secure Region UnLock Bits	0x7	NVMCTRL.SULCK
5:3	NSULCK	NVM Non-Secure Region UnLock Bits	0x7	NVMCTRL.NSULCK
6	Reserved	Reserved	Reserved	Reserved
12:7	BOD33 Level	BOD33 threshold level at power-on.	0x6	SUPC.BOD33
13	BOD33 Disable	BOD33 Disable at power-on	0x0	SUPC.BOD33
15:14	BOD33 Action	BOD33 Action at power-on	0x1	SUPC.BOD33
24:16	BOD12 Calibration Parameters	**Do not change(See Note 1 under Caution)**	**0x08F**	Reserved

Bit Pos.	Name	Usage	Factory Setting	Related Peripheral Register
25	WDT_RUNSTDBY	WDT Runstdby at power-on	0x0	WDT.CTRLA
26	WDT_ENABLE	WDT Enable at power-on	0x0	WDT.CTRLA
27	WDT_ALWAYSON	WDT Always-On at power-on	0x0	WDT.CTRLA
31:28	WDT_PER	WDT Period at power-on	0xB	WDT.CONFIG
35:32	WDT_WINDOW	WDT Window mode time-out at power-on	0xB	WDT.CONFIG
39:36	WDT_EWOFFSET	WDT Early Warning Interrupt Time Offset at power-on	0xB	WDT.EWCTRL
40	WDT_WEN	WDT Timer Window Mode Enable at power-on	0x0	WDT.CTRLA
41	BOD33_HYST	BOD33 Hysteresis configuration at power-on	0x0	SUPC.BOD33
42	Reserved	Reserved	Reserved	Reserved
43	RXN	RAM is eXecute Never	0x1	IDAU.SECCTRL
44	DXN	Data Flash is eXecute Never	0x1	NVMCTRL.SECCTRL
63:45	Reserved	Reserved	Reserved	Reserved
71:64	AS	Flash Application Secure Size = AS*0x100	0xFF	IDAU.SCFGA
77:72	ANSC	Flash Application Non-Secure Callable Size = ANSC*0x20	0x0	IDAU.SCFGA
79:78	Reserved	Reserved	Reserved	Reserved
83:80	DS	Data Flash Secure Size = DS*0x100	0x8	IDAU.SCFGA
87:84	Reserved	Reserved	Reserved	Reserved
94:88	RS	RAM Secure Size = RS*0x80	0x7F	IDAU.SCFGR
95	Reserved	Reserved	Reserved	Reserved
96	URWEN	User Row Write Enable	0x1	NVMCTRL.SCFGAD
127:97	Reserved	Reserved	Reserved	Reserved
159:128	NONSECA(1)	Peripherals Non-Secure Status Fuses for Bridge A	0x0000_0000	PAC.NONSECA
191:160	NONSECB(2, 3)	Peripherals Non-Secure Status Fuses for Bridge B	0x0000_0000	PAC.NONSECB
223:192	NONSECC	Peripherals Non-Secure Status Fuses for Bridge C	0x0000_0000	PAC.NONSECC
255:224	USERCRC	CRC of NVM User Row bits 223:64	0x8433651E	Boot ROM

Note:

1. The PAC Peripheral is always secured regardless of its bit value
2. The IDAU and NVMCTRL peripherals are always secured regardless of their bit values.
3. The DSU peripheral is always non-secured regardless of its bit value.

⚠ CAUTION

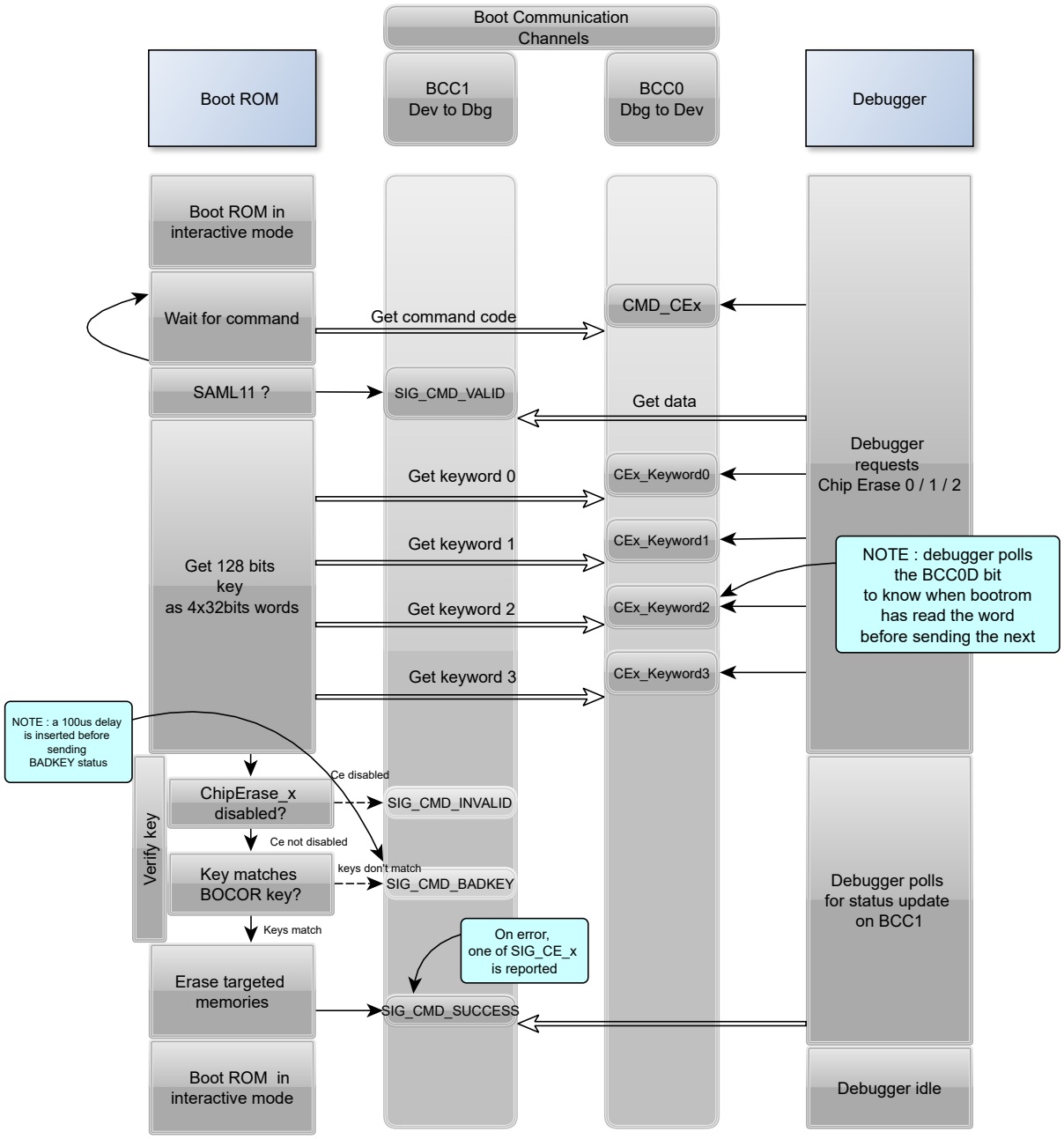
1. BOD12 is calibrated in production and its calibration parameters must not be changed to ensure the correct device behavior.

Table 10-11. SAM L11 UROW Mapping

Offset	Bit Pos.	Name			
0x00	7:0	BOD33 Level	-	NSULCK	SULCK
0x01	15:8	BOD33 Action		BOD33 Disable	BOD33 Level
0x02	23:16	BOD12 Calibration Parameters			

14.4.5.5.1 CMD_CEx (SAM L11 only)

Figure 14-11. CMD_CEx Flow diagram



14.4.5.6 NVM Memory Regions Integrity Checks (CMD_CRC)

The Boot ROM provides a way to check the integrity of the embedded non-volatile memories which may be of interest in case of a failure analysis.

This requires the user to place tables describing the memory area to be checked with their expected CRC values.

Note: During this integrity check process, the debugger sends the CRC table address to the device.

17.6 Power Consumption vs. Speed

When targeting for either a low-power or a fast acting system, some considerations have to be taken into account due to the nature of the asynchronous clocking of the peripherals:

If clocking a peripheral with a very low clock, the active power consumption of the peripheral will be lower. At the same time the synchronization to the synchronous (CPU) clock domain is dependent on the peripheral clock speed, and will take longer with a slower peripheral clock. This will cause worse response times and longer synchronization delays.

17.7 Clocks after Reset

On any Reset the synchronous clocks start to their initial state:

- OSC16M is enabled and configured to run at 4MHz
- Generic Clock Generator 0 uses OSC16M as source and generates GCLK_MAIN and CLK_MAIN
- CPU and BUS clocks are undivided

On a Power-on Reset, the 32KHz clock sources are reset and the GCLK module starts to its initial state:

- All Generic Clock Generators are disabled except Generator 0
- All Peripheral Channels in GCLK are disabled.

On a User Reset the GCLK module starts to its initial state, except for:

- Generic Clocks that are write-locked, i.e., the according WRTLOCK is set to 1 prior to Reset

Related Links

19.6.2.6 Peripheral Clock Masking

19.6.2.2 Enabling, Disabling, and Resetting

The MCLK module is always enabled and cannot be reset.

19.6.2.3 Selecting the Main Clock Source

Refer to the Generic Clock Controller description for details on how to configure the clock source of the GCLK_MAIN clock.

Refer to the Oscillators Controller (OSCCTRL) description for details on how to configure the clock source of the CLK_DFLLULP clock.

Related Links

18. GCLK - Generic Clock Controller

19.6.2.4 Selecting the Synchronous Clock Division Ratio

The main clock CLK_MAIN feeds an 8-bit prescaler, which can be used to generate the synchronous clocks. By default, the synchronous clocks run on the undivided main clock. The user can select a prescaler division for the CPU clock domain by writing the Division (DIV) bits in the CPU Clock Division register CPUDIV, resulting in a CPU clock domain frequency determined by this equation:

$$f_{CPU} = \frac{f_{main}}{CPUDIV}$$

If the application attempts to write forbidden values in CPUDIV register, registers are written but these bad values are not used and a violation is reported to the PAC module.

Division bits (DIV) can be written without halting or disabling peripheral modules. Writing DIV bits allows a new clock setting to be written to all synchronous clocks belonging to the corresponding clock domain at the same time.

Note that clocks should only be switched off if it is certain that the module will not be used: Switching off the clock for the NVM Controller (NVMCTRL) will cause a problem if the CPU needs to read from the Flash Memory. Switching off the clock to the MCLK module (which contains the mask registers) or the corresponding APBx bridge, will make it impossible to write the mask registers again. In this case, they can only be re-enabled by a system reset.

19.6.3 DMA Operation

Not applicable.

19.6.4 Interrupts

The peripheral has the following interrupt sources:

- Clock Ready (CKRDY): indicates that CPU clocks are ready. This interrupt is a synchronous wake-up source.

Each interrupt source has an interrupt flag associated with it. The interrupt flag in the Interrupt Flag Status and Clear (INTFLAG) register is set when the interrupt condition occurs. Each interrupt can be enabled individually by writing a '1' to the corresponding enabling bit in the Interrupt Enable Set (INTENSET) register, and disabled by writing a '1' to the corresponding clearing bit in the Interrupt Enable Clear (INTENCLR) register.

An interrupt request is generated when the interrupt flag is set and the corresponding interrupt is enabled. The interrupt request remains active until the interrupt flag is cleared, the interrupt is disabled or the peripheral is reset. An interrupt flag is cleared by writing a '1' to the corresponding bit in the INTFLAG register. Each peripheral can have one interrupt request line per interrupt source or one common interrupt request line for all the interrupt sources.If the peripheral has one common interrupt request line for all the interrupt sources, the user must read the INTFLAG register to determine which interrupt condition is present.

Related Links

22. PM – Power Manager

22.6.3.3 Sleep Mode Controller

19.6.5 Events

Not applicable.

19.6.6 Sleep Mode Operation

In all IDLE sleep modes, the MCLK is still running on the selected main clock.

In STANDBY sleep mode, the MCLK is frozen if no synchronous clock is required.

32.8.12 Event Input Control

Name: EVCTRL
Offset: 0x2C
Reset: 0x00000000
Property: PAC Write-Protection, Secure

Tip: The I/O pins are assembled in pin groups (”PORT groups”) with up to 32 pins. Group 0 consists of the PA pins, group 1 is for the PB pins, etc. Each pin group has its own PORT registers, with a 0x80 address spacing. For example, the register address offset for the Data Direction (DIR) register for group 0 (PA00 to PA31) is 0x00, and the register address offset for the DIR register for group 1 (PB00 to PB31) is 0x80.

There are up to four input event pins for each PORT group. Each byte of this register addresses one Event input pin.

Bit	31	30	29	28	27	26	25	24
	PORTEIx	EVACTx[1:0]		PIDx[4:0]				
Access	RW/-/RW	RW/-/RW	RW/-/RW	RW/-/RW	RW/-/RW	RW/-/RW	RW/-/RW	RW/-/RW
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PORTEIx	EVACTx[1:0]		PIDx[4:0]				
Access	RW/-/RW	RW/-/RW	RW/-/RW	RW/-/RW	RW/-/RW	RW/-/RW	RW/-/RW	RW/-/RW
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PORTEIx	EVACTx[1:0]		PIDx[4:0]				
Access	RW/-/RW	RW/-/RW	RW/-/RW	RW/-/RW	RW/-/RW	RW/-/RW	RW/-/RW	RW/-/RW
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PORTEIx	EVACTx[1:0]		PIDx[4:0]				
Access	RW/-/RW	RW/-/RW	RW/-/RW	RW/-/RW	RW/-/RW	RW/-/RW	RW/-/RW	RW/-/RW
Reset	0	0	0	0	0	0	0	0

Bits 31,23,15,7 – PORTEIx PORT Event Input Enable x [x = 3..0]

Value	Description
0	The event action x (EVACTx) will not be triggered on any incoming event.
1	The event action x (EVACTx) will be triggered on any incoming event.

Bits 30:29, 22:21,14:13,6:5 – EVACTx PORT Event Action x [x = 3..0]
These bits define the event action the PORT will perform on event input x. See also Table 32-4.

Bits 28:24,20:16,12:8,4:0 – PIDx PORT Event Pin Identifier x [x = 3..0]
These bits define the I/O pin on which the event action will be performed, according to Table 32-5.

Related Links

22. PM – Power Manager

34.5.3 Clocks

The SERCOM bus clock (CLK_SERCOMx_APB) can be enabled and disabled in the Main Clock Controller. Refer to *Peripheral Clock Masking* for details and default status of this clock.

The SERCOM uses two generic clocks: GCLK_SERCOMx_CORE and GCLK_SERCOMx_SLOW. The core clock (GCLK_SERCOMx_CORE) is required to clock the SERCOM while working as a master. The slow clock (GCLK_SERCOMx_SLOW) is only required for certain functions. See specific mode chapters for details.

These clocks must be configured and enabled in the Generic Clock Controller (GCLK) before using the SERCOM.

The generic clocks are asynchronous to the user interface clock (CLK_SERCOMx_APB). Due to this asynchronicity, writing to certain registers will require synchronization between the clock domains. Refer to 34.6.8 Synchronization for details.

Related Links

18. GCLK - Generic Clock Controller
19. MCLK – Main Clock

34.5.4 DMA

The DMA request lines are connected to the DMA Controller (DMAC). The DMAC must be configured before the SERCOM DMA requests are used.

Related Links

28. DMAC – Direct Memory Access Controller

34.5.5 Interrupts

The interrupt request line is connected to the Interrupt Controller (NVIC). The NVIC must be configured before the SERCOM interrupts are used.

34.5.6 Events

Not applicable.

34.5.7 Debug Operation

When the CPU is halted in debug mode, this peripheral will continue normal operation. If the peripheral is configured to require periodical service by the CPU through interrupts or similar, improper operation or data loss may result during debugging. This peripheral can be forced to halt operation during debugging - refer to the Debug Control (DBGCTRL) register for details.

34.5.8 Register Access Protection

All registers with write-access can be write-protected optionally by the Peripheral Access Controller (PAC), except for the following registers:

- Interrupt Flag Clear and Status register (INTFLAG)
- Status register (STATUS)
- Data register (DATA)
- Address register (ADDR)

Value	Description
0	STATUS.BUFOVF is asserted when it occurs in the data stream.
1	STATUS.BUFOVF is asserted immediately upon buffer overflow.

Bit 7 – RUNSTDBY Run In Standby
This bit defines the functionality in standby sleep mode.

This bit is not synchronized.

RUNSTDBY	External Clock	Internal Clock
0x0	External clock is disconnected when ongoing transfer is finished. All reception is dropped.	Generic clock is disabled when ongoing transfer is finished. The device can wake up on Transfer Complete interrupt.
0x1	Wake on Receive Complete interrupt.	Generic clock is enabled in all sleep modes. Any interrupt can wake up the device.

Bits 4:2 – MODE[2:0] Operating Mode
These bits select the USART serial communication interface of the SERCOM.

These bits are not synchronized.

Value	Description
0x0	USART with external clock
0x1	USART with internal clock

Bit 1 – ENABLE Enable
Due to synchronization, there is delay from writing CTRLA.ENABLE until the peripheral is enabled/disabled. The value written to CTRLA.ENABLE will read back immediately and the Enable Synchronization Busy bit in the Synchronization Busy register (SYNCBUSY.ENABLE) will be set. SYNCBUSY.ENABLE is cleared when the operation is complete.

This bit is not enable-protected.

Value	Description
0	The peripheral is disabled or being disabled.
1	The peripheral is enabled or being enabled.

Bit 0 – SWRST Software Reset
Writing '0' to this bit has no effect.

Writing '1' to this bit resets all registers in the SERCOM, except DBGCTRL, to their initial state, and the SERCOM will be disabled.

Writing '1' to CTRLA.SWRST will always take precedence, meaning that all other writes in the same write-operation will be discarded. Any register write access during the ongoing reset will result in an APB error. Reading any register will return the reset value of the register.

Due to synchronization, there is a delay from writing CTRLA.SWRST until the reset is complete. CTRLA.SWRST and SYNCBUSY.SWRST will both be cleared when the reset is complete.

This bit is not enable-protected.

37.6.2.4 I²C Master Operation

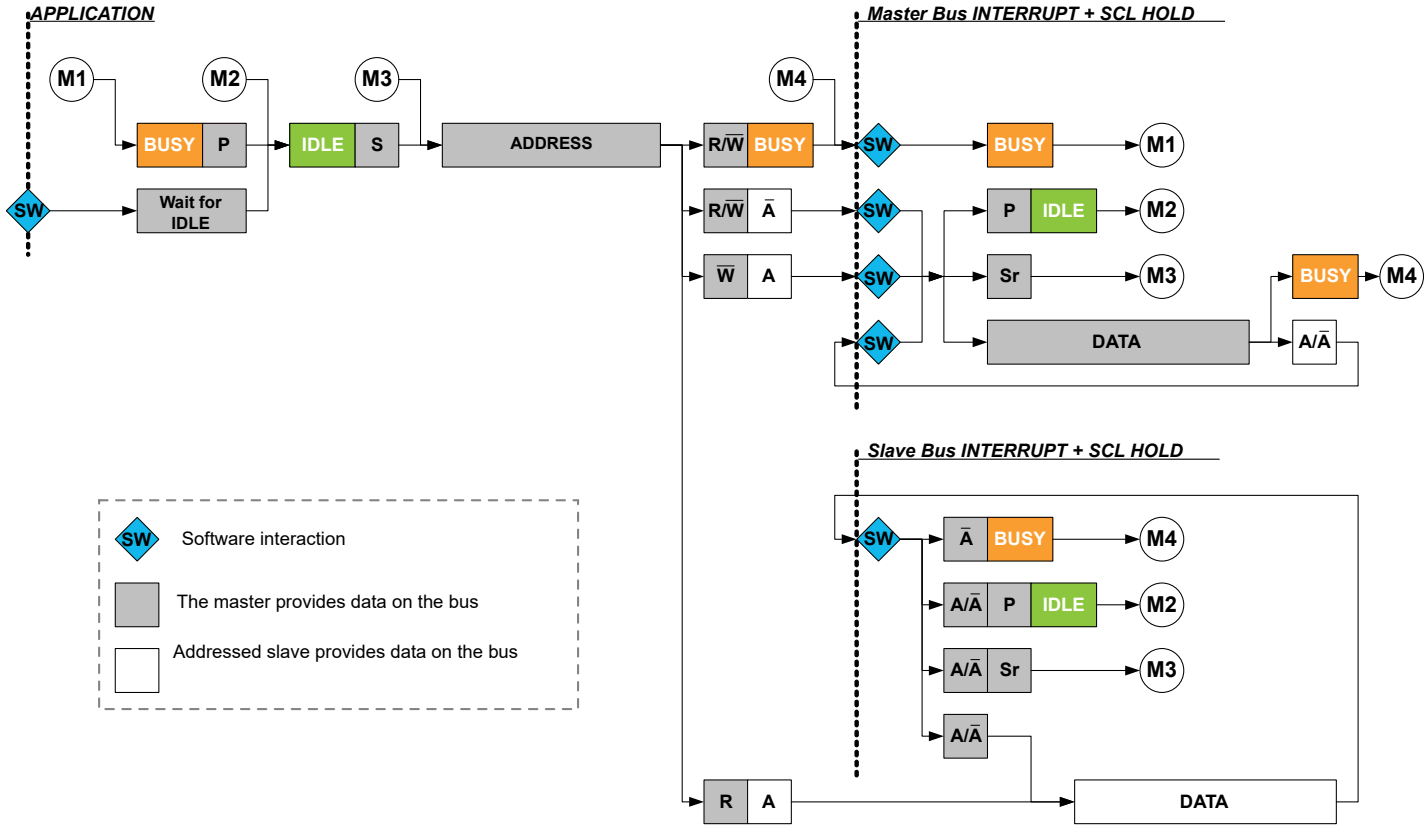
The I²C master is byte-oriented and interrupt based. The number of interrupts generated is kept at a minimum by automatic handling of most incidents. The software driver complexity and code size are reduced by auto-triggering of operations, and a special smart mode, which can be enabled by the Smart Mode Enable bit in the Control A register (CTRLA.SMEN).

The I²C master has two interrupt strategies.

When SCL Stretch Mode (CTRLA.SCLSM) is '0', SCL is stretched before or after the acknowledge bit . In this mode the I²C master operates according to Master Behavioral Diagram (SCLSM=0). The circles labelled "M*n*" (M1, M2..) indicate the nodes the bus logic can jump to, based on software or hardware interaction.

This diagram is used as reference for the description of the I²C master operation throughout the document.

Figure 37-5. I²C Master Behavioral Diagram (SCLSM=0)



In the second strategy (CTRLA.SCLSM=1), interrupts only occur after the ACK bit, as in Master Behavioral Diagram (SCLSM=1). This strategy can be used when it is not necessary to check DATA before acknowledging.

Note: I²C High-speed (*Hs*) mode requires CTRLA.SCLSM=1.

The missing ACK response can indicate that the I²C slave is busy with other tasks or sleeping. Therefore, it is not able to respond. In this event, the next step can be either issuing a stop condition (recommended) or resending the address packet by a repeated start condition. When using SMBus logic, the slave must ACK the address. If there is no response, it means that the slave is not available on the bus.

Case 3: Address packet transmit complete – Write packet, Master on Bus set

If the I²C master receives an acknowledge response from the I²C slave, INTFLAG.MB will be set and STATUS.RXNACK will be cleared. The clock hold is active at this point, preventing further activity on the bus.

In this case, the software implementation becomes highly protocol dependent. Three possible actions can enable the I²C operation to continue:

- Initiate a data transmit operation by writing the data byte to be transmitted into DATA.DATA.
- Transmit a new address packet by writing ADDR.ADDR. A repeated start condition will automatically be inserted before the address packet.
- Issue a stop condition, consequently terminating the transaction.

Case 4: Address packet transmit complete – Read packet, Slave on Bus set

If the I²C master receives an ACK from the I²C slave, the I²C master proceeds to receive the next byte of data from the I²C slave. When the first data byte is received, the Slave on Bus bit in the Interrupt Flag register (INTFLAG.SB) will be set and STATUS.RXNACK will be cleared. The clock hold is active at this point, preventing further activity on the bus.

In this case, the software implementation becomes highly protocol dependent. Three possible actions can enable the I²C operation to continue:

- Let the I²C master continue to read data by acknowledging the data received. ACK can be sent by software, or automatically in smart mode.
- Transmit a new address packet.
- Terminate the transaction by issuing a stop condition.

Note: An ACK or NACK will be automatically transmitted if smart mode is enabled. The Acknowledge Action bit in the Control B register (CTRLB.ACKACT) determines whether ACK or NACK should be sent.

37.6.2.4.3 Transmitting Data Packets

When an address packet with direction Master Write (see Figure 37-3) was transmitted successfully , INTFLAG.MB will be set. The I²C master will start transmitting data via the I²C bus by writing to DATA.DATA, and monitor continuously for packet collisions. I

If a collision is detected, the I²C master will lose arbitration and STATUS.ARBLOST will be set. If the transmit was successful, the I²C master will receive an ACK bit from the I²C slave, and STATUS.RXNACK will be cleared. INTFLAG.MB will be set in both cases, regardless of arbitration outcome.

It is recommended to read STATUS.ARBLOST and handle the arbitration lost condition in the beginning of the I²C Master on Bus interrupt. This can be done as there is no difference between handling address and data packet arbitration.

STATUS.RXNACK must be checked for each data packet transmitted before the next data packet transmission can commence. The I²C master is not allowed to continue transmitting data packets if a NACK is received from the I²C slave.

37.6.4.2 Interrupts

The I²C slave has the following interrupt sources. These are asynchronous interrupts. They can wake-up the device from any sleep mode:

- Error (ERROR)
- Data Ready (DRDY)
- Address Match (AMATCH)
- Stop Received (PREC)

The I²C master has the following interrupt sources. These are asynchronous interrupts. They can wake-up the device from any sleep mode:

- Error (ERROR)
- Slave on Bus (SB)
- Master on Bus (MB)

Each interrupt source has its own interrupt flag. The interrupt flag in the Interrupt Flag Status and Clear register (INTFLAG) will be set when the interrupt condition is meet. Each interrupt can be individually enabled by writing '1' to the corresponding bit in the Interrupt Enable Set register (INTENSET), and disabled by writing '1' to the corresponding bit in the Interrupt Enable Clear register (INTENCLR). An interrupt request is generated when the interrupt flag is set and the corresponding interrupt is enabled. The interrupt request active until the interrupt flag is cleared, the interrupt is disabled or the I²C is reset. See the INTFLAG register for details on how to clear interrupt flags.

The value of INTFLAG indicates which interrupt is executed. Note that interrupts must be globally enabled for interrupt requests. Refer to *Nested Vector Interrupt Controller* for details.

37.6.4.3 Events

Not applicable.

37.6.5 Sleep Mode Operation

I²C Master Operation

The generic clock (GCLK_SERCOMx_CORE) will continue to run in Idle Sleep mode. If the Run In Standby bit in the Control A register (CTRLA.RUNSTDBY) is '1', the GLK_SERCOMx_CORE will also run in standby Sleep mode. Any interrupt can wake up the device.

If CTRLA.RUNSTDBY=0, the GLK_SERCOMx_CORE will be disabled after any ongoing transaction is finished. Any interrupt can wake up the device.

I²C Slave Operation

Writing CTRLA.RUNSTDBY=1 will allow the Address Match interrupt to wake up the device.

When CTRLA.RUNSTDBY=0, all receptions will be dropped.

37.6.6 Synchronization

Due to asynchronicity between the main clock domain and the peripheral clock domains, some registers need to be synchronized when written or read.

The following bits are synchronized when written:

- Software Reset bit in the CTRLA register (CTRLA.SWRST)
- Enable bit in the CTRLA register (CTRLA.ENABLE)
- Command bits in CTRLB register (CTRLB.CMD)

38.7.1.11 Debug Control

Name: DBGCTRL
Offset: 0x0F
Reset: 0x00
Property: PAC Write-Protection

Bit	7	6	5	4	3	2	1	0
								DBGRUN
Access								R/W
Reset								0

Bit 0 – DBGRUN Run in Debug Mode
This bit is not affected by a software Reset, and should not be changed by software while the TC is enabled.

Value	Description
0	The TC is halted when the device is halted in debug mode.
1	The TC continues normal operation when the device is halted in debug mode.

41.8.15 Gain Correction

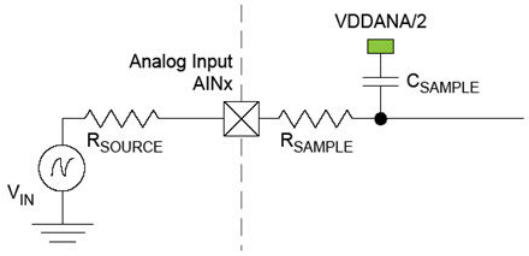
Name: GAINCORR
Offset: 0x12
Reset: 0x0000
Property: PAC Write-Protection, Write-Synchronized

Bit	15	14	13	12	11	10	9	8
					GAINCORR[11:8]			
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit	7	6	5	4	3	2	1	0
	GAINCORR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 11:0 – GAINCORR[11:0] Gain Correction Value
If CTRLC.CORREN=1, these bits define how the ADC conversion result is compensated for gain error before being written to the result register. The gain correction is a fractional value, a 1-bit integer plus an 11-bit fraction, and therefore ½ <= GAINCORR < 2. GAINCORR values range from 0.10000000000 to 1.11111111111.

Figure 46-2. ADC Analog Input AINx



The minimum sampling time $t_{samplehold}$ for a given R_{source} can be found using this formula:

$$t_{samplehold} \geq \left(R_{sample} + R_{source}\right) \times C_{sample} \times \left(n + 2\right) \times \ln\left(2\right)$$

For 12-bit accuracy:

$$t_{samplehold} \geq \left(R_{sample} + R_{source}\right) \times C_{sample} \times 9.7$$

where $t_{samplehold} \geq \frac{1}{2 \times f_{ADC}}$.

46.11.5 Digital-to-Analog Converter (DAC) Characteristics

Table 46-26. Operating Conditions(1)

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
AVREF	External reference voltage		1	-	VDDANA-0.6	V
	Internal reference voltage 1		-	1	-	V
	Internal reference voltage 2		-	VDDANA	-	V
	Linear output voltage range		0.05	-	VDDANA-0.05	V
	Minimum resistive load		5	-	-	kOhm
	Maximum capacitance load		-	-	100	pF
IDD	DC supply current(2)	Voltage pump disabled	-	175	247	µA

Note:

1. The values in this table are based on specifications otherwise noted.
2. These values are based on characterization. These values are not covered in test limits in production.

Table 46-27. Clock and Timing

Parameter	Conditions		Min.	Typ.	Max.	Units
Conversion rate	Cload=100pF Rload > 5kOhm	Normal mode			350	ksps
		For DDATA=+/-1			1000	
Startup time	VDDANA > 2.6V	VDDANA > 2.6V	-	-	2.85	µs
	VDDANA < 2.6V	VDDANA < 2.6V	-	-	10	µs

Note: These values are based on simulation. These values are not covered by test limits in production or characterization.

Table 47-3. Standby and Off Mode Current Consumption

Mode	Conditions	Regulator Mode	Vcc	Ta	Typ.	Max.	Units
STANDBY	All 16kB RAM retained, PDSW domain in active state	LPEFF Disable	1,8V	25°C	1.3	3.5	µA
				125°C	121.7	304.8	
		LPEFF Enable	3,3V	25°C	1.1	3.0	
				125°C	74.5	282.6	
		BUCK in standby PL0 (VREG.RUNSTDBY=1 and VREG.STDBYPL0=1)	1,8V	25°C	1.2	2.9	
				125°C	78.0	188.7	
			3,3V	25°C	1.1	2.2	
				125°C	50.9	122.9	µA
	All 16kB RAM retained, PDSW domain in retention	LPEFF Disable	1,8V	25°C	0.6	1.1	
				125°C	27.1	81.0	
		LPEFF Enable	3,3V	25°C	0.5	1.0	
				125°C	23.1	52.8	
		BUCK in standby PL0 (VREG.RUNSTDBY=1 and VREG.STDBYPL0=1)	1,8V	25°C	0.8	1.1	
				125°C	23.0	53.7	
			3,3V	25°C	0.8	1.5	
				125°C	17.3	37.6	
	12 kB RAM retained,PDSW domain in retention	LPEFF Disable	1,8V	25°C	0.6	1.1	
				125°C	25.5	73.7	
		LPEFF Enable	3,3V	25°C	0.5	1.0	
				125°C	21.6	48.8	
		Buck in standby PL0 (VREG.RUNSTDBY=1 and VREG.STDBYPL0=1)	1,8V	25°C	0.7	1.1	
				125°C	21.5	50.5	
			3,3V	25°C	0.8	1.5	
				125°C	16.4	35.4	
	8kB RAM retained,PDSW domain in retention	LPEFF Disable	1,8V	25°C	0.5	1.0	µA
				125°C	23.8	67.1	
		LPEFF Enable	3,3V	25°C	0.5	0.9	
				125°C	20.2	45.4	
		BUCK in standby PL0 (VREG.RUNSTDBY=1 and VREG.STDBYPL0=1)	1,8V	25°C	0.7	1.0	
				125°C	19.9	46.5	
			3,3V	25°C	0.7	1.4	

Symbol	Parameters	Conditions		Measurements			Unit
				Min	Typ	Max	
			Vref=Vddana=1.6V to 3.6V	-	+/-0.15	+/-0.9	
Offset	Offset Error	without offset compensation	Vref=1V Vddana=1.6V to 3.6V	-	+/-0.13	+/-15.8	mV
			Vref=3V Vddana=1.6V to 3.6V	-	+/-1.82	+/-14.9	
			Bandgap Reference	-	+/-2.07	+/-15.8	
			Vref=Vddana=1.6V to 3.6V	-	+/-1.82	+/-15.3	
SFDR	Spurious Free Dynamic Range	Fs = 1MHz / Fin = 13 kHz / Full range Input signal	Vref=2.0V Vddana=3.0V	58.1	70.5	77.5	dB
SINAD	Signal to Noise and Distortion ratio			56.7	63.4	66.5	
SNR	Signal to Noise ratio			56.5	64.4	67.1	
THD	Total Harmonic Distortion			-74.7	-68.7	-57.7	
	Noise RMS	External Reference voltage	External Reference voltage	-	0.42	-	mV

Note:

1. These are given without any ADC oversampling and decimation features enabled.

Table 49-10. Device and Package Maximum Weight

187.322	mg

Table 49-11. Package Characteristics

Moisture Sensitivity Level	MSL3

Table 49-12. Package Reference

JEDEC Drawing Reference	MO-150
JESD97 Classification	E3

Figure 50-13. 20-pin IDC JTAG Connector

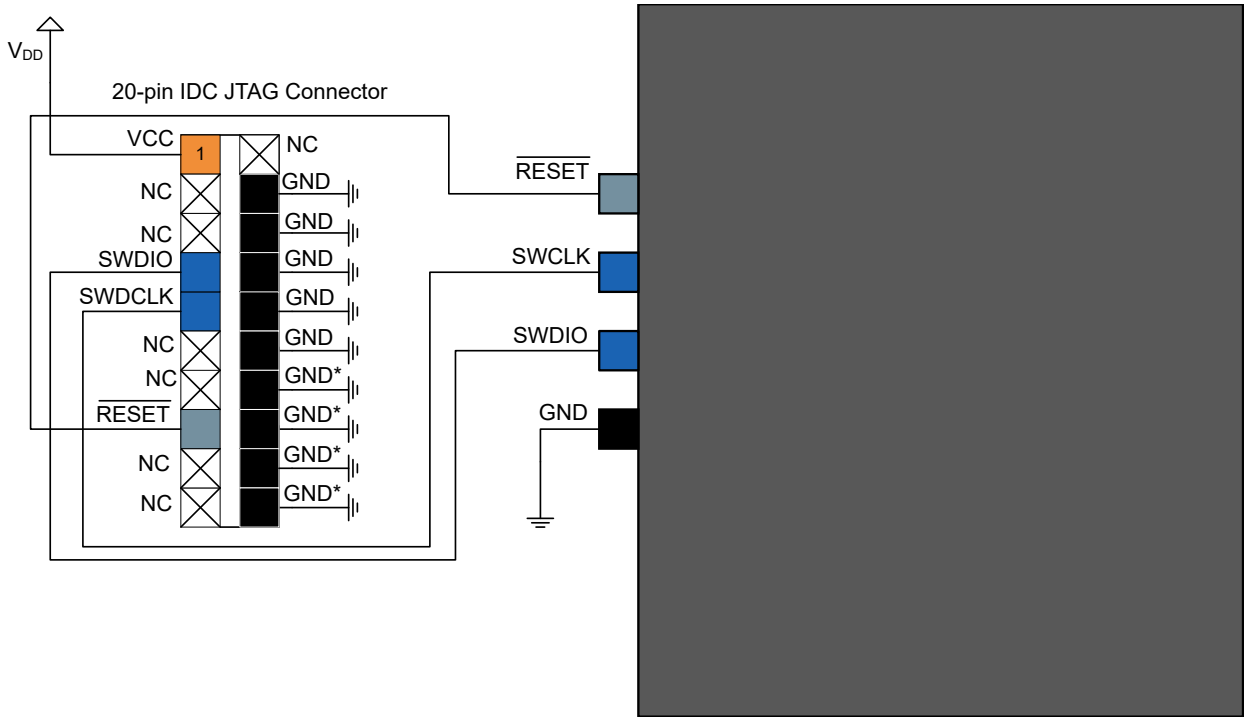


Table 50-9. 20-pin IDC JTAG Connector

Header Signal Name	Description
SWDCLK	Serial wire clock pin
SWDIO	Serial wire bidirectional data pin
$\overline{\text{RESET}}$	Target device reset pin, active low
VCC	Target voltage sense, should be connected to the device V_{DD}
GND	Ground
GND*	These pins are reserved for firmware extension purposes. They can be left unconnected or connected to GND in normal debug environment. They are not essential for SWD in general.

50.8 Peripherals Considerations

ADC Accuracy

The ADC accuracy may depend on different parameters, such as its input sources, as well as its conversion speed.

Please refer to the *Analog-to-Digital Converter (ADC) Characteristics* section in the *Electrical Characteristics* chapters for more details.