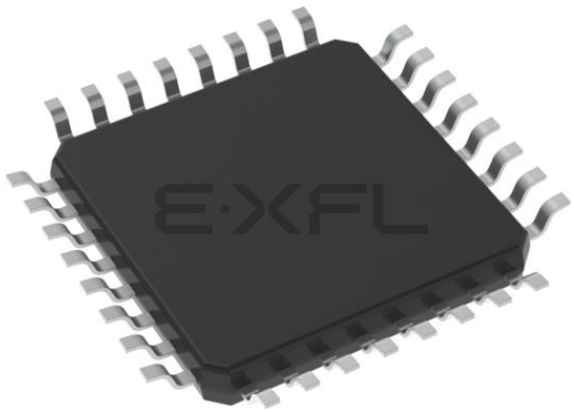

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M23
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	25
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.63V
Data Converters	A/D 10x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	32-TQFP
Supplier Device Package	32-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsaml11e15a-aft

Pin				Pin Name	Supply	A	B(1)						C(2)(3)	D(2)(3)	E	G	H	I	Reset State
SSOP24	VQFN24	WLCSP32	TQFP32 / VQFN32			EIC	REF	ADC	AC	PTC	DAC	OPAMP	SERCOM	SERCOM ALTERNATIVE	TC	RTC/ Debug	AC/ GCLK	CCL	
		C4	7	PA06	VDDANA	EXTINT[6]		AIN[4]	AIN[2]	XY[5]		OA0POS		SERCOM0/ PAD[2]	TC1/ WO[0]			IN[2]	I/O, Hi-Z
		B5	8	PA07	VDDANA	EXTINT[7]		AIN[5]	AIN[3]			OA0OUT		SERCOM0/ PAD[3]	TC1/ WO[1]			OUT[0]	I/O, Hi-Z
11	8	B6	9	VDDANA															-
12	9	C6	10	GNDANA															-
13	10	D4	11	PA08	VDDIO	NMI		AIN[6]		XY[6]			SERCOM1/ PAD[0]	SERCOM2/ PAD[0]		RTC/ IN[0]		IN[3]	I/O, Hi-Z
		D6	12	PA09	VDDIO	EXTINT[0]		AIN[7]		XY[7]			SERCOM1/ PAD[1]	SERCOM2/ PAD[1]		RTC/ IN[1]		IN[4]	I/O, Hi-Z
		C5	13	PA10	VDDIO	EXTINT[1]		AIN[8]		XY[8]			SERCOM1/ PAD[2]	SERCOM2/ PAD[2]			GCLK_IO[4]	IN[5]	I/O, Hi-Z
		D5	14	PA11	VDDIO	EXTINT[2]		AIN[9]		XY[9]			SERCOM1/ PAD[3]	SERCOM2/ PAD[3]			GCLK_IO[3]	OUT[1]	I/O, Hi-Z
14	11	E6	15	PA14 / XOSC	VDDIO	EXTINT[3]				XY[10]			SERCOM2/ PAD[2]	SERCOM0/ PAD[2]	TC0/ WO[0]		GCLK_IO[0]		I/O, Hi-Z
15	12	E5	16	PA15 / XOUT	VDDIO	EXTINT[4]				XY[11]			SERCOM2/ PAD[3]	SERCOM0/ PAD[3]	TC0/ WO[1]		GCLK_IO[1]		I/O, Hi-Z
16	13	D3	17	PA16(4)	VDDIO	EXTINT[5]				XY[12]			SERCOM1/ PAD[0]	SERCOM0/ PAD[0]		RTC/ IN[2]	GCLK_IO[2]	IN[0]	I/O, Hi-Z
17	14	F5	18	PA17(4)	VDDIO	EXTINT[6]				XY[13]			SERCOM1/ PAD[1]	SERCOM0/ PAD[1]		RTC/ IN[3]	GCLK_IO[3]	IN[1]	I/O, Hi-Z
18	15	E4	19	PA18	VDDIO	EXTINT[7]				XY[14]			SERCOM1/ PAD[2]	SERCOM0/ PAD[2]	TC2/ WO[0]	RTC/ OUT[0]	AC/ CMP[0]	IN[2]	I/O, Hi-Z
19	16	E3	20	PA19	VDDIO	EXTINT[0]				XY[15]			SERCOM1/ PAD[3]	SERCOM0/ PAD[3]	TC2/ WO[1]	RTC/ OUT[1]	AC/ CMP[1]	OUT[0]	I/O, Hi-Z
20	17	F4	21	PA22(4)	VDDIO	EXTINT[1]				XY[16]			SERCOM0/ PAD[0]	SERCOM2/ PAD[0]	TC0/ WO[0]	RTC/ OUT[2]	GCLK_IO[2]		I/O, Hi-Z
21	18	F3	22	PA23(4)	VDDIO	EXTINT[2]				XY[17]			SERCOM0/ PAD[1]	SERCOM2/ PAD[1]	TC0/ WO[1]	RTC/ OUT[3]	GCLK_IO[1]		I/O, Hi-Z
		F2	23	PA24	VDDIO	EXTINT[3]							SERCOM0/ PAD[2]	SERCOM2/ PAD[2]	TC1/ WO[0]				I/O, Hi-Z
		E2	24	PA25	VDDIO	EXTINT[4]							SERCOM0/ PAD[3]	SERCOM2/ PAD[3]	TC1/ WO[1]				I/O, Hi-Z
		D2	25	PA27	VDDIO	EXTINT[5]											GCLK_IO[0]		I/O, Hi-Z
22	19	C2	26	$\overline{\text{RESET}}$	VDDIO														I, PU
23	20	E1	27	VDDCORE															-
24	21	D1	28	GND															-
1	22	C1	29	VDDOUT															-
2	23	B1	30	VDDIO															-

5. Signal Descriptions List

The following table provides details on signal names classified by peripherals.

Table 5-1. Signal Descriptions List

Signal Name	Function	Type
Generic Clock Generator - GCLK		
GCLK_IO[4:0]	Generators Clock Source (Input) or Generic Clock Signal (Output)	Digital I/O
Oscillators Control - OSCCTRL		
XIN	Crystal Oscillator or External Clock Input	Analog Input (Crystal Oscillator)/Digital Input (External Clock)
XOUT	Crystal Oscillator Output	Analog Output
32 kHz Oscillators Control - OSC32KCTRL		
XIN32	32.768 kHz Crystal Oscillator or External Clock Input	Analog Input (Crystal Oscillator)/Digital Input (External Clock)
XOUT32	32.768 kHz Crystal Oscillator Output	Analog Output
Serial Communication Interface - SERCOMx		
PAD[3:0]	General SERCOM Pins	Digital I/O
Timer Counter - TCx		
WO[1:0]	Capture Inputs or Waveform Outputs	Digital I/O
Real Timer Clock - RTC		
IN[3:0]	Tamper Detection Inputs	Digital Input
OUT[3:0]	Tamper Detection Outputs	Digital Output
Analog Comparators - AC		
AIN[3:0]	AC Comparator Inputs	Analog Input
CMP[1:0]	AC Comparator Outputs	Digital Output
Analog Digital Converter - ADC		
AIN[9:0]	ADC Input Channels	Analog Input
VREFA(1)	ADC External Reference Voltage A	Analog Input
VREFB	ADC External Reference Voltage B	Analog Input
Digital Analog Converter - DAC		
VOUT	DAC Voltage Output	Analog Output
VREFA(1)	DAC External Reference Voltage A	Analog Input
Operational Amplifier - OPAMP		
OA[2:0]NEG	OPAMP Negative Inputs	Analog Input
OA[2:0]POS	OPAMP Positive Inputs	Analog Input
OA0OUT / OA2OUT	OPAMP Outputs	Analog Output
Peripheral Touch Controller - PTC		
XY[19:0]	X-lines and Y-lines	Digital Output (X-line) /Analog I/O (Y-line)
Custom Control Logic - CCL		
IN[5:0]	Inputs to lookup table	Digital Output
OUT[1:0]	Outputs from lookup table	Digital Input

10. Memories

10.1 Embedded Memories

The 32-bit physical memory address space is mapped as follows:

Table 10-1. Memory Sizes

Memory	Base Address	Size [KB]			
		SAM L11x16(1) SAM L10x16(1)	SAM L11x15(1) SAM L10x15(1)	SAM L11x14 (1)	SAM L10x14 (1)
Flash	0x00000000	64	32	16	16
Data Flash	0x00400000	2	2	2	2
SRAM	0x20000000	16	8	8	4
Boot ROM	0x02000000	8	8	8	8

Note: 1. x = E or D.

10.1.1 Flash

SAM L10/L11 devices embed 16 KB, 32 KB or 64 KB of internal Flash mapped at address 0x0000 0000.

The Flash has a 512-byte (64 lines of 8 bytes) direct-mapped cache which is disabled by default after power up.

The Flash is organized into rows, where each row contains four pages. The Flash has a row-erase and a page-write granularity.

Table 10-2. Flash Memory Parameters

Device	Memory Size [KB]	Number of Rows	Row size [Bytes]	Number of Pages	Page size [Bytes]
SAM L11x16 / SAM L10x16 (1)	64	256	256	1024	64
SAM L11x15 / SAM L10x15 (1)	32	128	256	512	64
SAM L11x14 / SAM L10x14 (1)	16	64	256	256	64

Note:

1. x = E or D.

The Flash is divided in different regions. Each region has a dedicated lock bit preventing from writing and erasing pages on it. Refer to the NVM Memory Organization figures in the *NVMCTRL* chapter to get the different regions definition.

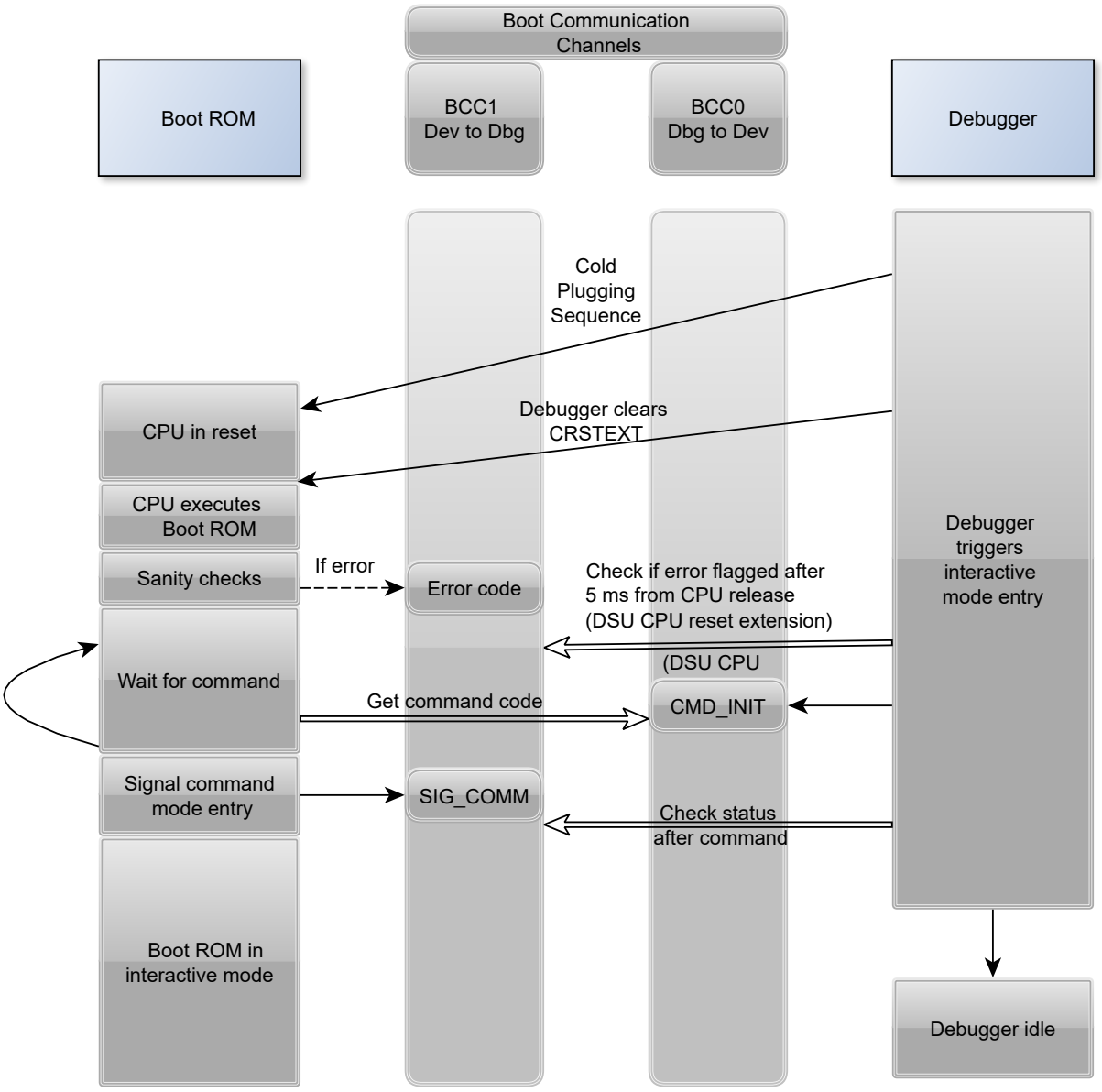
Note: The regions size is configured by the Boot ROM at device startup by reading the NVM Boot Configuration Row (BOCOR). Please refer to the 14. Boot ROM chapter for more information.

Table 10-3. Flash Lock Regions Parameters

Device	SAM L10	SAM L11
Number of FLASH Lock Regions	2	4
Regions Name	Flash Boot / Flash Application	Flash Boot Secure / Flash Boot Non-Secure Flash Application Secure / Flash Application Non-Secure

14.4.5.1.1 CMD_INIT

Figure 14-7. CMD_INIT Flow diagram



14.4.5.2 Exit Interactive Mode (CMD_EXIT)

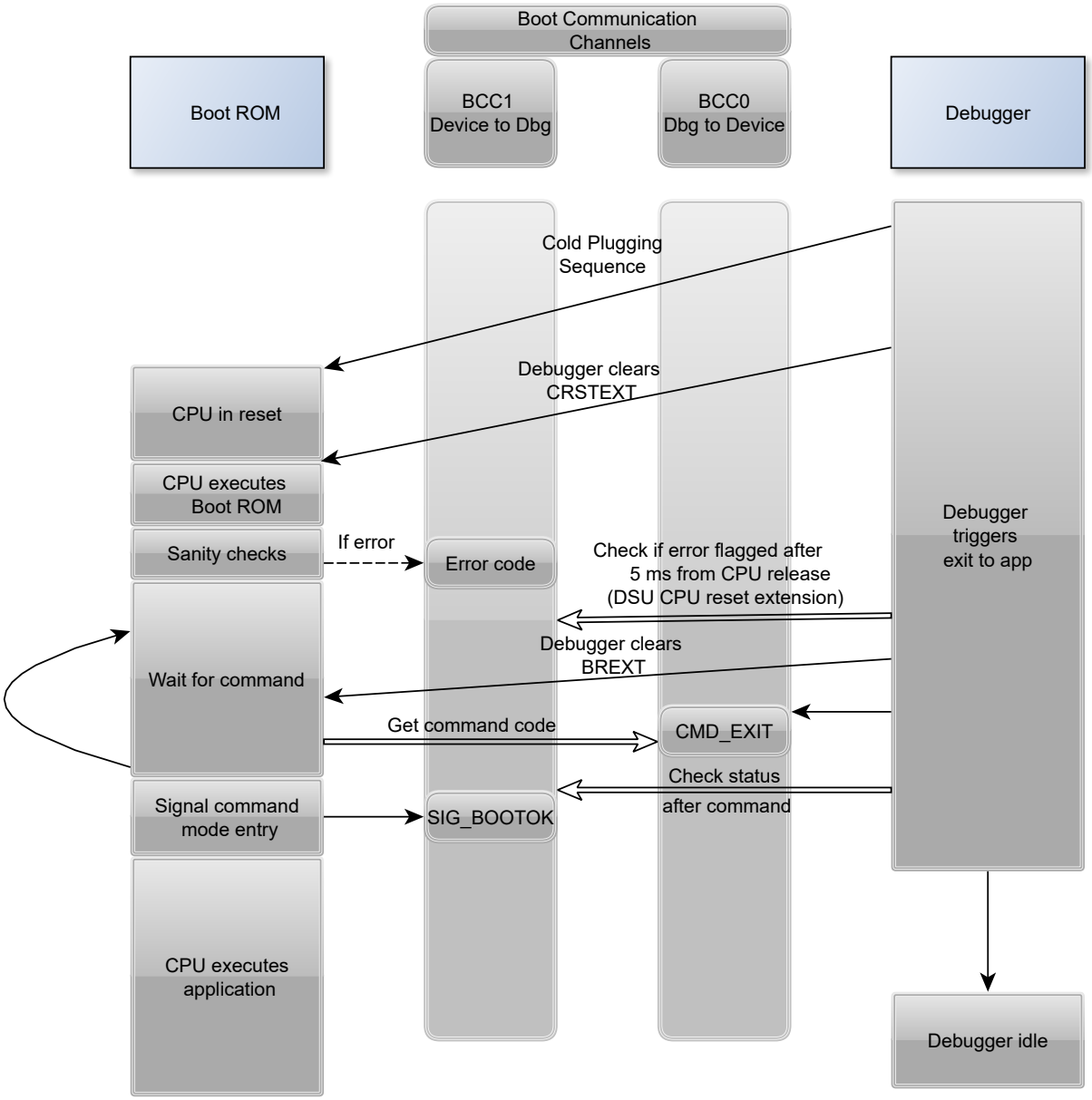
This command allows exiting the Boot Interactive mode.

Exiting the Boot Interactive mode allows to jump to one of the following:

- The Application
- The CPU Park Mode

14.4.5.2.1 CMD_EXIT

Figure 14-8. CMD_EXIT to APP flow diagram



This bit is set when a DSU operation is completed.

interrupt flag bit in the Interrupt Flag register (INTFLAG.CLKFAIL) are set. If the CLKFAIL bit in the Interrupt Enable Set register (INTENSET.CLKFAIL) is set, an interrupt is generated as well. If the Event Output enable bit in the Event Control register (EVCTRL.CFDEO) is set, an output event is generated, too.

After a clock failure was issued the monitoring of the XOSC clock is continued, and the Clock Failure Detector status bit in the Status register (STATUS.CLKFAIL) reflects the current XOSC activity.

Clock Switch

When a clock failure is detected, the XOSC clock is replaced by the safe clock in order to maintain an active clock during the XOSC clock failure. The safe clock source is the OSC16M oscillator clock. The safe clock source can be scaled down by a configurable prescaler to ensure that the safe clock frequency does not exceed the operating conditions selected by the application. When the XOSC clock is switched to the safe clock, the Clock Switch bit in the Status register (STATUS.CLKSW) is set.

When the CFD has switched to the safe clock, the XOSC is not disabled. If desired, the application must take the necessary actions to disable the oscillator. The application must also take the necessary actions to configure the system clocks to continue normal operations.

If the application can recover the XOSC, the application can switch back to the XOSC clock by writing a '1' to Switch Back Enable bit in the Clock Failure Control register (XOSCCTRL.SWBACK). Once the XOSC clock is switched back, the Switch Back bit (XOSCCTRL.SWBACK) is cleared by hardware.

Prescaler

The CFD has an internal configurable prescaler to generate the safe clock from the OSC16M oscillator. The prescaler size allows to scale down the OSC16M oscillator so the safe clock frequency is not higher than the XOSC clock frequency monitored by the CFD. The division factor is 2^P, with P being the value of the CFD Prescaler bits in the CFD Prescaler Register (CFDPRESC.CFDPRESC).

Example 23-1.

For an external crystal oscillator at 0.4 MHz and the OSC16M frequency at 16 MHz, the CFDPRESC.CFDPRESC value should be set scale down by more than factor 16/0.4=80, for example 128, for a safe clock of adequate frequency.

Event

If the Event Output Enable bit in the Event Control register (EVCTRL.CFDEO) is set, the CFD clock failure will be output on the Event Output. When the CFD is switched to the safe clock, the CFD clock failure will not be output on the Event Output.

Sleep Mode

The CFD is halted depending on configuration of the XOSC and the peripheral clock request. For further details, refer to the Sleep Behavior table above. The CFD interrupt can be used to wake up the device from sleep modes.

23.6.4 16MHz Internal Oscillator (OSC16M) Operation

The OSC16M is an internal oscillator operating in open-loop mode and generating 4, 8, 12, or 16MHz frequency. The OSC16M frequency is selected by writing to the Frequency Select field in the OSC16M register (OSC16MCTRL.FSEL). OSC16M is enabled by writing '1' to the Oscillator Enable bit in the OSC16M Control register (OSC16MCTRL.ENABLE), and disabled by writing a '0' to this bit. Frequency selection must be done when OSC16M is disabled.

27.8.16 Tamper Control B

Name: TAMPCTRLB
Offset: 0x6C
Reset: 0x00000000
Property: PAC Write-Protection, Enable-Protected

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
					ALSI3	ALSI2	ALSI1	ALSI0
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bits 0, 1, 2, 3 – ALSI Active Layer Internal Select n

Value	Description
0	Active layer Protection is monitoring the RTC signal using INn and OUTn tamper pins
1	Active layer Protection is monitoring the RTC signal on the TrustRAM shield

27.12.12 Alarm Mask in Clock/Calendar mode (CTRLA.MODE=2)

Name: MASK
Offset: 0x24
Reset: 0x00
Property: PAC Write-Protection, Write-Synchronized

Bit	7	6	5	4	3	2	1	0
						SEL[2:0]		
Access						R/W	R/W	R/W
Reset						0	0	0

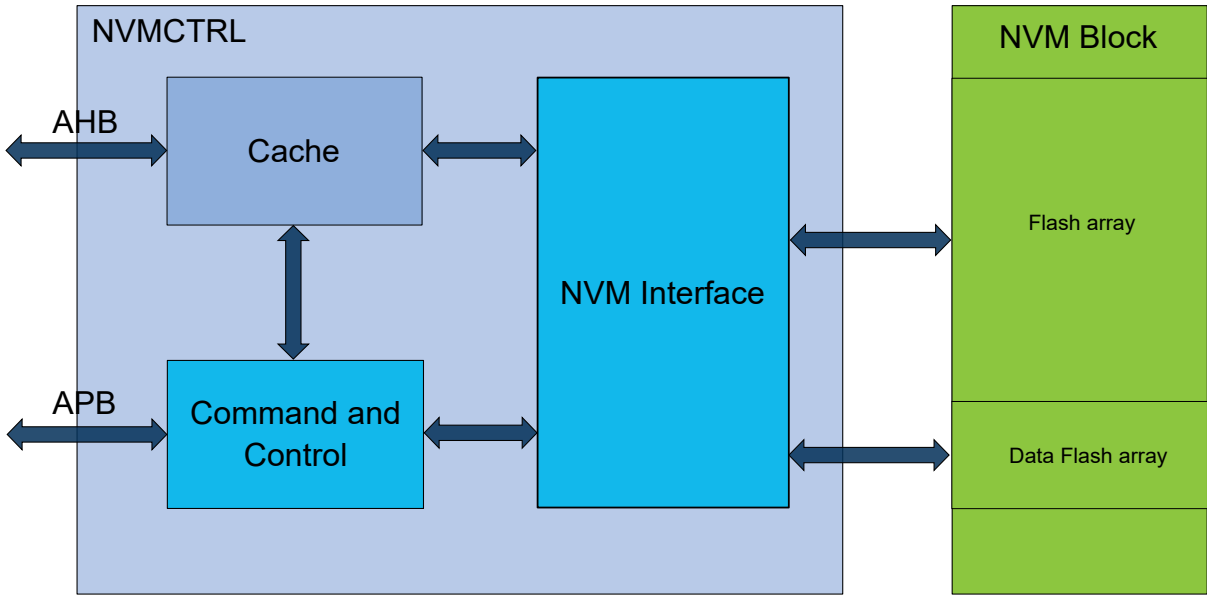
Bits 2:0 – SEL[2:0] Alarm Mask Selection
These bits define which bit groups of ALARM are valid.

Value	Name	Description
0x0	OFF	Alarm Disabled
0x1	SS	Match seconds only
0x2	MMSS	Match seconds and minutes only
0x3	HHMMSS	Match seconds, minutes, and hours only
0x4	DDHHMMSS	Match seconds, minutes, hours, and days only
0x5	MMDDHHMMSS	Match seconds, minutes, hours, days, and months only
0x6	YYMMDDHHMMSS	Match seconds, minutes, hours, days, months, and years
0x7	-	Reserved

Value	Description
0	EXTINTx is secure.
1	EXTINTx is non-secure.

30.3 Block Diagram

Figure 30-1. Block Diagram



30.4 Signal Description

Not applicable.

30.5 Product Dependencies

In order to use this peripheral, other parts of the system must be configured correctly, as described in the following sections.

30.5.1 Power Management

The NVMCTRL will continue to operate in any sleep mode where the selected source clock is running. The NVMCTRL interrupts can be used to wake up the device from sleep modes.

The Power Manager will automatically put the NVM block into a low-power state when entering sleep mode. This is based on the Control B register (CTRLB) SLEEPPRM bit setting. Refer to the 30.8.2 CTRLB.SLEEPPRM register description for more details. The NVM block goes into low-power mode automatically when the device enters STANDBY mode regardless of SLEEPPRM. The NVM Page Buffer is lost when the NVM goes into low power mode therefore a write command must be issued prior entering the NVM low power mode. NVMCTRL SLEEPPRM can be disabled to avoid such loss when the CPU goes into sleep except if the device goes into STANDBY mode for which there is no way to retain the Page Buffer.

Related Links

22. PM – Power Manager

30.5.2 Clocks

Two synchronous clocks are used by the NVMCTRL. One is provided by the AHB bus (CLK_NVMCTRL_AHB) and the other is provided by the APB bus (CLK_NVMCTRL_APB). For higher

30.8.5 Interrupt Enable Clear

Name: INTENCLR
Offset: 0x0C
Reset: 0x00
Property: PAC Write-Protection, Write-Mix-Secure

Important: For **SAM L11 Non-Secure** accesses, write accesses (W*) are allowed only if Non-Secure Write is set in the NONSEC register.

This register allows the user to disable an interrupt without doing a read-modify-write operation. Changes in this register will also be reflected in the Interrupt Enable Set register (INTENSET).

Bit	7	6	5	4	3	2	1	0
			NSCHK	KEYE	NVME	LOCKE	PROGE	DONE
Access			RW/RW*/RW	RW/RW*/RW	RW/RW*/RW	RW/RW*/RW	RW/RW*/RW	RW/RW*/RW
Reset			0	0	0	0	0	0

Bit 5 – NSCHK Non-secure Check Interrupt Enable
Writing a '0' to this bit has no effect.

Writing a '1' to this bit clears the NSCHK interrupt enable.

This bit will read as the current value of the NSCHK interrupt enable.

Bit 4 – KEYE Key Error Interrupt Enable
Writing a '0' to this bit has no effect.

Writing a '1' to this bit clears the KEYE interrupt enable.

This bit will read as the current value of the KEYE interrupt enable.

Bit 3 – NVME NVM internal Error Interrupt Clear
Writing a '0' to this bit has no effect.

Writing a '1' to this bit clears the NVME interrupt enable.

This bit will read as the current value of the NVME interrupt enable.

Bit 2 – LOCKE Lock Error Interrupt Enable
Writing a '0' to this bit has no effect.

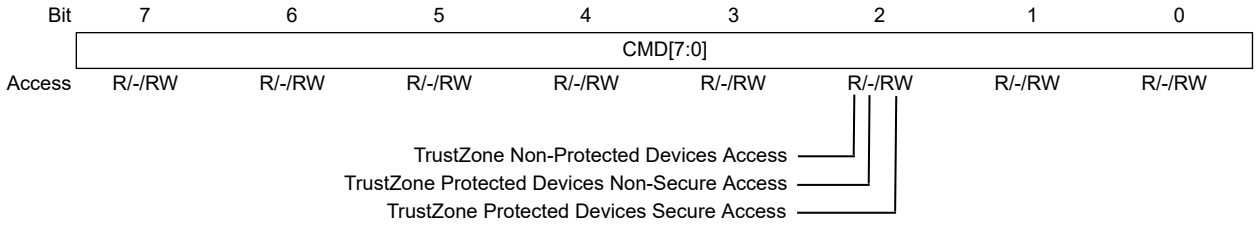
Writing a '1' to this bit sets the LOCKE interrupt enable.

This bit will read as the current value of the LOCKE interrupt enable.

Bit 1 – PROGE Programming Error Interrupt Clear
Writing a '0' to this bit has no effect.

Writing a '1' to this bit clears the PROGE interrupt enable.

This bit will read as the current value of the PROGE interrupt enable.



Related Links

15. PAC - Peripheral Access Controller

33.4.8 Register Access Protection

Related Links

22. PM – Power Manager

34.5.3 Clocks

The SERCOM bus clock (CLK_SERCOMx_APB) can be enabled and disabled in the Main Clock Controller. Refer to *Peripheral Clock Masking* for details and default status of this clock.

The SERCOM uses two generic clocks: GCLK_SERCOMx_CORE and GCLK_SERCOMx_SLOW. The core clock (GCLK_SERCOMx_CORE) is required to clock the SERCOM while working as a master. The slow clock (GCLK_SERCOMx_SLOW) is only required for certain functions. See specific mode chapters for details.

These clocks must be configured and enabled in the Generic Clock Controller (GCLK) before using the SERCOM.

The generic clocks are asynchronous to the user interface clock (CLK_SERCOMx_APB). Due to this asynchronicity, writing to certain registers will require synchronization between the clock domains. Refer to 34.6.8 Synchronization for details.

Related Links

18. GCLK - Generic Clock Controller
19. MCLK – Main Clock

34.5.4 DMA

The DMA request lines are connected to the DMA Controller (DMAC). The DMAC must be configured before the SERCOM DMA requests are used.

Related Links

28. DMAC – Direct Memory Access Controller

34.5.5 Interrupts

The interrupt request line is connected to the Interrupt Controller (NVIC). The NVIC must be configured before the SERCOM interrupts are used.

34.5.6 Events

Not applicable.

34.5.7 Debug Operation

When the CPU is halted in debug mode, this peripheral will continue normal operation. If the peripheral is configured to require periodical service by the CPU through interrupts or similar, improper operation or data loss may result during debugging. This peripheral can be forced to halt operation during debugging - refer to the Debug Control (DBGCTRL) register for details.

34.5.8 Register Access Protection

All registers with write-access can be write-protected optionally by the Peripheral Access Controller (PAC), except for the following registers:

- Interrupt Flag Clear and Status register (INTFLAG)
- Status register (STATUS)
- Data register (DATA)
- Address register (ADDR)

If CMD 0x1 is issued, a repeated start will be issued followed by the transmission of the current address in ADDR.ADDR. If another address is desired, ADDR.ADDR must be written instead of the CMD bits. This will trigger a repeated start followed by transmission of the new address.

Issuing a command will set the System Operation bit in the Synchronization Busy register (SYNCBUSY.SYSOP).

Table 37-4. Command Description

CMD[1:0]	Direction	Action
0x0	X	(No action)
0x1	X	Execute acknowledge action succeeded by repeated Start
0x2	0 (Write)	No operation
	1 (Read)	Execute acknowledge action succeeded by a byte read operation
0x3	X	Execute acknowledge action succeeded by issuing a stop condition

These bits are not enable-protected.

Bit 9 – QCEN Quick Command Enable
This bit is not write-synchronized.

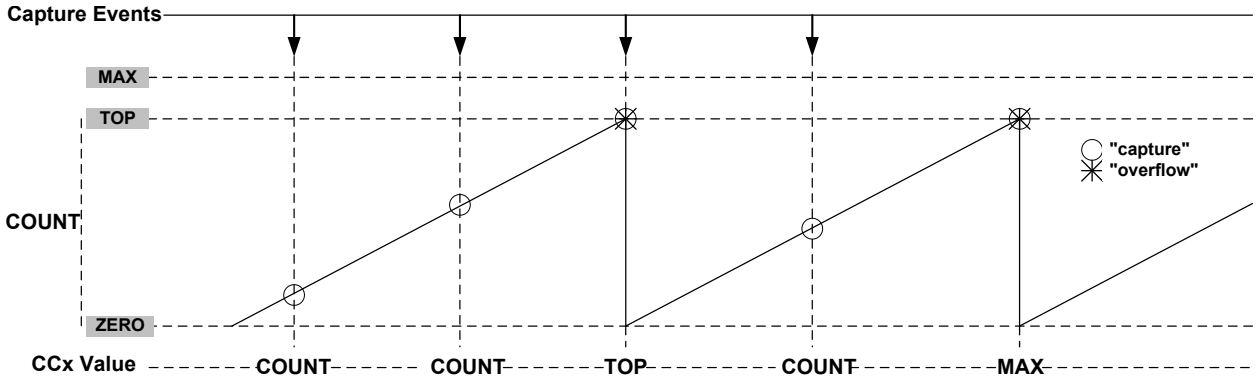
Value	Description
0	Quick Command is disabled.
1	Quick Command is enabled.

Bit 8 – SMEN Smart Mode Enable
When smart mode is enabled, acknowledge action is sent when DATA.DATA is read.

This bit is not write-synchronized.

Value	Description
0	Smart mode is disabled.
1	Smart mode is enabled.

Figure 38-15. Time-Stamp



38.6.4 DMA Operation

The TC can generate the following DMA requests:

- Overflow (OVF): the request is set when an update condition (overflow, underflow or re-trigger) is detected, the request is cleared by hardware on DMA acknowledge.
- Match or Capture Channel x (MCx): for a compare channel, the request is set on each compare match detection, the request is cleared by hardware on DMA acknowledge. For a capture channel, the request is set when valid data is present in the CCx register, and cleared when CCx register is read.

38.6.5 Interrupts

The TC has the following interrupt sources:

- Overflow/Underflow (OVF)
- Match or Capture Channel x (MCx)
- Capture Overflow Error (ERR)

Each interrupt source has an interrupt flag associated with it. The interrupt flag in the Interrupt Flag Status and Clear register (INTFLAG) is set when the interrupt condition occurs.

Each interrupt can be individually enabled by writing a '1' to the corresponding bit in the Interrupt Enable Set register (INTENSET), and disabled by writing a '1' to the corresponding bit in the Interrupt Enable Clear register (INTENCLR).

An interrupt request is generated when the interrupt flag is set and the corresponding interrupt is enabled. The interrupt request remains active until either the interrupt flag is cleared, the interrupt is disabled, or the TC is reset. See INTFLAG for details on how to clear interrupt flags.

The TC has one common interrupt request line for all the interrupt sources. The user must read the INTFLAG register to determine which interrupt condition is present.

Note that interrupts must be globally enabled for interrupt requests to be generated. Refer to *Nested Vector Interrupt Controller* for details.

38.6.6 Events

The TC can generate the following output events:

- Overflow/Underflow (OVF)
- Match or Capture Channel x (MCx)

38.7.2.2 Control B Clear

Name: CTRLBCLR
Offset: 0x04
Reset: 0x00
Property: PAC Write-Protection, Read-Synchronized, Write-Synchronized

This register allows the user to clear bits in the CTRLB register without doing a read-modify-write operation. Changes in this register will also be reflected in the Control B Set register (CTRLBSET).

Bit	7	6	5	4	3	2	1	0
	CMD[2:0]					ONESHOT	LUPD	DIR
Access	R/W	R/W	R/W			R/W	R/W	R/W
Reset	0	0	0			0	0	0

Bits 7:5 – CMD[2:0] Command
These bits are used for software control of the TC. The commands are executed on the next prescaled GCLK_TC clock cycle. When a command has been executed, the CMD bit group will be read back as zero.

Writing 0x0 to these bits has no effect.

Writing a '1' to any of these bits will clear the pending command.

Bit 2 – ONESHOT One-Shot on Counter
This bit controls one-shot operation of the TC.

Writing a '0' to this bit has no effect

Writing a '1' to this bit will disable one-shot operation.

Value	Description
0	The TC will wrap around and continue counting on an overflow/underflow condition.
1	The TC will wrap around and stop on the next underflow/overflow condition.

Bit 1 – LUPD Lock Update
This bit controls the update operation of the TC buffered registers.

When CTRLB.LUPD is set, no any update of the registers with value of its buffered register is performed on hardware UPDATE condition. Locking the update ensures that all buffer registers are valid before an hardware update is performed. After all the buffer registers are loaded correctly, the buffered registers can be unlocked.

This bit has no effect when input capture operation is enabled.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the LUPD bit.

Value	Description
0	The CCBUFx and PERBUF buffer registers value are copied into CCx and PER registers on hardware update condition.
1	The CCBUFx and PERBUF buffer registers value are not copied into CCx and PER registers on hardware update condition.

- If the peripheral is configured as Non-Secure in the PAC:
  - Secure access and Non-Secure access are granted
- If the peripheral is configured as Secure in the PAC:
  - Secure access is granted
  - Non-Secure access is discarded (Write is ignored, read 0x0) and a PAC error is triggered

Refer to *Peripherals Security Attribution* for more information.

44.6.11 ADC Driver

44.6.11.1 Buffer/PGA for ADC

Each OPAMP can be configured as a buffer or a PGA for the other modules (such as ADC or AC). OPAMPs can also be cascaded to increase the programmable gain.

The output to the OPAMP must be enabled by writing a '1' to the Analog Output bit in the Operational Amplifier x Control register (OPAMPCTRLx.ANAOUT). The ADC input mux must be configured to select OPAMP as input. Refer to *ADC – Analog-to-Digital Converter* for details on configuring the ADC.

Related Links

41. ADC – Analog-to-Digital Converter

44.6.11.2 Offset and Gain Compensation

When the OPAMP is used in combination with the ADC, the OPAMP offset and gain errors can be compensated. To calculate offset and gain error compensation values

1. Configure OPAMP as Voltage Follower
2. Route the OPAMP output to the ADC:
   - Write a '1' to the Analog Output bit in the Operational Amplifier x Control register (OPAMPCTRLx.ANAOUT)
   - Select the OPAMP as input for the ADC, see *ADC – Analog-to-Digital Converter*.
3. Measure and set the Offset Correction value for the ADC OFFSETCORR register as in 44.6.11.3 Offset Compensation.
4. Measure and set the Gain Correction value for the ADC GAINCORR register as in 44.6.11.4 Gain Compensation.

The offset error compensation must be determined before gain error compensation.

The relation for offset and gain error compensation is shown in this equation:

Result = (converted value + OFFSETCORR)*GAINCORR

Related Links

41. ADC – Analog-to-Digital Converter

44.6.11.3 Offset Compensation

To determine the offset compensation value, the positive input must be tied to ground. The result of the ADC conversion gives directly the offset compensation value that must be written in the ADC OFFSETCORR register.

Mode	Conditions	Regulator	PL	CPU Clock	Vcc	Ta	Typ.	Max.	Units
		BUCK	PL0	DFLLUP at 8 MHz	1.8V		28.1	72	
					3.3V		18.5	47	
				OSC 8 MHz	1.8V		32.2	73	
					3.3V		25.3	51	
				OSC 4 MHz	1.8V		38.4	121	
					3.3V		31.9	86	
			PL2	FDPLL96 at 32 MHz	1.8V		41.5	55	
					3.3V		24.6	34	
				DFLLULP at 32 MHz	1.8V		37.1	53	
					3.3V		22.0	32	
IDLE		LDO	PL0	DFLLUP at 8 MHz	1.8V		16.0	81	
					3.3V		16.2	82	
				OSC 8 MHz	1.8V		19.8	82	
					3.3V		22.0	85	
				OSC 4 MHz	1.8V		26.2	152	
					3.3V		29.2	157	
			PL2	FDPLL96 at 32 MHz	1.8V		20.3	54	
					3.3V		20.4	54	
				DFLLULP at 32 MHz	1.8V		14.3	32	
					3.3V		14.4	33	
		BUCK	PL0	DFLLUP at 8 MHz	1.8V		11.1	52	
					3.3V		8.3	35	
				OSC 8 MHz	1.8V		15.5	55	
					3.3V		15.2	40	
				OSC 4 MHz	1.8V		21.3	100	
					3.3V		21.6	73	
			PL2	FDPLL96 at 32 MHz	1.8V		14.9	30	
					3.3V		9.1	19	
				DFLLULP at 32 MHz	1.8V		10.6	24	
					3.3V		6.7	15	