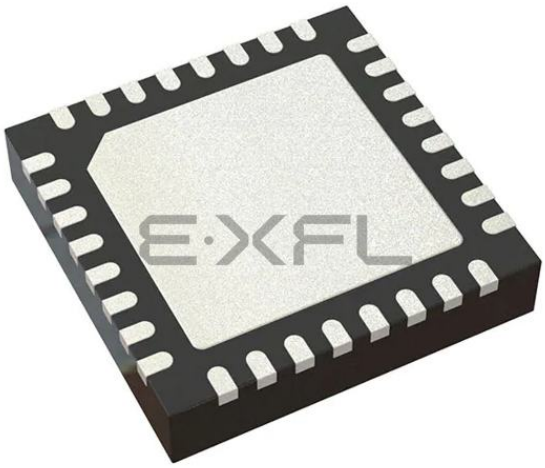

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Details	
Product Status	Active
Core Processor	ARM® Cortex®-M23
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	25
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.63V
Data Converters	A/D 10x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VFQFN Exposed Pad
Supplier Device Package	32-VQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsaml11e16a-mf

7. Analog Peripherals Considerations

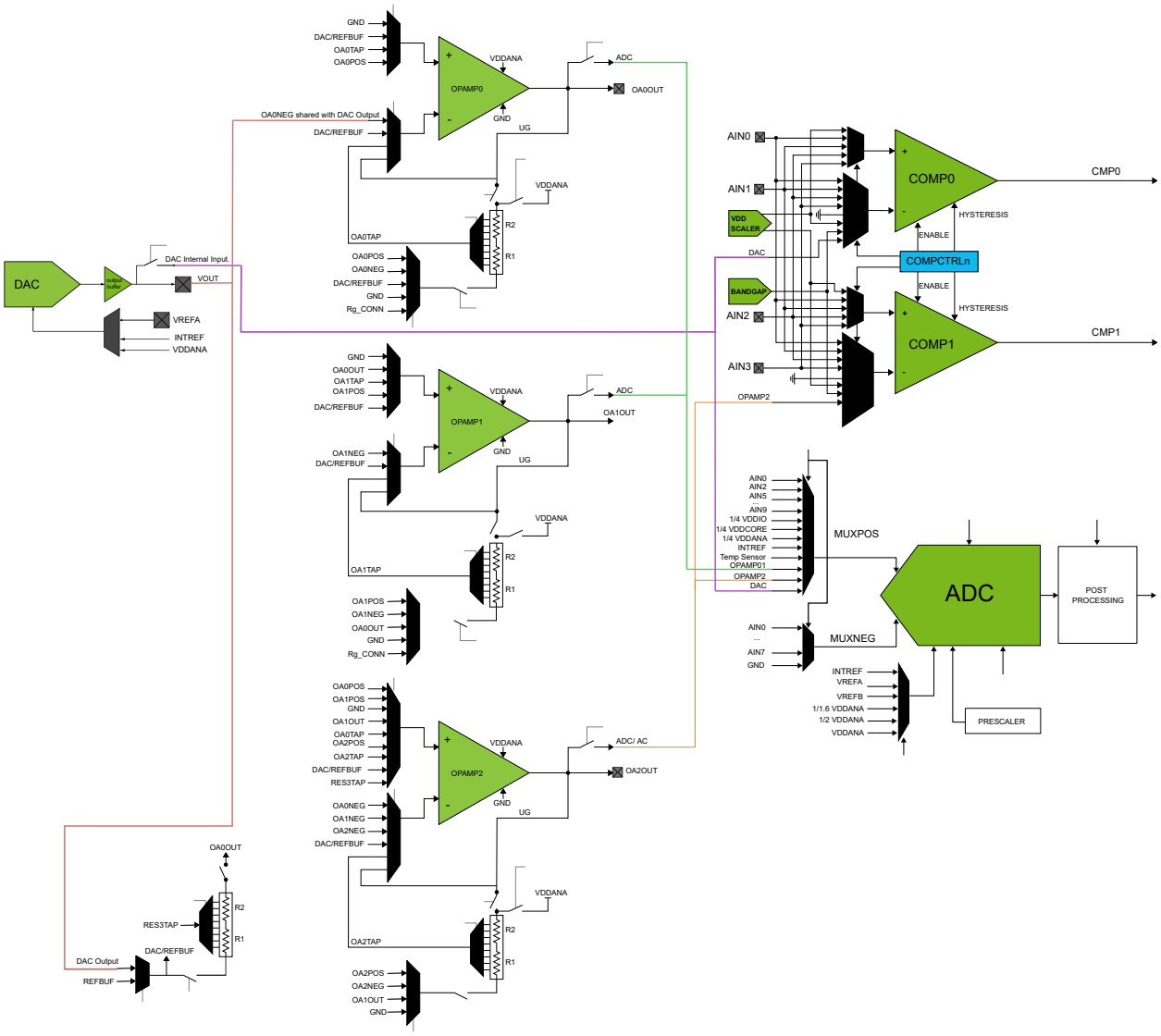
This chapter provides a global view of the analog system, which is composed of the following analog peripherals: AC, ADC, DAC, OPAMP.

The analog peripherals can be connected to each other as illustrated in the following block diagram.

Important:
When an analog peripheral is enabled, each analog output of the peripheral will be prevented from using the alternative functions of the output pads. This is also true even when the peripheral is used for internal purposes.

Analog inputs do not interfere with alternate pad functions.

Figure 7-1. Analog Signal Components Interconnections



19.8.8 APBB Mask

Name: APBBMASK
Offset: 0x18
Reset: 0x00000017
Property: PAC Write-Protection

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
				HMATRIXHS		NVMCTRL	DSU	IDAU
Access				R/W		R/W	R/W	R/W
Reset				1		1	1	1

Bit 4 – HMATRIXHS HMATRIXHS APBB Clock Enable

Value	Description
0	The APBB clock for the HMATRIXHS is stopped
1	The APBB clock for the HMATRIXHS is enabled

Bit 2 – NVMCTRL NVMCTRL APBB Clock Enable

Value	Description
0	The APBB clock for the NVMCTRL is stopped
1	The APBB clock for the NVMCTRL is enabled

Bit 1 – DSU DSU APBB Clock Enable

Value	Description
0	The APBB clock for the DSU is stopped
1	The APBB clock for the DSU is enabled

Bit 0 – IDAU IDAU APBB Clock Enable

Value	Description
0	The APBB clock for the IDAU is stopped
1	The APBB clock for the IDAU is enabled

Value	Description
0	The APBC clock for the EVSYS is stopped.
1	The APBC clock for the EVSYS is enabled.

Value	Description
0	DPLL Lock rise edge not detected.
1	DPLL Lock rise edge detected.

Bit 10 – DFLLULPNOLOCK DFLLULP No Lock

Value	Description
0	DFLLULP Tuner no lock state is not detected.
1	DFLLULP Tuner no lock state is detected.

Bit 9 – DFLLULPLOCK DFLLULP Lock

Value	Description
0	DFLLULP Tuner lock state is not detected.
1	DFLLULP Tuner lock state is detected.

Bit 8 – DFLLULPRDY DFLLULP Ready

Value	Description
0	DFLLULP is not ready.
1	DFLLULP is stable and ready to be used as a clock source.

Bit 4 – OSC16MRDY OSC16M Ready

Value	Description
0	OSC16M is not ready.
1	OSC16M is stable and ready to be used as a clock source.

Bit 2 – CLKSW XOSC Clock Switch

Value	Description
0	XOSC is not switched and provides the external clock or crystal oscillator clock.
1	XOSC is switched and provides the safe clock.

Bit 1 – CLKFAIL XOSC Clock Failure

Value	Description
0	No XOSC failure detected.
1	A XOSC failure was detected.

Bit 0 – XOSCRDY XOSC Ready

Value	Description
0	XOSC is not ready.
1	XOSC is stable and ready to be used as a clock source.

23.8.12 DFLLULP Delay Value

Name: DFLLULPDLY
Offset: 0x20
Reset: 0x00000080
Property: PAC Write-Protection, Write-Synchronized

Bit	31	30	29	28	27	26	25	24
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DELAY[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	0	0	0	0	0	0	0

Bits 7:0 – DELAY[7:0] Delay Value
Writing a value to this field sets the oscillator delay. A small value will produce a fast clock and a large value will produce a slow clock. If the tuner is enabled, writing to this field will cause the tuner to start tuning from the written value. Reading this value will return the last written delay or the oscillator delay when a synchronization was requested from the DFLLULPRREQ register. Writing a value to this register while a write synchronization or a read request synchronization is on-going will have no effect and produce a PAC error.

Bit 14 – TAMPEREO Tamper Event Output Enable

Value	Description
0	Tamper event output is disabled, and will not be generated
1	Tamper event output is enabled, and will be generated for every tamper input.

Bit 8 – ALARMEO Alarm 0 Event Output Enable

Value	Description
0	Alarm 0 event is disabled and will not be generated.
1	Alarm 0 event is enabled and will be generated for every compare match.

Bits 0, 1, 2, 3, 4, 5, 6, 7 – PEREOn Periodic Interval n Event Output Enable [n = 7..0]

Value	Description
0	Periodic Interval n event is disabled and will not be generated.
1	Periodic Interval n event is enabled and will be generated.

29.7 Register Summary

Important:
For SAM L11, the EIC register map is automatically duplicated in a Secure and Non-Secure alias:

- The Non-Secure alias is at the peripheral base address
- The Secure alias is located at the peripheral base address + 0x200

Refer to *Mix-Secure Peripherals* for more information on register access rights

Offset	Name	Bit Pos.								
0x00	CTRLA	7:0				CKSEL			ENABLE	SWRST
0x01	NMICTRL	7:0				NMIASYNCH	NMIFILTEN	NMISENSE[2:0]		
0x02	NMIFLAG	7:0								NMI
		15:8								
0x04	SYNCBUSY	7:0							ENABLE	SWRST
		15:8								
		23:16								
		31:24								
0x08	EVCTRL	7:0	EXTINTEO[7:0]							
		15:8								
		23:16								
		31:24								
0x0C	INTENCLR	7:0	EXTINT[7:0]							
		15:8								
		23:16								
		31:24	NSCHK							
0x10	INTENSET	7:0	EXTINT[7:0]							
		15:8								
		23:16								
		31:24	NSCHK							
0x14	INTFLAG	7:0	EXTINT[7:0]							
		15:8								
		23:16								
		31:24	NSCHK							
0x18	ASYNCH	7:0	ASYNCH[7:0]							
		15:8								
		23:16								
		31:24								
0x1C	CONFIG	7:0	FILTENx	SENSEx[2:0]			FILTENx	SENSEx[2:0]		
		15:8	FILTENx	SENSEx[2:0]			FILTENx	SENSEx[2:0]		
		23:16	FILTENx	SENSEx[2:0]			FILTENx	SENSEx[2:0]		
		31:24	FILTENx	SENSEx[2:0]			FILTENx	SENSEx[2:0]		
0x20 ... 0x2F	Reserved									

Optional write-protection by the Peripheral Access Controller (PAC) is denoted by the "PAC Write-Protection" property in each individual register description.

PAC write-protection does not apply to accesses through an external debugger.

Related Links

15. PAC - Peripheral Access Controller

34.5.9 SAM L11 TrustZone Specific Register Access Protection

On **SAM L11** devices, this peripheral has different access permissions depending on PAC Security Attribution (Secure or Non-Secure):

- If the peripheral is configured as Non-Secure in the PAC:
  - Secure access and Non-Secure access are granted
- If the peripheral is configured as Secure in the PAC:
  - Secure access is granted
  - Non-Secure access is discarded (Write is ignored, read 0x0) and a PAC error is triggered

Refer to *Peripherals Security Attribution* for more information.

34.5.10 Analog Connections

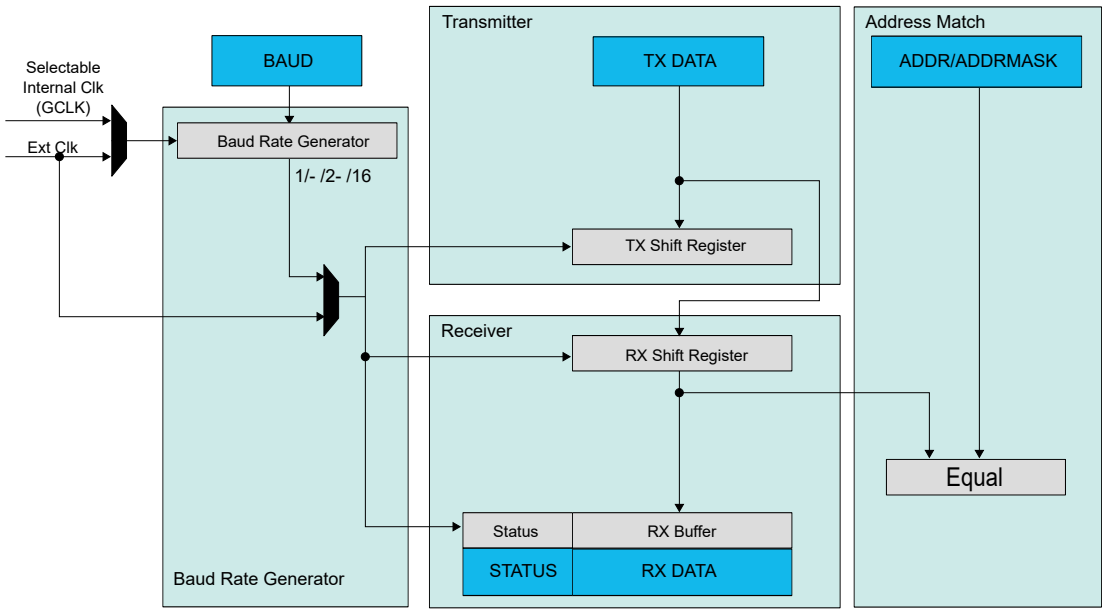
Not applicable.

34.6 Functional Description

34.6.1 Principle of Operation

The basic structure of the SERCOM serial engine is shown in Figure 34-2. Labels in capital letters are synchronous to the system clock and accessible by the CPU; labels in lowercase letters can be configured to run on the GCLK_SERCOMx_CORE clock or an external clock.

Figure 34-2. SERCOM Serial Engine



The transmitter consists of a single write buffer and a shift register.

35.8.9 Status

Name: STATUS
Offset: 0x1A
Reset: 0x0000
Property: -

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	ITER	TXE	COLL	ISF	CTS	BUFOVF	FERR	PERR
Access	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 7 – ITER Maximum Number of Repetitions Reached
This bit is set when the maximum number of NACK repetitions or retransmissions is met in ISO7816 T=0 mode.

Writing '0' to this bit has no effect.

Writing '1' to this bit will clear it.

Bit 6 – TXE Transmitter Empty
This bit will always read back as zero.

Writing '0' to this bit has no effect.

Writing '1' to this bit will clear it.

Bit 5 – COLL Collision Detected
This bit is cleared by writing '1' to the bit or by disabling the receiver.

This bit is set when collision detection is enabled (CTRLB.COLDEN) and a collision is detected.

Writing '0' to this bit has no effect.

Writing '1' to this bit will clear it.

Bit 4 – ISF Inconsistent Sync Field
This bit is cleared by writing '1' to the bit or by disabling the receiver.

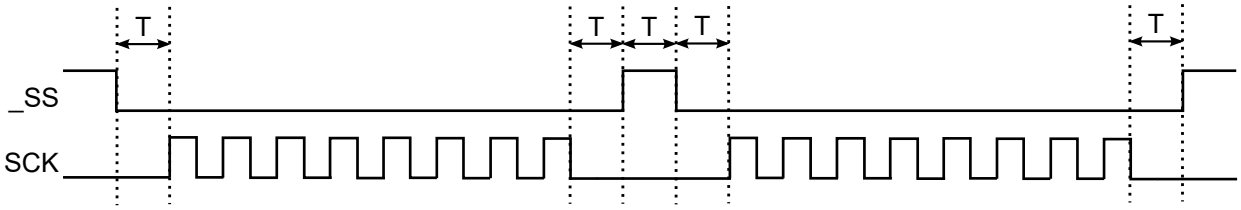
This bit is set when the frame format is set to auto-baud (CTRLA.FORM) and a sync field not equal to 0x55 is received.

Writing '0' to this bit has no effect.

Writing '1' to this bit will clear it.

Bit 3 – CTS Clear to Send
This bit indicates the current level of the CTS pin when flow control is enabled (CTRLA.TXPO).

Figure 36-7. Hardware Controlled $\overline{SS}$



T = 1 to 2 baud cycles

When CTRLB.MSSEN=0, the $\overline{SS}$ pin(s) is/are controlled by user software and normal GPIO.

36.6.3.6 Slave Select Low Detection

In slave mode, the SPI can wake the CPU when the slave select ($\overline{SS}$) goes low. When the Slave Select Low Detect is enabled (CTRLB.SSDE=1), a high-to-low transition will set the Slave Select Low interrupt flag (INTFLAG.SSL) and the device will wake up if applicable.

36.6.4 DMA, Interrupts, and Events

Table 36-4. Module Request for SERCOM SPI

Condition	Request		
	DMA	Interrupt	Event
Data Register Empty (DRE)	Yes (request cleared when data is written)	Yes	NA
Receive Complete (RXC)	Yes (request cleared when data is read)	Yes	
Transmit Complete (TXC)	NA	Yes	
Slave Select low (SSL)	NA	Yes	
Error (ERROR)	NA	Yes	

36.6.4.1 DMA Operation

The SPI generates the following DMA requests:

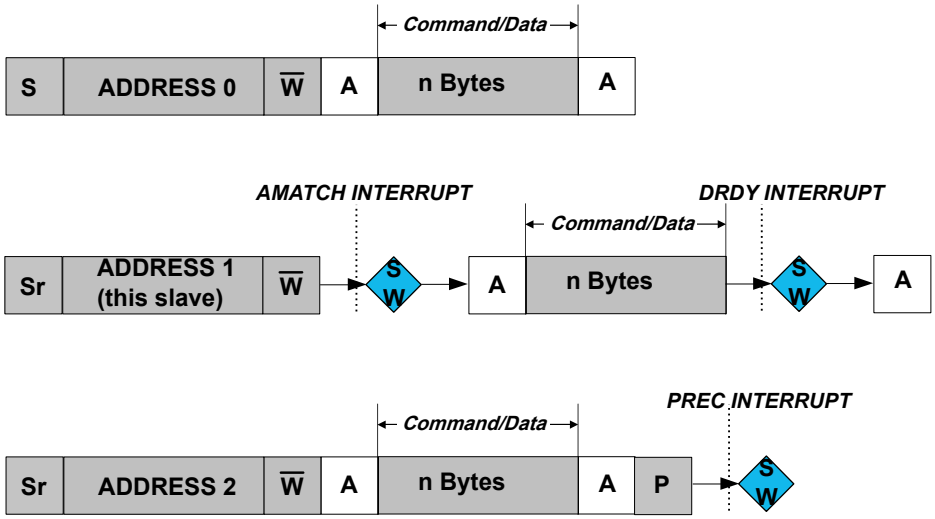
- Data received (RX): The request is set when data is available in the receive FIFO. The request is cleared when DATA is read.
- Data transmit (TX): The request is set when the transmit buffer (TX DATA) is empty. The request is cleared when DATA is written.

36.6.4.2 Interrupts

The SPI has the following interrupt sources. These are asynchronous interrupts, and can wake up the device from any sleep mode:

- Data Register Empty (DRE)
- Receive Complete (RXC)
- Transmit Complete (TXC)
- Slave Select Low (SSL)
- Error (ERROR)

Figure 37-13. PMBus Group Command Example



37.6.3 Additional Features

37.6.3.1 SMBus

The I^2C includes three hardware SCL low time-outs which allow a time-out to occur for SMBus SCL low time-out, master extend time-out, and slave extend time-out. This allows for SMBus functionality These time-outs are driven by the GCLK_SERCOM_SLOW clock. The GCLK_SERCOM_SLOW clock is used to accurately time the time-out and must be configured to use a 32KHz oscillator. The I^2C interface also allows for a SMBus compatible SDA hold time.

- $T_{TIMEOUT}$: SCL low time of 25..35ms – Measured for a single SCL low period. It is enabled by CTRLA.LOWTOUTEN.
- $T_{LOW:SEXT}$: Cumulative clock low extend time of 25 ms – Measured as the cumulative SCL low extend time by a slave device in a single message from the initial START to the STOP. It is enabled by CTRLA.SEXTTOEN.
- $T_{LOW:MEXT}$: Cumulative clock low extend time of 10 ms – Measured as the cumulative SCL low extend time by the master device within a single byte from START-to-ACK, ACK-to-ACK, or ACK-to-STOP. It is enabled by CTRLA.MEXTTOEN.

37.6.3.2 Smart Mode

The I^2C interface has a smart mode that simplifies application code and minimizes the user interaction needed to adhere to the I^2C protocol. The smart mode accomplishes this by automatically issuing an ACK or NACK (based on the content of CTRLB.ACKACT) as soon as DATA.DATA is read.

37.6.3.3 4-Wire Mode

Writing a '1' to the Pin Usage bit in the Control A register (CTRLA.PINOUT) will enable 4-wire mode operation. In this mode, the internal I^2C tri-state drivers are bypassed, and an external I^2C compliant tri-state driver is needed when connecting to an I^2C bus.

37.8.4 Interrupt Enable Set

Name: INTENSET
Offset: 0x16
Reset: 0x00
Property: PAC Write-Protection

This register allows the user to enable an interrupt without doing a read-modify-write operation. Changes in this register will also be reflected in the Interrupt Enable Clear register (INTENCLR).

Bit	7	6	5	4	3	2	1	0
	ERROR					DRDY	AMATCH	PREC
Access	R/W					R/W	R/W	R/W
Reset	0					0	0	0

Bit 7 – ERROR Error Interrupt Enable
Writing '0' to this bit has no effect.

Writing '1' to this bit will set the Error Interrupt Enable bit, which enables the Error interrupt.

Value	Description
0	Error interrupt is disabled.
1	Error interrupt is enabled.

Bit 2 – DRDY Data Ready Interrupt Enable
Writing '0' to this bit has no effect.

Writing '1' to this bit will set the Data Ready bit, which enables the Data Ready interrupt.

Value	Description
0	The Data Ready interrupt is disabled.
1	The Data Ready interrupt is enabled.

Bit 1 – AMATCH Address Match Interrupt Enable
Writing '0' to this bit has no effect.

Writing '1' to this bit will set the Address Match Interrupt Enable bit, which enables the Address Match interrupt.

Value	Description
0	The Address Match interrupt is disabled.
1	The Address Match interrupt is enabled.

Bit 0 – PREC Stop Received Interrupt Enable
Writing '0' to this bit has no effect.

Writing '1' to this bit will set the Stop Received Interrupt Enable bit, which enables the Stop Received interrupt.

Value	Description
0	The Stop Received interrupt is disabled.
1	The Stop Received interrupt is enabled.

Bit 7 – CLKHOLD Clock Hold
The slave Clock Hold bit (STATUS.CLKHOLD) is set when the slave is holding the SCL line low, stretching the I2C clock. Software should consider this bit a read-only status flag that is set when INTFLAG.DRDY or INTFLAG.AMATCH is set.

This bit is automatically cleared when the corresponding interrupt is also cleared.

Bit 6 – LOWTOUT SCL Low Time-out
This bit is set if an SCL low time-out occurs.

This bit is cleared automatically if responding to a new start condition with ACK or NACK (write 3 to CTRLB.CMD) or when INTFLAG.AMATCH is cleared.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the status.

Value	Description
0	No SCL low time-out has occurred.
1	SCL low time-out has occurred.

Bit 4 – SR Repeated Start
When INTFLAG.AMATCH is raised due to an address match, SR indicates a repeated start or start condition.

This flag is only valid while the INTFLAG.AMATCH flag is one.

Value	Description
0	Start condition on last address match
1	Repeated start condition on last address match

Bit 3 – DIR Read / Write Direction
The Read/Write Direction (STATUS.DIR) bit stores the direction of the last address packet received from a master.

Value	Description
0	Master write operation is in progress.
1	Master read operation is in progress.

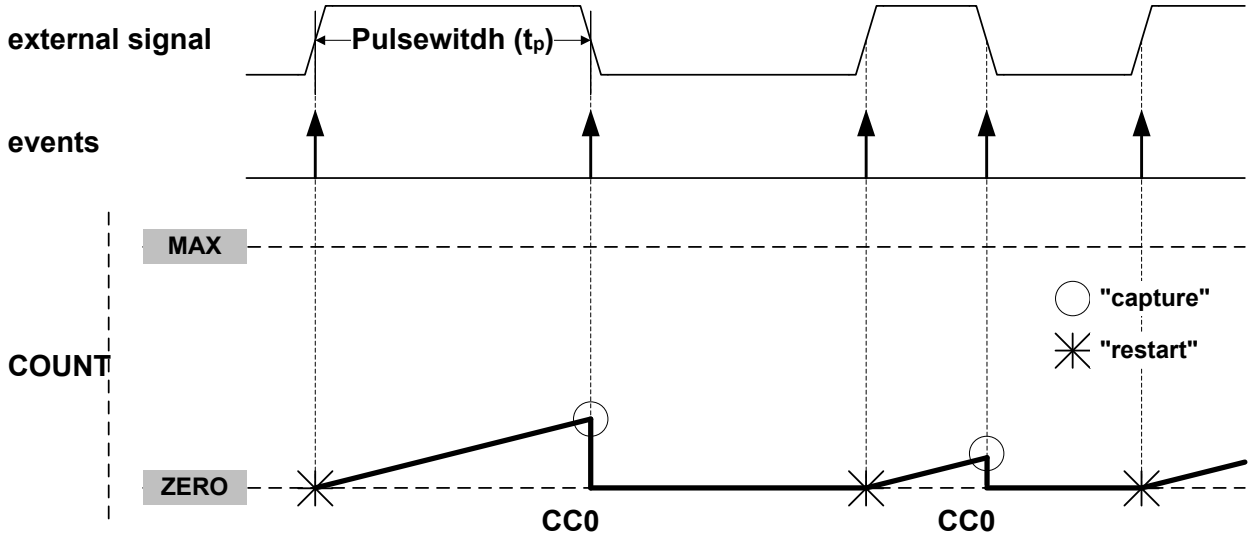
Bit 2 – RXNACK Received Not Acknowledge
This bit indicates whether the last data packet sent was acknowledged or not.

Value	Description
0	Master responded with ACK.
1	Master responded with NACK.

Bit 1 – COLL Transmit Collision
If set, the I2C slave was not able to transmit a high data or NACK bit, the I2C slave will immediately release the SDA and SCL lines and wait for the next packet addressed to it.

This flag is intended for the SMBus address resolution protocol (ARP). A detected collision in non-ARP situations indicates that there has been a protocol violation, and should be treated as a bus error.

Figure 38-14. Pulse-Width Capture on Channel 0



The TC can detect capture overflow of the input capture channels: When a new capture event is detected while the Capture Interrupt flag (INTFLAG.MCx) is still set, the new timestamp will not be stored and INTFLAG.ERR will be set.

38.6.3 Additional Features

38.6.3.1 One-Shot Operation

When one-shot is enabled, the counter automatically stops on the next counter overflow or underflow condition. When the counter is stopped, the Stop bit in the Status register (STATUS.STOP) is automatically set and the waveform outputs are set to zero.

One-shot operation is enabled by writing a '1' to the One-Shot bit in the Control B Set register (CTRLBSET.ONESHOT), and disabled by writing a '1' to CTRLBCLR.ONESHOT. When enabled, the TC will count until an overflow or underflow occurs and stops counting operation. The one-shot operation can be restarted by a re-trigger software command, a re-trigger event, or a start event. When the counter restarts its operation, STATUS.STOP is automatically cleared.

38.6.3.2 Time-Stamp Capture

This feature is enabled when the Capture Time Stamp (STAMP) Event Action in Event Control register (EVCTRL.EVACT) is selected. The counter TOP value must be smaller than MAX.

When a capture event is detected, the COUNT value is copied into the corresponding Channel x Compare/Capture Value (CCx) register. In case of an overflow, the MAX value is copied into the corresponding CCx register.

When a valid captured value is present in the capture channel register, the corresponding Capture Channel x Interrupt Flag (INTFLAG.MCx) is set.

The timer/counter can detect capture overflow of the input capture channels: When a new capture event is detected while the Capture Channel interrupt flag (INTFLAG.MCx) is still set, the new time-stamp will not be stored and INTFLAG.ERR will be set.

38.7.3.14 Period Value, 32-bit Mode

Name: PER
Offset: 0x1A
Reset: 0xFFFFFFFF
Property: Write-Synchronized

Bit	31	30	29	28	27	26	25	24
	PER[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PER[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PER[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PER[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	1

Bits 31:0 – PER[31:0] Period Value
These bits hold the value of the Period Buffer register PERBUF. The value is copied to PER register on UPDATE condition.

38.7.3.17 Channel x Compare Buffer Value, 32-bit Mode

Name: CCBUFx
Offset: 0x30 + x*0x04 [x=0..1]
Reset: 0x00000000
Property: Write-Synchronized

Bit	31	30	29	28	27	26	25	24
	CCBUF[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	CCBUF[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	CCBUF[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CCBUF[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – CCBUF[31:0] Channel x Compare Buffer Value
These bits hold the value of the Channel x Compare Buffer Value. When the buffer valid flag is '1' and double buffering is enabled (CTRLBCLR.LUPD=1), the data from buffer registers will be copied into the corresponding CCx register under UPDATE condition (CTRLBSET.CMD=0x3), including the software update command.

40.5.3 Clocks

The CCL bus clock (CLK_CCL_APB) can be enabled and disabled in the Main Clock module, MCLK (see *MCLK - Main Clock*), and the default state of CLK_CCL_APB can be found in *Peripheral Clock Masking*.

A generic clock (GCLK_CCL) is optionally required to clock the CCL. This clock must be configured and enabled in the Generic Clock Controller (GCLK) before using input events, filter, edge detection or sequential logic. GCLK_CCL is required when input events, a filter, an edge detector, or a sequential sub-module is enabled. Refer to *GCLK - Generic Clock Controller* for details.

This generic clock is asynchronous to the user interface clock (CLK_CCL_APB).

Related Links

19. MCLK – Main Clock

19.6.2.6 Peripheral Clock Masking

18. GCLK - Generic Clock Controller

40.5.4 DMA

Not applicable.

40.5.5 Interrupts

Not applicable.

40.5.6 Events

The CCL can use events from other peripherals and generate events that can be used by other peripherals. For this feature to function, the Events have to be configured properly. Refer to the Related Links below for more information about the Event Users and Event Generators.

Related Links

33. EVSYS – Event System

40.5.7 Debug Operation

When the CPU is halted in Debug mode the CCL continues normal operation. However, the CCL cannot be halted when the CPU is halted in Debug mode. If the CCL is configured in a way that requires it to be periodically serviced by the CPU, improper operation or data loss may result during debugging.

40.5.8 Register Access Protection

All registers with write-access can be write-protected optionally by the peripheral access controller (PAC). Refer to *PAC - Peripheral Access Controller* for details.

Optional write-protection by the Peripheral Access Controller (PAC) is denoted by the "PAC Write-Protection" property in each individual register description.

PAC write-protection does not apply to accesses through an external debugger.

Related Links

15. PAC - Peripheral Access Controller

40.5.9 SAM L11 TrustZone Specific Register Access Protection

On **SAM L11** devices, this peripheral has different access permissions depending on PAC Security Attribution (Secure or Non-Secure):

- If the peripheral is configured as Non-Secure in the PAC:
  - Secure access and Non-Secure access are granted

Sleep Mode	Condition	Typ	Unit
	L11 with BOOTOPT=0	4.1	
	L10 or L11 with BOOTOPT=1, BS = 0x40	210	
	L10 or L11 with BOOTOPT=1, BS = 0x80	410	
	L10 or L11 with BOOTOPT=2, BS = 0x40	210	
	L10 or L11 with BOOTOPT=2, BS = 0x80	410	

Note:

1. These values are based on simulation. They are not covered by production test limits or characterization.

46.9 I/O Pin Characteristics

There are two different pin types with three different speeds: Normal and High Sink(2).

The Drive Strength bit is located in the Pin Configuration register of the PORT (PORT.PINCFG.DRVSTR).

Table 46-11. I/O Pins Common Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IL}	Input low-level voltage	V_{DD}=1.62V-2.7V	-	-	0.25*V_{DD}	V
		V_{DD}=2.7V-3.63V	-	-	0.3*V_{DD}	
V_{IH}	Input high-level voltage	V_{DD}=1.62V-2.7V	0.7*V_{DD}	-	-	
		V_{DD}=2.7V-3.63V	0.55*V_{DD}	-	-	
V_{OL}	Output low-level voltage	V_{DD}>1.62V, I_{OL} max	-	0.1*V_{DD}	0.2*V_{DD}	
V_{OH}	Output high-level voltage	V_{DD}>1.62V, I_{OH} max	0.75*V_{DD}	0.85*V_{DD}	-	
R_{PULL}	Pull-up - Pull-down resistance		20	40	63	kΩ
I_{LEAK}	Input leakage current	Pull-up resistors disabled	-1	±0.015	1	µA

Table 46-12. I/O Pins Maximum Output Current

Symbol	Parameter	Conditions	Normal Pins	High Sink Pins(2)	Normal Pins	High Sink Pins(2)	Units
			DRVSTR=0		DRVSTR=1		
I_{OL}	Maximum Output low-level current	V_{DD}=1.62V-3V	1	2	2	4	mA
		V_{DD}=3V-3.63V	2.5	6	6	12	
I_{OH}	Maximum Output high-level current	V_{DD}=1.62V-3V	0.7	1.5	1.5	3	
		V_{DD}=3V-3.63V	2	5	5	10	

For 12-bit accuracy:

$t_{\text{samplehold}} \geq \left(R_{\text{sample}} + R_{\text{source}}\right) \times \left(C_{\text{sample}}\right) \times 9.7$

where $t_{\text{samplehold}} = \frac{1}{2 \times f_{\text{ADC}}}$.

47.4.3 Digital-to-Analog Converter (DAC) Characteristics

Table 47-10. Operating Conditions (1)

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
AVREF	External reference voltage		1	-	VDDANA-0.6	V
	Internal reference voltage 1		-	1	-	V
	Internal reference voltage 2		-	VDDANA	-	V
	Linear output voltage range		0.05	-	VDDANA-0.05	V
	Minimum resistive load		5	-	-	kOhm
	Maximum capacitance load		-	-	100	pF
IDD	DC supply current(2)	Voltage pump disabled	-	175	270	µA

Note:

1. The values in this table are based on specifications otherwise noted.
2. These values are based on characterization. These values are not covered in test limits in production.

Table 47-11. Clock and Timing (1)

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Units
	Conversion rate	Cload=100pF Rload > 5 kOhm	Normal mode	-	-	350	ksps
			For DDATA=+/-1	-	-	1000	
	Startup time	VDDANA > 2.6V	VDDANA > 2.6V	-	-	2.85	µs
		VDDANA < 2.6V	VDDANA < 2.6V	-	-	10	µs

Note:

1. These values are based on simulation. These values are not covered by test limits in production or characterization.

Table 47-12. Accuracy Characteristics (1)

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Units
RES	Input resolution			-	-	10	Bits
INL	Integral non-linearity	VREF= Ext 1.0V	VDD = 1.62V	+/-0,2	+/-0,5	+/-1.4	LSB
			VDD = 3.63V	+/-0,2	+/-0,4	+/-1,2	
		VREF = VDDANA	VDD = 1.62V	+/-0,2	+/-0,6	+/-2.1	
			VDD = 3.63V	+/-0,2	+/-0,5	+/-1,9	

Table 49-14. Package Characteristics

Moisture Sensitivity Level	MSL1

Table 49-15. Package Reference

JEDEC Drawing Reference	N/A
JESD97 Classification	E1

49.3 Soldering Profile

The following table gives the recommended soldering profile from J-STD-20.

Table 49-16. Recommended Soldering Profile

Profile Feature	Green Package
Average Ramp-up Rate (217°C to peak)	3°C/s max.
Preheat Temperature 175°C ±25°C	150-200°C
Time Maintained Above 217°C	60-150s
Time within 5°C of Actual Peak Temperature	30s
Peak Temperature Range	260°C
Ramp-down Rate	6°C/s max.
Time 25°C to Peak Temperature	8 minutes max.

A maximum of three reflow passes is allowed per component.