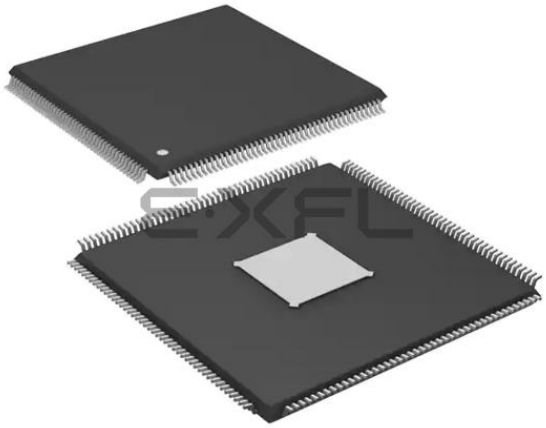

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A5
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	266MHz
Co-Processors/DSP	Multimedia; NEON™ MPE
RAM Controllers	LPDDR2, DDR3, DRAM
Graphics Acceleration	Yes
Display & Interface Controllers	DCU, GPU, LCD, VideoADC, VIU
Ethernet	10/100Mbps (2)
SATA	-
USB	USB 2.0 OTG + PHY (1)
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	-
Package / Case	176-LQFP Exposed Pad
Supplier Device Package	176-HLQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mvf30nn151cku26

Table of Contents

1 Ordering parts

1.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web.

1. To determine the orderable part numbers for this device, go to www.freescale.com and search the required part number. The part numbering format is described in the section that follows.

2 Part identification

2.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

2.2 Part Number Format

The figure below represents the format of part number of this device.

Field	Description	Values
R	Revision	• 1 = Rev 1.x
T	Temperature range (°C)	• C = -40 °C to +85 °C T_a
PP	Package type	• KU = 176LQFP • MK = 364 MAPBGA
S	Speed	• Speed A5 Core • 26 = 266MHz • 40 = 400MHz • 50 = 500MHz

2.4 Part Numbers

This table lists the part numbers on the device.

Part Number	Package	Description
MVF30NN151CKU26	LQFP-EP 176 24*24*1.6	A5-266, No Security, 176LQFP
MVF30NS151CKU26	LQFP-EP 176 24*24*1.6	A5-266, Security, 176LQFP
MVF50NN151CMK40	MAP 364 17*17*1.5 P0.8	A5-400, No Security, 364BGA
MVF50NS151CMK40	MAP 364 17*17*1.5 P0.8	A5-400, Security, 364BGA
MVF50NN151CMK50	MAP 364 17*17*1.5 P0.8	A5-500, No Security, 364BGA
MVF50NS151CMK50	MAP 364 17*17*1.5 P0.8	A5-500, Security, 364BGA
MVF51NN151CMK50	MAP 364 17*17*1.5 P0.8	A5-500, L2 Cache, No Security, 364BGA
MVF51NS151CMK50	MAP 364 17*17*1.5 P0.8	A5-500, L2 Cache, Security, 364BGA
MVF60NN151CMK40	MAP 364 17*17*1.5 P0.8	A5-400, M4, No Security, 364BGA
MVF60NS151CMK40	MAP 364 17*17*1.5 P0.8	A5-400, M4, Security, 364BGA
MVF60NN151CMK50	MAP 364 17*17*1.5 P0.8	A5-500, M4, No Security, 364BGA
MVF60NS151CMK50	MAP 364 17*17*1.5 P0.8	A5-500, M4, Security, 364BGA
MVF61NN151CMK50	MAP 364 17*17*1.5 P0.8	A5-500, M4, L2 Cache, No Security, 364BGA
MVF61NS151CMK50	MAP 364 17*17*1.5 P0.8	A5-500, M4, L2 Cache, Security, 364BGA
MVF62NN151CMK40	MAP 364 17*17*1.5 P0.8	A5-400, M4 Primary, No Security, 364BGA

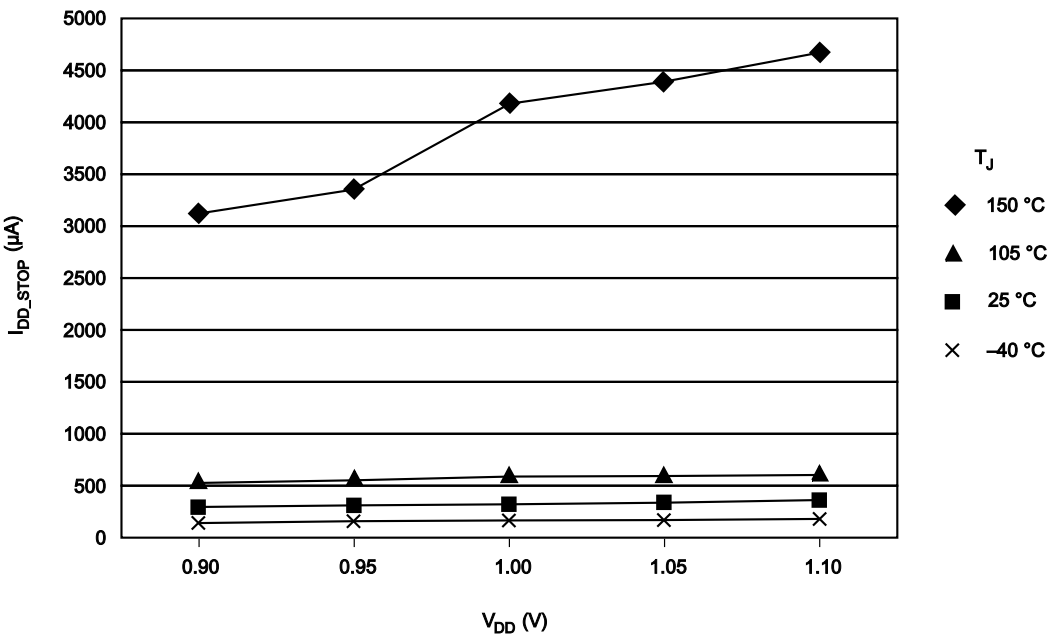
3.8.1 Example 1

This is an example of an operating behavior that includes a typical value:

Symbol	Description	Min.	Typ.	Max.	Unit
I_{WP}	Digital I/O weak pullup/pulldown current	10	70	130	µA

3.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions:



3.9 Typical Value Conditions

Typical values assume you meet the following conditions (or other conditions as specified):

Symbol	Description	Value	Unit
T_A	Ambient temperature	25	°C
V_{DD}	3.3 V supply voltage	3.3	V

6.2 Nonswitching electrical specifications

6.2.1 VREG electrical specifications

6.2.1.1 HPREG electrical characteristics

Table 2. HPREG electrical characteristics

Parameters	Min	Typ	Max	Unit	Comments
Power supply	3.0	3.3	3.6	V	-
Current Consumption	-	1.2	1.5	mA	@ no load
	-	2.0	2.5	mA	@ full load
Output current capacity	-	600	1200[1]	mA	DC load current
Output voltage @ no load		1.23	1.26	V	
Output voltage @ full load	1.20	1.21		V	
External decoupling cap	4.7		-	µF	-
	0.05		0.1	Ohms	ESR of external cap
			20	mOhms	Total effective PAD+PCB trace resistances
PSRR with 4.7uF output cap					
@ DC @noload @ DC @full load @ worst case any frequency			-48 -40 -20	dB	

1. This is peak and not continuous maximum value.

6.2.1.2 LPREG electrical characteristics

Table 3. LPREG electrical characteristics

Parameters	Min	Typ	Max	Unit	Comments
Power supply	3.0	3.3	3.6	V	
Current Consumption	350	400		µA	@ no load
	-	500	650	µA	@ full load
Output current capacity		100	200	mA	DC load current
Output voltage @ no load		1.22	1.240	V	
Output voltage @ full load	1.180			V	
External decoupling cap	4.7			µF	
	0.05		0.1	Ohms	ESR of external cap
			20	mOhms	Total PAD+PCB trace resistance

Table continues on the next page...

6.2.1.5 External NPN Ballast

The internal main regulator requires an external NPN ballast transistor to be connected as shown in the following figure as well as an external capacitance to be connected to the device in order to provide a stable 1.2V digital supply to the device. The HPREG design allows for collector voltage lower than VDDREG value. See AN4807 at www.freescale.com .

NOTE

To not overload BCTRL output, collector voltage should appear no later than VDDREG / VDD33 (3.3V).

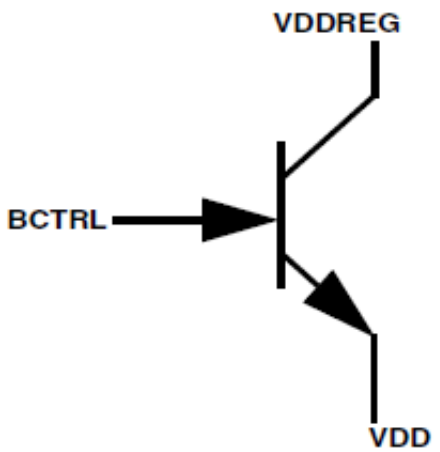


Figure 3. External NPN Ballast connections

Table 6. BCTRL OUTPUT specification

Parameter	Value	Comments
BCTRL OUTPUT specification	20mA	BCTRL driver can not drive more than 20mA current
Maximum pin voltage	VDDREG-0.5V	For Example, VDDREG =3.0V BCTRL should not exceed 2.5V.

Table 7. Assumptions For calculations

Parameter	Value
VDDREG	3.0V to 3.6V with typical value of 3.3V
Max DC Collector current	0.85A @85 °C
Emitter voltage	1.2V to 1.25V
Collector voltage	Equal to VDDREG

2. The Max numbers represent the single worst case value taken from a matrix lot of parts across normal process variation at maximum temperature.
3. CA5, CM4 cores halted
4. 24MHz operation, PLL Bypass
5. 32 kHz /128 kHz operation, PLL Off
6. Lowest power mode with all power retained, RAM retention and LVD protection.
7. Standby Mode. 64K RAM retention. I/O states held. ADCs/DACs optionally power-gated. RTC functional. Wakeup from interrupts. Fast IRC enabled.
8. Standby Mode 16K RAM retention. I/O states held. ADCs/DACs optionally power-gated. RTC functional. Wakeup from interrupts. Fast IRC enabled.
9. All supplies OFF, SRTC, 32kXOSC ON, tampers and monitors ON. 128k IRC optionally ON.

6.2.5 USB PHY current consumption

6.2.5.1 Power Down Mode

Everything powered down, including the VBUS valid detectors, typ condition.

Table 16. USB PHY Current Consumption in Normal Mode

	USBx_VBUS (3.0V) Avg	VDD33_LDOIN (2.5V) Avg	VDD33_LDOIN (1.1V) Avg
Current	5.1 µA	1.7 µA	<0.5 µA

NOTE

The currents on the 2.5 voltage regulator and 3.0 voltage regulator were identified to be the voltage divider circuits in the USB-specific level shifters.

6.2.6 EMC radiated emissions operating behaviors

Table 17. EMC radiated emissions operating behaviors

Symbol	Condition[1]	Clocks	Frequency band [2]	Level (Typ)[3]	Unit
V_{EME}	Device Configuration, test conditions and EM testing per standard IEC 61967-2; Supply voltages: VDD= 5.0 V VDD33 = 3.3 V VDD15 = 1.5 V VDD12 = 1.2 V Temp = 25°C	FCPU = 396 MHz FBUS = 66 MHz External Crystal = 24 MHz	150 KHz – 50 MHz	22	dBµV
			50 MHz – 150 MHz	24	
			150 MHz – 500 MHz	25	
			500–1000	20	
			IEC level[4]	K	—

1. Measurements were made per IEC 61967-2 while the device was running basic application code.
2. Measurements were performed on the BGA364 version of the device

Table 22. Output Buffer Average Impedance (3.3V power mode) (continued)

Symbol	Parameter	Drive strength[1]	Min	Typ	Max	Unit
		1 0 0	30	37	58	
		1 0 1	24	30	46	
		1 1 0 Extra drive strength	20	25	38	
		1 1 1	17	20	32	

1. The drive strengths are controlled by the DSE bit of the Software MUX Pad Control Register. For details, see IOMUX Controller chapter of the device reference manual.

7.2 DDR parameters

Table 23. DDR operating conditions

Symbol	Parameter	Min	Typ	Max	Unit
vddi	Core internal supply voltage	1.16	1.23	1.26	V
ovdd	I/O output supply voltage (DDR3 mode)	1.425	1.5	1.575	V
ovdd	I/O output supply voltage (LPDDR2 mode)	1.14	1.2	1.26	V
vdd2p5	I/O PD predriver and level shifters supply voltage	2.25	2.5	2.75	V

Table 24. LPDDR2 mode DC Electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
Voh	High-level output voltage		0.9*ovdd			V	Note that the JEDEC LPDDR2 specification (JESD209_2B) supersedes any specification in this document.
Vol	Low-level output voltage				0.1*ovdd	V	
Vref	Input reference voltage		0.49*ovdd	0.5*ovdd	0.51*ovdd	V	
Vih(dc)	DC input high voltage		Vref+0.13		ovdd	V	
Vil(dc)	DC input low voltage		ovss		Vref-0.13	V	
Vih(diff)	DC differential input logic high		0.26		Note[1]	V	
Vil(diff)	DC differential input logic low		Note[1]		-0.26	V	

Table continues on the next page...

Table 25. DDR3 mode DC Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
Tri-state I/O supply current[3]	Icc-ovdd	Vin = ovdd or 0			5		
Tri-state vdd2p5 supply current[3]	Icc-vdd2p5	Vi = vddi or 0			1.5		
Tri-state core supply current[3]	Icc-vddi				1		
Driver unit (240 Ohm) calibration resolution	Rres				10	Ohm	

1. The single-ended signals need to be within the respective limits (Vih(dc) max, Vil(dc) min) for single-ended signals as well as the limitations for overshoot and undershoot.
2. Vtt is expected to track ovdd/2.
3. Typ condition: typ model, 1.5 V, and 25 °C. Max condition: bcs model, 1.575V, and -40 °C. Min condition: wcs model, 1.425V, and max Tj °C 125 °C junction

Table 26. LPDDR2 mode AC Electrical characteristics

Symbol	Parameter	Test condition	Min	Max	Unit	Notes
Vih(ac)	AC input logic high		Vref+0.22	ovdd	V	Note that the Jedec LPDDR2 specification (JESD209-2B) supersedes any specification in this document.
Vil(ac)	AC input logic low			Vref-0.22	V	
Vidh(ac)[1]	AC differential input high voltage		0.44	-	V	
Vidl(ac)[1]	AC differential input low voltage			0.44	V	
Vix(ac)[2]	AC differential input crosspoint voltage	Relative to ovdd/2	-0.12	0.12	V	
Vpeak	Over/undershoot peak			0.35	V	
Varea	Over/undershoot area (above ovdd or below ovss)	at 800MHz data rate		0.3	V*ns	
tsr	Single output slew rate		0.4	2	V/ns	
tskd	Skew between pad rise/fall asymmetry + skew cased by SSN			0.2	ns	

Module	Name	Recommendation if Unused
USB	USB_DCAP, USB0_VBUS, USB1_VBUS	Connect USBx_VBUS and USB_DCAP together and tie to ground through a 10K ohm resistor. Do NOT tie directly to ground, latch-up risk.
	USB0_GND, USB1_GND	Ground
	USB0_VBUS_DETECT, USB1_VBUS_DETECT	Float
	USB0_DM, USB0_DP, USB1_DM, USB1_DP	Float
Video ADC	VDDA33_AFE	3.3V or Float
	VDD12_AFE	1.2V or Float
	VADC_AFE_BANDGAP	Float
	VADCSE0, VADCSE1, VADCSE2, VADCSE3	Ground or Float

9 Peripheral operating requirements and behaviours

9.1 Analog

9.1.1 12-bit ADC electrical characteristics

9.1.1.1 12-bit ADC operating conditions

Table 31. 12-bit ADC Operating Conditions

Characteristic	Conditions	Symb	Min	Typ [1]	Max	Unit	Comment
Supply voltage	Absolute	V_{DDAD}	2.5	-	3.6	V	-
	Delta to V_{DDAD} (VDD-VDDAD) [2]	ΔVDDAD	-100	0	100	mV	-
Ground voltage	Delta to V_{SSAD} (VSS-VSSAD) [2]	ΔVSSAD	-100	0	100	mV	-
Ref Voltage High	-	V_{REFH}	1.5	V_{DDAD}	V_{DDAD}	V	-
Ref Voltage Low	-	V_{REFL}	V_{SSAD}	V_{SSAD}	V_{SSAD}	V	-
Input Voltage	-	V_{ADIN}	V_{REFL}	-	V_{REFH}	V	-
Input Capacitance	8/10/12 bit modes	C_{ADIN}	-	1.5	2	pF	-
Input Resistance	ADLPC=0, ADHSC=1	R_{ADIN}	-	5	7	kohms	-
	ADLPC=0, ADHSC=0		-	12.5	15	kohms	-
	ADLPC=1, ADHSC=0		-	25	30	kohms	-

Table continues on the next page...

9.1.1.2 12-bit ADC characteristics

Table 32. 12-bit ADC Characteristics (V_{REFH} = V_{DDAD}, V_{REFL} = V_{SSAD})

Characteristic	Conditions[1]	Symb	Min	Typ [2]	Max	Unit	Comment
Supply Current	ADLPC=1, ADHSC=0	I_{DDAD}		250		µA	ADLSMP=0 ADSTS=10 ADCO=1
	ADLPC=0, ADHSC=0			350			
	ADLPC=0, ADHSC=1			400			
Supply Current	Stop, Reset, Module Off	I_{DDAD}		0.01	0.8	µA	
ADC Asynchronous Clock Source	ADHSC=0	f_{ADACK}		10		MHz	t_{ADACK} = $1/f_{ADACK}$
	ADHSC=1			20			
Sample Cycles	ADLSMP=0, ADSTS=00	Csamp		2		cycles	
	ADLSMP=0, ADSTS=01			4			
	ADLSMP=0, ADSTS=10			6			
	ADLSMP=0, ADSTS=11			8			
	ADLSMP=1, ADSTS=00			12			
	ADLSMP=1, ADSTS=01			16			
	ADLSMP=1, ADSTS=10			20			
	ADLSMP=1, ADSTS=11			24			
Conversion Cycles	ADLSMP=0 ADSTS=00	Cconv		28		cycles	
	ADLSMP=0 ADSTS=01			30			
	ADLSMP=0 ADSTS=10			32			
	ADLSMP=0 ADSTS=11			34			
	ADLSMP=1 ADSTS=00			38			
	ADLSMP=1 ADSTS=01			42			
	ADLSMP=1 ADSTS=10			46			
	ADLSMP=1, ADSTS=11			50			
Conversion Time	ADLSMP=0 ADSTS=00	Tconv		0.7		µs	Fadc=40 MHz
	ADLSMP=0 ADSTS=01			0.75			

Table continues on the next page...

Table 40. Receive signal timing for RMII interfaces (continued)

	Characteristic	RMII Mode		Unit
		Min	Max	
E4, E8	RMII_CLK pulse width low	35%	65%	RMII_CLK period
E1	RXD[1:0], CVS_DV, RXER to RMII_CLK setup	4	—	ns
E2	RMII_CLK to RXD[1:0], CRS_DV, RXER hold	2	—	ns
E6	RMII_CLK to TXD[1:0], TXEN valid	—	14	ns
E5	RMII_CLK to TXD[1:0], TXEN invalid	4	—	ns

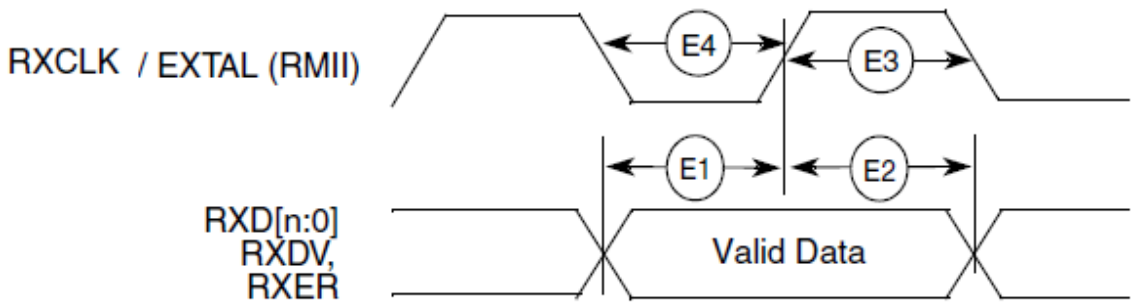


Figure 19. RMII receive signal timing diagram

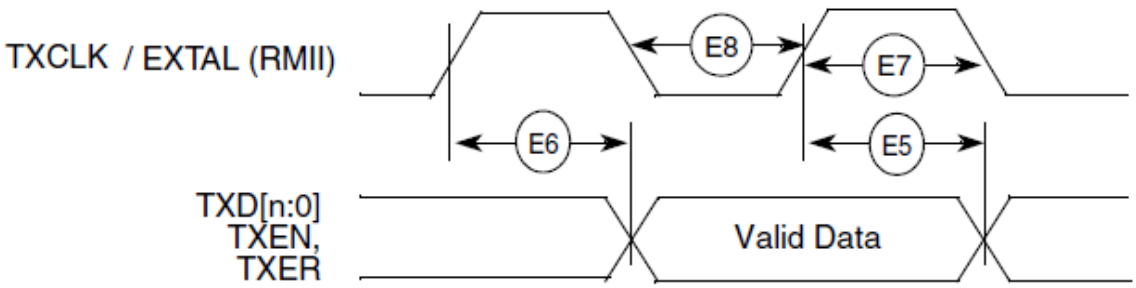


Figure 20. RMII transmit signal timing diagram

NOTE

See the most current device errata document when using the internally generated RXCLK and TXCLK clocks.

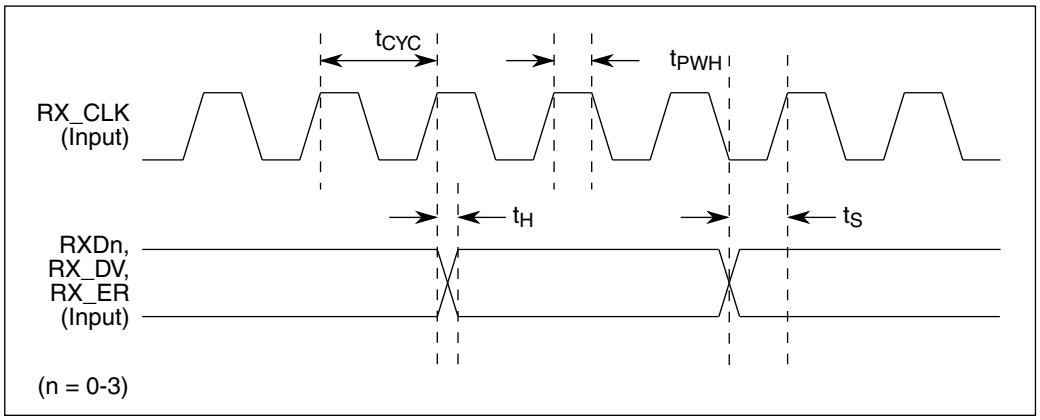


Figure 21. MII receive signal timing diagram

Table 41. Receive signal timing for MII interfaces

Characteristic		MII Mode			Unit
		Min	Typ	Max	
RX_CLK clock period (100/10 MBPS)	t_{CYC}		40/400		ns
RX_CLK duty cycle, t_{PWH}/t_{CYC}		45	50	55	%
Input setup time before RX_CLK	t_S	5			ns
Input setup time after RX_CLK	t_H	5			ns

9.3.3 Receive and Transmit signal timing specifications for MII interfaces

This section provides timing specs that meet the requirements for MII interfaces for a range of transceiver devices.

NOTE

Measurements were done using balanced load and 25 ohms resistor from outputs to VDD_REF.

9.5.4.5 LPDDR2 Read Cycle

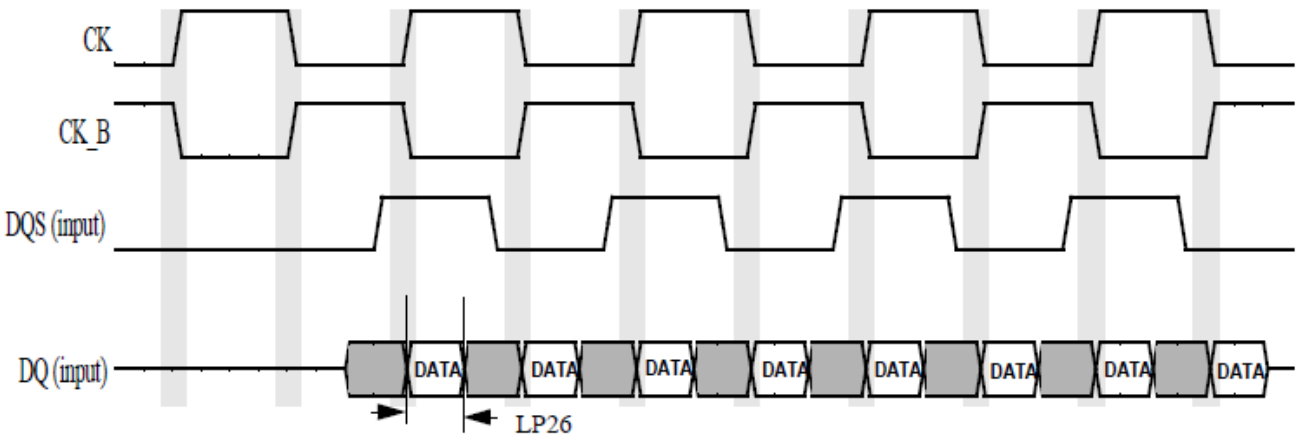


Figure 45. LPDDR2 Read cycle

Table 58. LPDDR2 Read Cycle

ID	Parameter	Symbol	CK = 400 MHz		Unit
			Min	Max	
LP26	Minimum required DQ valid window width for LPDDR2	-	270	-	ps

NOTE

To receive the reported setup and hold values, read calibration should be performed in order to locate the DQS in the middle of DQ window.

NOTE

All measurements are in reference to Vref level.

NOTE

Measurements were done using balanced load and 25 ohms resistor from outputs to VDD_REF

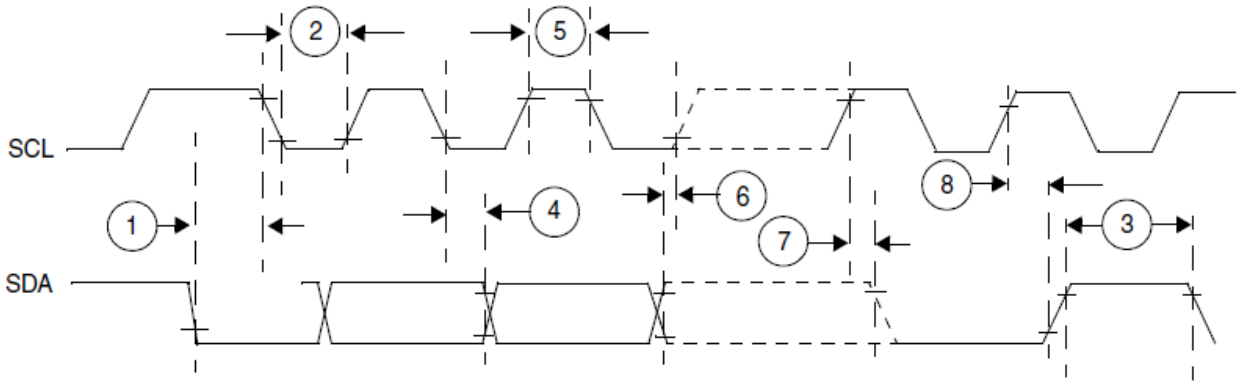


Figure 51. I2C input/output timing

9.6.3 SDHC specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface. A load of 50 pF is assumed.

Table 63. SDHC switching specifications

Num	Symbol	Description	Min.	Max.	Unit
		Operating voltage	1.71	3.6	V
	Card input clock				
SD1	fpp	Clock frequency (low speed)	0	400	kHz
	fpp	Clock frequency (SD\SDIO full speed\high speed)	0	25\50	MHz
	fpp	Clock frequency (MMC full speed\high speed)	0	20\50	MHz
	f_{OD}	Clock frequency (identification mode)	0	400	kHz
SD2	t_{WL}	Clock low time	7	—	ns
SD3	t_{WH}	Clock high time	7	—	ns
SD4	t_{TLH}	Clock rise time	—	3	ns
SD5	t_{THL}	Clock fall time	—	3	ns
	SDHC output / card inputs SDHC_CMD, SDHC_DAT (reference to SDHC_CLK)				
SD6	t_{OD}	SDHC output delay (output valid)	-5	4	ns
	SDHC input / card inputs SDHC_CMD, SDHC_DAT (reference to SDHC_CLK)				
SD7	t_{ISU}	SDHC input setup time	5	—	ns
SD8	t_{IH}	SDHC input hold time	0	—	ns

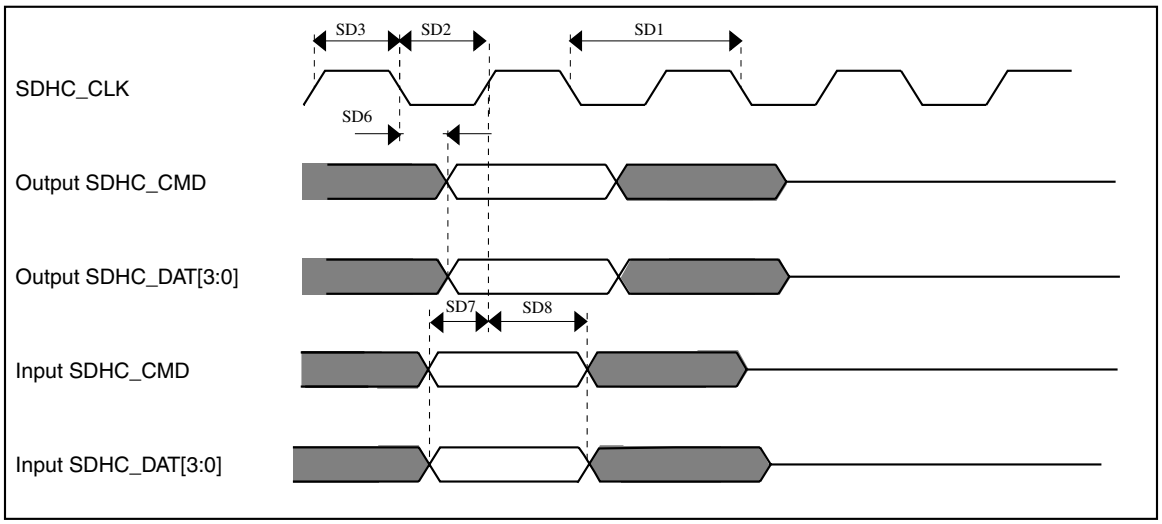


Figure 52. SDHC timing

9.6.4 USB PHY specifications

This section describes the USB-OTG PHY and the USB Host port PHY parameters.

The USB PHY meets the electrical compliance requirements defined in the Universal Serial Bus Revision 2.0 OTG, USB Host with the amendments below (On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification is not applicable to Host port).

- USB ENGINEERING CHANGE NOTICE
  - Title: 5V Short Circuit Withstand Requirement Change
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- Errata for USB Revision 2.0 April 27, 2000 as of 12/7/2000
- USB ENGINEERING CHANGE NOTICE
  - Title: Pull-up/Pull-down resistors
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- USB ENGINEERING CHANGE NOTICE
  - Title: Suspend Current Limit Changes
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification
  - Revision 2.0 plus errata and ecn June 4, 2010
- Battery Charging Specification (available from USB-IF)
  - Revision 1.2, December 7, 2010

364 MAP BGA	176 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
K2	4	JTDI	JTDI	PTA9	JTDI	RMII_ CLKOUT	RMII_CLKIN/ MII0_TXCLK	DCU0_R1		WDOG_b		
K1	5	JTDO	JTDO/ TRACESWO	PTA10	JTDO	EXT_AUDIO_ MCLK		DCU0_G0		ENET_TS_ CLKIN	MLBSIGNAL	
L1	6	JTMS/ SWDIO	JTMS/ SWDIO	PTA11	JTMS/ SWDIO			DCU0_G1			MLBDATA	
L3	7	PTA12		PTA12	TRACECK	EXT_AUDIO_ MCLK				VIU_DATA13	I2C0_SCL	
Y5	43	PTA16		PTA16	TRACED0	USB0_ VBUS_EN	ADC1_SE0	LCD29	SAI2_TX_ BCLK	VIU_DATA14	I2C0_SDA	
Y6	44	PTA17		PTA17	TRACED1	USB0_ VBUS_OC	ADC1_SE1	LCD30	USB0_SOF_ PULSE	VIU_DATA15	I2C1_SCL	
V6	46	PTA18		PTA18	TRACED2	ADC0_SE0	FTM1_QD_ PHA	LCD31	SAI2_TX_ DATA	VIU_DATA16	I2C1_SDA	
U6	47	PTA19		PTA19	TRACED3	ADC0_SE1	FTM1_QD_ PHB	LCD32	SAI2_TX_ SYNC	VIU_DATA17	QSPI1_A_ SCK	
B18	143	PTA20		PTA20	TRACED4			LCD33		SCI3_TX	DCU1_ HSYNC/ DCU1_ TCON1	
D18	145	PTA21		PTA21/ MII0_RXCLK	TRACED5				SAI2_RX_ BCLK	SCI3_RX	DCU1_ VSYNC/ DCU1_ TCON2	
E17	147	PTA22		PTA22	TRACED6				SAI2_RX_ DATA	I2C2_SCL	DCU1_TAG/ DCU1_ TCON0	
C17	148	PTA23		PTA23	TRACED7				SAI2_RX_ SYNC	I2C2_SDA	DCU1_DE/ DCU1_ TCON3	
R16	—	PTA24		PTA24	TRACED8	USB1_ VBUS_EN			SDHC1_CLK	DCU1_ TCON4		
R17	—	PTA25		PTA25	TRACED9	USB1_ VBUS_OC			SDHC1_CMD	DCU1_ TCON5		
R19	—	PTA26		PTA26	TRACED10	SAI3_TX_ BCLK			SDHC1_ DAT0	DCU1_ TCON6		
R20	—	PTA27		PTA27	TRACED11	SAI3_RX_ BCLK			SDHC1_ DAT1	DCU1_ TCON7		
P20	—	PTA28		PTA28	TRACED12	SAI3_RX_ DATA	ENET1_ 1588_TMR0	SCI4_TX	SDHC1_ DAT2	DCU1_ TCON8		
P18	—	PTA29		PTA29	TRACED13	SAI3_TX_ DATA	ENET1_ 1588_TMR1	SCI4_RX	SDHC1_ DAT3	DCU1_ TCON9		
P17	—	PTA30		PTA30	TRACED14	SAI3_RX_ SYNC	ENET1_ 1588_TMR2	SCI4_RTS	I2C3_SCL		SCI3_TX	
P16	—	PTA31		PTA31	TRACED15	SAI3_TX_ SYNC	ENET1_ 1588_TMR3	SCI4_CTS	I2C3_SDA		SCI3_RX	
T6	49	PTB0		PTB0	FTM0_CH0	ADC0_SE2	TRACECTL	LCD34	SAI2_RX_ BCLK	VIU_DATA18	QSPI1_A_ CS0	

364 MAP BGA	176 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
N16	103	PTE0	BOOTMOD1	PTE0	DCU0_ HSYNC/ DCU0_ TCON1	BOOTMOD1		LCD0				
N18	104	PTE1	BOOTMOD0	PTE1	DCU0_ VSYNC/ DCU0_ TCON2	BOOTMOD0		LCD1				
N19	105	PTE2		PTE2	DCU0_PCLK			LCD2				
Y15	80	PTE3		PTE3	DCU0_TAG/ DCU0_ TCON0			LCD3				
N20	106	PTE4		PTE4	DCU0_DE/ DCU0_ TCON3			LCD4				
T16	—	PTE5		PTE5	DCU0_R0			LCD5				
W16	—	PTE6		PTE6	DCU0_R1			LCD6				
M20	109	PTE7	RCON0	PTE7	DCU0_R2		RCON0	LCD7				
M19	110	PTE8	RCON1	PTE8	DCU0_R3		RCON1	LCD8				
M17	111	PTE9	RCON2	PTE9	DCU0_R4		RCON2	LCD9				
M16	112	PTE10	RCON3	PTE10	DCU0_R5		RCON3	LCD10				
L16	113	PTE11	RCON4	PTE11	DCU0_R6		RCON4	LCD11				
L17	114	PTE12	RCON5	PTE12	DCU0_R7	SPI1_PCS3	RCON5	LCD12			LPT_ALT0	
Y16	—	PTE13		PTE13	DCU0_G0			LCD13				
W15	—	PTE14		PTE14	DCU0_G1			LCD14				
L18	115	PTE15	RCON6	PTE15	DCU0_G2		RCON6	LCD15				
L20	116	PTE16	RCON7	PTE16	DCU0_G3		RCON7	LCD16				
K20	117	PTE17	RCON8	PTE17	DCU0_G4		RCON8	LCD17				
K19	118	PTE18	RCON9	PTE18	DCU0_G5		RCON9	LCD18				
K18	119	PTE19	RCON10	PTE19	DCU0_G6		RCON10	LCD19	I2C0_SCL			
A12	170	PTE20	RCON11	PTE20	DCU0_G7		RCON11	LCD20	I2C0_SDA		EWM_in	
V16	81	PTE21		PTE21	DCU0_B0			LCD21				
W17	84	PTE22		PTE22	DCU0_B1			LCD22				
J17	122	PTE23	RCON12	PTE23	DCU0_B2		RCON12	LCD23				
D19	134	PTE24	RCON13	PTE24	DCU0_B3		RCON13	LCD24				
C19	135	PTE25	RCON14	PTE25	DCU0_B4		RCON14	LCD25				
C20	137	PTE26	RCON15	PTE26	DCU0_B5		RCON15	LCD26				
B20	138	PTE27	RCON16	PTE27	DCU0_B6		RCON16	LCD27	I2C1_SCL			
K16	120	PTE28	RCON17	PTE28	DCU0_B7		RCON17	LCD28	I2C1_SDA		EWM_out	
V15	79	PTA7		PTA7	VIU_PIX_ CLK							
T14	76	EXT_ TAMPER0			EXT_ TAMPER0							

Table 76. Special Signal Considerations (continued)

Special Signal	Comments
JTCLK, JTDI, JTDO, JTMS	For JTAG the use of external resistors is unnecessary. However, if external resistors are used, the user must ensure that the on-chip pull-up/down configuration is matched. For example, do not use an external pull down on an input that has on-chip pull-up. JTDO is configured with a keeper circuit such that the floating condition is eliminated if an external pull resistor is not present. An external pull resistor on JTDO is detrimental and should be avoided.
LVDS0N, LVDS0P	Not recommended for application use, intended for clock observation purposes during debug only.
RESETB/RESET_OUT	Active low input used to generate a system wide reset (except the SRTC). A glitch filter is include to help prevent unexpected resets, a minimum pulse width of 125 nsecs is required to guarantee a reset is detected.
XTAL, EXTAL	A 24.0 MHz fundamental mode crystal should be connected between XTAL and EXTAL. The crystal must be rated for a drive level of 250 µW or higher. An ESR (equivalent series resistance) of 80 Ω or less is recommended. This clock is used as a reference for USB, so there are strict frequency tolerance and jitter requirements. The crystal can be eliminated if an external 24 MHz oscillator is available in the system. In this case, XTAL must be directly driven by the external oscillator and EXTAL floated. The XTAL signal level must swing from ~0.8 x DECAP_V11_ LDO_OUT to ~0.2 V.
XTAL32, EXTAL32	If the user wishes to configure XTAL32 and EXTAL32 as an RTC oscillator, a 32.768 kHz crystal, (≤50 kΩ ESR, 10 pF load) should be connected between XTAL32 and EXTAL32. Keep in mind the capacitors implemented on either side of the crystal are about twice the crystal load capacitor. To hit the exact oscillation frequency, the board capacitors need to be reduced to account for board and chip parasitics. The integrated oscillation amplifier is self biasing, but relatively weak. Care must be taken to limit parasitic leakage from XTAL32 and EXTAL32 to either power or ground (>100 MΩ). This will debias the amplifier and cause a reduction of startup margin. Typically XTAL32 and EXTAL32 should bias to approximately 0.5 V. If it is desired to feed an external low frequency clock into XTAL32 the EXTAL32 pin should be left floating or driven with a complimentary signal. The logic level of this forcing clock should not exceed DECAP_V11_ LDO_OUT level and the frequency should be <100 kHz under typical conditions. In the case where the SIRC is used, it is recommended to connect XTAL32 to ground and leave EXTAL32 floating.

Table 77. Power Supply Pins (continued)

Supply Rail Name	364 MAP BGA	176 LQFP (F-series ONLY)	Comment
VSS	A1, A20, B3, B5, B8, B11, B13, B16, B19, C2, D17, E5, E8, E11, E14, E19, F2, G8, G10, G12, G14, G17, H4, H7, H9, H11, H13, H19, J2, J8, J9, J10, J11, J12, J14, J18, K7, K9, K10, K11, K12, K13, L8, L9, L10, L11, L12, L14, L19, M2, M4, M7, M9, M10, M11, M12, M13, M18, N8, N10, N12, N14, P7, P9, P11, P13, P19, R2, R18, U7, U19, V11, V13, V17, W6, Y1, Y20	1, 13, 24, 32, 45, 67, 82, 96, 107, 139, 144, 157, 175, 176, FLG	Ground—connect "Flag pad (FLG)" to the internal GND plane with numerous vias, for both electrical and thermal purposes.
VSSA33_ADC	V2	39	ATD Ground
VSS12_AFE	R5	Video ADC not supported in LQFP	Video ADC Ground
VSSA33_AFE	V4	Video ADC not supported in LQFP	Video ADC Ground
VSS_KEL0	U11	66	Ground (VSS and VSS_KEL0 are NOT connected internally)

14 Functional Assignment Pins

14.1 Functional Assignment Pins

Table 78. Functional Assignment Pins

Signal Name	364 MAP BGA	176 LQFP (F-series ONLY)	Power Group	Pad Type	Default Mode (Reset)	Default Function	Input/ Output	Value
ADC0SE8	Y2	—	VDDA33_ADC	Analog	—	ADC0SE8	—	—
ADC0SE9	W2	—	VDDA33_ADC	Analog	—	ADC0SE9	—	—
ADC1SE8	W3	—	VDDA33_ADC	Analog	—	ADC1SE8	—	—
ADC1SE9	Y3	—	VDDA33_ADC	Analog	—	ADC1SE9	—	—
BCTRL	T2	33	VDDREG	Analog	—	BCTRL	—	—
DACO0	U1	36	VDDA33_ADC	Analog	—	DACO0	—	—
DACO1	U2	37	VDDA33_ADC	Analog	—	DACO1	—	—

Table continues on the next page...