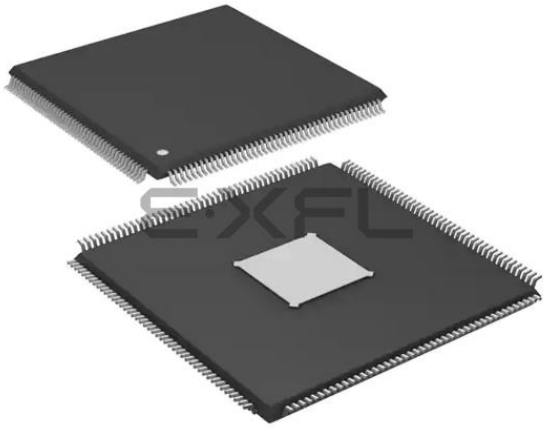

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A5
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	266MHz
Co-Processors/DSP	Multimedia; NEON™ MPE
RAM Controllers	LPDDR2, DDR3, DRAM
Graphics Acceleration	Yes
Display & Interface Controllers	DCU, GPU, LCD, VideoADC, VIU
Ethernet	10/100Mbps (2)
SATA	-
USB	USB 2.0 OTG + PHY (1)
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	-
Package / Case	176-LQFP Exposed Pad
Supplier Device Package	176-HLQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mvf30nn152cku26

Field	Description	Values
R	Revision	• 1 = Rev 1.x
T	Temperature range (°C)	• C = -40 °C to +85 °C T_a
PP	Package type	• KU = 176LQFP • MK = 364 MAPBGA
S	Speed	• Speed A5 Core • 26 = 266MHz • 40 = 400MHz • 50 = 500MHz

2.4 Part Numbers

This table lists the part numbers on the device.

Part Number	Package	Description
MVF30NN151CKU26	LQFP-EP 176 24*24*1.6	A5-266, No Security, 176LQFP
MVF30NS151CKU26	LQFP-EP 176 24*24*1.6	A5-266, Security, 176LQFP
MVF50NN151CMK40	MAP 364 17*17*1.5 P0.8	A5-400, No Security, 364BGA
MVF50NS151CMK40	MAP 364 17*17*1.5 P0.8	A5-400, Security, 364BGA
MVF50NN151CMK50	MAP 364 17*17*1.5 P0.8	A5-500, No Security, 364BGA
MVF50NS151CMK50	MAP 364 17*17*1.5 P0.8	A5-500, Security, 364BGA
MVF51NN151CMK50	MAP 364 17*17*1.5 P0.8	A5-500, L2 Cache, No Security, 364BGA
MVF51NS151CMK50	MAP 364 17*17*1.5 P0.8	A5-500, L2 Cache, Security, 364BGA
MVF60NN151CMK40	MAP 364 17*17*1.5 P0.8	A5-400, M4, No Security, 364BGA
MVF60NS151CMK40	MAP 364 17*17*1.5 P0.8	A5-400, M4, Security, 364BGA
MVF60NN151CMK50	MAP 364 17*17*1.5 P0.8	A5-500, M4, No Security, 364BGA
MVF60NS151CMK50	MAP 364 17*17*1.5 P0.8	A5-500, M4, Security, 364BGA
MVF61NN151CMK50	MAP 364 17*17*1.5 P0.8	A5-500, M4, L2 Cache, No Security, 364BGA
MVF61NS151CMK50	MAP 364 17*17*1.5 P0.8	A5-500, M4, L2 Cache, Security, 364BGA
MVF62NN151CMK40	MAP 364 17*17*1.5 P0.8	A5-400, M4 Primary, No Security, 364BGA

3 Terminology and guidelines

3.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

3.1.1 Example

This is an example of an operating requirement:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	0.9	1.1	V

3.2 Definition: Operating behavior

Unless otherwise specified, an *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

3.2.1 Example

This is an example of an operating behavior:

Symbol	Description	Min.	Max.	Unit
I_{WP}	Digital I/O weak pullup/ pulldown current	10	130	µA

3.3 Definition: Attribute

An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

Table 3. LPREG electrical characteristics (continued)

Parameters	Min	Typ	Max	Unit	Comments
PSRR with 4.7uF output cap					
@ DC @noload			-40	dB	
@ DC @full load			-35		
Worst case @ any frequency			-12		

6.2.1.3 ULPREG electrical characteristics

Table 4. ULPREG electrical characteristics

Parameters	Min	Typ	Max	Unit	Comments
Power supply	3.0	3.3	3.6	V	
Current Consumption	1.88	2.3	2.86	µA	@ no load
	-	610	670	µA	@ full load
Output current capacity			20	mA	DC load current
Output voltage @ no load			1.175	V	
Output voltage @ full load	1.125			V	
PSRR with 500 pF output cap	-20			dB	Worst case at any frequency across corners
@ DC @noload			-50	dB	
@200KHz @noload			-37		
@ DC @full load			-42		
@200KHz @full load			-37		
Worst case @ any frequency @ any load			-15		

6.2.1.4 WBREG electrical characteristics

Table 5. WBREG electrical characteristics

Parameters	Min	Typ	Max	Unit	Comments
Power supply	3	3.3	3.6	V	-
Current Consumption	-	2	5	µA	@ no load
	-	2	5	µA	@ full load
Output current capacity	-	1	2	mA	DC load current
Output voltage @ no load		1.4	1.425	V	
Output voltage @ full load	1.375	1.398		V	
Output voltage programmability	1.4	1.4	1.7	V	16 steps of 25 mV each

Table 20. GPIO DC Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
		VOH/VOL values are with respect to DSE=001[1]				
Vol	Low-level output voltage	Iol= 1mA			0.15	V
Vih [2]	High-Level DC input voltage		0.7*ovdd		ovdd	V
Vil[2]	Low-Level DC input voltage		0		0.3*ovdd	V
Vhys	Input Hysteresis	ovdd=3.3 V	250			mV
Vt+[2, 3]	Schmitt trigger VT+		0.5*ovdd			V
Vt-[2, 3]	Schmitt trigger VT-				0.5*ovdd	V
Iin[4]	Input current (no pull-up/down)	Vin = ovdd or 0	-1		1	uA
Iin_22pu	Input current (22KOhm PU)	Vin = 0			212	uA
		Vin = ovdd			1	
Iin_47pu	Input current (47KOhm PU)	Vin = 0			100	
		Vin = ovdd			1	
Iin_100pu	Input current (100KOhm PU)	Vin = 0			50	
		Vin = ovdd			1	
Iin_100pd	Input current (100KOhm PD)	Vin = 0			1	
		Vin = ovdd			50	
R_Keeper	Keeper Circuit Resistance	Vin = 0.3 x OVDD VI = 0.7 x OVDD	105		175	Ohm
Issod	Sink current in open drain mode	Vin = ovdd			7	mA
Issop	Sink/source current in Push Pull mode	Vin = ovdd			7	mA

1. For details about Software MUX Pad Control Register DSE bit, see IOMUX Controller chapter of the device reference manual.
2. To maintain a valid level, the transitioning edge of the input must sustain a constant slew rate (monotonic) from the current DC level through to the target DC level, VIL or VIH. Monotonic input transition time is from 0.1ns to 1s. Vil and Vih do not apply when hysteresis is enabled.
3. Hysteresis of 250 mV is guaranteed over all operating conditions when hysteresis is enabled.
4. Typ condition: typ model, 3.3V, and 25°C. Max condition: bcs model, 3.6V, and -40°C. Min condition: wcs model, 3.0V and 85 °C. These values are for digital IO buffer cells.

Table 24. LPDDR2 mode DC Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
Iin[2]	Input current (no pull-up/ down)	Vin = ovdd or 0			2.5	uA	
Tri-state I/O supply current[2]	Icc-ovdd	Vin = ovdd or 0			4		
Tri-state vdd2p5 supply current[2]	Icc-vdd2p5	Vi = vddi or 0			1.5		
Tri-state core supply current[2]	Icc-vddi				1		
Driver unit (240 Ohm) calibration resolution	Rres				10	Ohm	

1. The single-ended signals need to be within the respective limits (Vih(dc) max, Vil(dc) min) for single-ended signals as well as the limitations for overshoot and undershoot.
2. Typ condition: typ model, 1.2 V, and 25 °C junction. Max condition: bcs model, 1.26V, and -40 °C. Min condition: wcs model, 1.14V, and Tj 125 °C.

Table 25. DDR3 mode DC Electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
Voh	High-level output voltage		0.8*ovdd			V	Note that the JEDEC JESD79_3E specification supersedes any specification in this document
Vol	Low-level output voltage	Iol= 1mA			0.2*ovdd	V	
Vref	Input reference voltage		0.49*ovdd	0.5*ovdd	0.51*ovdd	V	
Vih(dc)	DC input high voltage		Vref+0.1		ovdd	V	
Vil(dc)	DC input low voltage		ovss		Vref-0.1	V	
Vih(diff)	DC differential input logic high		0.2		Note[1]	V	
Vil(diff)	DC differential input logic low		Note[1]		-0.2	V	
Vtt[2]	Termination voltage	Vin = ovdd or 0	0.49*ovdd	0.5*ovdd	0.51*ovdd		
Iin[3]	Input current (no pullup/ pulldown)	Vi = 0 Vi = ovdd			3	uA	

Table continues on the next page...

Table 28. Power sequencing (continued)

Power Supply (PKG Level)	Board Level Power Nets	Parameters	Power Order	Comment
VDD33_LDOIN	VDD33	LDO input supply (LDO1P1, LDO2P5, LDO1P1_RTC)	1	VDD33_LDOIN,VDDREG and VDD33 should come from a common supply source (represented as 3.3V SMPS in the Figure 4)
VDDREG	VDD33	Device PMU regulator and External ballast supply	1	
VDD33	VDD33	GPIO 3.3V IO supply, LCD Supply	1	
SDRAMC_VDD1P5	SDRAMC_VDD1P5	1.2/1.5 DDR Main IO supply	NA	In case the Ballast transistor's collector is connected to the 1.5V DRAM supply (instead of the 3.3V supply), turn this 1.5V supply on before turning on the 3.3V.
VDDA33_ADC	VDDA33_ADC	3.3V supply for ADC, DAC and IO segment	1	
VREFH_ADC	VREFH_ADC	High Reference of ADC, DAC	1	
VDDA33_AFE	VDDA33_AFE	3.3V supply of AFE (Video ADC)	1	
VDD12_AFE	VDD	1.2V supply for AFE (Video ADC)	2	
FA_VDD	VDD	Shorted with VDD at Board Level in 364BGA (Test pin only)	NA	
VDD	VDD	1.2V core supply from External ballast	2	
USB0_VBUS 1	USB_VBUS	VBUS supply for USB	NA	
USB1_VBUS 2	USB_VBUS	VBUS supply for USB	NA	

1. Power sequencing of USB0_VBUS is independent of any other power supply.
2. Power sequencing of USB1_VBUS is independent of any other power supply.

NOTE

NA stands for no sequencing needs, for example, the supply can come in any order.

NOTE

All supplies grouped together e.g. 1,2, others. These have no power sequencing restriction in between them.

NOTE

If none of the SDRAMC pins are connected on the board, the SDRAMC supply could be left floating.

NOTE

At power up, 1.2V supply will follow 3.3V supply. At power down, it should be checked that 1.2V falls before 3.3V.

NOTE

The standby current on USBx_VBUS is 300 - 500 uA. This is well below the 2.5 mA limit set by the USB 2.0 specification.

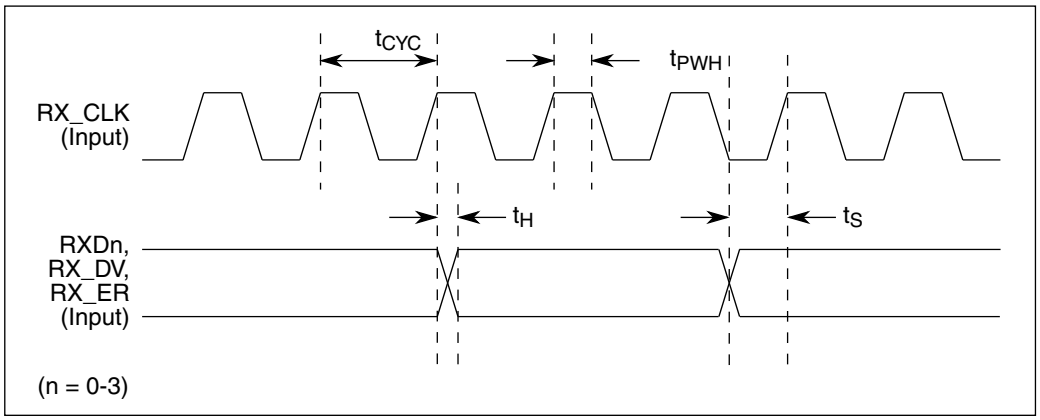

Figure 21. MII receive signal timing diagram

Table 41. Receive signal timing for MII interfaces

Characteristic		MII Mode			Unit
		Min	Typ	Max	
RX_CLK clock period (100/10 MBPS)	t_{CYC}		40/400		ns
RX_CLK duty cycle, t_{PWH}/t_{CYC}		45	50	55	%
Input setup time before RX_CLK	t_S	5			ns
Input setup time after RX_CLK	t_H	5			ns

9.3.3 Receive and Transmit signal timing specifications for MII interfaces

This section provides timing specs that meet the requirements for MII interfaces for a range of transceiver devices.

9.4.2 SPDIF Timing Parameters

The Sony/Philips Digital Interconnect Format (SPDIF) data is sent using the bi-phase marking code. When encoding, the SPDIF data signal is modulated by a clock that is twice the bit rate of the data signal. Table and Figure below show SPDIF timing parameters for the Sony/Philips Digital Interconnect Format (SPDIF), including the timing of the modulating Rx clock (SRCK) for SPDIF in Rx mode and the timing of the modulating Tx clock (STCLK) for SPDIF in Tx mode.

Table 45. SPDIF Timing Parameters

Characteristic	Symbol	Timing Parameter Range		Unit
		Min	Max	
SPDIFIN Skew: asynchronous inputs, no specs apply			0.7	ns
SPDIFOUT output (Load = 50pf) • Skew • Transition rising • Transition falling			• 1.5 • 24.2 • 31.3	ns
SPDIFOUT1 output (Load = 30pf) - Skew			1.5	ns
• Transition rising • Transition falling		Refer Table 21		
Modulating Rx clock (SRCK) period	srckp	40		ns
SRCK high period	srckph	16		ns
SRCK low period	srckpl	16		ns
Modulating Tx clock (STCLK) period	stclkp	40		ns
STCLK high period	stclkph	16		ns
STCLK low period	stclkpl	16		ns

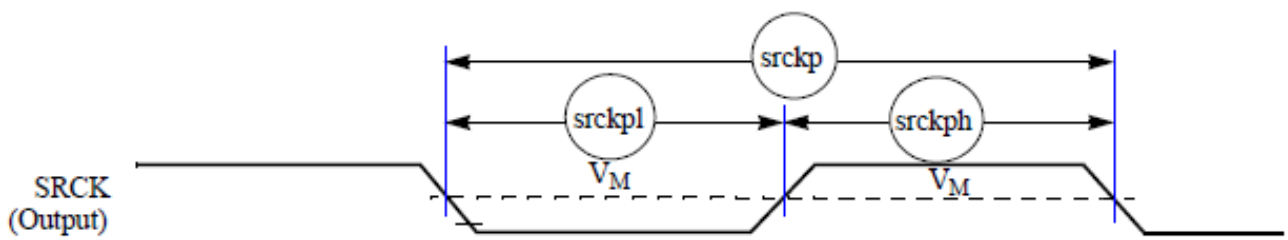

Figure 26. SRCK Timing Diagram

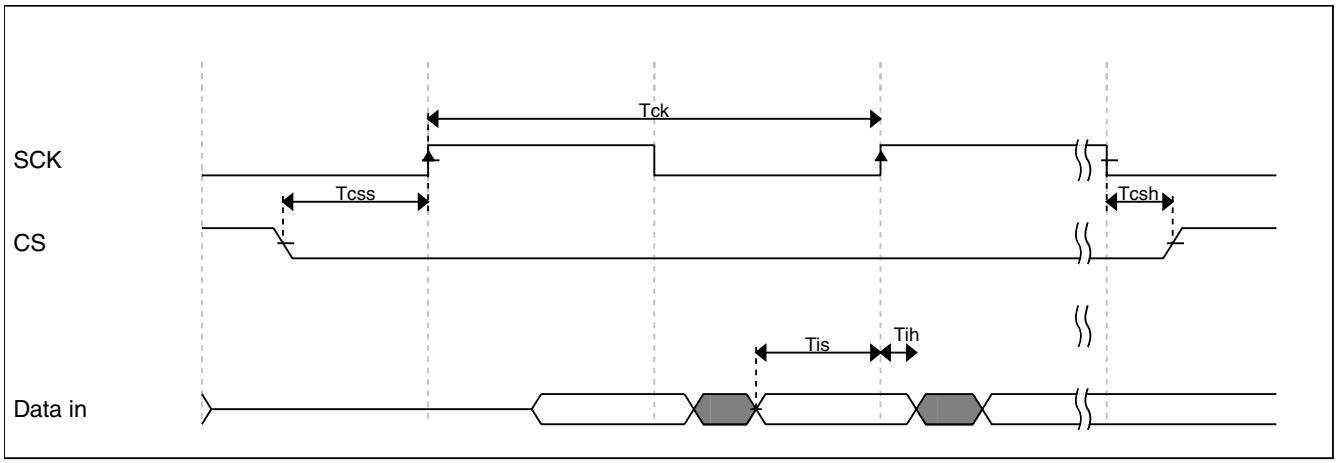

Figure 32. QuadSPI Input/Read timing (DDR mode)

NOTE

- The numbers are for a setting of 0x1 in regiater QuadSPI_SMPR[DDRSMP]
- Read frequency calculations should be: SCK/2 > (flash access time) + Setup (Tis) - (QuadSPI_SMPR[DDRSMP])x SCK/4
- Frequency calculator guideline (Max read frequency): SCK/2 > (Flash access time)max + (Tis)max - (QuadSPI_SMPR[DDRSMP]) xSCK/4
- Hold timing: flash_access (min) + flash_data_valid (min) > SCK/2 + HOLD(Tih) + (QuadSPI_SMPR[DDRSMP])SCK/4
- A negative time indicates the actual capture edge inside the device is earlier than clock appearing at pad.

Table 50. QuadSPI Input/Read timing (DDR mode)

Symbol	Parameter	Value		Unit
		Min	Max	
T_{is}	Setup time for incoming data	6.4	—	ns
T_{ih}	Hold time requirement for incoming data	-3.0	—	ns

NOTE

Table 52. NFC specifications

Num	Description	Min.	Max.	Unit
t_{CLS}	NFC_CLE setup time	$2T_H + T_L - 1$	—	ns
t_{CLH}	NFC_CLE hold time	$T_H + T_L - 1$	—	ns
t_{CS}	$\overline{\text{NFC\_CEn}}$ setup time	$2T_H + T_L - 1$	—	ns
t_{CH}	$\overline{\text{NFC\_CEn}}$ hold time	$T_H + T_L$	—	ns
t_{WP}	$\overline{\text{NFC\_WP}}$ pulse width	$T_L - 1$	—	ns
t_{ALS}	NFC_ALE setup time	$2T_H + T_L$	—	ns
t_{ALH}	NFC_ALE hold time	$T_H + T_L$	—	ns
t_{DS}	Data setup time	$T_L - 1$	—	ns
t_{DH}	Data hold time	$T_H - 1$	—	ns
t_{WC}	Write cycle time	$T_H + T_L - 1$	—	ns
t_{WH}	$\overline{\text{NFC\_WE}}$ hold time	$T_H - 1$	—	ns
t_{RR}	Ready to $\overline{\text{NFC\_RE}}$ low	$4T_H + 3T_L + 90$	—	ns
t_{RP}	$\overline{\text{NFC\_RE}}$ pulse width	$T_L + 1$	—	ns
t_{RC}	Read cycle time	$T_L + T_H - 1$	—	ns
t_{REH}	$\overline{\text{NFC\_RE}}$ high hold time	$T_H - 1$	—	ns
t_{IS}	Data input setup time	11	—	ns

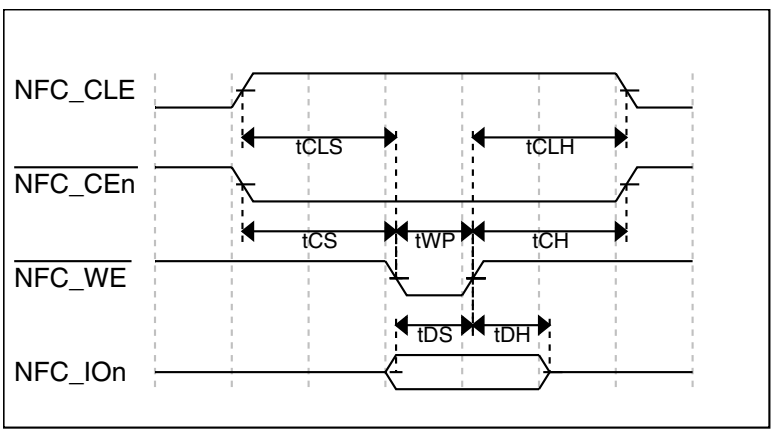

Figure 34. Command latch cycle timing

9.5.4.6 LPDDR2 Write Cycle

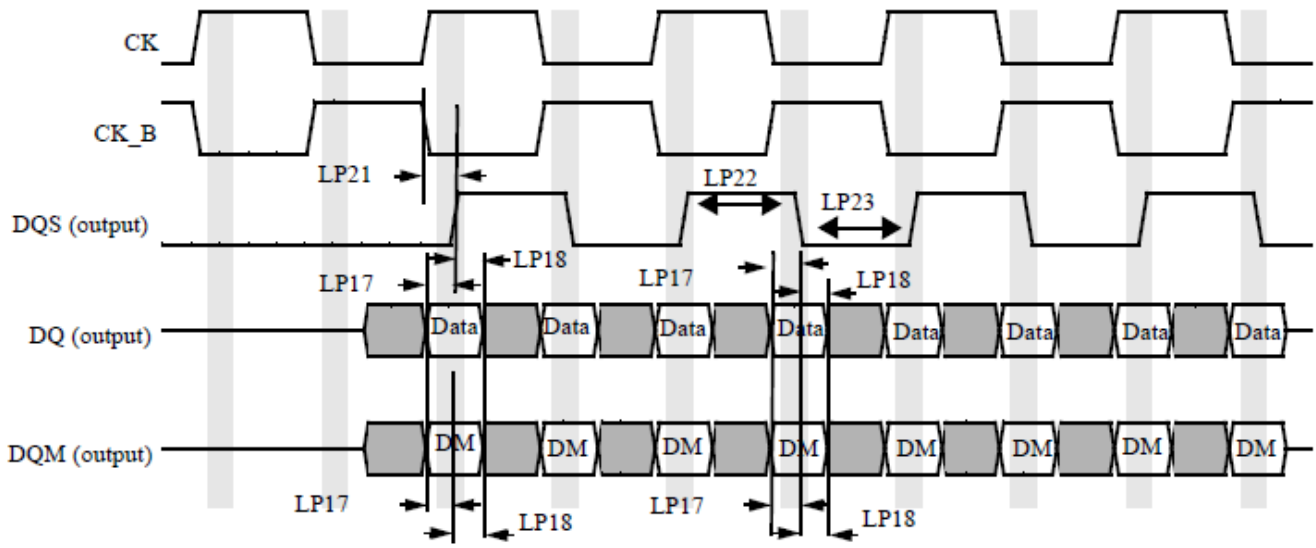

Figure 46. LPDDR3 Write Cycle

Table 59. LPDDR2 Write Cycle

ID	Parameter	Symbol	CK = 400 MHz		Unit
			Min	Max	
LP17	DQ and DQM setup time to DQS (differential strobe)	tDS	220	0.55	ps
LP18	DQ and DQM hold time to DQS (differential strobe)	tDH	220	0.55	ps
LP21	DQS latching rising transitions to associated clock edges	tDQSS	-0.25	+0.25	tCK
LP22	DQS high level width	tDQSH	0.4	-	tCK
LP23	DQS low level width	tDQSL	0.4	-	tCK

NOTE

To receive the reported setup and hold values, write calibration should be performed in order to locate the DQS in the middle of DQ window.

NOTE

All measurements are in reference to Vref level.

NOTE

Measurements were done using balanced load and 25 ohms resistor from outputs to VDD_REF.

Table 66. Fast internal oscillator electrical characteristics (continued)

Symbol	Parameter	Condition[1]	Value			
			Min	Typ	Max	Unit
RCMVAR	RC oscillator variation in temperature and supply with respect to f_{RC} at T_A = 55 °C in high frequency configuration		-5		+5	%

1. V_{DD} = 1.2 V , T_A = -40 to +85 °C, unless otherwise specified.

9.7.4 Slow internal RC oscillator (128 KHz) electrical characteristics

This section describes a slow internal RC oscillator (SIRC). This can be used as the reference clock for the RTC module.

Table 67. Slow internal RC oscillator electrical characteristics

Symbol	Parameter	Condition[1]	Value			
			Min	Typ	Max	Unit
f_{RCL}	RC oscillator low frequency	T_A= 25 °C, trimmed	—	128	—	kHz
I_{RCL}	RC oscillator low frequency current	T_A= 25 °C, trimmed	—	3.1		µA
RCLTRIM	RC oscillator precision after trimming of f_{RCL}	T_A= 25 °C	-1	—	+1	%
RCLVAR 3	RC oscillator variation in temperature and supply with respect to f_{RC} at T_A = 55 °C in high frequency configuration	High frequency configuration	-5	—	+5	%

1. V_{DD} = 1.2 V , T_A = -40 to +85 °C, unless otherwise specified.

9.7.5 PLL1 and PLL2 (528 MHz System PLL) Electrical Parameters

Table 68. PLL1 and PLL2 Electrical Parameters

Parameter	Value
Clock output range	528 MHz PLL output
Reference clock	24 MHz
Lock time	<7500 reference cycles
Period jitter(p2p)	<140ps
Duty Cycle	48.9%~51.7% PLL output

5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

11 Dimensions

11.1 Obtaining package dimensions

Package dimensions are provided in package drawing.

To find a package drawing, go to www.freescale.com and perform a keyword search for the drawing's document number:

Package	Freescale Document Number
176-pin LQFP	98ASA00452D
364 MAPBGA	98ASA00418D

12 Pinouts

12.1 Pinouts

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The IOMUX Controller (IOMUXC) Module is responsible for selecting which ALT functionality is available on each pin.

NOTE

The 176 LQFP parts are not pin compatible between the F-Series and R-Series families.

364 MAP BGA	176 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
Y2	—	ADC0SE8	N/A		ADC0_SE8							
W2	—	ADC0SE9			ADC0_SE9							
W3	—	ADC1SE8			ADC1_SE8							
Y3	—	ADC1SE9			ADC1_SE9							
W1	41	VREFH_ADC			VREFH_ADC							
U3	40	VREFL_ADC			VREFL_ADC							

364 MAP BGA	176 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
V1	38	VDDA33_ ADC			VDDA33_ ADC							
V2	39	VSSA33_ ADC			VSSA33_ ADC							
U1	36	DACO0			DACO0							
U2	37	DACO1			DACO1							
Y4	—	VADCSE0			VADCSE0							
U4	—	VADCSE1			VADCSE1							
W4	—	VADCSE2			VADCSE2							
V5	—	VADCSE3			VADCSE3							
V3	—	VDDA33_ AFE			VDDA33_ AFE							
V4	—	VSSA33_AFE			VSSA33_AFE							
T5	—	VDD12_AFE			VDD12_AFE							
R5	—	VSS12_AFE			VSS12_AFE							
U5	—	VADC_AFE_ BANDGAP			VADC_AFE_ BANDGAP							
Y13	73	EXTAL			EXTAL							
W13	72	XTAL			XTAL							
Y12	70	EXTAL32			EXTAL32							
W12	71	XTAL32			XTAL32							
T4	35	RESETB/ RESET_OUT	RESETB/ RESET_OUT		RESETB/ RESET_OUT							
N5	19	PTA6		PTA6	RMII_ CLKOUT	RMII_CLKIN/ MII0_TXCLK		DCU1_ TCON11			DCU1_R2	
T3	34	TEST			TEST							
T1	30	Ext_POR			TEST2							
V12	69	DECAP_ V11_LDO_ OUT			DECAP_ V11_LDO_ OUT							
T11	65	DECAP_ V25_LDO_ OUT			DECAP_ V25_LDO_ OUT							
T2	33	BCTRL			BCTRL							
P5	31	VDDREG			VDDREG							
T12	68	VDD33_ LDOIN			VDD33_ LDOIN							
V11	67	VSS			VSS							
U11	66	VSS_KEL0			VSS_KEL0							
W14	—	LVDS0P			LVDS0P							
Y14	—	LVDS0N			LVDS0N							
K4	3	JTCLK/ SWCLK	JTCLK/ SWCLK	PTA8	JTCLK/ SWCLK			DCU0_R0			MLBCLK	

364 MAP BGA	176 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
K2	4	JTDI	JTDI	PTA9	JTDI	RMII_ CLKOUT	RMII_CLKIN/ MII0_TXCLK	DCU0_R1		WDOG_b		
K1	5	JTDO	JTDO/ TRACESWO	PTA10	JTDO	EXT_AUDIO_ MCLK		DCU0_G0		ENET_TS_ CLKIN	MLBSIGNAL	
L1	6	JTMS/ SWDIO	JTMS/ SWDIO	PTA11	JTMS/ SWDIO			DCU0_G1			MLBDATA	
L3	7	PTA12		PTA12	TRACECK	EXT_AUDIO_ MCLK				VIU_DATA13	I2C0_SCL	
Y5	43	PTA16		PTA16	TRACED0	USB0_ VBUS_EN	ADC1_SE0	LCD29	SAI2_TX_ BCLK	VIU_DATA14	I2C0_SDA	
Y6	44	PTA17		PTA17	TRACED1	USB0_ VBUS_OC	ADC1_SE1	LCD30	USB0_SOF_ PULSE	VIU_DATA15	I2C1_SCL	
V6	46	PTA18		PTA18	TRACED2	ADC0_SE0	FTM1_QD_ PHA	LCD31	SAI2_TX_ DATA	VIU_DATA16	I2C1_SDA	
U6	47	PTA19		PTA19	TRACED3	ADC0_SE1	FTM1_QD_ PHB	LCD32	SAI2_TX_ SYNC	VIU_DATA17	QSPI1_A_ SCK	
B18	143	PTA20		PTA20	TRACED4			LCD33		SCI3_TX	DCU1_ HSYNC/ DCU1_ TCON1	
D18	145	PTA21		PTA21/ MII0_RXCLK	TRACED5				SAI2_RX_ BCLK	SCI3_RX	DCU1_ VSYNC/ DCU1_ TCON2	
E17	147	PTA22		PTA22	TRACED6				SAI2_RX_ DATA	I2C2_SCL	DCU1_TAG/ DCU1_ TCON0	
C17	148	PTA23		PTA23	TRACED7				SAI2_RX_ SYNC	I2C2_SDA	DCU1_DE/ DCU1_ TCON3	
R16	—	PTA24		PTA24	TRACED8	USB1_ VBUS_EN			SDHC1_CLK	DCU1_ TCON4		
R17	—	PTA25		PTA25	TRACED9	USB1_ VBUS_OC			SDHC1_CMD	DCU1_ TCON5		
R19	—	PTA26		PTA26	TRACED10	SAI3_TX_ BCLK			SDHC1_ DAT0	DCU1_ TCON6		
R20	—	PTA27		PTA27	TRACED11	SAI3_RX_ BCLK			SDHC1_ DAT1	DCU1_ TCON7		
P20	—	PTA28		PTA28	TRACED12	SAI3_RX_ DATA	ENET1_ 1588_TMR0	SCI4_TX	SDHC1_ DAT2	DCU1_ TCON8		
P18	—	PTA29		PTA29	TRACED13	SAI3_TX_ DATA	ENET1_ 1588_TMR1	SCI4_RX	SDHC1_ DAT3	DCU1_ TCON9		
P17	—	PTA30		PTA30	TRACED14	SAI3_RX_ SYNC	ENET1_ 1588_TMR2	SCI4_RTS	I2C3_SCL		SCI3_TX	
P16	—	PTA31		PTA31	TRACED15	SAI3_TX_ SYNC	ENET1_ 1588_TMR3	SCI4_CTS	I2C3_SDA		SCI3_RX	
T6	49	PTB0		PTB0	FTM0_CH0	ADC0_SE2	TRACECTL	LCD34	SAI2_RX_ BCLK	VIU_DATA18	QSPI1_A_ CS0	

364 MAP BGA	176 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
T7	50	PTB1	RCON30	PTB1	FTM0_CH1	ADC0_SE3	RCON30	LCD35	SAI2_RX_DATA	VIU_DATA19	QSPI1_A_DATA3	
V7	51	PTB2	RCON31	PTB2	FTM0_CH2	ADC1_SE2	RCON31	LCD36	SAI2_RX_SYNC	VIU_DATA20	QSPI1_A_DATA2	
W7	53	PTB3		PTB3	FTM0_CH3	ADC1_SE3	EXTRIG	LCD37		VIU_DATA21	QSPI1_A_DATA1	
Y7	54	PTB4		PTB4	FTM0_CH4	SCI1_TX	ADC0_SE4	LCD38	VIU_FID	VIU_DATA22	QSPI1_A_DATA0	
Y8	55	PTB5		PTB5	FTM0_CH5	SCI1_RX	ADC1_SE4	LCD39	VIU_DE	VIU_DATA23	QSPI1_A_DQS	
W8	56	PTB6		PTB6	FTM0_CH6	SCI1_RTS	QSPI0_A_CS1	LCD40	FB_CLKOUT	VIU_HSYNC	SCI2_TX	
D13	166	PTB7		PTB7	FTM0_CH7	SCI1_CTS	QSPI0_B_CS1	LCD41		VIU_VSYNC	SCI2_RX	
J16	121	PTB8		PTB8	FTM1CH0		FTM1_QD_PHA		VIU_DE		DCU1_R6	
J19	123	PTB9		PTB9	FTM1CH1		FTM1_QD_PHB				DCU1_R7	
B15	159	PTB10		PTB10	SCI0_TX			DCU0_TCON4	VIU_DE	CKO1	ENET_TS_CLKIN	
D14	164	PTB11		PTB11	SCI0_RX			DCU0_TCON5	SNVS_ALARM_OUT_B	CKO2	ENET0_1588_TMR0	
E13	165	PTB12		PTB12	SCI0_RTS		SPI0_PCS5	DCU0_TCON6	FB_AD1		ENET0_1588_TMR1	
D15	156	PTB13		PTB13	SCI0_CTS		SPI0_PCS4	DCU0_TCON7	FB_AD0	TRACECTL		
B14	162	PTB14		PTB14	CAN0_RX	I2C0_SCL		DCU0_TCON8			DCU1_PCLK	
A14	161	PTB15		PTB15	CAN0_TX	I2C0_SDA		DCU0_TCON9			VIU_PIX_CLK	
C14	163	PTB16		PTB16	CAN1_RX	I2C1_SCL		DCU0_TCON10				
A15	160	PTB17		PTB17	CAN1_TX	I2C1_SDA		DCU0_TCON11				
B12	171	PTB18		PTB18	SPI0_PCS1	EXT_AUDIO_MCLK		CKO1		VIU_DATA9	CCM_OBS0	
C13	167	PTB19		PTB19	SPI0_PCS0					VIU_DATA10	CCM_OBS1	
A13	169	PTB20		PTB20	SPI0_SIN			LCD42		VIU_DATA11	CCM_OBS2	
E12	173	PTB21		PTB21	SPI0_SOUT			LCD43		VIU_DATA12	DCU1_PCLK	
D12	172	PTB22		PTB22	SPI0_SCK				VIU_FID			
V10	61	USB0_GND			USB0_GND							
T10	63	USB0_DP			USB0_DP							
T9	62	USB0_DM			USB0_DM							
W11	60	USB0_VBUS			USB0_VBUS							
Y10	59	USB_DCAP			USB_DCAP							

Table 75. RGPIO versus Pins (continued)

RGPIO	In GPIO module	Corresponding Pin on the chip	IOMUX register name	IOMUX register address
RGPIO[1]	PORT0[1]	PTA8	IOMUXC_PTA8	40048004
RGPIO[2]	PORT0[2]	PTA9	IOMUXC_PTA9	40048008
RGPIO[3]	PORT0[3]	PTA10	IOMUXC_PTA10	4004800C
RGPIO[4]	PORT0[4]	PTA11	IOMUXC_PTA11	40048010
RGPIO[5]	PORT0[5]	PTA12	IOMUXC_PTA12	40048014
RGPIO[6]	PORT0[6]	PTA16	IOMUXC_PTA16	40048018
RGPIO[7]	PORT0[7]	PTA17	IOMUXC_PTA17	4004801C
RGPIO[8]	PORT0[8]	PTA18	IOMUXC_PTA18	40048020
RGPIO[9]	PORT0[9]	PTA19	IOMUXC_PTA19	40048024
RGPIO[10]	PORT0[10]	PTA20	IOMUXC_PTA20	40048028
RGPIO[11]	PORT0[11]	PTA21	IOMUXC_PTA21	4004802C
RGPIO[12]	PORT0[12]	PTA22	IOMUXC_PTA22	40048030
RGPIO[13]	PORT0[13]	PTA23	IOMUXC_PTA23	40048034
RGPIO[14]	PORT0[14]	PTA24	IOMUXC_PTA24	40048038
RGPIO[15]	PORT0[15]	PTA25	IOMUXC_PTA25	4004803C
RGPIO[16]	PORT0[16]	PTA26	IOMUXC_PTA26	40048040
RGPIO[17]	PORT0[17]	PTA27	IOMUXC_PTA27	40048044
RGPIO[18]	PORT0[18]	PTA28	IOMUXC_PTA28	40048048
RGPIO[19]	PORT0[19]	PTA29	IOMUXC_PTA29	4004804C
RGPIO[20]	PORT0[20]	PTA30	IOMUXC_PTA30	40048050
RGPIO[21]	PORT0[21]	PTA31	IOMUXC_PTA31	40048054
RGPIO[22]	PORT0[22]	PTB0	IOMUXC_PTB0	40048058
RGPIO[23]	PORT0[23]	PTB1	IOMUXC_PTB1	4004805C
RGPIO[24]	PORT0[24]	PTB2	IOMUXC_PTB2	40048060
RGPIO[25]	PORT0[25]	PTB3	IOMUXC_PTB3	40048064
RGPIO[26]	PORT0[26]	PTB4	IOMUXC_PTB4	40048068
RGPIO[27]	PORT0[27]	PTB5	IOMUXC_PTB5	4004806C
RGPIO[28]	PORT0[28]	PTB6	IOMUXC_PTB6	40048070
RGPIO[29]	PORT0[29]	PTB7	IOMUXC_PTB7	40048074
RGPIO[30]	PORT0[30]	PTB8	IOMUXC_PTB8	40048078
RGPIO[31]	PORT0[31]	PTB9	IOMUXC_PTB9	4004807C
RGPIO[32]	PORT1[0]	PTB10	IOMUXC_PTB10	40048080
RGPIO[33]	PORT1[1]	PTB11	IOMUXC_PTB11	40048084
RGPIO[34]	PORT1[2]	PTB12	IOMUXC_PTB12	40048088
RGPIO[35]	PORT1[3]	PTB13	IOMUXC_PTB13	4004808C
RGPIO[36]	PORT1[4]	PTB14	IOMUXC_PTB14	40048090
RGPIO[37]	PORT1[5]	PTB15	IOMUXC_PTB15	40048094
RGPIO[38]	PORT1[6]	PTB16	IOMUXC_PTB16	40048098
RGPIO[39]	PORT1[7]	PTB17	IOMUXC_PTB17	4004809C

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Table 78. Functional Assignment Pins (continued)

Signal Name	364 MAP BGA	176 LQFP (F-series ONLY)	Power Group	Pad Type	Default Mode (Reset)	Default Function	Input/ Output	Value
DDR_DQS[0]	D3	—	SDRAMC_VDD2P5	DDR	—	DDR_DQS[0]	—	—
DDR_DQS_b[0]	E3	—	SDRAMC_VDD2P5	DDR	—	DDR_DQS_b[0]	—	—
DDR_DQS[1]	E1	—	SDRAMC_VDD2P5	DDR	—	DDR_DQS[1]	—	—
DDR_DQS_b[1]	F1	—	SDRAMC_VDD2P5	DDR	—	DDR_DQS_b[1]	—	—
DDR_ODT[0]	C4	—	SDRAMC_VDD2P5	DDR	—	DDR_ODT[0]	—	—
DDR_ODT[1]	B1	—	SDRAMC_VDD2P5	DDR	—	DDR_ODT[1]	—	—
DDR_RAS_b	A4	—	SDRAMC_VDD2P5	DDR	—	DDR_RAS_b	—	—
DDR_RESET	D6	—	SDRAMC_VDD2P5	DDR	—	DDR_RESET	—	—
DDR_VREF	G5	—	SDRAMC_VDD2P5	DDR	—	DDR_VREF	—	—
DDR_WE_b	C6	—	SDRAMC_VDD2P5	DDR	—	DDR_WE_b	—	—
DDR_ZQ	A3	—	SDRAMC_VDD2P5	DDR	—	DDR_ZQ	—	—
EXT_POR	T1	30	VDD33	GPIO	—	EXT_POR	—	—
EXT_TAMPER0	T14	76	VBAT	Analog	—	EXT_TAMPER0	—	—
EXT_TAMPER1	U14	74	VBAT	Analog	—	EXT_TAMPER1	—	—
EXT_TAMPER2/ EXT_WM0_TAMPER_IN	T13	—	VBAT	Analog	—	EXT_TAMPER2/ EXT_WM0_TAMPER_IN	—	—
EXT_TAMPER3/ EXT_WM0_TAMPER_OUT	U13	—	VBAT	Analog	—	EXT_TAMPER3/ EXT_WM0_TAMPER_OUT	—	—
EXT_TAMPER4/ EXT_WM1_TAMPER_IN	U12	—	VBAT	Analog	—	EXT_TAMPER4/ EXT_WM1_TAMPER_IN	—	—

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Table 78. Functional Assignment Pins (continued)

Signal Name	364 MAP BGA	176 LQFP (F-series ONLY)	Power Group	Pad Type	Default Mode (Reset)	Default Function	Input/ Output	Value
EXT_TAMPER5/ EXT_WM1_TAMPER_OUT	U10	—	VBAT	Analog	—	EXT_TAMPER5/ EXT_WM1_TAMPER_OUT	—	—
EXTAL	Y13	73	DECAP_V11_LDO_OUT	Analog	—	EXTAL	—	—
EXTAL32	Y12	70	DECAP_V11_LDO_OUT	Analog	—	EXTAL32	—	—
JTCLK/ SWCLK	K4	3	VDD33	GPIO	ALT1	JTAG	Input	100K PU
JTDI	K2	4	VDD33	GPIO	ALT1	JTAG	Input	100K PU
JTDO	K1	5	VDD33	GPIO	ALT1	JTAG	Disabled	—
JTMS/ SWDIO	L1	6	VDD33	GPIO	ALT1	JTAG	Input	100K PU
LVDS0P	W14	—	DECAP_V25_LDO_OUT	Analog	—	LVDS0P	—	—
LVDS0N	Y14	—	DECAP_V25_LDO_OUT	Analog	—	LVDS0N	—	—
PTA6	N5	19	VDD33	GPIO	ALT0	GPIO	Disabled	
PTA7	V15	79	VDD33	GPIO	ALT0	GPIO	Disabled	
PTA12	L3	7	VDD33	GPIO	ALT0	GPIO	Disabled	
PTA16	Y5	43	VDD33	GPIO	ALT0	GPIO	Disabled	
PTA17	Y6	44	VDD33	GPIO	ALT0	GPIO	Disabled	
PTA18	V6	46	VDD33	GPIO	ALT0	GPIO	Disabled	
PTA19	U6	47	VDD33	GPIO	ALT0	GPIO	Disabled	
PTA20	B18	143	VDD33	GPIO	ALT0	GPIO	Disabled	
PTA21	D18	145	VDD33	GPIO	ALT0	GPIO	Disabled	
PTA22	E17	147	VDD33	GPIO	ALT0	GPIO	Disabled	
PTA23	C17	148	VDD33	GPIO	ALT0	GPIO	Disabled	
PTA24	R16	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTA25	R17	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTA26	R19	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTA27	R20	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTA28	P20	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTA29	P18	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTA30	P17	—	VDD33	GPIO	ALT0	GPIO	Disabled	

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Table 78. Functional Assignment Pins (continued)

Signal Name	364 MAP BGA	176 LQFP (F-series ONLY)	Power Group	Pad Type	Default Mode (Reset)	Default Function	Input/ Output	Value
PTD22	F20	126	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD23	G20	124	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD24	G19	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD25	G18	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD26	G16	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD27	H16	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD28	H17	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD29	H18	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD30	H20	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD31	J20	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTE0	N16	103	VDD33	GPIO	ALT2	BMODE1	Input	Disabled
PTE1	N18	104	VDD33	GPIO	ALT2	BMODE0	Input	Disabled
PTE2	N19	105	VDD33	GPIO	ALT0	GPIO	Disabled	
PTE3	Y15	80	VDD33	GPIO	ALT0	GPIO	Disabled	
PTE4	N20	106	VDD33	GPIO	ALT0	GPIO	Disabled	
PTE5	T16	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTE6	W16	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTE7	M20	109	VDD33	GPIO	ALT3	RCON0	Input	Disabled
PTE8	M19	110	VDD33	GPIO	ALT3	RCON1	Input	Disabled
PTE9	M17	111	VDD33	GPIO	ALT3	RCON2	Input	Disabled
PTE10	M16	112	VDD33	GPIO	ALT3	RCON3	Input	Disabled
PTE11	L16	113	VDD33	GPIO	ALT3	RCON4	Input	Disabled
PTE12	L17	114	VDD33	GPIO	ALT3	RCON5	Input	Disabled
PTE13	Y16	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTE14	W15	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTE15	L18	115	VDD33	GPIO	ALT3	RCON6	Input	Disabled
PTE16	L20	116	VDD33	GPIO	ALT3	RCON7	Input	Disabled
PTE17	K20	117	VDD33	GPIO	ALT3	RCON8	Input	Disabled
PTE18	K19	118	VDD33	GPIO	ALT3	RCON9	Input	Disabled
PTE19	K18	119	VDD33	GPIO	ALT3	RCON10	Input	Disabled
PTE20	A12	170	VDD33	GPIO	ALT3	RCON11	Input	Disabled
PTE21	V16	81	VDD33	GPIO	ALT0	GPIO	Disabled	
PTE22	W17	84	VDD33	GPIO	ALT0	GPIO	Disabled	
PTE23	J17	122	VDD33	GPIO	ALT3	RCON12	Input	Disabled
PTE24	D19	134	VDD33	GPIO	ALT3	RCON13	Input	Disabled
PTE25	C19	135	VDD33	GPIO	ALT3	RCON14	Input	Disabled
PTE26	C20	137	VDD33	GPIO	ALT3	RCON15	Input	Disabled

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