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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A5
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	Multimedia; NEON™ MPE
RAM Controllers	LPDDR2, DDR3, DRAM
Graphics Acceleration	Yes
Display & Interface Controllers	DCU, GPU, LCD, VideoADC, VIU
Ethernet	10/100Mbps (2)
SATA	-
USB	USB 2.0 OTG + PHY (1)
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	-
Package / Case	364-LFBGA
Supplier Device Package	364-LFBGA (17x17)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mvf50nn151cmk40

5 Operating Requirements

5.1 Thermal operating requirements

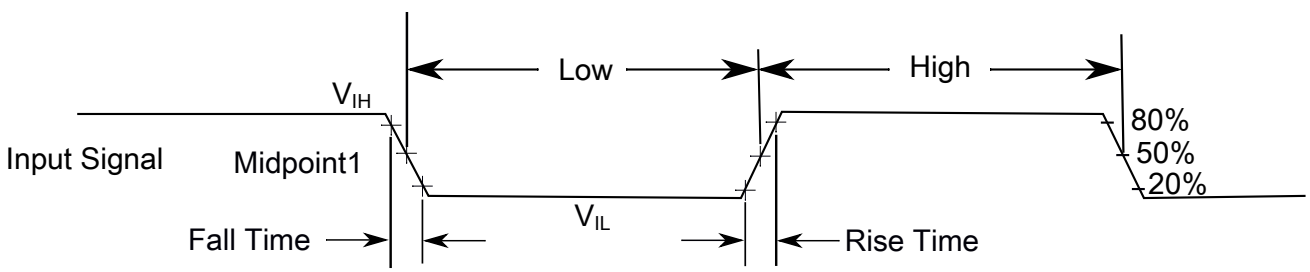
Table 1. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit
T_A	Ambient temperature	–40	85	°C
T_J	Junction temperature		105	°C

6 General

6.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.



The midpoint is $V_{IL} + (V_{IH} - V_{IL}) / 2$

Figure 2. Input signal measurement reference

6.2.1.5 External NPN Ballast

The internal main regulator requires an external NPN ballast transistor to be connected as shown in the following figure as well as an external capacitance to be connected to the device in order to provide a stable 1.2V digital supply to the device. The HPREG design allows for collector voltage lower than VDDREG value. See AN4807 at www.freescale.com .

NOTE

To not overload BCTRL output, collector voltage should appear no later than VDDREG / VDD33 (3.3V).

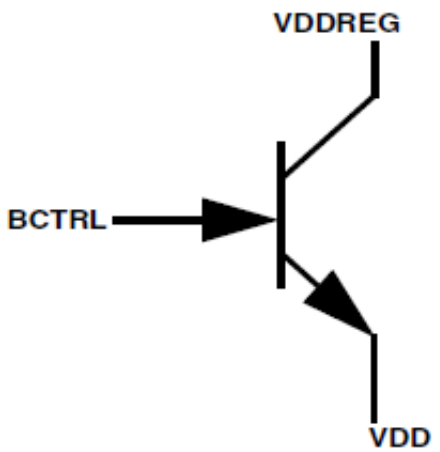


Figure 3. External NPN Ballast connections

Table 6. BCTRL OUTPUT specification

Parameter	Value	Comments
BCTRL OUTPUT specification	20mA	BCTRL driver can not drive more than 20mA current
Maximum pin voltage	VDDREG-0.5V	For Example, VDDREG =3.0V BCTRL should not exceed 2.5V.

Table 7. Assumptions For calculations

Parameter	Value
VDDREG	3.0V to 3.6V with typical value of 3.3V
Max DC Collector current	0.85A @85 °C
Emitter voltage	1.2V to 1.25V
Collector voltage	Equal to VDDREG

6.2.2 LVD electrical specifications

6.2.2.1 Main Supply electrical characteristics

Table 9. LVD_MAIN supply electrical characteristics

Main Supply LVD Parameters	Min	Typ	Max	Unit	Comments
Power supply	3.0	3.3	3.6	V	
Upper voltage threshold (value @27°C)		2.76	2.915	V	
Lower voltage threshold (value @27°C)	2.656	2.73		V	
Time constant of RC filter at LVD input (0.69*RC)	3.3			µs	3.3 V noise rejection at LVD comparator input

6.2.2.2 LVD DIG characteristics

Table 10. LVD DIG electrical specifications [HPREG(RUN MODE) and LPREG(STOP MODE)]

LVD DIG Parameters	Min	Typ	Max	Unit	Comments
Power supply	3.0	3.3	3.6	V	
Upper voltage threshold	1.135	1.16	1.185	V	
Lower voltage threshold	1.105	1.13	1.155	V	
Time constant of RC filter at LVD input	200			ns	1.2V noise rejection at the input of LVD comparator

Table 11. LVD DIG electrical specifications [ULPREG(STANDBY MODE)]

LVD DIG Parameters	Min	Typ	Max	Unit	Comments
Power supply	3.0	3.3	3.6	V	
Upper voltage threshold	1.105	1.13	1.155	V	
Lower voltage threshold	1.075	1.10	1.125	V	
Time constant of RC filter at LVD input	200			ns	1.2V noise rejection at the input of LVD comparator

2. The Max numbers represent the single worst case value taken from a matrix lot of parts across normal process variation at maximum temperature.
3. CA5, CM4 cores halted
4. 24MHz operation, PLL Bypass
5. 32 kHz /128 kHz operation, PLL Off
6. Lowest power mode with all power retained, RAM retention and LVD protection.
7. Standby Mode. 64K RAM retention. I/O states held. ADCs/DACs optionally power-gated. RTC functional. Wakeup from interrupts. Fast IRC enabled.
8. Standby Mode 16K RAM retention. I/O states held. ADCs/DACs optionally power-gated. RTC functional. Wakeup from interrupts. Fast IRC enabled.
9. All supplies OFF, SRTC, 32kXOSC ON, tampers and monitors ON. 128k IRC optionally ON.

6.2.5 USB PHY current consumption

6.2.5.1 Power Down Mode

Everything powered down, including the VBUS valid detectors, typ condition.

Table 16. USB PHY Current Consumption in Normal Mode

	USBx_VBUS (3.0V) Avg	VDD33_LDOIN (2.5V) Avg	VDD33_LDOIN (1.1V) Avg
Current	5.1 µA	1.7 µA	<0.5 µA

NOTE

The currents on the 2.5 voltage regulator and 3.0 voltage regulator were identified to be the voltage divider circuits in the USB-specific level shifters.

6.2.6 EMC radiated emissions operating behaviors

Table 17. EMC radiated emissions operating behaviors

Symbol	Condition[1]	Clocks	Frequency band [2]	Level (Typ)[3]	Unit
V_{EME}	Device Configuration, test conditions and EM testing per standard IEC 61967-2; Supply voltages: VDD= 5.0 V VDD33 = 3.3 V VDD15 = 1.5 V VDD12 = 1.2 V Temp = 25°C	FCPU = 396 MHz FBUS = 66 MHz External Crystal = 24 MHz	150 KHz – 50 MHz	22	dBµV
			50 MHz – 150 MHz	24	
			150 MHz – 500 MHz	25	
			500–1000	20	
			IEC level[4]	K	—

1. Measurements were made per IEC 61967-2 while the device was running basic application code.
2. Measurements were performed on the BGA364 version of the device

Table 31. 12-bit ADC Operating Conditions (continued)

Characteristic	Conditions	Symb	Min	Typ [1]	Max	Unit	Comment
Analog Source Resistance	12 bit mode f_{ADCK} = 40MHz ADLSMP=0, ADSTS=10, ADHSC=1	R_{AS}	-	-	1	kohms	T_{samp}=150 ns
R_{AS} depends on Sample Time Setting (ADLSMP, ADSTS) and ADC Power Mode (ADHSC, ADLPC). See charts for Minimum Sample Time vs R_{AS}							
ADC Conversion Clock Frequency	ADLPC=0, ADHSC=1 12 bit mode	f_{ADCK}	4	-	40	MHz	-
	ADLPC=0, ADHSC=0 12 bit mode		4	-	30	MHz	-
	ADLPC=1, ADHSC=0 12 bit mode		4	-	20	MHz	-

1. Typical values assume VDDAD = 3.3 V, Temp = 25°C, f_{ADCK}=20 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
2. DC potential difference

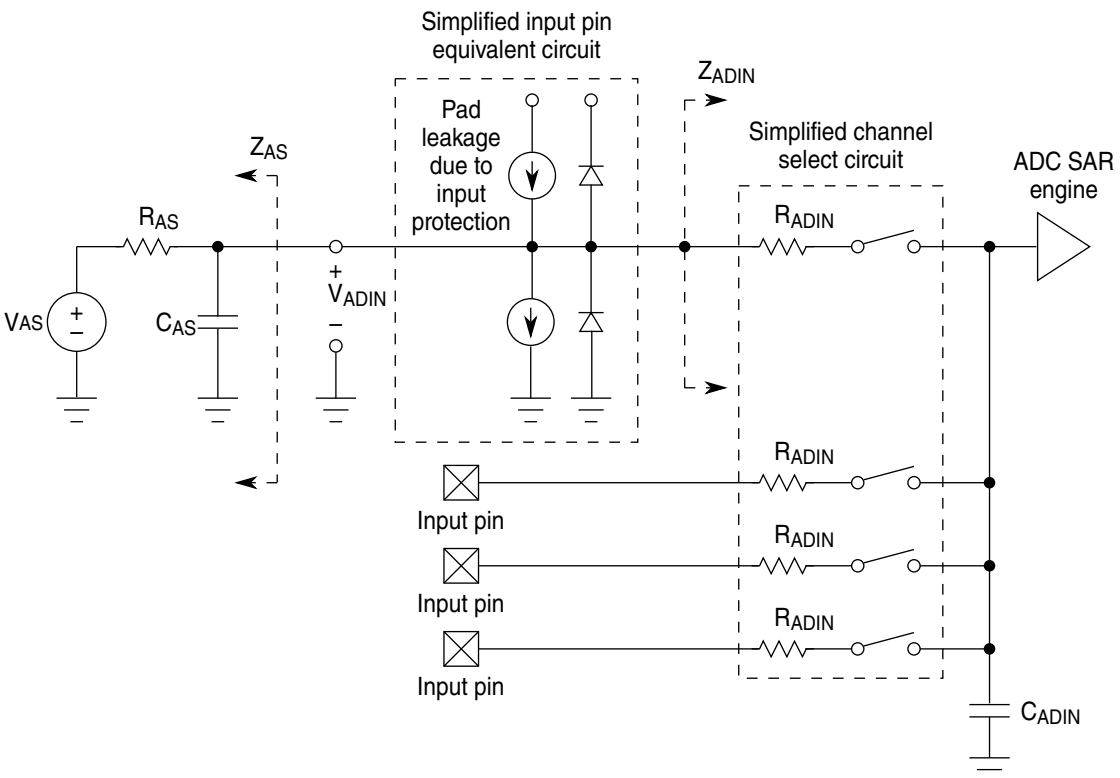


Figure 5. 12-bit ADC Input Impedance Equivalency Diagram

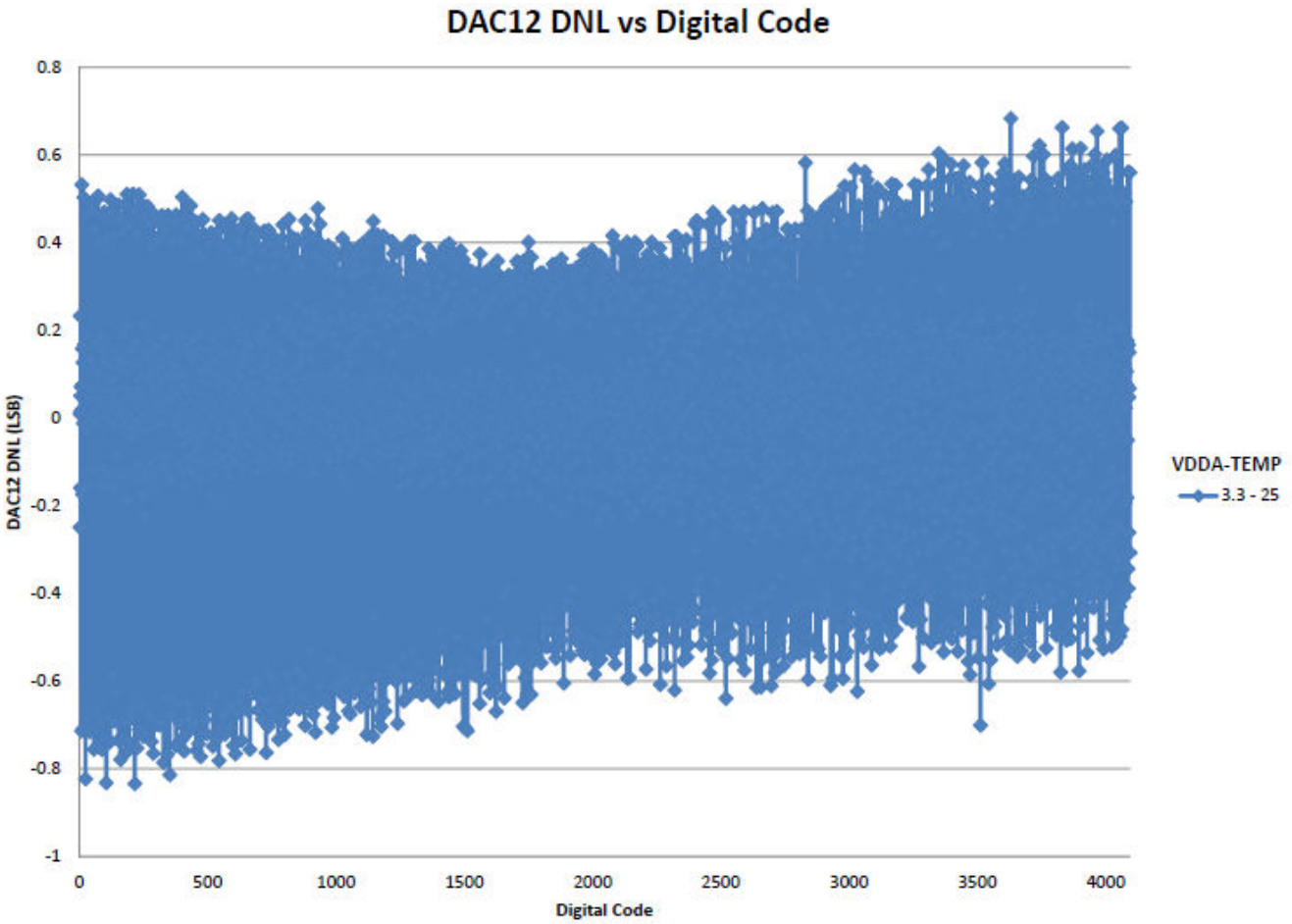


Figure 10. DNL error vs. digital code

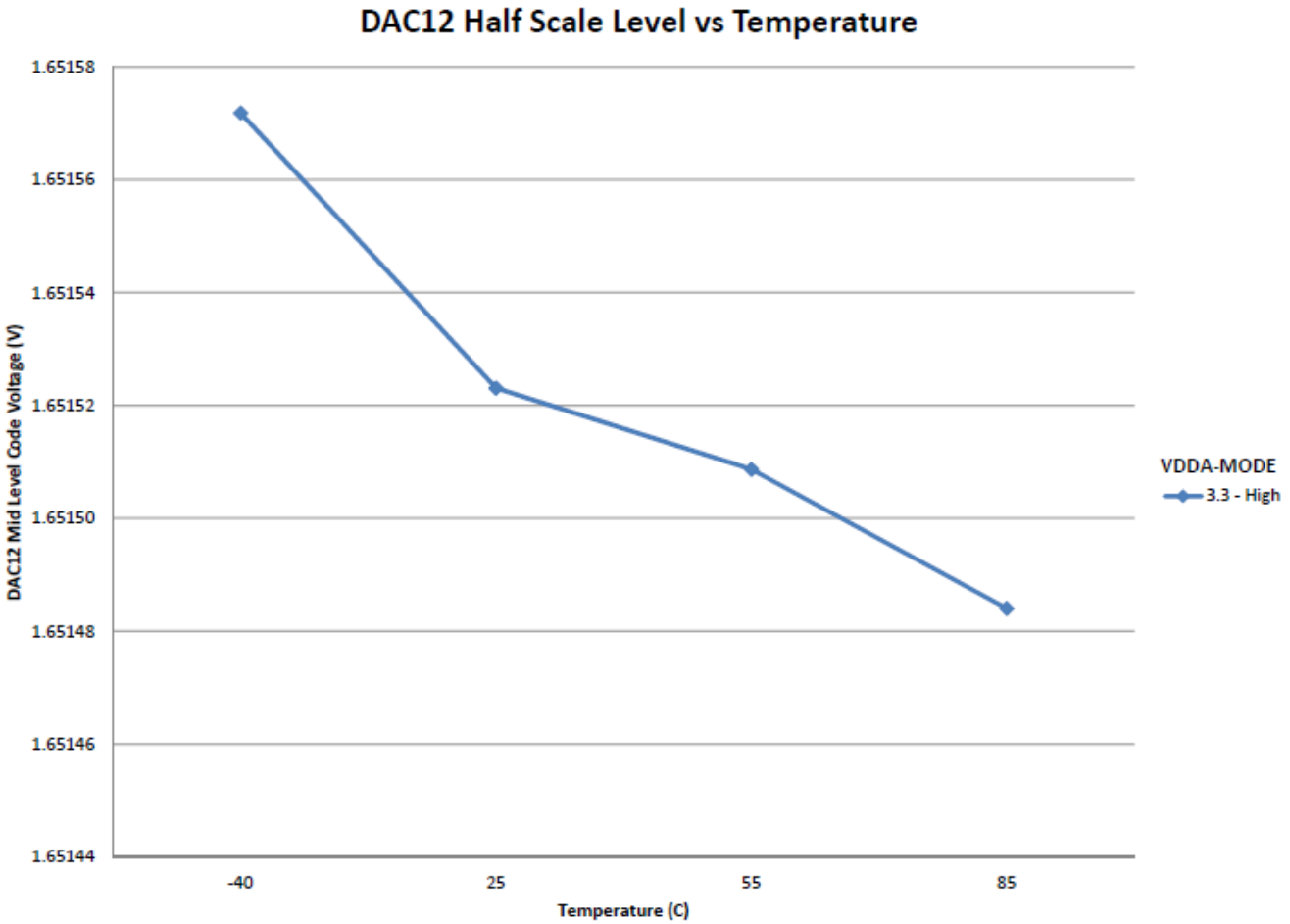


Figure 11. Offset at half scale vs. temperature

9.1.3 VideoADC Specifications

This section describes the electrical specification and characteristics of the VideoADC Analog Front End.

Table 35. VideoADC Specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
VDDA33_AFE	Supply voltage	3.0	3.3	3.6	V	—
	Supply current	—	—	41	mA	—
VDDA12_AFE	Supply voltage	1.1	1.2	1.26	V	—
	Supply current	—	—	14	mA	—
V_{in}	Input signal voltage range	0	0.5	1.4	V	—
	External AC coupling	10	47		nF	The external AC coupling capacitance cannot be too large.

Table continues on the next page...

Table 35. VideoADC Specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{BG}	Bandgap voltage	—	0.6	—	V	Bandgap voltage on VADC_AFE_BANDGAP pin. Pin should be decoupled with a 100nF capacitor

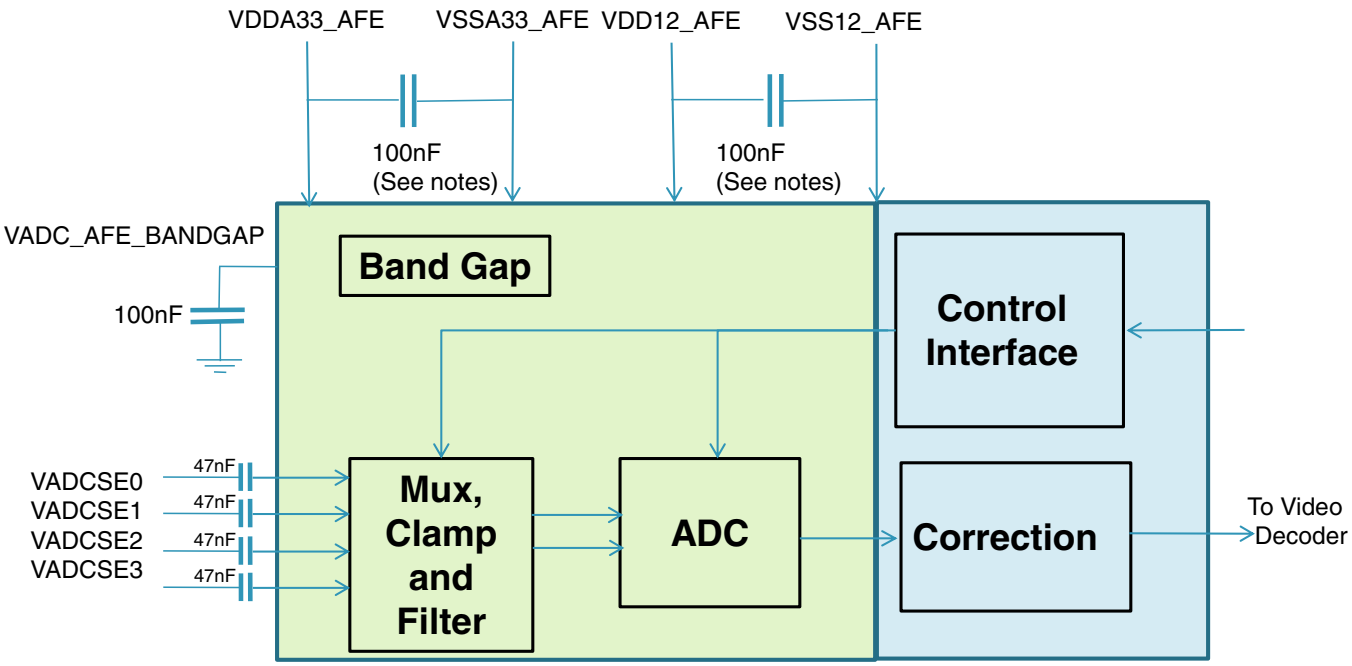


Figure 12. VideoADC supply scheme

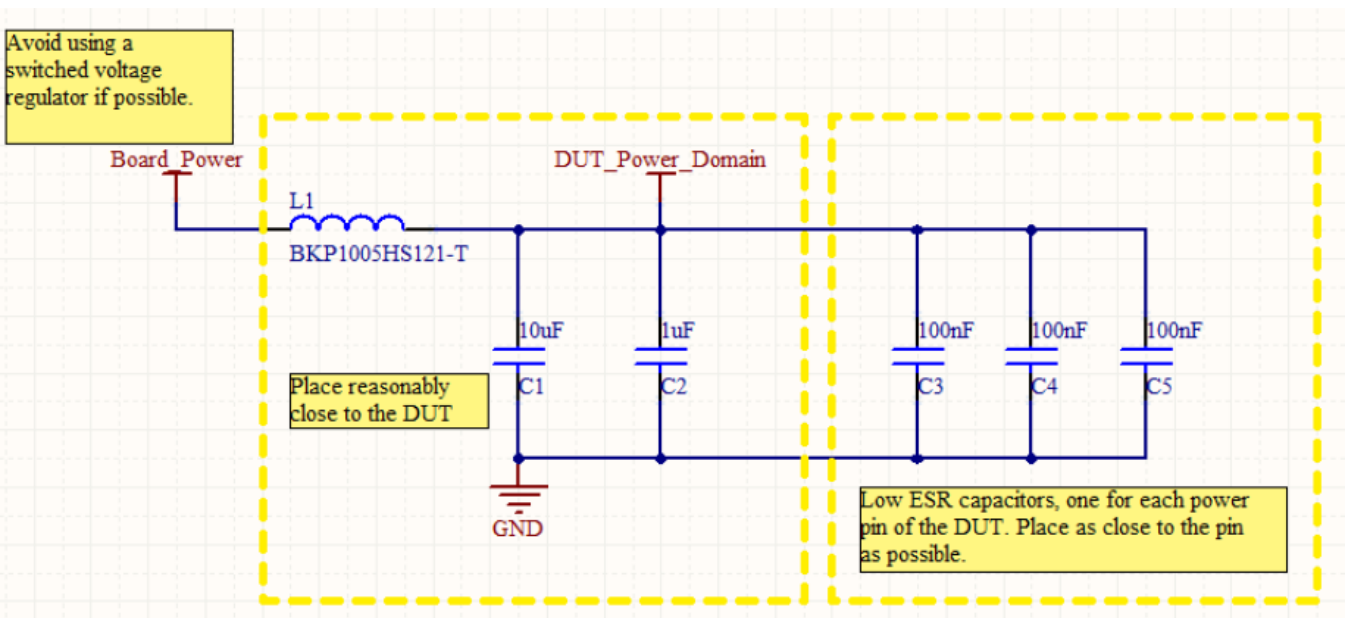


Figure 13. VideoADC supply decoupling

NOTE

VideoADC 3.3V and 1.2V power supply pins should be decoupled to their respective grounds using low-ESR 100nF capacitors

NOTE

If possible, avoid using switched voltage regulators for the AFE power domains. Use linear voltage regulators instead.

NOTE

The 3.3V and 1.2V power domains should be separated from other circuitry on the board by inductors/beads to filter out high frequency noise.

9.2 Display and Video interfaces

9.2.1 DCU Switching Specifications

9.2.1.1 Interface to TFT panels (DCU0/1)

This section provides the LCD interface timing for a generic active matrix color TFT panel. In the figure below, signals are shown with positive polarity. The sequence of events for active matrix interface timing:

- PCLK latches data into the panel on its positive edge (when positive polarity is selected). In active mode, PCLK runs continuously. This signal frequency could be from 5 to 66 MHz depending on the panel type.
- HSYNC causes the panel to start a new line. It always encompasses at least one PCLK pulse.
- VSYNC causes the panel to start a new frame. It always encompasses at least one HSYNC pulse.
- DE acts like an output enable signal to the LCD panel. This output enables the data to be shifted onto the display. When disabled, the data is invalid and the trace is off.

Figure 14. TFT LCD interface timing overview[1]

1. In the figure, LD[23:0]" signal is "line data," an aggregation of the DCU's RGB signals—R[0:7], G[0:7] and B[0:7].

9.2.3 LCD driver electrical characteristics

This section provides LCD driver electrical specification at V_{DD33} = 3.3 V ± 10%.

Table 39. LCD driver specifications

Symbol	Parameter	Min	Typical	Max	Unit
VLCD	Voltage on VLCD (LCD supply) pin with respect to VSS	0		VDD33 + 0.3	V
$Z_{BP/FP}$	LCD output impedance (BP[n-1:0],FP[m-1:0]) for output levels VDDE, VSS	_	_	5.0	KΩ
$I_{BP/FP}$	LCD output current (BP[n-1:0],FP[m-1:0]) for outputs charge/discharge voltage levels VDDE2/3, VDDE1/2, VDDE/3)[1]	_	25	_	µA

1. With PWR=10, BSTEN=0, and BSTAO=0

9.3 Ethernet specifications

9.3.1 Ethernet Switching Specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface. All Ethernet signals use pad type pad_fsr. The timing specifications described i the section assume a pad slew rate setting of 11 and a load of 50 pF[2].

9.3.2 Receive and Transmit signal timing specifications

This section provides timing specs that meet the requirements for RMII interfaces for a range of transceiver devices.

Table 40. Receive signal timing for RMII interfaces

	Characteristic	RMII Mode		Unit
		Min	Max	
—	EXTAL frequency (RMII input clock RMII_CLK)	—	50	MHz
E3, E7	RMII_CLK pulse width high	35%	65%	RMII_CLK period

Table continues on the next page...

2. These timing parameters are specified assuming maximum operating frequency and the fastest pad slew rate setting (11). When operating this interface at lower frequencies, increase the slew rate by using the 10, 01, or 00 setting to increase edge rise and fall times, thus reducing EMI.

9.4 Audio interfaces

9.4.1 Enhanced Serial Audio Interface (ESAI) Timing Parameters

The ESAI consists of independent transmitter and receiver sections, each section with its own clock generator. The following table shows the interface timing values.

Table 44. Enhanced Serial Audio Interface (ESAI) Timing

No	Characteristics	Symbol	Min	Max	Condition[1]	Unit
1	Clock cycle[2]	t_{SSICC}	30.0 (4 × T_c)	— —	master	ns
2	Clock high period: • master • slave	— —	6 (2 × T_c – 9.0) 15 (2 × T_c)	— —	— —	ns
3	Clock low period: • master • slave	— —	6 (2 × T_c – 9.0) 15 (2 × T_c)	— —	— —	ns
4	FSR Input and Data Input setup time before SCKR (SCK in synchronous mode) falling edge	— —	6 15	— —	Slave Master	ns
5	FSR Input and Data Input hold time after SCKR falling edge	— —	2 0	— —	Slave Master	ns
6	SCKT rising edge to FST out and Data out valid	— —	— —	15 6	Slave Master	ns
7	SCKT rising edge to FST out and Data out hold	— —	— —	0 0	Slave Master	ns
8	FST input setup time before SCKT falling edge	— —	6 15	— —	Slave Master	ns
9	FST input hold time after SCKT falling edge	— —	2 0	— —	Slave Master	ns
10	HCKR/HCKT clock cycle	—	15 (2 x T_C)	—	—	ns
11	HCKT input rising edge to SCKT output	—	—	18.0	—	ns
12	HCKR input rising edge to SCKR output	—	—	18.0	—	ns

1. SCKT(SCKT pin) = transmit clock SCKR(SCKR pin) = receive clock FST(FST pin) = transmit frame sync FSR(FSR pin) = receive frame sync HCKT(HCKT pin) = transmit high frequency clock HCKR(HCKR pin) = receive high frequency clock
2. For the internal clock, the external clock cycle is defined by Icyc and the ESAI control register.

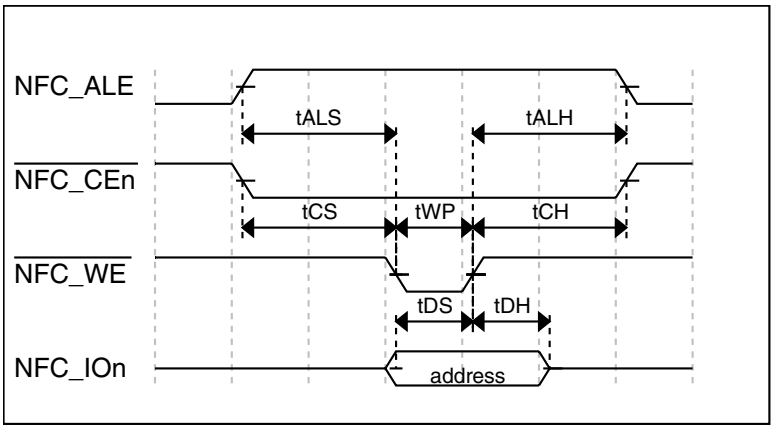


Figure 35. Address latch cycle timing

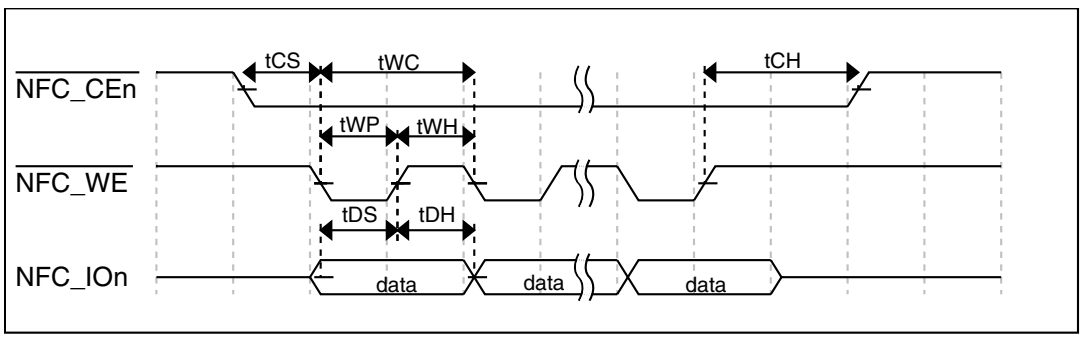


Figure 36. Write data latch cycle timing

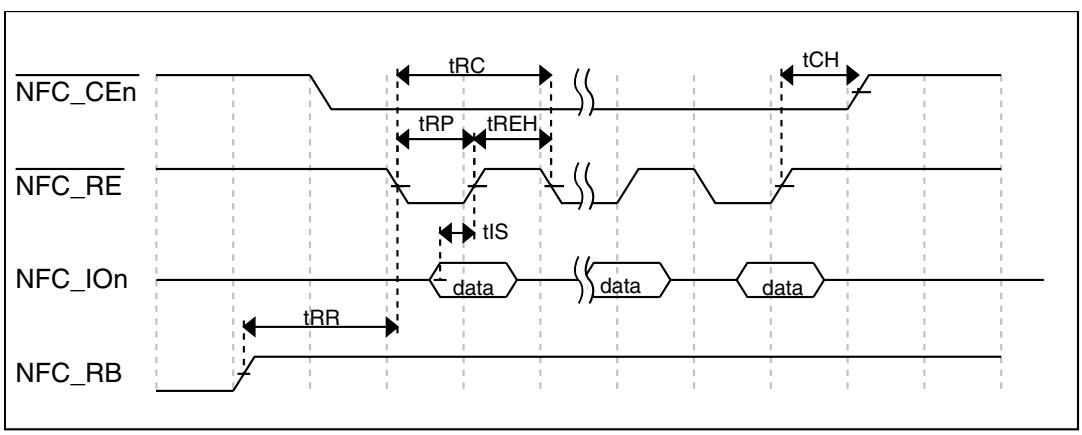


Figure 37. Read data latch cycle timing in non-fast mode

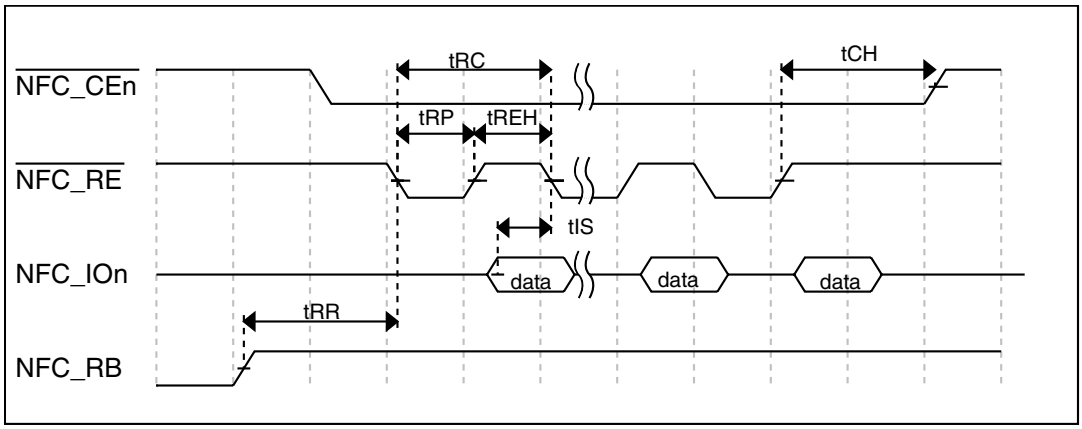


Figure 38. Read data latch cycle timing in fast mode

9.5.3 FlexBus timing specifications

This section provides FlexBus timing parameters. All processor bus timings are synchronous; input setup/hold and output delay are given in respect to the rising edge of a reference clock, FB_CLK. The FB_CLK frequency may be the same as the internal system bus frequency.

The following timing numbers indicate when data is latched or driven onto the external bus, relative to the FlexBus output clock (FB_CLK). All other timing relationships can be derived from these values.

All FlexBus signals use pad type pad_fsr. The following timing specifications assume a pad slew rate setting of 11 and a load of 50 pF[3]

Table 53. FlexBus timing specifications

Num	Characteristic	Min	Max	Unit
	Frequency of operation	—	83[1] (with Wait state)	MHz
			57[2] without Wait state , -1	
FB1	Clock Period	12	—	ns
FB4	Input setup	10.6	—	ns
FB5	Input hold	0	—	ns
FB2	Output valid	—	6.4	ns
FB3	Output hold	0	—	ns

1. Freq = 1000/(11+ access time of external memory+ trace delay for clk and data)
2. Freq = 1000/(17+access time of external memory)

3. These timing parameters are specified assuming maximum operating frequency and the fastest pad slew rate setting (11).

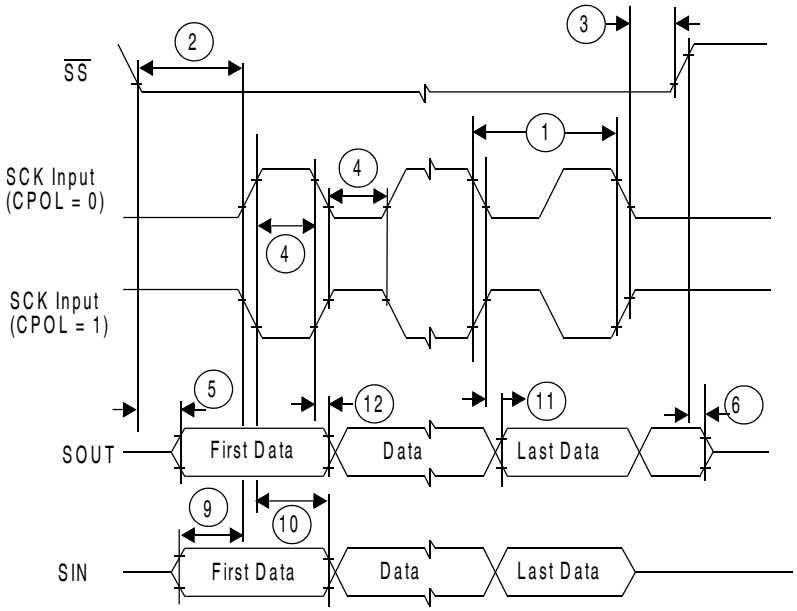


Figure 49. DSPI classic SPI timing slave, CPHA=0

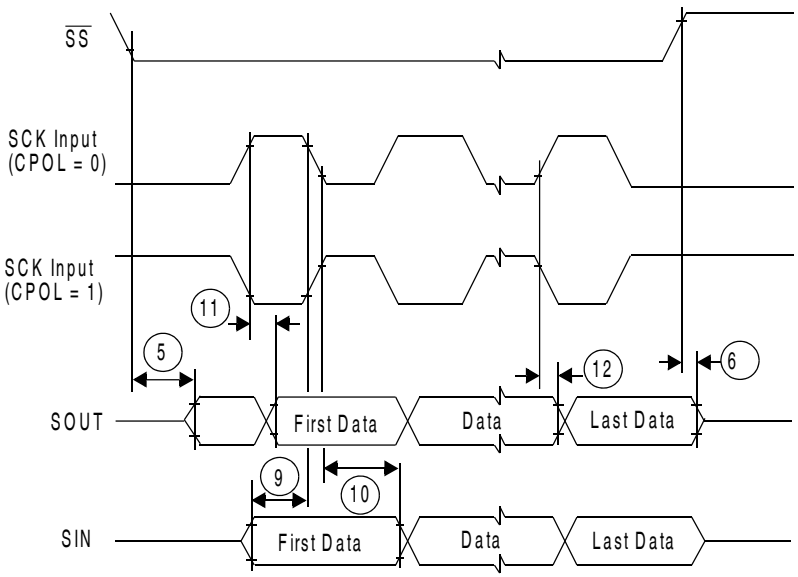


Figure 50. DSPI classic SPI timing slave, CPHA=1

9.6.2 I2C timing

Table 61. I2C input timing specifications — SCL and SDA[1]

No.	Parameter	Min.	Max.	Unit
1	Start condition hold time	2	—	PER_CLK Cycle[2]
2	Clock low time	8	—	PER_CLK Cycle

Table continues on the next page...

9.7.6 PLL3 and PLL7 (480 MHz USB PLL) Electrical Parameters

Table 69. PLL3 and PLL7 Electrical Parameters

Parameter	Value
Clock output range	480 MHz PLL output
Reference clock	24 MHz
Lock time	<425 reference cycles
Period jitter(p2p)	<140 ps
Duty Cycle	48.9%~51.7% PLL output

9.7.7 PLL5 (Ethernet PLL) Electrical Parameters

Table 70. PLL5 Electrical Parameters

Parameter	Value
Clock output range	500 MHz
Reference clock	24 MHz
Lock time	<7500 reference cycles
Cycle to cycle jitter (p2p)[1]	<400ps @ 50 MHz
Duty Cycle	45%~55%

1. Jitter numbers are measured at divided PLL clock because high frequency cannot be brought-out IO pad.

9.7.8 PLL4 (Audio PLL) Electrical Parameters

Table 71. PLL4 Electrical Parameters

Parameter	Value
Clock output range	650 MHz ~1.3 GHz
Reference clock	24 MHz
Lock time	<7500 reference cycles
Long term jitter(RMS)	<42ps @1128MHz
Period jitter(p2p)[1]	<115ps@1128MHz
Duty Cycle	43%~57%

1. Jitter numbers are measured at divided PLL clock because high frequency cannot be brought-out on IO pad.

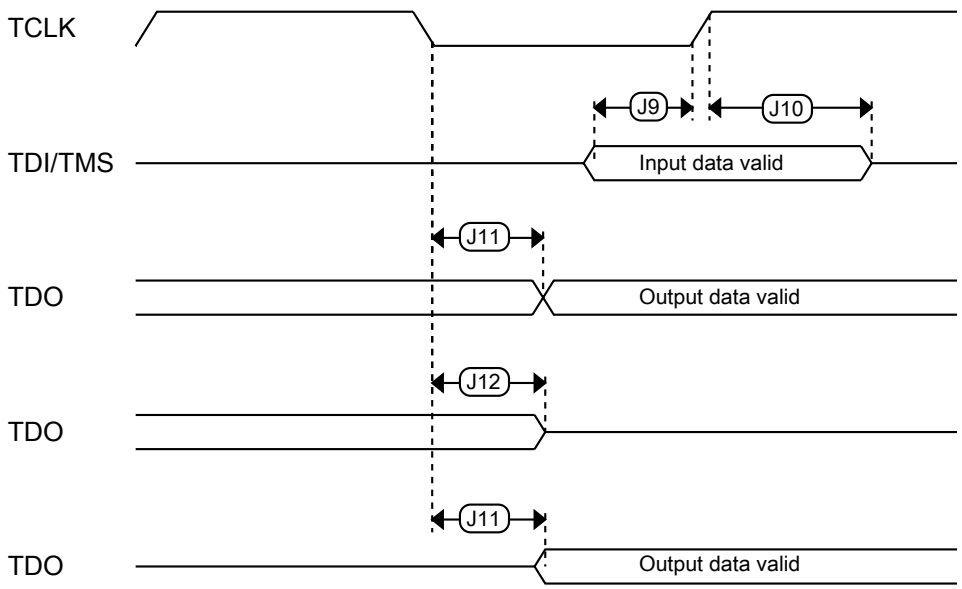


Figure 55. Test Access Port timing

9.8.2 Debug trace timing specifications

Table 74. Debug trace operating behaviors

Symbol	Description	Min.	Max.	Unit
T_{cyc}	Clock period	50		MHz
T_{wl}	Low pulse width	2	—	ns
T_{wh}	High pulse width	2	—	ns
T_r	Clock and data rise time	Refer Table 21		ns
T_f	Clock and data fall time Refer			ns
tDV	Data output valid	3	—	ns
tHO	Data output hold	1	—	ns

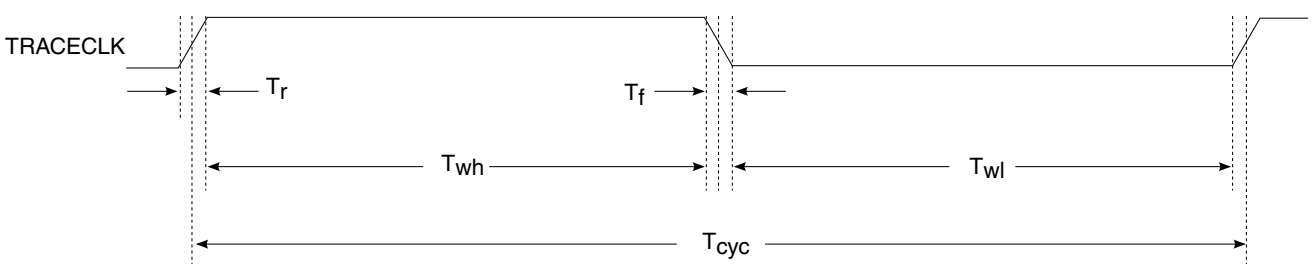


Figure 56. TRACE_CLKOUT specifications

13 Power Supply Pins

13.1 Power Supply Pins

Table 77. Power Supply Pins

Supply Rail Name	364 MAP BGA	176 LQFP (F-series ONLY)	Comment
DECAP_V11_ LDO_OUT	V12	69	On-chip 1.1V LDO output
DECAP_V25_ LDO_OUT	T11	65	On-chip 2.5V LDO output (Intended to supply DRAM IO when required)
FA_VDD	N7	—	Factory Use Only (Connect to VDD, internally bonded in LQFP)
SDRAMC_ VDD1P5	D5, D11, E4, E7, E9, F5, H5, K5	DRAM not supported in LQFP	1.5V DDR3 DRAM Supply (1.2V for LPDDR2)
SDRAMC_ VDD2P5	E6, E10, J5	DRAM not supported in LQFP	2.5V DRAM Supply
USB_DCAP	Y10	59	On-chip 3V LDO output (Intended to be fed by external USB VBUS supply)
USB0_GND	V10	61	
USB1_GND	Y9	USB1 not supported in LQFP	
VADC_AFE_ BANDGAP	U5	Video ADC not supported in LQFP	Video ADC Bandgap Output
VBAT	V14	75	On-chip SNVS regulator battery back-up supply option
VDD	G7, G9, G11, G13, H8, H10, H12, H14, J7, J13, K8, K14, L7, L13, M8, M14, N9, N11, N13, P8, P10, P12, P14	2, 22, 48, 85, 102, 125, 136, 174	1.2V Core Supply (Internally Regulated)
VDD33	C12, C15, C18, F18, K3, K17, N3, N17, T17, U16, V8, W18	10, 25, 52, 83, 95, 108, 127, 140, 146, 158, 168	3.3V IO Supply
VDDA33_ADC	V1	38	3.3V Analog To Digital convertor supply
VDD12_AFE	T5	Video ADC not supported in LQFP	1.2V Analog Front End supply for Video ADC
VDDA33_AFE	V3	Video ADC not supported in LQFP	3.3V Analog Front End supply for Video ADC
VDD33_ LDOIN	T12	68	On-chip 2.5V LDO, 1.1V LDO and SNVS regulators input supply
VDDREG	P5	31	On-chip HPREG, LPREG, WBREG and ULPREG regulators input supply
VREFH_ADC	W1	41	ATD High Voltage Reference
VREFL_ADC	U3	40	ATD Low Voltage Reference

Table continues on the next page...

Table 79. Revision History (continued)

Rev. No.	Date	Substantial Changes
		Updated Power supply diagram Updated AC electrical specification of following modules: DCU, 12-bit DAC, Ethernet, Enhanced Serial Audio Interface (ESAI), SAI/I2S, Flexbus, MLB, DSPI, 24MHz External Oscillator, JTAG, Debug, ESAI, QSPI Updated Thermal Attributes for 364 MAPBGA Updated Freescale document number for 176-pin LQFP and 364 MAPBGA Updated VREG specifications Added WBREG specifications Updated Recommended operating conditions table Updated DAC INL and DNL charts Updated Pinouts
Rev 4.1	12/2012	Editorial updates: Removed instances of VF7xx and VF4xx.
Rev 5	April 2013	• Removed references to VF1xxR and refernces to F100 and 144 LQFP and 256 MAPBGA • Replaced references to Auto and IMM by R-series and F-series respectively • In the feature list, the ARM Core frequency changed to 500 MHz for F-series • In the feature list, changed the DRAM controller frequency • Updated Part Nummbering format • Clarified the Fields table as per Marketing • Sample numbers updated • From the VREG electrical specifications tables, deleted pre-trimming rows and comments • .In the HPREG electrical characteristics table, add footnote on maximum Output Current Capacity • In the ULPREG electrical characteristics table, clarified max value of Output voltage @ no load and min value of Output voltage @ full load • In the WBREG electrical characteristics table, clarified max value of Output voltage @ no load and min value of Output voltage @ full load

Table continues on the next page...

Table 79. Revision History

Rev. No.	Date	Substantial Changes
		resistance) of 80 Ω or less is recommended to achieve a gain margin of 5." • In "Pinouts" section, for the 176LQFP package, added information about exposed pad on the bottom side. • In "Special Signal Considerations" table, added that a "fundamental-mode" crystal should be connected between XTAL and EXTAL; updated maximum drive level of crystal rating to 250 µW.

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