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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A5
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	500MHz
Co-Processors/DSP	Multimedia; NEON™ MPE
RAM Controllers	LPDDR2, DDR3, DRAM
Graphics Acceleration	Yes
Display & Interface Controllers	DCU, GPU, LCD, VideoADC, VIU
Ethernet	10/100Mbps (2)
SATA	-
USB	USB 2.0 OTG + PHY (1)
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	-
Package / Case	364-LFBGA
Supplier Device Package	364-LFBGA (17x17)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mvf50nn151cmk50

Field	Description	Values
R	Revision	• 1 = Rev 1.x
T	Temperature range (°C)	• C = -40 °C to +85 °C T_a
PP	Package type	• KU = 176LQFP • MK = 364 MAPBGA
S	Speed	• Speed A5 Core • 26 = 266MHz • 40 = 400MHz • 50 = 500MHz

2.4 Part Numbers

This table lists the part numbers on the device.

Part Number	Package	Description
MVF30NN151CKU26	LQFP-EP 176 24*24*1.6	A5-266, No Security, 176LQFP
MVF30NS151CKU26	LQFP-EP 176 24*24*1.6	A5-266, Security, 176LQFP
MVF50NN151CMK40	MAP 364 17*17*1.5 P0.8	A5-400, No Security, 364BGA
MVF50NS151CMK40	MAP 364 17*17*1.5 P0.8	A5-400, Security, 364BGA
MVF50NN151CMK50	MAP 364 17*17*1.5 P0.8	A5-500, No Security, 364BGA
MVF50NS151CMK50	MAP 364 17*17*1.5 P0.8	A5-500, Security, 364BGA
MVF51NN151CMK50	MAP 364 17*17*1.5 P0.8	A5-500, L2 Cache, No Security, 364BGA
MVF51NS151CMK50	MAP 364 17*17*1.5 P0.8	A5-500, L2 Cache, Security, 364BGA
MVF60NN151CMK40	MAP 364 17*17*1.5 P0.8	A5-400, M4, No Security, 364BGA
MVF60NS151CMK40	MAP 364 17*17*1.5 P0.8	A5-400, M4, Security, 364BGA
MVF60NN151CMK50	MAP 364 17*17*1.5 P0.8	A5-500, M4, No Security, 364BGA
MVF60NS151CMK50	MAP 364 17*17*1.5 P0.8	A5-500, M4, Security, 364BGA
MVF61NN151CMK50	MAP 364 17*17*1.5 P0.8	A5-500, M4, L2 Cache, No Security, 364BGA
MVF61NS151CMK50	MAP 364 17*17*1.5 P0.8	A5-500, M4, L2 Cache, Security, 364BGA
MVF62NN151CMK40	MAP 364 17*17*1.5 P0.8	A5-400, M4 Primary, No Security, 364BGA

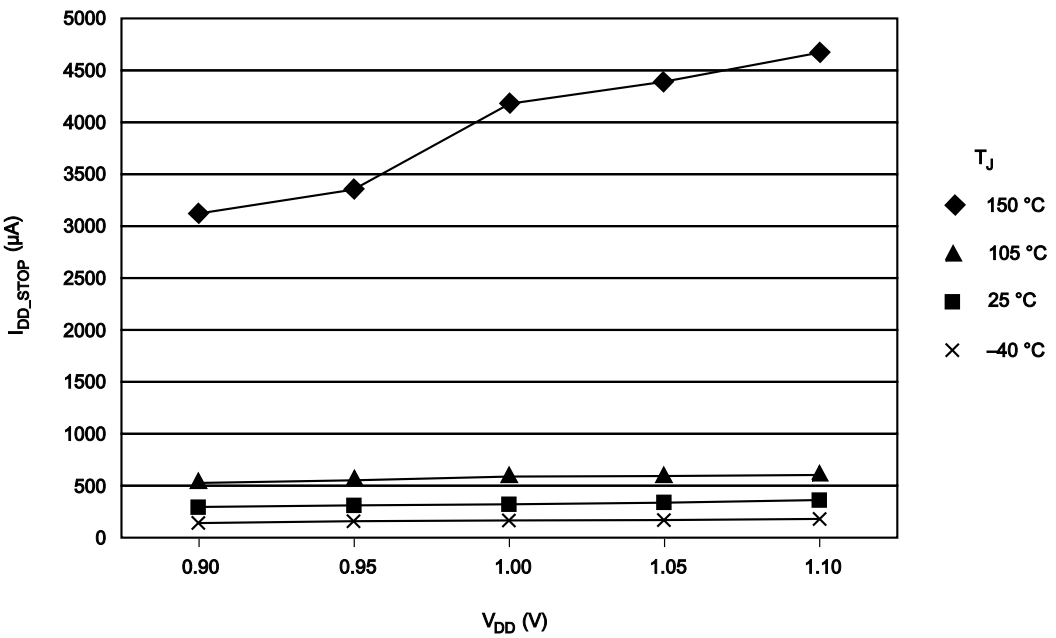
3.8.1 Example 1

This is an example of an operating behavior that includes a typical value:

Symbol	Description	Min.	Typ.	Max.	Unit
I_{WP}	Digital I/O weak pullup/pulldown current	10	70	130	µA

3.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions:



3.9 Typical Value Conditions

Typical values assume you meet the following conditions (or other conditions as specified):

Symbol	Description	Value	Unit
T_A	Ambient temperature	25	°C
V_{DD}	3.3 V supply voltage	3.3	V

Table 3. LPREG electrical characteristics (continued)

Parameters	Min	Typ	Max	Unit	Comments
PSRR with 4.7uF output cap					
@ DC @noload			-40	dB	
@ DC @full load			-35		
Worst case @ any frequency			-12		

6.2.1.3 ULPREG electrical characteristics

Table 4. ULPREG electrical characteristics

Parameters	Min	Typ	Max	Unit	Comments
Power supply	3.0	3.3	3.6	V	
Current Consumption	1.88	2.3	2.86	µA	@ no load
	-	610	670	µA	@ full load
Output current capacity			20	mA	DC load current
Output voltage @ no load			1.175	V	
Output voltage @ full load	1.125			V	
PSRR with 500 pF output cap	-20			dB	Worst case at any frequency across corners
@ DC @noload			-50	dB	
@200KHz @noload			-37		
@ DC @full load			-42		
@200KHz @full load			-37		
Worst case @ any frequency @ any load			-15		

6.2.1.4 WBREG electrical characteristics

Table 5. WBREG electrical characteristics

Parameters	Min	Typ	Max	Unit	Comments
Power supply	3	3.3	3.6	V	-
Current Consumption	-	2	5	µA	@ no load
	-	2	5	µA	@ full load
Output current capacity	-	1	2	mA	DC load current
Output voltage @ no load		1.4	1.425	V	
Output voltage @ full load	1.375	1.398		V	
Output voltage programmability	1.4	1.4	1.7	V	16 steps of 25 mV each

Table 8. General guidelines for selection of NPN ballast

Symbol	Parameters	Value	Unit	Comments
Hfe	Minimum DC current gain (Beta)	42.5		As BCTRL pin can not drive more than 20mA Minimum value of beta for a collector current of 0.85A comes out to be 42.5.
PD (Junction to ambient)	Minimum power dissipation @ TA=85 °C	2.04	W	Assuming 0.85A collector current with Collector voltage of Ballast 3.6V(max) we get VCE= 3.6V-1.2V=2.4V So power dissipated is 2.4V*0.85A=2.04W . This should be met for junction to ambient power dissipation spec of ballast
IcmaxDC peak	Maximum peak DC collector current	0.85	A	1.2A and above capacity device preferable
VBE	Maximum voltage that BCTRL pin can drive	1.25V for 0.85A @ 85 °C	V	For a VDDREG of 3.0 V (min.), BCTRL pin can drive voltage up to VDDREG - 0.5 V = 2.5 V. Since emitter of ballast is fixed at 1.25 V (max) if chosen ballast can supply 0.85 A collector current @ 85 °C with a base-to-emitter voltage of 1.25 V or lower, it is suitable for application.
Ft	Unity current gain Frequency of Ballast	50	MHz	

Reducing the collector-to-emitter voltage drop lowers the ballast transistor heat dissipation. This can be implemented in two ways:

1. By introducing series resistor or diode(s) between the collector and VDDREG (placed far enough from the transistor for proper cooling)
2. By connecting the collector to a separate lower-voltage supply

In both of the above cases the transistor has to stay away from the deep saturation region; otherwise, due to significant Hfe degradation, its base current exceeds the BCTRL output maximum value.

In general, the transistor must be selected such that its Vce saturation voltage is lower than the expected minimum Collector-Emitter voltage, and at the same time, the base current is less than 20 mA for the maximum expected collector current. More information can be found in collateral documentation at http://www.freescale.com

Table 20. GPIO DC Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
		VOH/VOL values are with respect to DSE=001[1]				
Vol	Low-level output voltage	Iol= 1mA			0.15	V
Vih [2]	High-Level DC input voltage		0.7*ovdd		ovdd	V
Vil[2]	Low-Level DC input voltage		0		0.3*ovdd	V
Vhys	Input Hysteresis	ovdd=3.3 V	250			mV
Vt+[2, 3]	Schmitt trigger VT+		0.5*ovdd			V
Vt-[2, 3]	Schmitt trigger VT-				0.5*ovdd	V
Iin[4]	Input current (no pull-up/down)	Vin = ovdd or 0	-1		1	uA
Iin_22pu	Input current (22KOhm PU)	Vin = 0			212	uA
		Vin = ovdd			1	
Iin_47pu	Input current (47KOhm PU)	Vin = 0			100	
		Vin = ovdd			1	
Iin_100pu	Input current (100KOhm PU)	Vin = 0			50	
		Vin = ovdd			1	
Iin_100pd	Input current (100KOhm PD)	Vin = 0			1	
		Vin = ovdd			50	
R_Keeper	Keeper Circuit Resistance	Vin = 0.3 x OVDD VI = 0.7 x OVDD	105		175	Ohm
Issod	Sink current in open drain mode	Vin = ovdd			7	mA
Issop	Sink/source current in Push Pull mode	Vin = ovdd			7	mA

1. For details about Software MUX Pad Control Register DSE bit, see IOMUX Controller chapter of the device reference manual.
2. To maintain a valid level, the transitioning edge of the input must sustain a constant slew rate (monotonic) from the current DC level through to the target DC level, VIL or VIH. Monotonic input transition time is from 0.1ns to 1s. Vil and Vih do not apply when hysteresis is enabled.
3. Hysteresis of 250 mV is guaranteed over all operating conditions when hysteresis is enabled.
4. Typ condition: typ model, 3.3V, and 25°C. Max condition: bcs model, 3.6V, and -40°C. Min condition: wcs model, 3.0V and 85 °C. These values are for digital IO buffer cells.

Table 22. Output Buffer Average Impedance (3.3V power mode) (continued)

Symbol	Parameter	Drive strength[1]	Min	Typ	Max	Unit
		1 0 0	30	37	58	
		1 0 1	24	30	46	
		1 1 0 Extra drive strength	20	25	38	
		1 1 1	17	20	32	

1. The drive strengths are controlled by the DSE bit of the Software MUX Pad Control Register. For details, see IOMUX Controller chapter of the device reference manual.

7.2 DDR parameters

Table 23. DDR operating conditions

Symbol	Parameter	Min	Typ	Max	Unit
vddi	Core internal supply voltage	1.16	1.23	1.26	V
ovdd	I/O output supply voltage (DDR3 mode)	1.425	1.5	1.575	V
ovdd	I/O output supply voltage (LPDDR2 mode)	1.14	1.2	1.26	V
vdd2p5	I/O PD predriver and level shifters supply voltage	2.25	2.5	2.75	V

Table 24. LPDDR2 mode DC Electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
Voh	High-level output voltage		0.9*ovdd			V	Note that the JEDEC LPDDR2 specification (JESD209_2B) supersedes any specification in this document.
Vol	Low-level output voltage				0.1*ovdd	V	
Vref	Input reference voltage		0.49*ovdd	0.5*ovdd	0.51*ovdd	V	
Vih(dc)	DC input high voltage		Vref+0.13		ovdd	V	
Vil(dc)	DC input low voltage		ovss		Vref-0.13	V	
Vih(diff)	DC differential input logic high		0.26		Note[1]	V	
Vil(diff)	DC differential input logic low		Note[1]		-0.26	V	

Table continues on the next page...

NOTE

WBREG is the Well Bias Regulator. Supplies PD1 WELL during well bias modes.

8.3 Absolute maximum ratings

NOTE

These are the values above which device can get damaged. Refer to the recommended operating conditions table for intended use case values

Table 29. Absolute maximum ratings

Symbol	Parameters	Min	Max	Unit
USB0_VBUS	VBUS supply for USB	-	5.25	V
USB1_VBUS	VBUS supply for USB	-	5.25	V
USB_DCAP	USB LDO 5V->3.3V Outpu	-0.3	3.6	V
VBAT	Battery supply in case of LDOIN fails	-0.3	3.6	V
VDD33_LDOIN	LDO input supply	-0.3	3.6	V
DECAP_V11_LDO_OUT	LDO 3.3V -> 1.1V Output	-0.3	1.3	V
DECAP_V25_LDO_OUT	LDO 3.3V -> 2.5 Output for PLL, DDR, EFUSE	-0.3	3.6	V
VDD33	GPIO 3.3V IO supply	-0.3	3.6	V
VDDREG	Device PMU regulator and External ballast supply	-0.3	3.6	V
VDDA33_ADC	3.3V supply for ADC, DAC and IO segment	-0.3	3.6	V
VREFH_ADC	3.3V supply of AFE (Video ADC)	-0.3	3.6	V
VDDA33_AFE	3.3V supply of AFE (Video ADC)	-0.3	3.6	V
VDD12_AFE	1.2V supply for AFE (Video ADC)	-0.3	1.3	V
FA_VDD	Test purpose only	-0.3	1.3	V
VDD	1.2V core supply	-0.3	1.3	V
SDRAMC_VDD1P5	1.2/1.5 DDR Main IO supply	-0.3	1.975	V
SDRAMC_VDD2P5	2.5V DDR pre-drive supply DD2P5_LDO_OUT	-0.3	3.6	V

8.4 Recommended operating conditions

Table 30. Recommended operating conditions

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
USB0_VBUS	VBUS supply for USB w.r.t USB0_GND		4.4	5	5.25	V
USB1_VBUS	VBUS supply for USB w.r.t USB1_GND		4.4	5	5.25	V
USB_DCAP	USB LDO 5V->3 V Output	External DCAP (10uF termination for USBREG)		3		V
VBAT	Battery supply in case of LDOIN fails	External CAP 0.1uF	2.4	3.3	3.6	V
VDD33_LDOIN	LDO input supply		3	3.3	3.6	V
DECAP_V11_LDO_OUT	LDO 3.3V -> 1.1V Output	Recommended External DCAP: 1uF(Min) 10uF (Max)		1.1		V
DECAP_V25_LDO_OUT	LDO 3.3V -> 2.5 Output for PLL, DDR pre-driver, EFUSE	Recommended External DCAP: 1uF(Min) 10uF (Max)		2.5		V
VDD33	GPIO 3.3V IO supply	External CAP (10uF)	3	3.3	3.6	V
VDDREG	Device PMU regulator and External ballast supply	External CAP (10uF)	3	3.3	3.6	V
VDDA33_ADC	3.3V supply for ADC, DAC and IO segment	External CAP (10uF)	3	3.3	3.6	V
VREFH_ADC	High reference voltage for ADC and DAC	Relation with VDDDA33_ADC (1uF)	2.5	3.3	VDDA33_ADC	V
VREFL_ADC	Low reference voltage for ADC and DAC	External CAP (10uF)		0		V
VDDA33_AFE	3.3V supply of AFE (Video ADC)	External CAP 10uF	3	3.3	3.6	V
VDD12_AFE	1.2V supply for AFE (Video ADC)		1.16	1.23	1.26	V
FA_VDD	For testing purpose only should be shorted to VDD on board.		1.16	1.23	1.26	V
VDD[1]	1.2V core supply	4.7uF with a low ESR value (100 milliohms)	1.16	1.23	1.26	V
USB0_GND	Ground supply for USB			0		V
USB1_GND	Ground supply for USB			0		V
VSS_KEL0	USB LDO ground output			0		V
VSS	VSS ground			0		V
VSSA33_ADC	Ground supply for ADC, DAC and IO segment			0		V

Table continues on the next page...

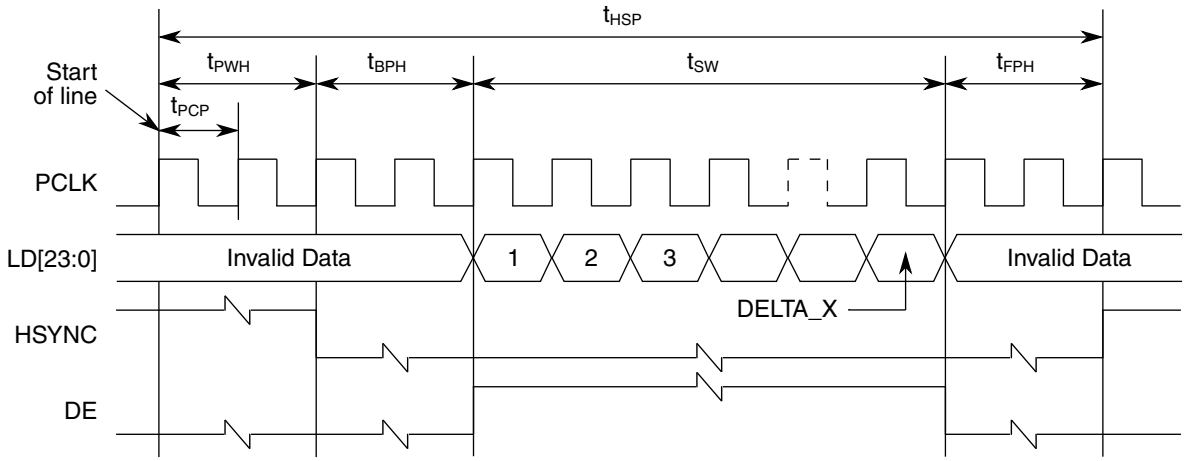


Figure 15. Horizontal sync timing

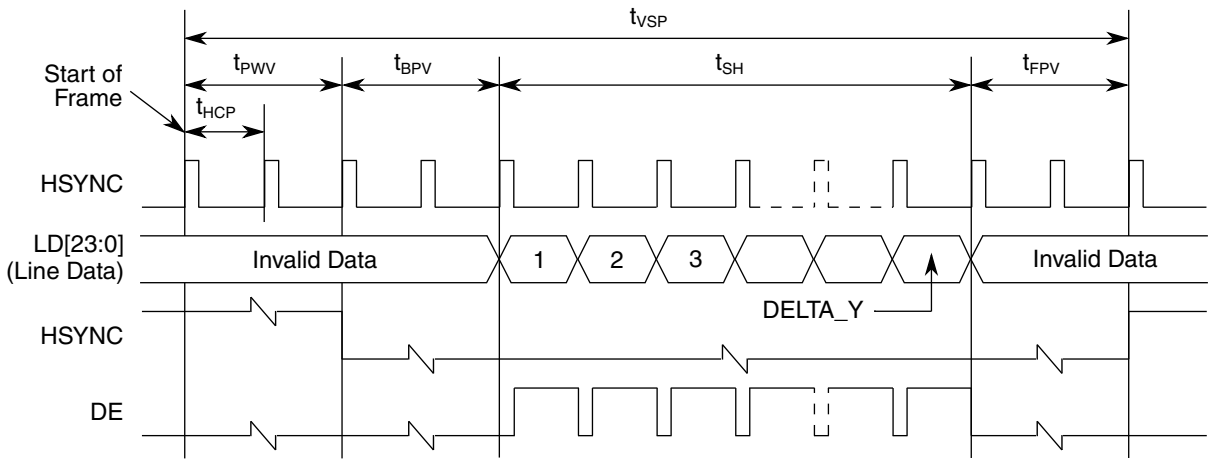


Figure 16. Vertical sync pulse

9.2.1.3 Interface to TFT LCD panels—access level

This section provides the access level timing parameters of the LCD interface.

Table 37. LCD Interface Timing Parameters1, 2, 3—Access Level

Symbol	Description	Min	Max	Unit
t_{CKP}	Pixel Clock Period	11.2	_	ns
t^{DV}	TFT interface data valid after pixel clock	_	4.4	ns
t^{DV}	TFT interface HSYNC valid after pixel clock	_	4.4	ns
t^{DV}	TFT interface VSYNC valid after pixel clock	_	4.4	ns
t^{DV}	TFT interface DE valid after pixel clock	_	4.4	ns
t^{HO}	TFT interface output hold time for data and control bits	0	_	ns
	Relative skew between the data bits	_	4.4	ns

1. The characteristics in this table are based on the assumption that data is output at +ve edge and displays latch data on -ve edg6

2. Intra bit skew is less than 2 ns
3. Load CL = 50 pf

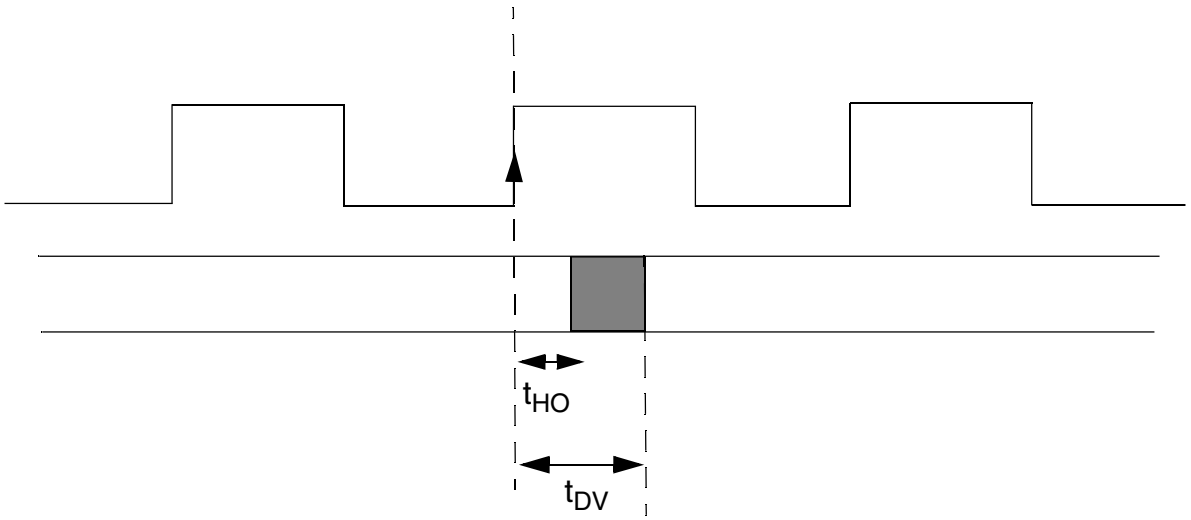


Figure 17. LCD Interface Timing Parameters—Access Level

9.2.2 Video Input Unit timing

This section provides the timing parameters of the Video Input Unit (VIU) interface.

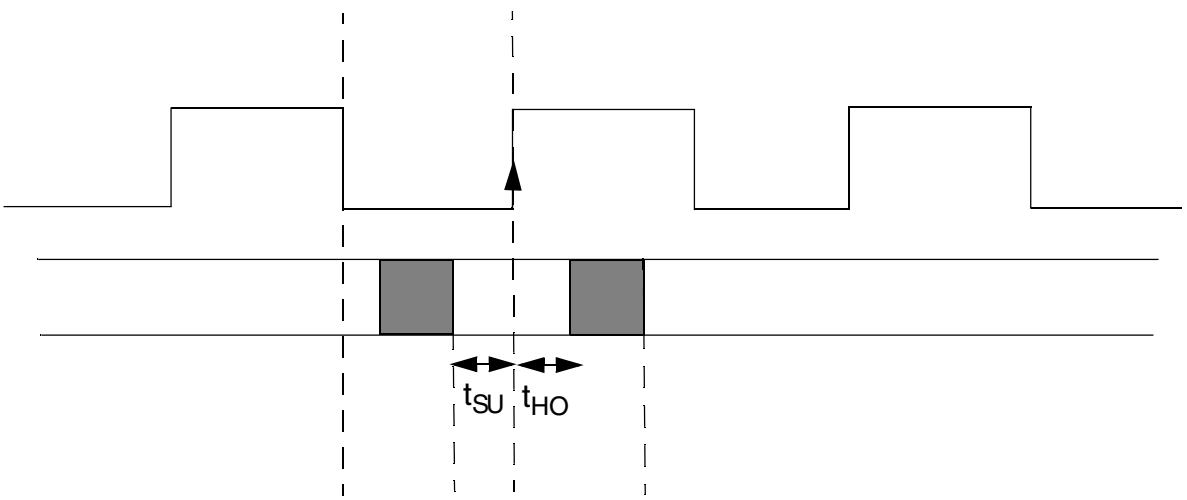


Figure 18. VIU Timing Parameters

Table 38. VIU Timing Parameters

Symbol	Characteristic	Min Value	Max Value	Unit
f_{PIX_CK}	VIU pixel clock frequency	_	64	MHz
t_{DSU}	VIU data setup time	4	_	ns
t_{DHD}	VIU data hold time	1	_	ns

9.6 Communication interfaces

9.6.1 DSPI timing specifications

Table 60. DSPI timing

No.	Symbol	Characteristic	Condition	Min	Max	Unit
1	t_{SCK}	SCK Cycle Time	—	t_{SYS} * 2	—	ns
4	t_{SDC}	SCK Clock Pulse Width	—	40%	60%	t_{SCK}
2	t_{CSC}	CS to SCK Delay	Master	16	—	ns
3	t_{ASC}	After SCK Delay	Master	16	—	ns
5	t_A	Slave Access Time (SS active to SOUT driven)	Slave	—	15	ns
6	t_{DI}	Slave Disable Time (SS inactive to SOUT High-Z or invalid)	Slave	—	10	ns
9	t_{SUI}	Data Setup Time for Inputs	Master	9	—	ns
			Slave	4	—	
10	t_{HI}	Data Hold Time for Inputs	Master	0	—	ns
			Slave	2	—	
11	t_{DV}	Data Valid (after SCK edge) for Outputs	Master	—	5	ns
			Slave	—	10	
12	t_{HO}	Data Hold Time for Outputs	Master	0	—	ns
			Slave	0	—	

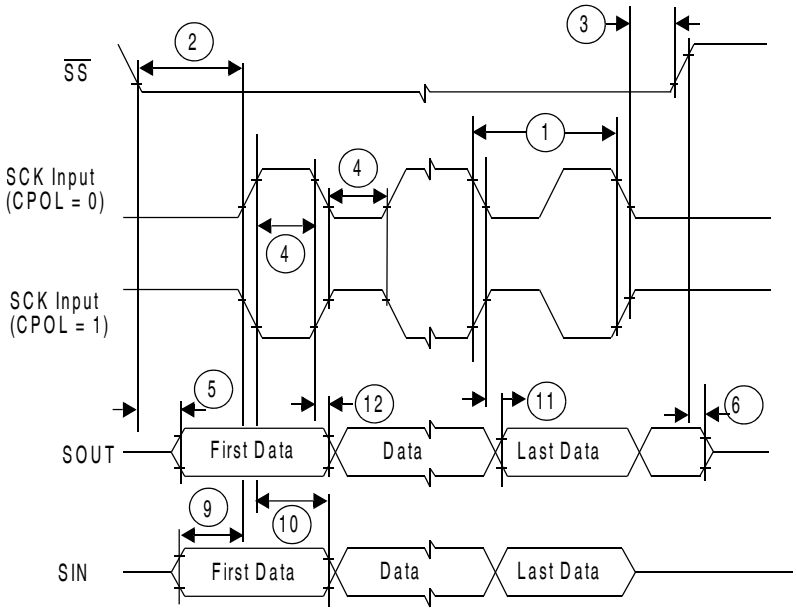


Figure 49. DSPI classic SPI timing slave, CPHA=0

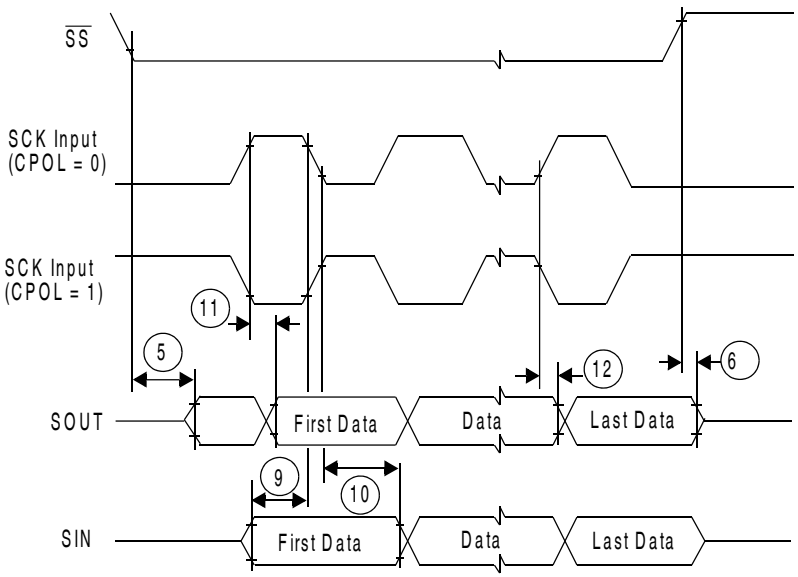


Figure 50. DSPI classic SPI timing slave, CPHA=1

9.6.2 I2C timing

Table 61. I2C input timing specifications — SCL and SDA[1]

No.	Parameter	Min.	Max.	Unit
1	Start condition hold time	2	—	PER_CLK Cycle[2]
2	Clock low time	8	—	PER_CLK Cycle

Table continues on the next page...

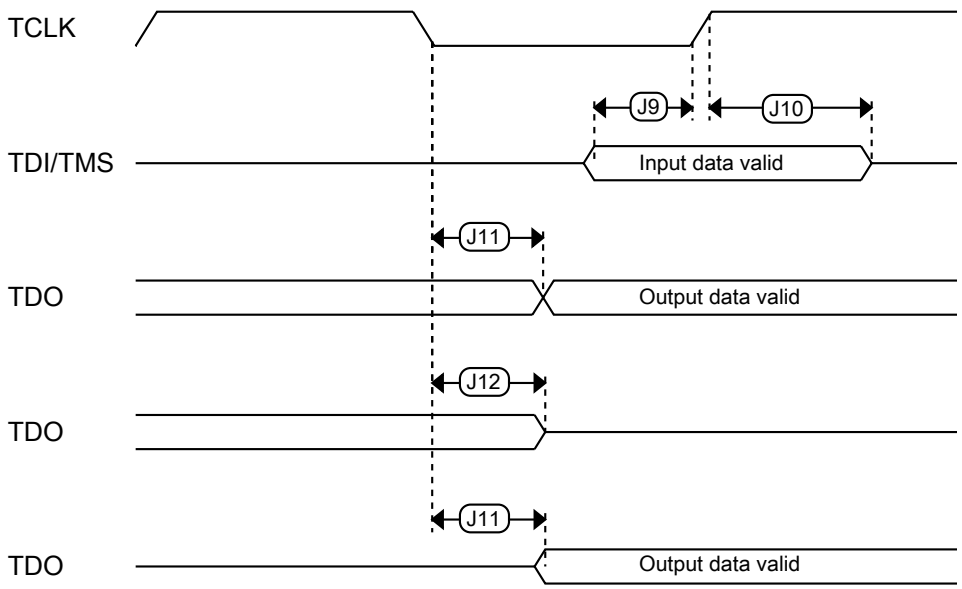


Figure 55. Test Access Port timing

9.8.2 Debug trace timing specifications

Table 74. Debug trace operating behaviors

Symbol	Description	Min.	Max.	Unit
T_{cyc}	Clock period	50		MHz
T_{wl}	Low pulse width	2	—	ns
T_{wh}	High pulse width	2	—	ns
T_r	Clock and data rise time	Refer Table 21		ns
T_f	Clock and data fall time Refer			ns
tDV	Data output valid	3	—	ns
tHO	Data output hold	1	—	ns

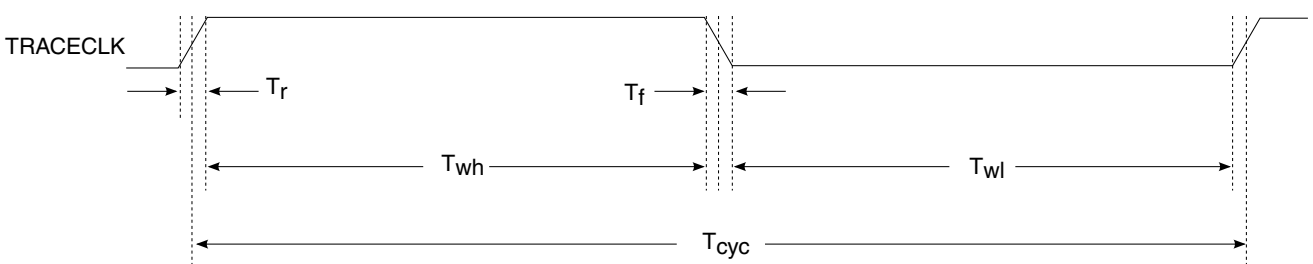


Figure 56. TRACE_CLKOUT specifications

364 MAP BGA	176 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
Y11	64	USB0_ VBUS_ DETECT			USB0_ VBUS_ DETECT							
Y9	—	USB1_GND			USB1_GND							
W9	—	USB1_DP			USB1_DP							
V9	—	USB1_DM			USB1_DM							
W10	—	USB1_VBUS			USB1_VBUS							
U9	—	USB1_ VBUS_ DETECT			USB1_ VBUS_ DETECT							
L4	8	PTC0		PTC0	RMII0_MDC/ MII0_MDC	FTM1CH0	SPI0_PCS3	ESAI_SCKT	SDHC0_CLK	VIU_DATA0	RCON18	
L5	9	PTC1		PTC1	RMII0_MDIO/ MII0_MDC	FTM1CH1	SPI0_PCS2	ESAI_FST	SDHC0_CMD	VIU_DATA1	RCON19	
M5	11	PTC2		PTC2	RMII0_CRS_ DV	SCI1_TX		ESAI_SDO0	SDHC0_ DAT0	VIU_DATA2	RCON20	
M3	12	PTC3		PTC3	RMII0_RXD1/ MII0_RXD[1]	SCI1_RX		ESAI_SDO1	SDHC0_ DAT1	VIU_DATA3	DCU0_R0	
L2	14	PTC4		PTC4	RMII0_RXD0/ MII0_RXD[0]	SCI1_RTS	SPI1_PCS1	ESAI_SDO2/ ESAI_SDI3	SDHC0_ DAT2	VIU_DATA4	DCU0_R1	
M1	15	PTC5		PTC5	RMII0_RXER/ MII0_RXER	SCI1_CTS	SPI1_PCS0	ESAI_SDO3/ ESAI_SDI2	SDHC0_ DAT3	VIU_DATA5	DCU0_G0	
N1	16	PTC6		PTC6	RMII0_TXD1/ MII0_TXD[1]		SPI1_SIN	ESAI_SDO5/ ESAI_SDI0	SDHC0_WP	VIU_DATA6	DCU0_G1	
N2	17	PTC7		PTC7	RMII0_TXD0/ MII0_TXD[0]		SPI1_SOUT	ESAI_SDO4/ ESAI_SDI1		VIU_DATA7	DCU0_B0	
N4	18	PTC8		PTC8	RMII0_TXEN/ MII0_TXEN		SPI1_SCK			VIU_DATA8	DCU0_B1	
T15	77	PTC9		PTC9	RMII1_MDC		ESAI_SCKT			MLBCLK		
U15	78	PTC10		PTC10	RMII1_MDIO		ESAI_FST			MLBSIGNAL		
P4	20	PTC11		PTC11	RMII1_CRS_ DV		ESAI_SDO0			MLBDATA		
P3	21	PTC12		PTC12	RMII1_RXD1		ESAI_SDO1		SAI2_TX_ BCLK			
P1	23	PTC13		PTC13	RMII1_RXD0		ESAI_SDO2/ ESAI_SDI3		SAI2_RX_ BCLK			
R1	26	PTC14		PTC14	RMII1_RXER		ESAI_SDO3/ ESAI_SDI2	SCI5_TX	SAI2_RX_ DATA	ADC0_SE6		
P2	27	PTC15		PTC15	RMII1_TXD1		ESAI_SDI0	SCI5_RX	SAI2_TX_ DATA	ADC0_SE7		
R3	29	PTC16		PTC16	RMII1_TXD0		ESAI_SDO4/ ESAI_SDI1	SCI5_RTS	SAI2_RX_ SYNC	ADC1_SE6		
R4	28	PTC17		PTC17	RMII1_TXEN		ADC1_SE7	SCI5_CTS	SAI2_TX_ SYNC	USB1_SOF_ PULSE		
B10	—	DDR_A[15]			DDR_A15							
D9	—	DDR_A[14]			DDR_A14							

364 MAP BGA	176 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
Y19	89	PTD3		PTD3	QSPI0_A_DATA2	SCI2_CTS	SPI1_PCS2	FB_AD12	SPDIF_PLOCK			
W19	90	PTD4		PTD4	QSPI0_A_DATA1		SPI1_PCS1	FB_AD11	SPDIF_SRCLK			
W20	91	PTD5		PTD5	QSPI0_A_DATA0		SPI1_PCS0	FB_AD10				
V20	92	PTD6		PTD6	QSPI0_A_DQS		SPI1_SIN	FB_AD9				
V19	93	PTD7		PTD7	QSPI0_B_SCK		SPI1_SOUT	FB_AD8				
U17	94	PTD8		PTD8	QSPI0_B_CS0	FB_CLKOUT	SPI1_SCK	FB_AD7				
U18	97	PTD9		PTD9	QSPI0_B_DATA3	SPI3_PCS1		FB_AD6		SAI1_TX_SYNC	DCU1_B0	
U20	98	PTD10		PTD10	QSPI0_B_DATA2	SPI3_PCS0		FB_AD5			DCU1_B1	
T20	99	PTD11		PTD11	QSPI0_B_DATA1	SPI3_SIN		FB_AD4				
T19	100	PTD12		PTD12	QSPI0_B_DATA0	SPI3_SOUT		FB_AD3				
T18	101	PTD13		PTD13	QSPI0_B_DQS	SPI3_SCK		FB_AD2				
A19	141	PTB23		PTB23	SAI0_TX_BCLK	SCI1_TX		FB_MUXED_ALE	FB_TS_b	SCI3_RTS	DCU1_G3	
A18	142	PTB24		PTB24	SAI0_RX_BCLK	SCI1_RX		FB_MUXED_TSIZ0	NF_WE_b	SCI3_CTS	DCU1_G4	
B17	149	PTB25		PTB25	SAI0_RX_DATA	SCI1_RTS		FB_CS1_b	NF_CE0_b		DCU1_G5	
A17	150	PTB26	RCON21	PTB26	SAI0_TX_DATA	SCI1_CTS	RCON21	FB_CS0_b	NF_CE1_b		DCU1_G6	
U8	57	PTB27	RCON22	PTB27	SAI0_RX_SYNC		RCON22	FB_OE_b	FB_MUXED_TBST_b	NF_RE_b	DCU1_G7	
A16	151	PTB28	RCON23	PTB28	SAI0_TX_SYNC		RCON23	FB_RW_b			DCU1_B6	
D16	153	PTC26	RCON24	PTC26	SAI1_TX_BCLK	SPI0_PCS5	RCON24	FB_TA_b	NF_RB_b		DCU1_B7	
E16	154	PTC27	RCON25	PTC27	SAI1_RX_BCLK	SPI0_PCS4	RCON25	FB_BE3_b	FB_CS3_b	NF_ALE	DCU1_B2	
E15	155	PTC28	RCON26	PTC28	SAI1_RX_DATA	SPI0_PCS3	RCON26	FB_BE2_b	FB_CS2_b	NF_CLE	DCU1_B3	
C16	152	PTC29	RCON27	PTC29	SAI1_TX_DATA	SPI0_PCS2	RCON27	FB_BE1_b	FB_MUXED_TSIZ1		DCU1_B4	
T8	58	PTC30	RCON28	PTC30	SAI1_RX_SYNC	SPI1_PCS2	RCON28	FB_MUXED_BE0_b	FB_TSIZ0	ADC0_SE5	DCU1_B5	
W5	42	PTC31	RCON29	PTC31	SAI1_TX_SYNC		RCON29			ADC1_SE5	DCU1_B6	

364 MAP BGA	176 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
B3	24	VSS			VSS							
B5	32	VSS			VSS							
B8	—	VSS			VSS							
B11	—	VSS			VSS							
B13	—	VSS			VSS							
B16	—	VSS			VSS							
B19	—	VSS			VSS							
C2	—	VSS			VSS							
D17	—	VSS			VSS							
E5	—	VSS			VSS							
E8	—	VSS			VSS							
E11	—	VSS			VSS							
E14	—	VSS			VSS							
E19	—	VSS			VSS							
F2	—	VSS			VSS							
G17	—	VSS			VSS							
H4	—	VSS			VSS							
J2	—	VSS			VSS							
J18	—	VSS			VSS							
M2	—	VSS			VSS							
M4	—	VSS			VSS							
M18	—	VSS			VSS							
R2	—	VSS			VSS							
R18	—	VSS			VSS							
U7	—	VSS			VSS							
U19	—	VSS			VSS							
V13	—	VSS			VSS							
W6	—	VSS			VSS							
V17	—	VSS			VSS							
Y1	—	VSS			VSS							
Y20	—	VSS			VSS							
H19	—	VSS			VSS							
L19	—	VSS			VSS							
P19	—	VSS			VSS							
J5	—	SDRAMC_ VDD2P5			SDRAMC_ VDD2P5							
E6	—	SDRAMC_ VDD2P5			SDRAMC_ VDD2P5							
E10	—	SDRAMC_ VDD2P5			SDRAMC_ VDD2P5							

Table 75. RGPIO versus Pins (continued)

RGPIO	In GPIO module	Corresponding Pin on the chip	IOMUX register name	IOMUX register address
RGPIO[79]	PORT2[15]	PTD0	IOMUXC_PTD0	4004813C
RGPIO[80]	PORT2[16]	PTD1	IOMUXC_PTD1	40048140
RGPIO[81]	PORT2[17]	PTD2	IOMUXC_PTD2	40048144
RGPIO[82]	PORT2[18]	PTD3	IOMUXC_PTD3	40048148
RGPIO[83]	PORT2[19]	PTD4	IOMUXC_PTD4	4004814C
RGPIO[84]	PORT2[20]	PTD5	IOMUXC_PTD5	40048150
RGPIO[85]	PORT2[21]	PTD6	IOMUXC_PTD6	40048154
RGPIO[86]	PORT2[22]	PTD7	IOMUXC_PTD7	40048158
RGPIO[87]	PORT2[23]	PTD8	IOMUXC_PTD8	4004815C
RGPIO[88]	PORT2[24]	PTD9	IOMUXC_PTD9	40048160
RGPIO[89]	PORT2[25]	PTD10	IOMUXC_PTD10	40048164
RGPIO[90]	PORT2[26]	PTD11	IOMUXC_PTD11	40048168
RGPIO[91]	PORT2[27]	PTD12	IOMUXC_PTD12	4004816C
RGPIO[92]	PORT2[28]	PTD13	IOMUXC_PTD13	40048170
RGPIO[93]	PORT2[29]	PTB23	IOMUXC_PTB23	40048174
RGPIO[94]	PORT2[30]	PTB24	IOMUXC_PTB24	40048178
RGPIO[95]	PORT2[31]	PTB25	IOMUXC_PTB25	4004817C
RGPIO[96]	PORT3[0]	PTB26	IOMUXC_PTB26	40048180
RGPIO[97]	PORT3[1]	PTB27	IOMUXC_PTB27	40048184
RGPIO[98]	PORT3[2]	PTB28	IOMUXC_PTB28	40048188
RGPIO[99]	PORT3[3]	PTC26	IOMUXC_PTC26	4004818C
RGPIO[100]	PORT3[4]	PTC27	IOMUXC_PTC27	40048190
RGPIO[101]	PORT3[5]	PTC28	IOMUXC_PTC28	40048194
RGPIO[102]	PORT3[6]	PTC29	IOMUXC_PTC29	40048198
RGPIO[103]	PORT3[7]	PTC30	IOMUXC_PTC30	4004819C
RGPIO[104]	PORT3[8]	PTC31	IOMUXC_PTC31	400481A0
RGPIO[105]	PORT3[9]	PTE0	IOMUXC_PTE0	400481A4
RGPIO[106]	PORT3[10]	PTE1	IOMUXC_PTE1	400481A8
RGPIO[107]	PORT3[11]	PTE2	IOMUXC_PTE2	400481AC
RGPIO[108]	PORT3[12]	PTE3	IOMUXC_PTE3	400481B0
RGPIO[109]	PORT3[13]	PTE4	IOMUXC_PTE4	400481B4
RGPIO[110]	PORT3[14]	PTE5	IOMUXC_PTE5	400481B8
RGPIO[111]	PORT3[15]	PTE6	IOMUXC_PTE6	400481BC
RGPIO[112]	PORT3[16]	PTE7	IOMUXC_PTE7	400481C0
RGPIO[113]	PORT3[17]	PTE8	IOMUXC_PTE8	400481C4
RGPIO[114]	PORT3[18]	PTE9	IOMUXC_PTE9	400481C8
RGPIO[115]	PORT3[19]	PTE10	IOMUXC_PTE10	400481CC
RGPIO[116]	PORT3[20]	PTE11	IOMUXC_PTE11	400481D0
RGPIO[117]	PORT3[21]	PTE12	IOMUXC_PTE12	400481D4

Table continues on the next page...

Table 75. RGPIO versus Pins (continued)

RGPIO	In GPIO module	Corresponding Pin on the chip	IOMUX register name	IOMUX register address
RGPIO[118]	PORT3[22]	PTE13	IOMUXC_PTE13	400481D8
RGPIO[119]	PORT3[23]	PTE14	IOMUXC_PTE14	400481DC
RGPIO[120]	PORT3[24]	PTE15	IOMUXC_PTE15	400481E0
RGPIO[121]	PORT3[25]	PTE16	IOMUXC_PTE16	400481E4
RGPIO[122]	PORT3[26]	PTE17	IOMUXC_PTE17	400481E8
RGPIO[123]	PORT3[27]	PTE18	IOMUXC_PTE18	400481EC
RGPIO[124]	PORT3[28]	PTE19	IOMUXC_PTE19	400481F0
RGPIO[125]	PORT3[29]	PTE20	IOMUXC_PTE20	400481F4
RGPIO[126]	PORT3[30]	PTE21	IOMUXC_PTE21	400481F8
RGPIO[127]	PORT3[31]	PTE22	IOMUXC_PTE22	400481FC
RGPIO[128]	PORT4[0]	PTE23	IOMUXC_PTE23	40048200
RGPIO[129]	PORT4[1]	PTE24	IOMUXC_PTE24	40048204
RGPIO[130]	PORT4[2]	PTE25	IOMUXC_PTE25	40048208
RGPIO[131]	PORT4[3]	PTE26	IOMUXC_PTE26	4004820C
RGPIO[132]	PORT4[4]	PTE27	IOMUXC_PTE27	40048210
RGPIO[133]	PORT4[5]	PTE28	IOMUXC_PTE28	40048214
RGPIO[134]	PORT4[6]	PTA7	IOMUXC_PTA7	40048218

12.2.2 Special Signal

Table 76. Special Signal Considerations

Special Signal	Comments
DDR_VREF	When using DDR_VREF with DDR I/O, the nominal reference voltage must be half of the SDRAMC_VDD1P5 supply. The user must tie DDR_VREF to a precision external resistor divider. Shunt each resistor with a closely-mounted 0.1 µF capacitor.
DDR_ZQ	DRAM calibration resistor 240 Ω 1% used as reference during DRAM output buffer driver calibration should be connected between this pad and GND
DECAP_V25_LDO_OUT	DCAP_V25_LDO_OUT can be tied to SDRAMC_VDD2P5 to provide the predriver supply for the DDR I/O segment. SDRAMC_VDD1P5 requires an external regulated supply. If SDRAMC_VDD2P5 uses an external 2.5V supply, do NOT tie it to DCAP_V25_LDO_OUT.
EXT_POR, TEST	Factory use only, tie to ground..
EXT_TAMPER0, EXT_TAMPER1, EXT_TAMPER2, EXT_TAMPER3, EXT_TAMPER4, EXT_TAMPER5	Security related tamper detection inputs, if not in use they must be tied to ground.
FA_VDD	Factory use only, tie to VDD.

Table continues on the next page...

Table 78. Functional Assignment Pins (continued)

Signal Name	364 MAP BGA	176 LQFP (F-series ONLY)	Power Group	Pad Type	Default Mode (Reset)	Default Function	Input/ Output	Value
PTD22	F20	126	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD23	G20	124	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD24	G19	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD25	G18	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD26	G16	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD27	H16	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD28	H17	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD29	H18	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD30	H20	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD31	J20	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTE0	N16	103	VDD33	GPIO	ALT2	BMODE1	Input	Disabled
PTE1	N18	104	VDD33	GPIO	ALT2	BMODE0	Input	Disabled
PTE2	N19	105	VDD33	GPIO	ALT0	GPIO	Disabled	
PTE3	Y15	80	VDD33	GPIO	ALT0	GPIO	Disabled	
PTE4	N20	106	VDD33	GPIO	ALT0	GPIO	Disabled	
PTE5	T16	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTE6	W16	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTE7	M20	109	VDD33	GPIO	ALT3	RCON0	Input	Disabled
PTE8	M19	110	VDD33	GPIO	ALT3	RCON1	Input	Disabled
PTE9	M17	111	VDD33	GPIO	ALT3	RCON2	Input	Disabled
PTE10	M16	112	VDD33	GPIO	ALT3	RCON3	Input	Disabled
PTE11	L16	113	VDD33	GPIO	ALT3	RCON4	Input	Disabled
PTE12	L17	114	VDD33	GPIO	ALT3	RCON5	Input	Disabled
PTE13	Y16	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTE14	W15	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTE15	L18	115	VDD33	GPIO	ALT3	RCON6	Input	Disabled
PTE16	L20	116	VDD33	GPIO	ALT3	RCON7	Input	Disabled
PTE17	K20	117	VDD33	GPIO	ALT3	RCON8	Input	Disabled
PTE18	K19	118	VDD33	GPIO	ALT3	RCON9	Input	Disabled
PTE19	K18	119	VDD33	GPIO	ALT3	RCON10	Input	Disabled
PTE20	A12	170	VDD33	GPIO	ALT3	RCON11	Input	Disabled
PTE21	V16	81	VDD33	GPIO	ALT0	GPIO	Disabled	
PTE22	W17	84	VDD33	GPIO	ALT0	GPIO	Disabled	
PTE23	J17	122	VDD33	GPIO	ALT3	RCON12	Input	Disabled
PTE24	D19	134	VDD33	GPIO	ALT3	RCON13	Input	Disabled
PTE25	C19	135	VDD33	GPIO	ALT3	RCON14	Input	Disabled
PTE26	C20	137	VDD33	GPIO	ALT3	RCON15	Input	Disabled

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Table 79. Revision History (continued)

Rev. No.	Date	Substantial Changes
Rev 6	Jan 2014	• Added QuadSPI electricals • Changed VBB references to VBAT • In the feature list, clarified that ECC supported for 8-bit mode only, not 16-bit. • Revised the part number format • Revised the field table • Added Absolute Maximum Rating table, which was madde non_cust in the previous version • In the Power Consumption Operating Behavior table, Revised min and max value of IDD_LPS3 and IDD_LPS2. Removed IDD_LPS1 row • In the USB PHY Current Consumption table, removed the Normal Mode • In the Power Sequence table, revised the Power UP/ Down Order column for USB0_VBUs and USB1_VBUS • In the Recommended operating conditions table, revised the min value of VBAT. Revised the min value of VREFH_ADC Revised the min and max values of SDRAMC_VDD1P5 • In the Recommended Connections for Unused Analog Interfaces section, added the notes. Revised the Recommendation if Unused column • In the 12-bit ADC operating conditions, revised Conditions for Ground voltage. Revised min Ref High Voltage • In the 12-bit DAC operating requirements, revised the min and max value of VREFH_ADC • In the SDHC switching specifications, revised the max value of SD6 • In the 24MHz external oscillator electrical characteristics table, revised the min value of VIH and max value of VIL
Rev 7	April 2014	• Updated Note in "Power supply" section. • Updated Absolute maximum ratings section: solute maximum ratings Table - FA_VDD row: Min and Max column • Updated figure "12-bit ADC Input Impedance Equivalency Diagram"

Table continues on the next page...