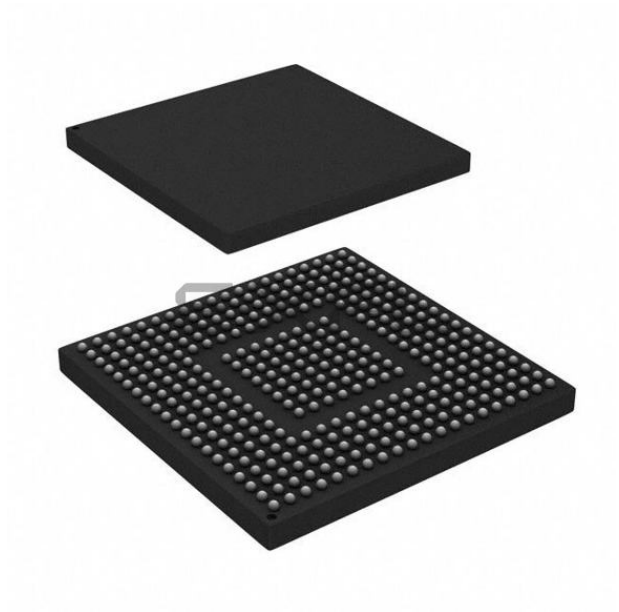

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A5
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	500MHz
Co-Processors/DSP	Multimedia; NEON™ MPE
RAM Controllers	LPDDR2, DDR3, DRAM
Graphics Acceleration	Yes
Display & Interface Controllers	DCU, GPU, LCD, VideoADC, VIU
Ethernet	10/100Mbps (2)
SATA	-
USB	USB 2.0 OTG + PHY (1)
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	-
Package / Case	364-LFBGA
Supplier Device Package	364-LFBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mvf50nn152cmk50

1 Ordering parts

1.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web.

1. To determine the orderable part numbers for this device, go to www.freescale.com and search the required part number. The part numbering format is described in the section that follows.

2 Part identification

2.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

2.2 Part Number Format

The figure below represents the format of part number of this device.

3.3.1 Example

This is an example of an attribute:

Symbol	Description	Min.	Max.	Unit
CIN_D	Input capacitance: digital pins	—	7	pF

3.4 Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

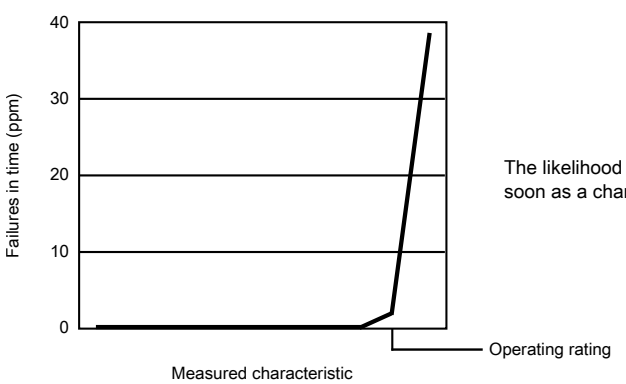
- *Operating ratings* apply during operation of the chip.
- *Handling ratings* apply when the chip is not powered.

3.4.1 Example

This is an example of an operating rating:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	–0.3	1.2	V

3.5 Result of exceeding a rating



The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.

Table 8. General guidelines for selection of NPN ballast

Symbol	Parameters	Value	Unit	Comments
Hfe	Minimum DC current gain (Beta)	42.5		As BCTRL pin can not drive more than 20mA Minimum value of beta for a collector current of 0.85A comes out to be 42.5.
PD (Junction to ambient)	Minimum power dissipation @ TA=85 °C	2.04	W	Assuming 0.85A collector current with Collector voltage of Ballast 3.6V(max) we get VCE= 3.6V-1.2V=2.4V So power dissipated is 2.4V*0.85A=2.04W . This should be met for junction to ambient power dissipation spec of ballast
IcmaxDC peak	Maximum peak DC collector current	0.85	A	1.2A and above capacity device preferable
VBE	Maximum voltage that BCTRL pin can drive	1.25V for 0.85A @ 85 °C	V	For a VDDREG of 3.0 V (min.), BCTRL pin can drive voltage up to VDDREG - 0.5 V = 2.5 V. Since emitter of ballast is fixed at 1.25 V (max) if chosen ballast can supply 0.85 A collector current @ 85 °C with a base-to-emitter voltage of 1.25 V or lower, it is suitable for application.
Ft	Unity current gain Frequency of Ballast	50	MHz	

Reducing the collector-to-emitter voltage drop lowers the ballast transistor heat dissipation. This can be implemented in two ways:

1. By introducing series resistor or diode(s) between the collector and VDDREG (placed far enough from the transistor for proper cooling)
2. By connecting the collector to a separate lower-voltage supply

In both of the above cases the transistor has to stay away from the deep saturation region; otherwise, due to significant Hfe degradation, its base current exceeds the BCTRL output maximum value.

In general, the transistor must be selected such that its Vce saturation voltage is lower than the expected minimum Collector-Emitter voltage, and at the same time, the base current is less than 20 mA for the maximum expected collector current. More information can be found in collateral documentation at http://www.freescale.com

6.2.3 LDO electrical specifications

6.2.3.1 LDO_1P1

Table 12. LDO_1P1 parameters

Specification	Min	Typ	Max	Unit	Comments
VDDIO	3	3.3	3.6	V	IO supply
VDD1P1_OUT	0.9	1.1	1.2	V	Regulator output
I_out	-		150	mA	>= 300mV drop out
Regulator output programming range	0.8	1.1	1.4	V	Programmable in 25mV steps
Brownout Voltage	0.85	0.94		V	
Brownout offset step	0	-	175	mV	Programmable in 25mV steps
Minimum external decoupling capacitor	1	-	-	µF	low ESR

For additional information, see the device reference manual.

6.2.3.2 LDO_2P5

Table 13. LDO_2P5 parameters

Specification	Min	Typ	Max	Unit	Comments
VDDIO	3	3.3	3.6	V	IO supply
VDD2P5_OUT	2.3	2.5	2.6	V	Regulator output
I_out	-		350	mA	@500mV drop out
Regulator output programming range	2.0	2.5	2.75	V	Programmable in 25mV steps
[P:][C:] Brownout Voltage	2.25	2.33		V	
Brownout offset step	0	-	175	mV	Programmable in 25mV steps
Minimum external decoupling capacitor	1	-	-	µF	low ESR

For additional information, see the reference manual.

Table 21. GPIO AC Electrical Characteristics (3.3V power mode)

Symbol	Parameter	Drive strength[1]	Slew rate	Test conditions	Min	Max	Unit
tpr	IO Output Transition Times (PA1), rise/fall	Max 1 1 1	slow	15pF Cload on pad, input edge rate 200ps	1.70	1.81	ns
			fast		1.04	1.18	
		High 1 0 1	slow		2.30	2.44	
			fast		1.69	1.79	
		Medium 1 0 0	slow		3.07	3.31	
			fast		2.45	2.61	
		Low 0 1 1	slow		5.13	5.44	
			fast		4.79	5.18	
tpo	IO Output Propagation Delay (PA2), rise/fall	Max 1 1 1	slow	15pF Cload on pad, input edge rate 200ps	5.01	5.04	ns
			fast		3.06	3.10	
		High 1 0 1	slow		5.55	5.68	
			fast		3.52	3.55	
		Medium 1 0 0	slow		6.37	6.67	
			fast		4.04	4.11	
		Low 0 1 1	slow		7.39	7.60	
			fast		5.54	6.10	
tpv	Output Enable to Output Valid Delay, rise/fall	Max 1 1 1	slow	15pF Cload on pad, input edge rate 200ps, 0->1, 1->0 pad transitions	5.12	5.21	ns
			fast		3.18	3.28	
		High 1 0 1	slow		5.72	5.80	
			fast		3.67	3.71	
		Medium 1 0 0	slow		6.55	6.80	
			fast		4.06	4.09	
		Low 0 1 1	slow		7.80	8.19	
			fast		5.72	6.22	
tpi	Input Pad Propagation Delay rise/fall	without hysteresis	-	150f Cload on, input edge rate from pad =1.2ns	1.06	1.31	ns
		with hysteresis	-		1.22	1.41	

1. The drive strengths are controlled by the DSE bit of the Software MUX Pad Control Register. For details, see IOMUX Controller chapter of the device reference manual.

7.1.1 Output Buffer Impedance measurement

Table 22. Output Buffer Average Impedance (3.3V power mode)

Symbol	Parameter	Drive strength[1]	Min	Typ	Max	Unit
Rdrv	Output driver impedance	0 0 1	116	150	220	Ohm
		0 1 0	58	75	110	
		0 1 1	39	50	73	

Table continues on the next page...

Table 28. Power sequencing (continued)

Power Supply (PKG Level)	Board Level Power Nets	Parameters	Power Order	Comment
VDD33_LDOIN	VDD33	LDO input supply (LDO1P1, LDO2P5, LDO1P1_RTC)	1	VDD33_LDOIN,VDDREG and VDD33 should come from a common supply source (represented as 3.3V SMPS in the Figure 4)
VDDREG	VDD33	Device PMU regulator and External ballast supply	1	
VDD33	VDD33	GPIO 3.3V IO supply, LCD Supply	1	
SDRAMC_VDD1P5	SDRAMC_VDD1P5	1.2/1.5 DDR Main IO supply	NA	In case the Ballast transistor's collector is connected to the 1.5V DRAM supply (instead of the 3.3V supply), turn this 1.5V supply on before turning on the 3.3V.
VDDA33_ADC	VDDA33_ADC	3.3V supply for ADC, DAC and IO segment	1	
VREFH_ADC	VREFH_ADC	High Reference of ADC, DAC	1	
VDDA33_AFE	VDDA33_AFE	3.3V supply of AFE (Video ADC)	1	
VDD12_AFE	VDD	1.2V supply for AFE (Video ADC)	2	
FA_VDD	VDD	Shorted with VDD at Board Level in 364BGA (Test pin only)	NA	
VDD	VDD	1.2V core supply from External ballast	2	
USB0_VBUS 1	USB_VBUS	VBUS supply for USB	NA	
USB1_VBUS 2	USB_VBUS	VBUS supply for USB	NA	

1. Power sequencing of USB0_VBUS is independent of any other power supply.
2. Power sequencing of USB1_VBUS is independent of any other power supply.

NOTE

NA stands for no sequencing needs, for example, the supply can come in any order.

NOTE

All supplies grouped together e.g. 1,2, others. These have no power sequencing restriction in between them.

NOTE

If none of the SDRAMC pins are connected on the board, the SDRAMC supply could be left floating.

NOTE

At power up, 1.2V supply will follow 3.3V supply. At power down, it should be checked that 1.2V falls before 3.3V.

NOTE

The standby current on USBx_VBUS is 300 - 500 uA. This is well below the 2.5 mA limit set by the USB 2.0 specification.

9.1.1.2 12-bit ADC characteristics

Table 32. 12-bit ADC Characteristics (V_{REFH} = V_{DDAD}, V_{REFL} = V_{SSAD})

Characteristic	Conditions[1]	Symb	Min	Typ [2]	Max	Unit	Comment
Supply Current	ADLPC=1, ADHSC=0	I_{DDAD}		250		µA	ADLSMP=0 ADSTS=10 ADCO=1
	ADLPC=0, ADHSC=0			350			
	ADLPC=0, ADHSC=1			400			
Supply Current	Stop, Reset, Module Off	I_{DDAD}		0.01	0.8	µA	
ADC Asynchronous Clock Source	ADHSC=0	f_{ADACK}		10		MHz	t_{ADACK} = $1/f_{ADACK}$
	ADHSC=1			20			
Sample Cycles	ADLSMP=0, ADSTS=00	Csamp		2		cycles	
	ADLSMP=0, ADSTS=01			4			
	ADLSMP=0, ADSTS=10			6			
	ADLSMP=0, ADSTS=11			8			
	ADLSMP=1, ADSTS=00			12			
	ADLSMP=1, ADSTS=01			16			
	ADLSMP=1, ADSTS=10			20			
	ADLSMP=1, ADSTS=11			24			
Conversion Cycles	ADLSMP=0 ADSTS=00	Cconv		28		cycles	
	ADLSMP=0 ADSTS=01			30			
	ADLSMP=0 ADSTS=10			32			
	ADLSMP=0 ADSTS=11			34			
	ADLSMP=1 ADSTS=00			38			
	ADLSMP=1 ADSTS=01			42			
	ADLSMP=1 ADSTS=10			46			
	ADLSMP=1, ADSTS=11			50			
Conversion Time	ADLSMP=0 ADSTS=00	Tconv		0.7		µs	Fadc=40 MHz
	ADLSMP=0 ADSTS=01			0.75			

Table continues on the next page...

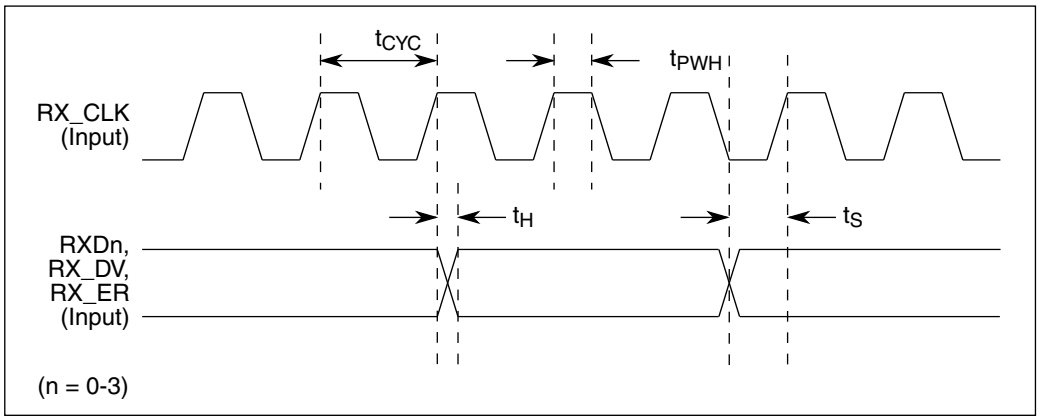


Figure 22. MII receive signal timing diagram

Table 42. Receive signal timing for MII interfaces

Characteristic		MII Mode			Unit
		Min	Typ	Max	
RX_CLK clock period (100/10 MBPS)	t_{CYC}		40/400		ns
RX_CLK duty cycle, t_{PWH}/t_{CYC}		45	50	55	%
Input setup time before RX_CLK	t_s	5			ns
Input hold time after RX_CLK	t_h	5			ns

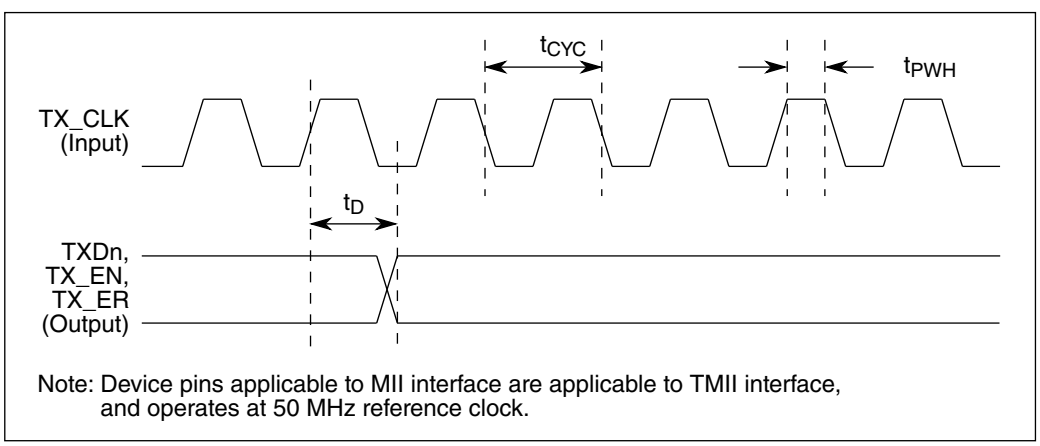


Figure 23. MII transmit signal timing diagram

Table 43. Transmit signal timing for MII interfaces

Characteristic		MII Mode			Unit
		Min	Typ	Max	
TX_CLK clock period (100/10 MBPS)	t_{CYC}		40/400		ns
TX_CLK duty cycle, t_{PWH}/t_{CYC}		45	50	55	%
Out delay from TX_CLK	t_D	2		25	ns

9.4 Audio interfaces

9.4.1 Enhanced Serial Audio Interface (ESAI) Timing Parameters

The ESAI consists of independent transmitter and receiver sections, each section with its own clock generator. The following table shows the interface timing values.

Table 44. Enhanced Serial Audio Interface (ESAI) Timing

No	Characteristics	Symbol	Min	Max	Condition[1]	Unit
1	Clock cycle[2]	t_{SSICC}	30.0 (4 × T_c)	— —	master	ns
2	Clock high period: • master • slave	— —	6 (2 × T_c – 9.0) 15 (2 × T_c)	— —	— —	ns
3	Clock low period: • master • slave	— —	6 (2 × T_c – 9.0) 15 (2 × T_c)	— —	— —	ns
4	FSR Input and Data Input setup time before SCKR (SCK in synchronous mode) falling edge	— —	6 15	— —	Slave Master	ns
5	FSR Input and Data Input hold time after SCKR falling edge	— —	2 0	— —	Slave Master	ns
6	SCKT rising edge to FST out and Data out valid	— —	— —	15 6	Slave Master	ns
7	SCKT rising edge to FST out and Data out hold	— —	— —	0 0	Slave Master	ns
8	FST input setup time before SCKT falling edge	— —	6 15	— —	Slave Master	ns
9	FST input hold time after SCKT falling edge	— —	2 0	— —	Slave Master	ns
10	HCKR/HCKT clock cycle	—	15 (2 x T_C)	—	—	ns
11	HCKT input rising edge to SCKT output	—	—	18.0	—	ns
12	HCKR input rising edge to SCKR output	—	—	18.0	—	ns

1. SCKT(SCKT pin) = transmit clock SCKR(SCKR pin) = receive clock FST(FST pin) = transmit frame sync FSR(FSR pin) = receive frame sync HCKT(HCKT pin) = transmit high frequency clock HCKR(HCKR pin) = receive high frequency clock
2. For the internal clock, the external clock cycle is defined by Icyc and the ESAI control register.

9.4.2 SPDIF Timing Parameters

The Sony/Philips Digital Interconnect Format (SPDIF) data is sent using the bi-phase marking code. When encoding, the SPDIF data signal is modulated by a clock that is twice the bit rate of the data signal. Table and Figure below show SPDIF timing parameters for the Sony/Philips Digital Interconnect Format (SPDIF), including the timing of the modulating Rx clock (SRCK) for SPDIF in Rx mode and the timing of the modulating Tx clock (STCLK) for SPDIF in Tx mode.

Table 45. SPDIF Timing Parameters

Characteristic	Symbol	Timing Parameter Range		Unit
		Min	Max	
SPDIFIN Skew: asynchronous inputs, no specs apply			0.7	ns
SPDIFOUT output (Load = 50pf) • Skew • Transition rising • Transition falling			• 1.5 • 24.2 • 31.3	ns
SPDIFOUT1 output (Load = 30pf) - Skew			1.5	ns
• Transition rising • Transition falling		Refer Table 21		
Modulating Rx clock (SRCK) period	srckp	40		ns
SRCK high period	srckph	16		ns
SRCK low period	srckpl	16		ns
Modulating Tx clock (STCLK) period	stclkp	40		ns
STCLK high period	stclkph	16		ns
STCLK low period	stclkpl	16		ns

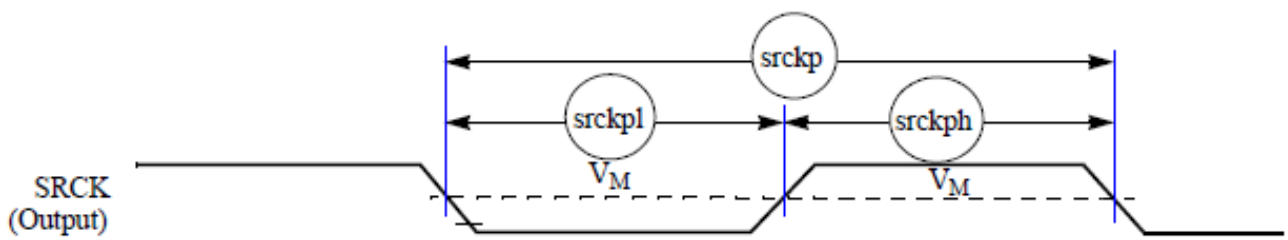


Figure 26. SRCK Timing Diagram

9.5 Memory interfaces

9.5.1 QuadSPI timing

- All data is based on a negative edge data launch from the device and a negative edge data capture, as shown in the timing diagrams in this section. This corresponds to the N/1 sample point as shown in the reference manual QSPI section "Internal Sampling of Serial Flash Input Data."
- Measurements are with a load of 35 pF on output pins. I/P Slew : 1ns
- Timings assume a setting of 0x0000_000x for QSPI_SMPR register (see the reference manual for details).

SDR mode

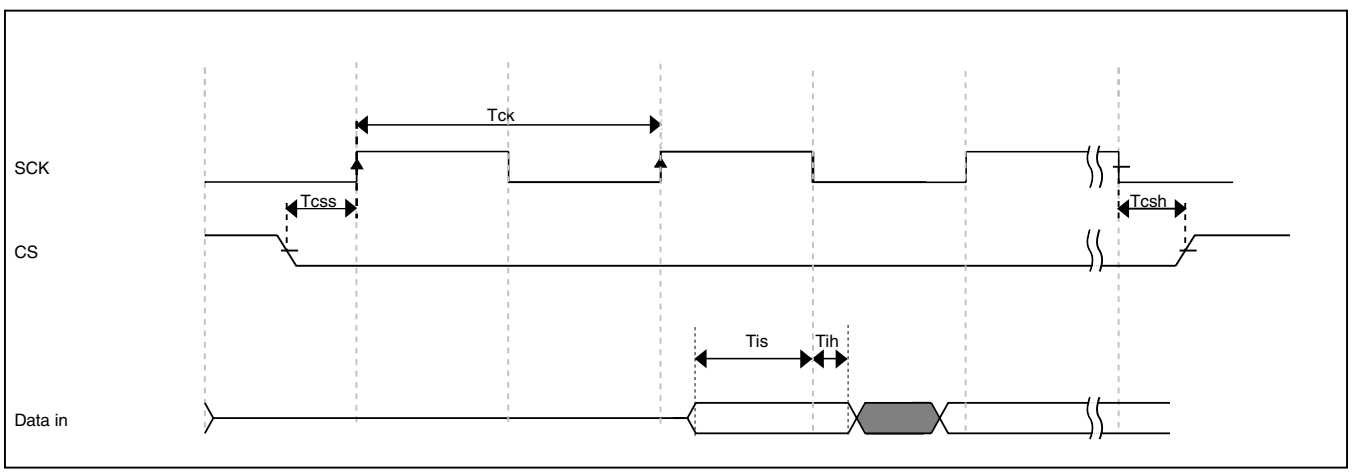


Figure 30. QuadSPI Input/Read timing (SDR mode)

Table 48. QuadSPI Input/Read timing (SDR mode)

Symbol	Parameter	Value		Unit
		Min	Max	
T_{is}	Setup time for incoming data	4.5	—	ns
T_{ih}	Hold time requirement for incoming data	0	—	ns

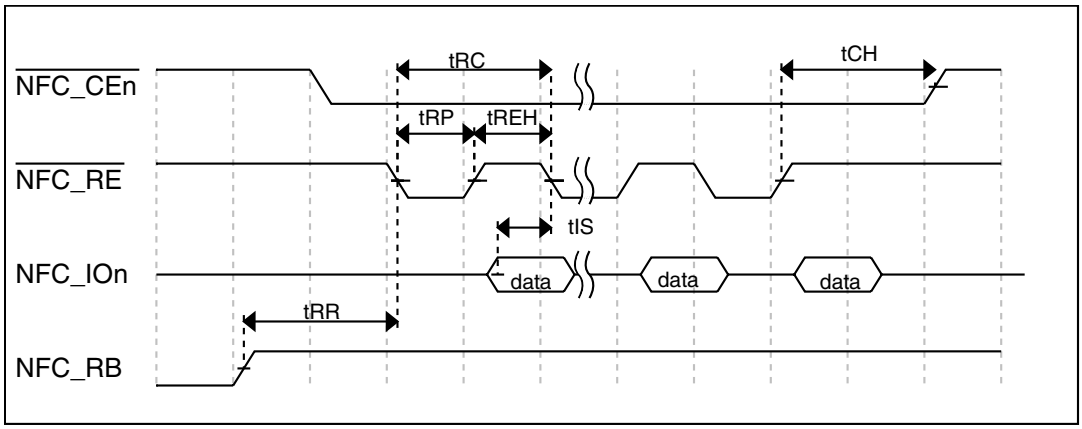


Figure 38. Read data latch cycle timing in fast mode

9.5.3 FlexBus timing specifications

This section provides FlexBus timing parameters. All processor bus timings are synchronous; input setup/hold and output delay are given in respect to the rising edge of a reference clock, FB_CLK. The FB_CLK frequency may be the same as the internal system bus frequency.

The following timing numbers indicate when data is latched or driven onto the external bus, relative to the FlexBus output clock (FB_CLK). All other timing relationships can be derived from these values.

All FlexBus signals use pad type pad_fsr. The following timing specifications assume a pad slew rate setting of 11 and a load of 50 pF[3]

Table 53. FlexBus timing specifications

Num	Characteristic	Min	Max	Unit
	Frequency of operation	—	83[1] (with Wait state)	MHz
			57[2] without Wait state , -1	
FB1	Clock Period	12	—	ns
FB4	Input setup	10.6	—	ns
FB5	Input hold	0	—	ns
FB2	Output valid	—	6.4	ns
FB3	Output hold	0	—	ns

1. Freq = 1000/(11+ access time of external memory+ trace delay for clk and data)
2. Freq = 1000/(17+access time of external memory)

3. These timing parameters are specified assuming maximum operating frequency and the fastest pad slew rate setting (11).

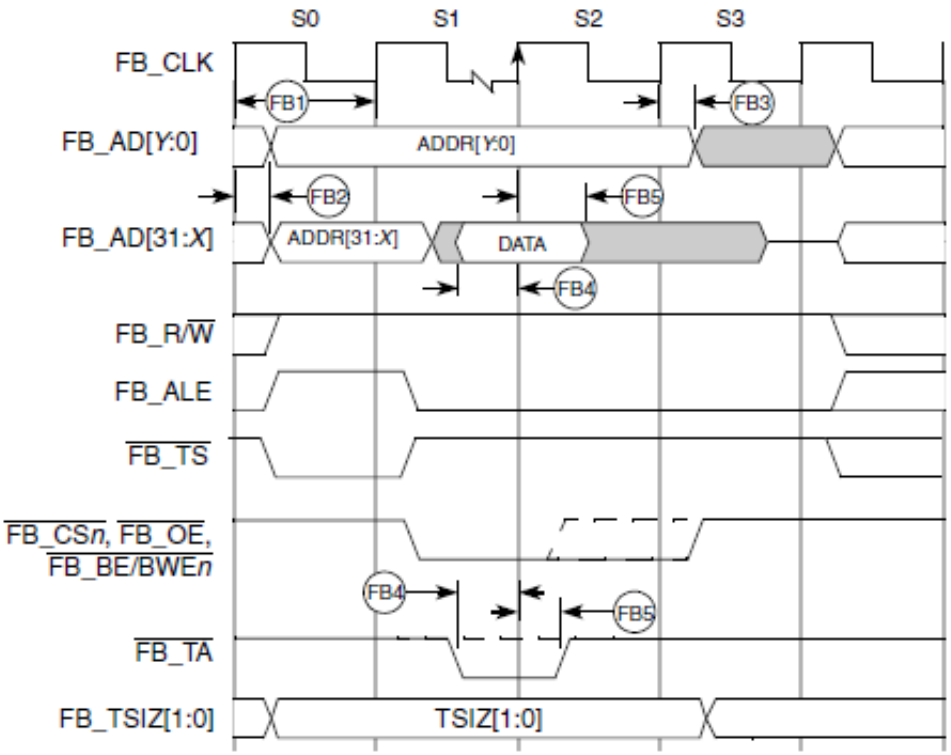


Figure 39. FlexBus read timing

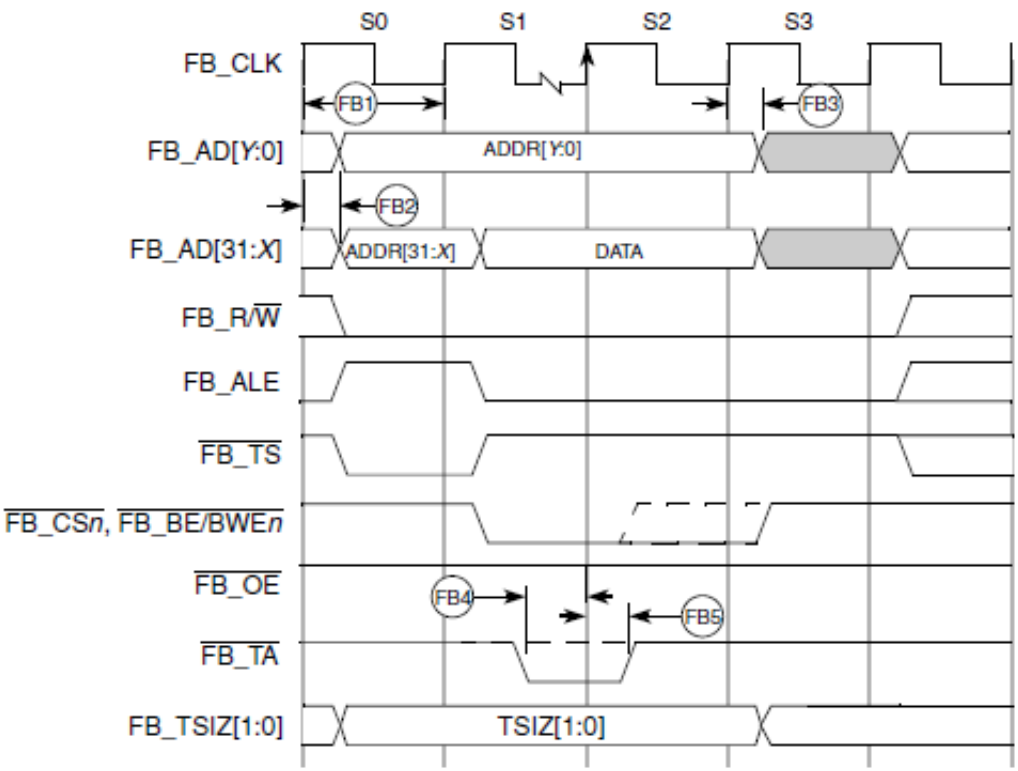


Figure 40. FlexBus write timing

9.5.4.3 DDR3 Write cycle

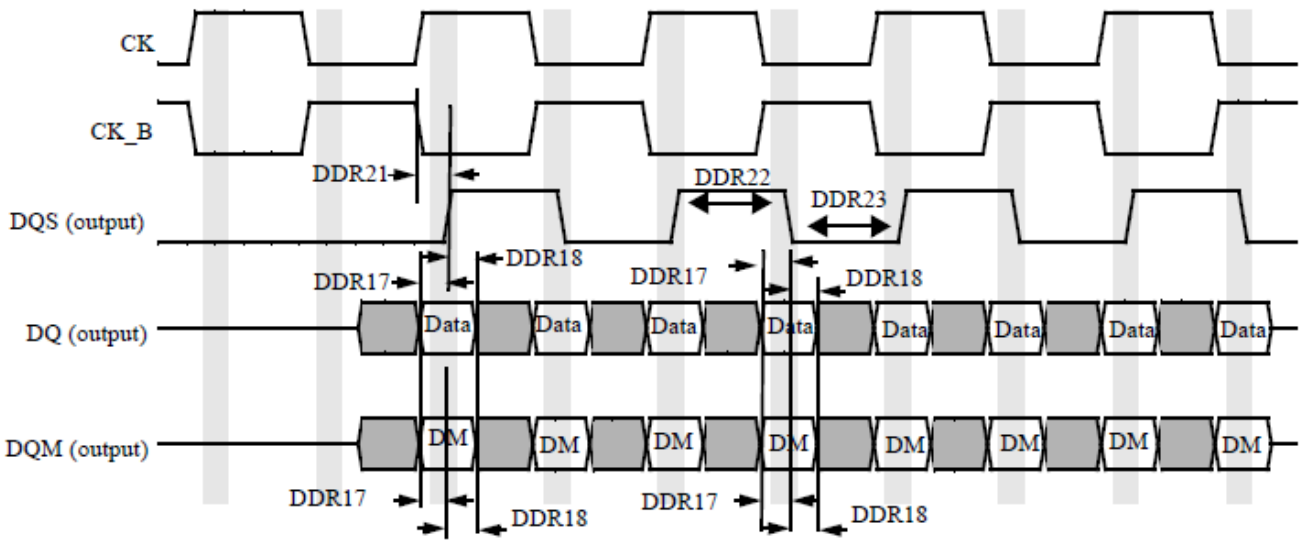


Figure 43. DDR3 Write cycle

Table 56. DDR3 Write cycle

ID	Parameter	Symbol	CK = 400 MHz		Unit
			Min	Max	
DDR17	DQ and DQM setup time to DQS (differential strobe)	tDS	240	—	ps
DDR18	DQ and DQM hold time to DQS (differential strobe)	tDH	215	—	ps
DDR21	DQS latching rising transitions to associated clock edges	tDQSS	-0.25	+0.25	tCK
DDR22	DQS high level width	tDQSH	0.45	0.55	tCK
DDR22	DQS low level width	tDQSL	0.45	0.55	tCK

NOTE

To receive the reported setup and hold values, write calibration should be performed in order to locate the DQS in the middle of DQ window.

NOTE

All measurements are in reference to Vref level.

NOTE

Measurements were done using balanced load and 25 ohms resistor from outputs to VDD_REF.

Board type	Symbol	Description	176LQFP	Unit	Notes
		to package top (natural convection)			

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance
2. Per JEDEC JESD51-2 with the single layer board (JESD51-3) horizontal
3. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

Board type	Symbol	Description	364 MAPBGA	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	45	°C/W	1, 2
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	28	°C/W	1, 3
Single-layer (1s)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./ min. air speed)	37	°C/W	1,3
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./ min. air speed)	24	°C/W	1,3
—	$R_{\theta JB}$	Thermal resistance, junction to board	17	°C/W	4
—	$R_{\theta JC}$	Thermal resistance, junction to case	10	°C/W	5
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	2	°C/W	6

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

364 MAP BGA	176 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
Y11	64	USB0_ VBUS_ DETECT			USB0_ VBUS_ DETECT							
Y9	—	USB1_GND			USB1_GND							
W9	—	USB1_DP			USB1_DP							
V9	—	USB1_DM			USB1_DM							
W10	—	USB1_VBUS			USB1_VBUS							
U9	—	USB1_ VBUS_ DETECT			USB1_ VBUS_ DETECT							
L4	8	PTC0		PTC0	RMII0_MDC/ MII0_MDC	FTM1CH0	SPI0_PCS3	ESAI_SCKT	SDHC0_CLK	VIU_DATA0	RCON18	
L5	9	PTC1		PTC1	RMII0_MDIO/ MII0_MDC	FTM1CH1	SPI0_PCS2	ESAI_FST	SDHC0_CMD	VIU_DATA1	RCON19	
M5	11	PTC2		PTC2	RMII0_CRS_ DV	SCI1_TX		ESAI_SDO0	SDHC0_ DAT0	VIU_DATA2	RCON20	
M3	12	PTC3		PTC3	RMII0_RXD1/ MII0_RXD[1]	SCI1_RX		ESAI_SDO1	SDHC0_ DAT1	VIU_DATA3	DCU0_R0	
L2	14	PTC4		PTC4	RMII0_RXD0/ MII0_RXD[0]	SCI1_RTS	SPI1_PCS1	ESAI_SDO2/ ESAI_SDI3	SDHC0_ DAT2	VIU_DATA4	DCU0_R1	
M1	15	PTC5		PTC5	RMII0_RXER/ MII0_RXER	SCI1_CTS	SPI1_PCS0	ESAI_SDO3/ ESAI_SDI2	SDHC0_ DAT3	VIU_DATA5	DCU0_G0	
N1	16	PTC6		PTC6	RMII0_TXD1/ MII0_TXD[1]		SPI1_SIN	ESAI_SDO5/ ESAI_SDI0	SDHC0_WP	VIU_DATA6	DCU0_G1	
N2	17	PTC7		PTC7	RMII0_TXD0/ MII0_TXD[0]		SPI1_SOUT	ESAI_SDO4/ ESAI_SDI1		VIU_DATA7	DCU0_B0	
N4	18	PTC8		PTC8	RMII0_TXEN/ MII0_TXEN		SPI1_SCK			VIU_DATA8	DCU0_B1	
T15	77	PTC9		PTC9	RMII1_MDC		ESAI_SCKT			MLBCLK		
U15	78	PTC10		PTC10	RMII1_MDIO		ESAI_FST			MLBSIGNAL		
P4	20	PTC11		PTC11	RMII1_CRS_ DV		ESAI_SDO0			MLBDATA		
P3	21	PTC12		PTC12	RMII1_RXD1		ESAI_SDO1		SAI2_TX_ BCLK			
P1	23	PTC13		PTC13	RMII1_RXD0		ESAI_SDO2/ ESAI_SDI3		SAI2_RX_ BCLK			
R1	26	PTC14		PTC14	RMII1_RXER		ESAI_SDO3/ ESAI_SDI2	SCI5_TX	SAI2_RX_ DATA	ADC0_SE6		
P2	27	PTC15		PTC15	RMII1_TXD1		ESAI_SDI0	SCI5_RX	SAI2_TX_ DATA	ADC0_SE7		
R3	29	PTC16		PTC16	RMII1_TXD0		ESAI_SDO4/ ESAI_SDI1	SCI5_RTS	SAI2_RX_ SYNC	ADC1_SE6		
R4	28	PTC17		PTC17	RMII1_TXEN		ADC1_SE7	SCI5_CTS	SAI2_TX_ SYNC	USB1_SOF_ PULSE		
B10	—	DDR_A[15]			DDR_A15							
D9	—	DDR_A[14]			DDR_A14							

364 MAP BGA	176 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
J4	—	DDR_DQM[0]			DDR_DQM0							
E1	—	DDR_DQS[1]			DDR_DQS1							
D3	—	DDR_DQS[0]			DDR_DQS0							
F1	—	DDR_DQS_b[1]			DDR_DQS_b1							
E3	—	DDR_DQS_b[0]			DDR_DQS_b0							
A4	—	DDR_RAS_b			DDR_RAS_b							
C6	—	DDR_WE_b			DDR_WE_b							
C4	—	DDR_ODT[0]			DDR_ODT0							
B1	—	DDR_ODT[1]			DDR_ODT1							
G5	—	DDR_VREF			DDR_VREF							
A3	—	DDR_ZQ			DDR_ZQ							
D6	—	DDR_RESET			DDR_RESET							
J20	—	PTD31		PTD31	FB_AD31	NF_IO15		FTM3_CH0	SPI2_PCS1			
H20	—	PTD30		PTD30	FB_AD30	NF_IO14		FTM3_CH1	SPI2_PCS0			
H18	—	PTD29		PTD29	FB_AD29	NF_IO13		FTM3_CH2	SPI2_SIN			
H17	—	PTD28		PTD28	FB_AD28	NF_IO12	I2C2_SCL	FTM3_CH3	SPI2_SOUT			
H16	—	PTD27		PTD27	FB_AD27	NF_IO11	I2C2_SDA	FTM3_CH4	SPI2_SCK			
G16	—	PTD26		PTD26	FB_AD26	NF_IO10		FTM3_CH5	SDHC1_WP			
G18	—	PTD25		PTD25	FB_AD25	NF_IO9		FTM3_CH6				
G19	—	PTD24		PTD24	FB_AD24	NF_IO8		FTM3_CH7				
G20	124	PTD23		PTD23/ MII0_ RXDATA[3]	FB_AD23	NF_IO7	FTM2CH0	ENET0_ 1588_TMR0	SDHC0_ DAT4	SCI2_TX	DCU1_R3	
F20	126	PTD22		PTD22/ MII0_ RXDATA[2]	FB_AD22	NF_IO6	FTM2CH1	ENET0_ 1588_TMR1	SDHC0_ DAT5	SCI2_RX	DCU1_R4	
F19	128	PTD21		PTD21/ MII0_CRS	FB_AD21	NF_IO5		ENET0_ 1588_TMR2	SDHC0_ DAT6	SCI2_RTS	DCU1_R5	
F17	129	PTD20		PTD20/ MII0_COL	FB_AD20	NF_IO4		ENET0_ 1588_TMR3	SDHC0_ DAT7	SCI2_CTS	DCU1_R0	
F16	130	PTD19		PTD19	FB_AD19	NF_IO3	ESAI_SCKR	I2C0_SCL	FTM2_QD_ PHA	MII0_ TXDATA[3]	DCU1_R1	
E18	131	PTD18		PTD18	FB_AD18	NF_IO2	ESAI_FSR	I2C0_SDA	FTM2_QD_ PHB	MII0_ TXDATA[2]	DCU1_G0	
E20	132	PTD17		PTD17	FB_AD17	NF_IO1	ESAI_HCKR	I2C1_SCL		MII0_TXERR	DCU1_G1	
D20	133	PTD16		PTD16	FB_AD16	NF_IO0	ESAI_HCKT	I2C1_SDA			DCU1_G2	
Y17	86	PTD0		PTD0	QSPI0_A_ SCK	SCI2_TX		FB_AD15	SPDIF_ EXTCLK			
Y18	87	PTD1		PTD1	QSPI0_A_ CS0	SCI2_RX		FB_AD14	SPDIF_IN1			
V18	88	PTD2		PTD2	QSPI0_A_ DATA3	SCI2_RTS	SPI1_PCS3	FB_AD13	SPDIF_OUT1			

Table 75. RGPIO versus Pins (continued)

RGPIO	In GPIO module	Corresponding Pin on the chip	IOMUX register name	IOMUX register address
RGPIO[118]	PORT3[22]	PTE13	IOMUXC_PTE13	400481D8
RGPIO[119]	PORT3[23]	PTE14	IOMUXC_PTE14	400481DC
RGPIO[120]	PORT3[24]	PTE15	IOMUXC_PTE15	400481E0
RGPIO[121]	PORT3[25]	PTE16	IOMUXC_PTE16	400481E4
RGPIO[122]	PORT3[26]	PTE17	IOMUXC_PTE17	400481E8
RGPIO[123]	PORT3[27]	PTE18	IOMUXC_PTE18	400481EC
RGPIO[124]	PORT3[28]	PTE19	IOMUXC_PTE19	400481F0
RGPIO[125]	PORT3[29]	PTE20	IOMUXC_PTE20	400481F4
RGPIO[126]	PORT3[30]	PTE21	IOMUXC_PTE21	400481F8
RGPIO[127]	PORT3[31]	PTE22	IOMUXC_PTE22	400481FC
RGPIO[128]	PORT4[0]	PTE23	IOMUXC_PTE23	40048200
RGPIO[129]	PORT4[1]	PTE24	IOMUXC_PTE24	40048204
RGPIO[130]	PORT4[2]	PTE25	IOMUXC_PTE25	40048208
RGPIO[131]	PORT4[3]	PTE26	IOMUXC_PTE26	4004820C
RGPIO[132]	PORT4[4]	PTE27	IOMUXC_PTE27	40048210
RGPIO[133]	PORT4[5]	PTE28	IOMUXC_PTE28	40048214
RGPIO[134]	PORT4[6]	PTA7	IOMUXC_PTA7	40048218

12.2.2 Special Signal

Table 76. Special Signal Considerations

Special Signal	Comments
DDR_VREF	When using DDR_VREF with DDR I/O, the nominal reference voltage must be half of the SDRAMC_VDD1P5 supply. The user must tie DDR_VREF to a precision external resistor divider. Shunt each resistor with a closely-mounted 0.1 µF capacitor.
DDR_ZQ	DRAM calibration resistor 240 Ω 1% used as reference during DRAM output buffer driver calibration should be connected between this pad and GND
DECAP_V25_LDO_OUT	DCAP_V25_LDO_OUT can be tied to SDRAMC_VDD2P5 to provide the predriver supply for the DDR I/O segment. SDRAMC_VDD1P5 requires an external regulated supply. If SDRAMC_VDD2P5 uses an external 2.5V supply, do NOT tie it to DCAP_V25_LDO_OUT.
EXT_POR, TEST	Factory use only, tie to ground..
EXT_TAMPER0, EXT_TAMPER1, EXT_TAMPER2, EXT_TAMPER3, EXT_TAMPER4, EXT_TAMPER5	Security related tamper detection inputs, if not in use they must be tied to ground.
FA_VDD	Factory use only, tie to VDD.

Table continues on the next page...

Table 79. Revision History (continued)

Rev. No.	Date	Substantial Changes
		Updated Power supply diagram Updated AC electrical specification of following modules: DCU, 12-bit DAC, Ethernet, Enhanced Serial Audio Interface (ESAI), SAI/I2S, Flexbus, MLB, DSPI, 24MHz External Oscillator, JTAG, Debug, ESAI, QSPI Updated Thermal Attributes for 364 MAPBGA Updated Freescale document number for 176-pin LQFP and 364 MAPBGA Updated VREG specifications Added WBREG specifications Updated Recommended operating conditions table Updated DAC INL and DNL charts Updated Pinouts
Rev 4.1	12/2012	Editorial updates: Removed instances of VF7xx and VF4xx.
Rev 5	April 2013	• Removed references to VF1xxR and refernces to F100 and 144 LQFP and 256 MAPBGA • Replaced references to Auto and IMM by R-series and F-series respectively • In the feature list, the ARM Core frequency changed to 500 MHz for F-series • In the feature list, changed the DRAM controller frequency • Updated Part Nummbering format • Clarified the Fields table as per Marketing • Sample numbers updated • From the VREG electrical specifications tables, deleted pre-trimming rows and comments • .In the HPREG electrical characteristics table, add footnote on maximum Output Current Capacity • In the ULPREG electrical characteristics table, clarified max value of Output voltage @ no load and min value of Output voltage @ full load • In the WBREG electrical characteristics table, clarified max value of Output voltage @ no load and min value of Output voltage @ full load

Table continues on the next page...

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