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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A5
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	Multimedia; NEON™ MPE
RAM Controllers	LPDDR2, DDR3, DRAM
Graphics Acceleration	Yes
Display & Interface Controllers	DCU, GPU, LCD, VideoADC, VIU
Ethernet	10/100Mbps (2)
SATA	-
USB	USB 2.0 OTG + PHY (1)
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	ARM TZ, CAAM, HAB, RTIC, Secure JTAG, SNVS, Tamper, TZ ASC, TZ WDOG
Package / Case	364-LFBGA
Supplier Device Package	364-LFBGA (17x17)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mvf50ns151cmk40

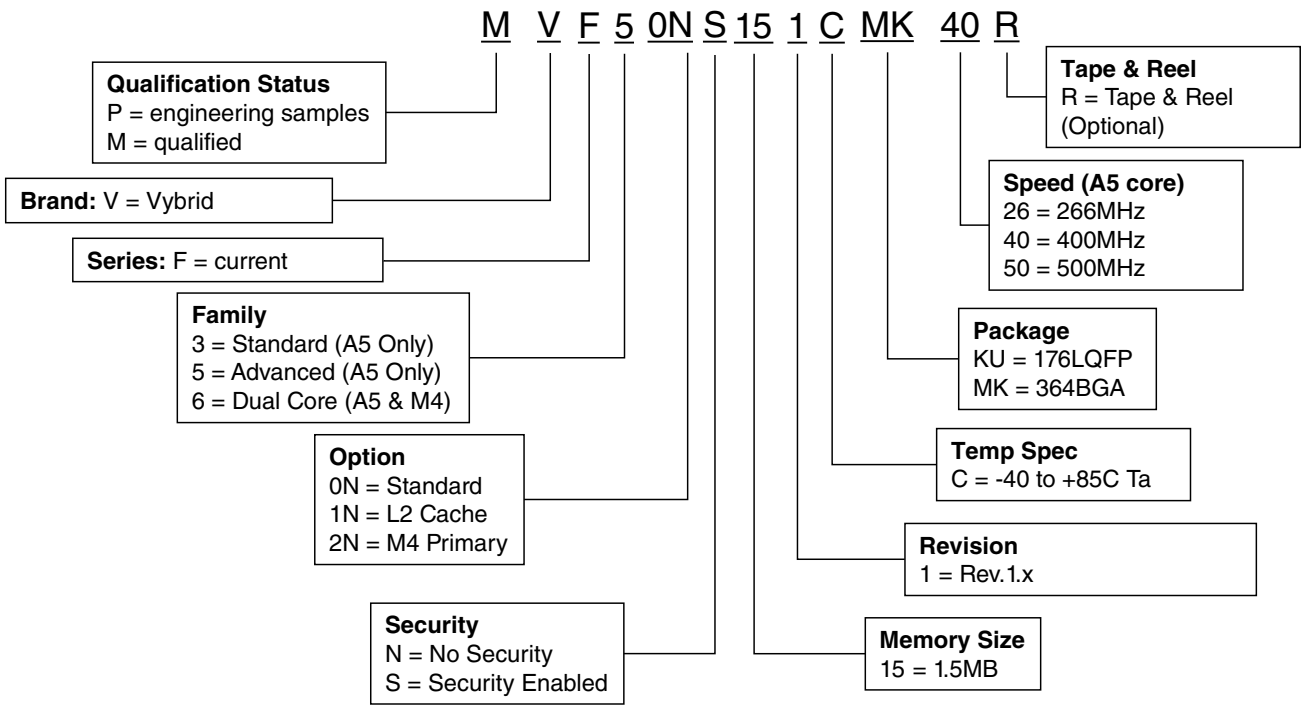


Figure 1. Part Number Format

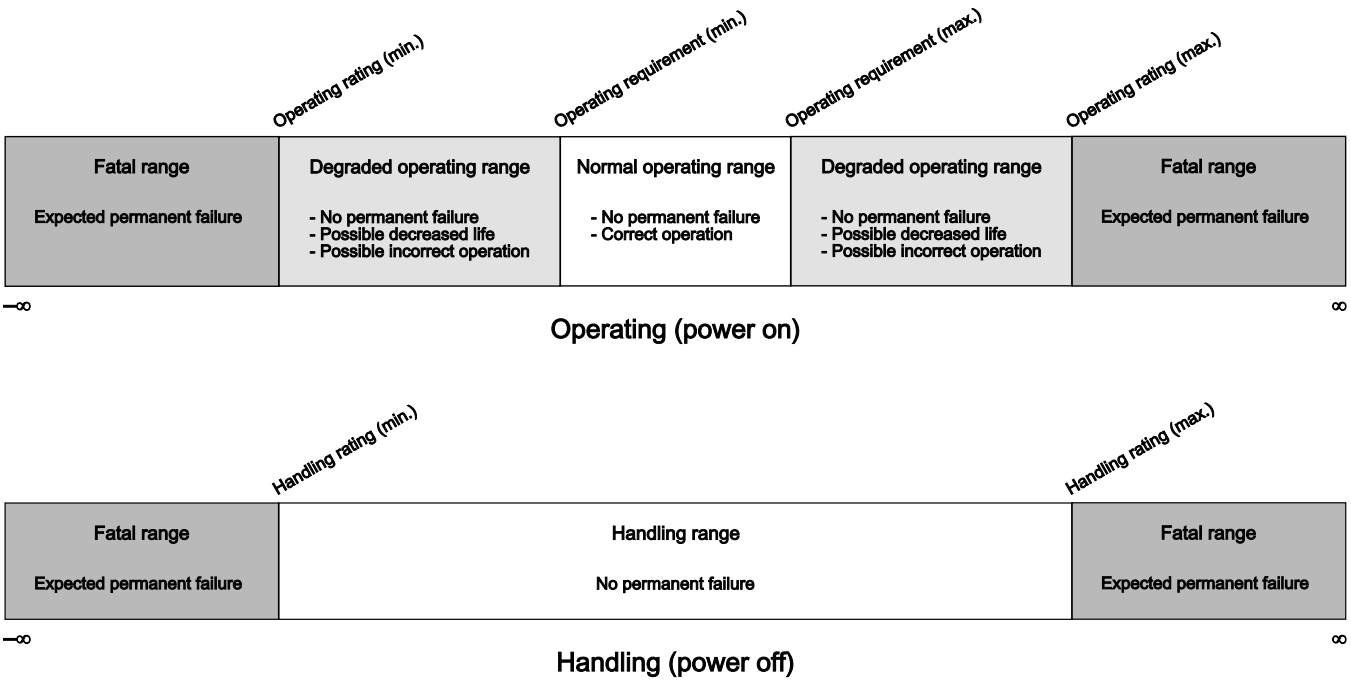
2.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
Q	Qualification status	• P = Engineering samples • M = Qualified
B	Brand	• V = Vybrid
S	Series	• F = current
F	Family	• 3 = Standard (A5 Only) • 5 = Advanced (A5 Only) • 6 = Dual Core (A5 & M4)
O	Option	• 0N = Standard • 1N = L2 Cache • 2N = M4 Primary
S	Security	• N = No Security • S = Security Enabled
MM	Memory size	• 15 = 1.5 MB

Table continues on the next page...

3.6 Relationship between ratings and operating requirements



3.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

3.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:

- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.

4 Handling ratings

4.1 ESD Handling Ratings Table [JEDEC]

Symbol	Description	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model	2000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model	Corner pins: 750 Other pins: 500	V	2

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.

4.2 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	–55	150	°C	1
T_{SDR}	Solder temperature, lead-free	—	260	°C	2
	Solder temperature, leaded	—	245		

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

4.3 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

6.2.3.3 LDO_3P0

Table 14. LDO_3P0 parameters

Specification	Min	Typ	Max	Unit	Comments
Input OTG VBUS Supply	4.4		5.25	V	
Input HOST VBUS Supply	4.4		5.25	V	
VDD3P0_OUT	2.9	3.0	3.1	V	Regulator output at default setting
I_out	-		50	mA	500 mV drop-out voltage
Regulator output programming range	2.625		3.4	V	Programmable in 25mV steps
[P:][C:] Brownout Voltage	2.75	2.85		V	
Brownout offset step	0	-	175	mV	Programmable in 25mV steps
Minimum external decoupling capacitor	1	-	-	µF	low ESR

NOTE

These values are with Anadig_REG_3P0[ENABLE_ILIMIT]= 0 and Anadig_REG_3P0[ENABLE_LINREG]= 1. It is required to set these values before using USB.

6.2.4 Power consumption operating behaviors

Table 15. Power consumption operating behaviors

Symbol	Description	Typ.[1]	Max.[2]	Unit	Notes
I_{DD_RUN}	Run mode current — All functionalities of the chip available	400	850	mA	
I_{DD_WAIT}	Wait mode high frequency current at 3.3 V ± 10%	80	500	mA	3
I_{DD_LPRUN}	Low-power run mode current at 3.3 V ± 10%, 24MHz operation, PLL Bypass.	13	325	mA	4
I_{DD_ULPRUN}	Ultra-low-power run mode current at 3.3 V ± 10%	12	395	mA	5
I_{DD_STOP}	Stop mode current at 3.3 V ± 10%	7	300	mA	6
I_{DD_LPS3}	Low-power stop3 mode current at 3.3 V ± 10%	300	1300	uA	7
I_{DD_LPS2}	Low-power stop 2 mode current at 3.3 V ± 10%	50	875	uA	8
I_{DD_VBAT}	Battery backup mode	5	45	uA	9

1. The Typ numbers represent the average value taken from a matrix lot of parts across normal process variation at ambient temperature.

Table 30. Recommended operating conditions (continued)

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
VSSA33_AFE	Ground supply of AFE (Video ADC)			0		V
VSS12_AFE	Ground supply for AFE (Video ADC)			0		V
SDRAMC_VDD1P5	LPDDR2	External CAP 10uF	1.142	1.2	1.26	V
SDRAMC_VDD1P5	DDR3	External CAP 10uF	1.425	1.5	1.575	V
SDRAMC_VDD2P5	2.5V DDR pre-drive supply DD2P5_LDO_OUT	External CAP 10uF	2.25	2.5	2.75	V
-	Maximum power supply ramp rate (Slew limit for power-up)		-		0.1	V/us

1. For customer applications, this is governed by ballast output which is controlled by the device and appropriate voltage ranges are maintained.

8.5 Recommended Connections for Unused Analog Interfaces

NOTE

There are two options to handle unused power pins:

1. Connect all unused supplies to their respective voltage. To save the power, do not enable the module and/or do not enable clock gate to the module.
2. Keep all unused supplies floating.

If pin is shared by several peripheral, then all peripherals connected to multiplexer have to be powered. For example: if pin is shared by GPIO and ADC input and GPIO functionality is used, then ADC has to be powered due to internal structure of the multiplexer. Keep unused input signals grounded if power pins are powered. Keep unused input signals floating if power pins are floating. Keep unused output signals floating.

Module	Name	Recommendation if Unused
ADC	VDDA33_ADC	3.3V or float (Note: Powers both ADC and DAC)
	VREFH_ADC, VREFL_ADC	VREFH_ADC same as VDDA33_ADC VREFL_ADC ground or float
	ADC0SE8, ADC0SE9, ADC1SE8, ADC1SE9	Ground or float
CCM	LVDS0P, LVDS0N	Float
DAC	DACO0, DACO1	Float

Table continues on the next page...

Table 31. 12-bit ADC Operating Conditions (continued)

Characteristic	Conditions	Symb	Min	Typ [1]	Max	Unit	Comment
Analog Source Resistance	12 bit mode f_{ADCK} = 40MHz ADLSMP=0, ADSTS=10, ADHSC=1	R_{AS}	-	-	1	kohms	T_{samp}=150 ns
R_{AS} depends on Sample Time Setting (ADLSMP, ADSTS) and ADC Power Mode (ADHSC, ADLPC). See charts for Minimum Sample Time vs R_{AS}							
ADC Conversion Clock Frequency	ADLPC=0, ADHSC=1 12 bit mode	f_{ADCK}	4	-	40	MHz	-
	ADLPC=0, ADHSC=0 12 bit mode		4	-	30	MHz	-
	ADLPC=1, ADHSC=0 12 bit mode		4	-	20	MHz	-

1. Typical values assume VDDAD = 3.3 V, Temp = 25°C, f_{ADCK}=20 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
2. DC potential difference

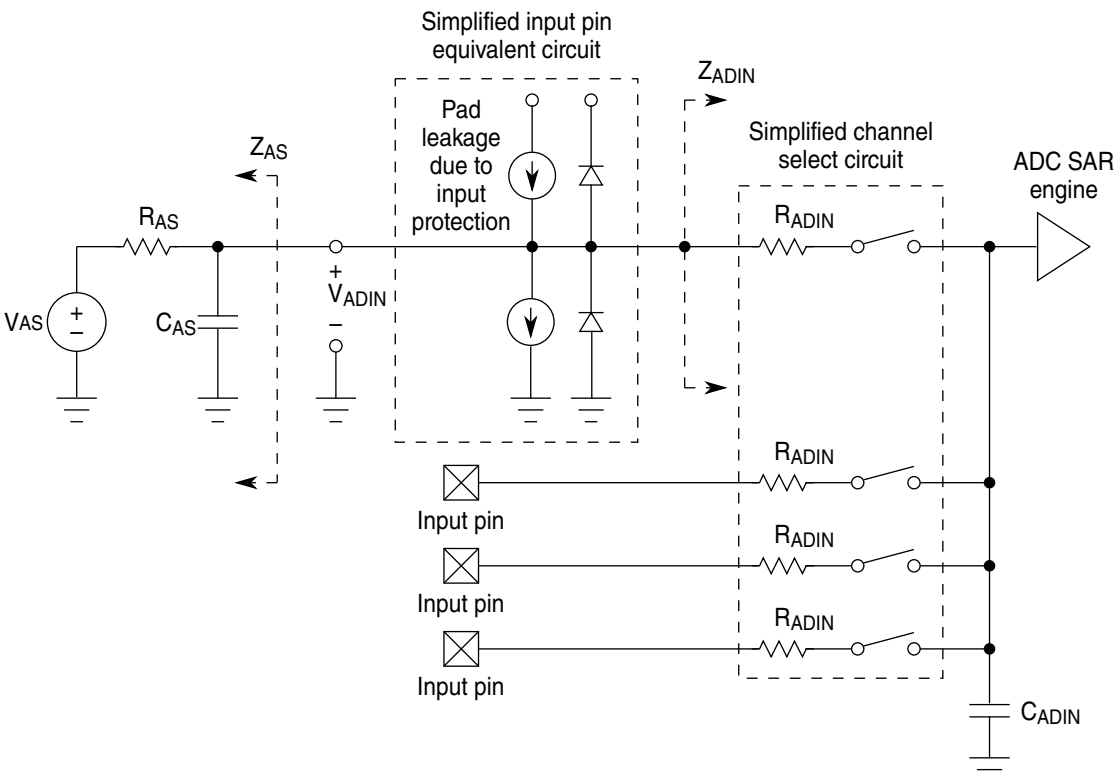


Figure 5. 12-bit ADC Input Impedance Equivalency Diagram

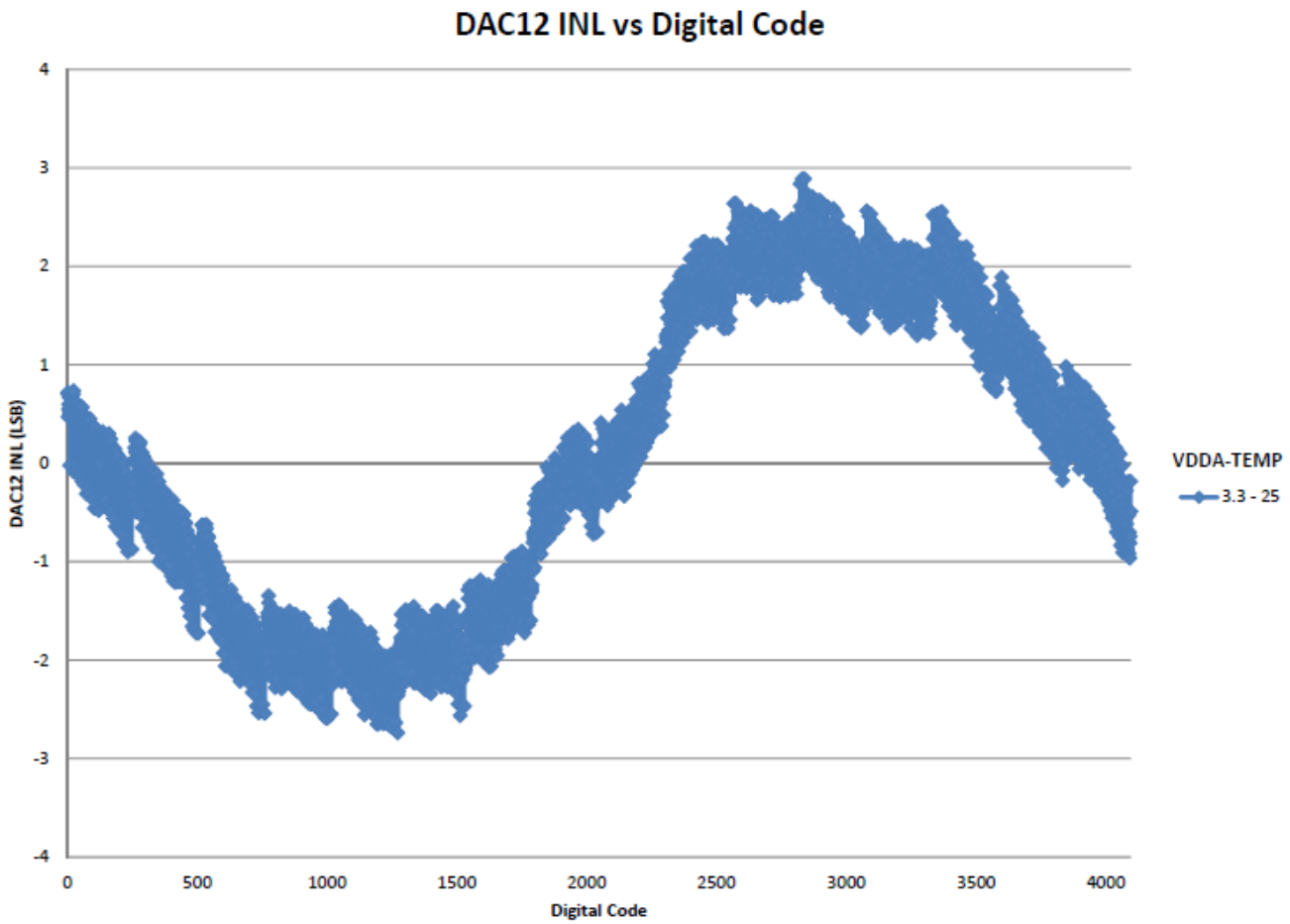


Figure 9. INL error vs. digital code

9.4.2 SPDIF Timing Parameters

The Sony/Philips Digital Interconnect Format (SPDIF) data is sent using the bi-phase marking code. When encoding, the SPDIF data signal is modulated by a clock that is twice the bit rate of the data signal. Table and Figure below show SPDIF timing parameters for the Sony/Philips Digital Interconnect Format (SPDIF), including the timing of the modulating Rx clock (SRCK) for SPDIF in Rx mode and the timing of the modulating Tx clock (STCLK) for SPDIF in Tx mode.

Table 45. SPDIF Timing Parameters

Characteristic	Symbol	Timing Parameter Range		Unit
		Min	Max	
SPDIFIN Skew: asynchronous inputs, no specs apply			0.7	ns
SPDIFOUT output (Load = 50pf) • Skew • Transition rising • Transition falling			• 1.5 • 24.2 • 31.3	ns
SPDIFOUT1 output (Load = 30pf) - Skew			1.5	ns
• Transition rising • Transition falling		Refer Table 21		
Modulating Rx clock (SRCK) period	srckp	40		ns
SRCK high period	srckph	16		ns
SRCK low period	srckpl	16		ns
Modulating Tx clock (STCLK) period	stclkp	40		ns
STCLK high period	stclkph	16		ns
STCLK low period	stclkpl	16		ns

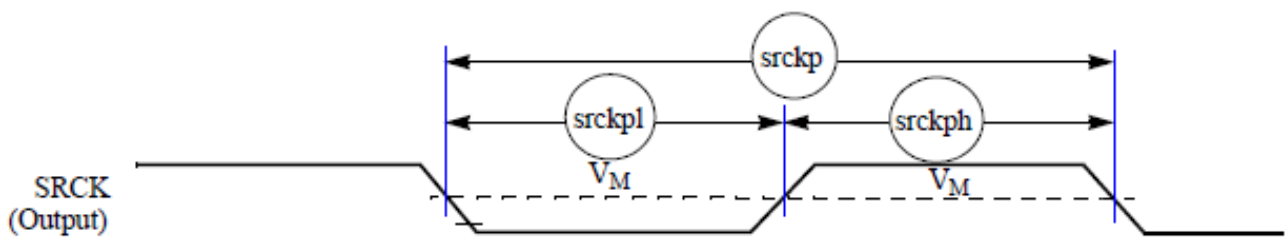


Figure 26. SRCK Timing Diagram

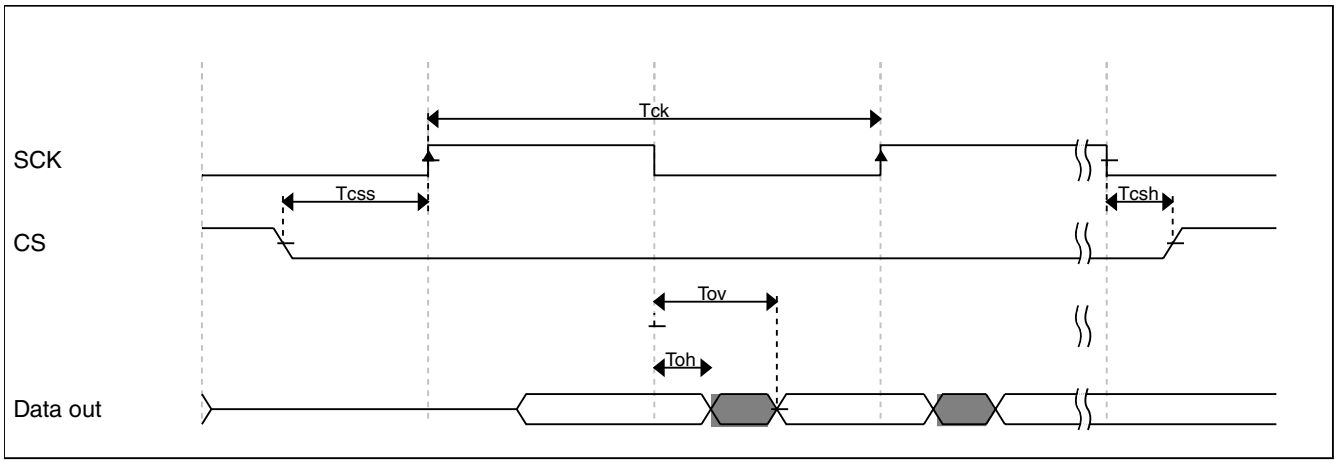


Figure 33. QuadSPI Output/Write timing (DDR mode)

Table 51. QuadSPI Output/Write timing (DDR mode)

Symbol	Parameter	Value		Unit
		Min	Max	
T_{ov}	Output Data Valid	—	3.2	ns
T_{oh}	Output Data Hold	0	—	ns
T_{ck}	SCK clock period	-	45	MHz
T_{css}	Chip select output setup time	3	-	Clk(sck)
T_{csh}	Chip select output hold time	3	-	Clk(sck)

9.5.2 NFC specifications

The NAND flash controller (NFC) implements the interface to standard NAND flash memory devices. This section describes the timing parameters of the NFC.

In the following table:

- T_H is the flash clock high time and
- T_L is flash clock low time,

which are defined as:

$T_{NFC} = T_H + T_L$

NOTE

Refer to the Reference Manual for further details on setting up the NFC clocks (CCM_CSCDR2[NFC_FRAC_DIV_EN + NFC_FRAC_DIV] and CCM_CSCDR3[NFC_PRE_DIV]).

9.5.4.2 DDR3 Read Cycle

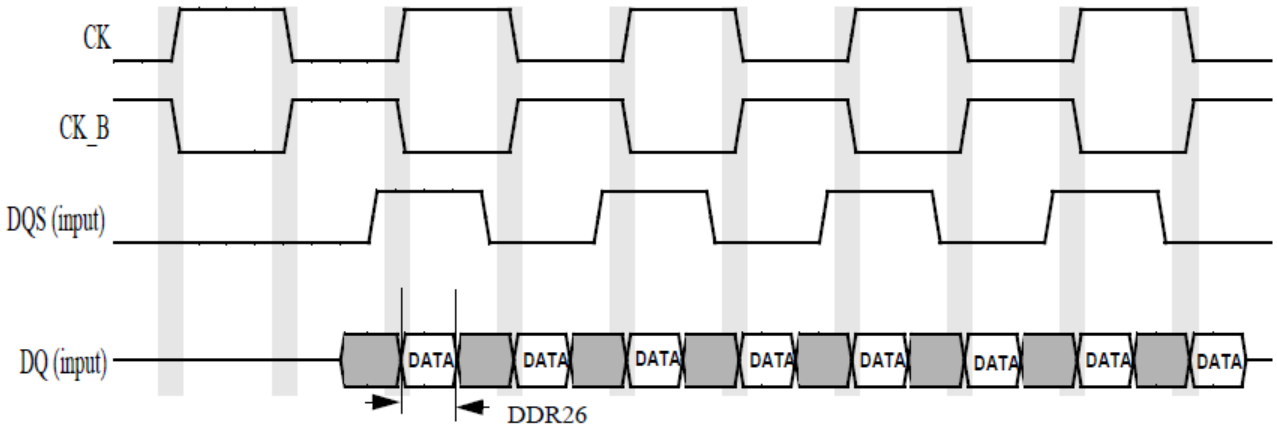


Figure 42. DDR3 Read Cycle

Table 55. DDR3 Read Cycle

ID	Parameter	Symbol	CK = 400 MHz		Unit
			Min	Max	
DDR26	Minimum required DQ valid window width	-	750	-	ps

NOTE

To receive the reported setup and hold values, read calibration should be performed in order to locate the DQS in the middle of DQ window.

NOTE

All measurements are in reference to Vref level.

NOTE

Measurements were done using balanced load and 25 ohms resistor from outputs to VDD_REF

9.6 Communication interfaces

9.6.1 DSPI timing specifications

Table 60. DSPI timing

No.	Symbol	Characteristic	Condition	Min	Max	Unit
1	t_{SCK}	SCK Cycle Time	—	t_{SYS} * 2	—	ns
4	t_{SDC}	SCK Clock Pulse Width	—	40%	60%	t_{SCK}
2	t_{CSC}	CS to SCK Delay	Master	16	—	ns
3	t_{ASC}	After SCK Delay	Master	16	—	ns
5	t_A	Slave Access Time (SS active to SOUT driven)	Slave	—	15	ns
6	t_{DI}	Slave Disable Time (SS inactive to SOUT High-Z or invalid)	Slave	—	10	ns
9	t_{SUI}	Data Setup Time for Inputs	Master	9	—	ns
			Slave	4	—	
10	t_{HI}	Data Hold Time for Inputs	Master	0	—	ns
			Slave	2	—	
11	t_{DV}	Data Valid (after SCK edge) for Outputs	Master	—	5	ns
			Slave	—	10	
12	t_{HO}	Data Hold Time for Outputs	Master	0	—	ns
			Slave	0	—	

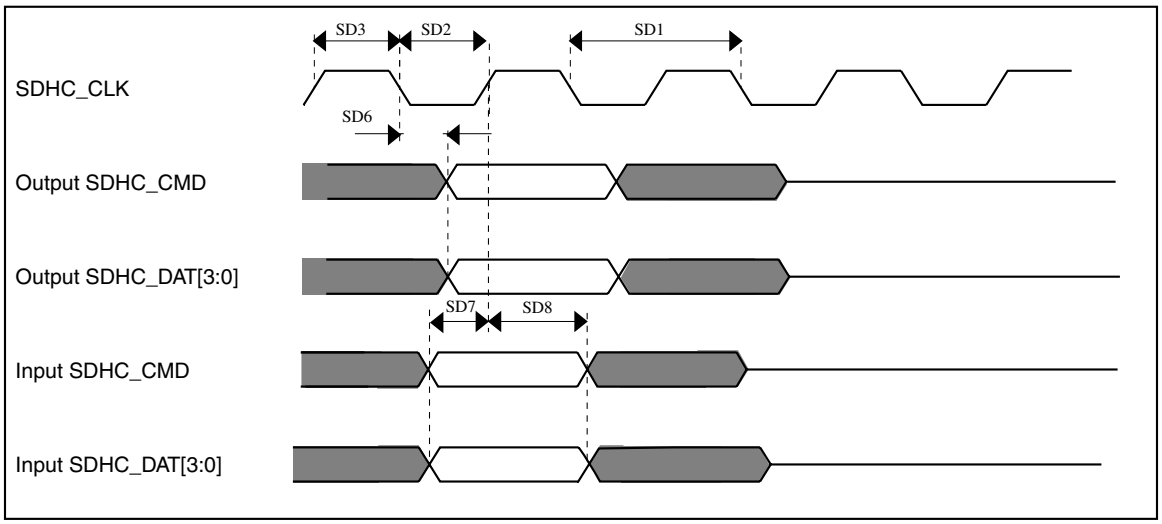


Figure 52. SDHC timing

9.6.4 USB PHY specifications

This section describes the USB-OTG PHY and the USB Host port PHY parameters.

The USB PHY meets the electrical compliance requirements defined in the Universal Serial Bus Revision 2.0 OTG, USB Host with the amendments below (On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification is not applicable to Host port).

- USB ENGINEERING CHANGE NOTICE
  - Title: 5V Short Circuit Withstand Requirement Change
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- Errata for USB Revision 2.0 April 27, 2000 as of 12/7/2000
- USB ENGINEERING CHANGE NOTICE
  - Title: Pull-up/Pull-down resistors
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- USB ENGINEERING CHANGE NOTICE
  - Title: Suspend Current Limit Changes
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification
  - Revision 2.0 plus errata and ecn June 4, 2010
- Battery Charging Specification (available from USB-IF)
  - Revision 1.2, December 7, 2010

9.7 Clocks and PLL Specifications

9.7.1 24 MHz Oscillator Specifications

The system crystal oscillator consists of a Pierce-type structure running off the digital supply. A straight forward biased-inverter implementation is used. The crystal must be rated for a drive level of 250 µW or higher. An ESR (equivalent series resistance) of 80 Ω or less is recommended to achieve a gain margin of 5.

Table 64. 24MHz external oscillator electrical characteristics

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
f_{osc}	Crystal oscillator range	—	—	24	—	MHz
I_{osc}	Startup current	—	—	< 5	—	mA
t_{uposc}	Oscillator startup time	—	—	< 5	—	ms
C_{IN}	Input Capacitance	EXTAL and XTAL pins	—	9	—	pF
VIH	XTAL pin input high voltage	—	0.8 x Vdd[1]	—	Vdd +0.3	V
VIL	XTAL pin input low voltage	—	Vss -0.3	—	0.2 x Vdd	V

1. V_{DD} =1.1 V ± 10%, TA = -40 to +85 °C, unless otherwise specified.

9.7.2 32 KHz Oscillator Specifications

This block implements an amplifier that when combined with a suitable quartz crystal and external load capacitors implements a low power oscillator. It also implements a power mux such that it can be powered from either a ~3 V backup battery or VDDIO such as the oscillator consumes power from VDDIO when that supply is available and transitions to the back up battery when VDDIO is lost.

In addition, if the clock monitor determines that the OSC32K is not present, then the source of the 32 K will automatically switch to the 128kHz internal RC clock divided by 4.

The OSC32k runs from vdd_rtc supply, generated inside OSC32k itself from VDDIO/ VBAT. The target battery is a ~3 V coin cell. Proper choice of coin cell type is necessary for chosen VDDIO range. Appropriate series resistor (Rs) must be used when connecting the coin cell. Rs depends on the charge current limit that depends on the chosen coin cell.

For example:

9.7.9 PLL6 (Video PLL) Electrical Parameters

Table 72. PLL6 Electrical Parameters

Parameter	Value
Clock output range	650 MHz ~1.3 GHz
Reference clock	24 MHz
Lock time	<7500 reference cycles
Long term jitter(RMS)[1]	<42ps @ 1128 MHz
Period jitter(p2p)	<130ps @960MHz
Duty Cycle	43%~57%

1. Jitter numbers are measured at divided PLL clock because high frequency cannot be brought-out on IO pad & at use case frequency.

9.8 Debug specifications

9.8.1 JTAG electricals

Table 73. JTAG limited voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
J1	TCLK frequency of operation			MHz
	• Boundary Scan	-	25	
	• JTAG and CJTAG	-	25	
	• Serial Wire Debug	-	25	
J2	TCLK cycle period	1/J1	—	ns
J3	TCLK clock pulse width			
	• Boundary Scan	20	—	ns
	• JTAG and CJTAG	20	—	ns
	• Serial Wire Debug	20	—	ns
J4	TCLK rise and fall times	Refer Table 21		ns
J5	Boundary scan input data setup time to TCLK rise	8	—	ns
J6	Boundary scan input data hold time after TCLK rise	1.3	—	ns
J7	TCLK low to boundary scan output data valid	—	17	ns
J8	TCLK low to boundary scan output high-Z	—	17	ns
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	TMS, TDI input data hold time after TCLK rise	1.3	—	ns
J11	TCLK low to TDO data valid	—	17	ns
J12	TCLK low to TDO high-Z	—	17	ns

364 MAP BGA	176 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
U14	74	EXT_ TAMPER1			EXT_ TAMPER1							
T13	—	EXT_ TAMPER2/ EXT_WM0_ TAMPER_IN			EXT_ TAMPER2/ EXT_WM0_ TAMPER_IN							
U13	—	EXT_ TAMPER3/ EXT_WM0_ TAMPER_ OUT			EXT_ TAMPER3/ EXT_WM0_ TAMPER_ OUT							
U12	—	EXT_ TAMPER4/ EXT_WM1_ TAMPER_IN			EXT_ TAMPER4/ EXT_WM1_ TAMPER_IN							
U10	—	EXT_ TAMPER5/ EXT_WM1_ TAMPER_ OUT			EXT_ TAMPER5/ EXT_WM1_ TAMPER_ OUT							
G7	2	VDD			VDD							
J7	—	VDD			VDD							
L7	22	VDD			VDD							
H8	48	VDD			VDD							
K8	85	VDD			VDD							
M8	102	VDD			VDD							
P8	125	VDD			VDD							
G9	136	VDD			VDD							
N9	174	VDD			VDD							
H10	—	VDD			VDD							
P10	—	VDD			VDD							
G11	—	VDD			VDD							
N11	—	VDD			VDD							
H12	—	VDD			VDD							
P12	—	VDD			VDD							
G13	—	VDD			VDD							
J13	—	VDD			VDD							
L13	—	VDD			VDD							
N13	—	VDD			VDD							
H14	—	VDD			VDD							
K14	—	VDD			VDD							
M14	—	VDD			VDD							
P14	—	VDD			VDD							
A1	1	VSS			VSS							
A20	13	VSS			VSS							

Table 75. RGPIO versus Pins (continued)

RGPIO	In GPIO module	Corresponding Pin on the chip	IOMUX register name	IOMUX register address
RGPIO[40]	PORT1[8]	PTB18	IOMUXC_PTB18	400480A0
RGPIO[41]	PORT1[9]	PTB19	IOMUXC_PTB19	400480A4
RGPIO[42]	PORT1[10]	PTB20	IOMUXC_PTB20	400480A8
RGPIO[43]	PORT1[11]	PTB21	IOMUXC_PTB21	400480AC
RGPIO[44]	PORT1[12]	PTB22	IOMUXC_PTB22	400480B0
RGPIO[45]	PORT1[13]	PTC0	IOMUXC_PTC0	400480B4
RGPIO[46]	PORT1[14]	PTC1	IOMUXC_PTC1	400480B8
RGPIO[47]	PORT1[15]	PTC2	IOMUXC_PTC2	400480BC
RGPIO[48]	PORT1[16]	PTC3	IOMUXC_PTC3	400480C0
RGPIO[49]	PORT1[17]	PTC4	IOMUXC_PTC4	400480C4
RGPIO[50]	PORT1[18]	PTC5	IOMUXC_PTC5	400480C8
RGPIO[51]	PORT1[19]	PTC6	IOMUXC_PTC6	400480CC
RGPIO[52]	PORT1[20]	PTC7	IOMUXC_PTC7	400480D0
RGPIO[53]	PORT1[21]	PTC8	IOMUXC_PTC8	400480D4
RGPIO[54]	PORT1[22]	PTC9	IOMUXC_PTC9	400480D8
RGPIO[55]	PORT1[23]	PTC10	IOMUXC_PTC10	400480DC
RGPIO[56]	PORT1[24]	PTC11	IOMUXC_PTC11	400480E0
RGPIO[57]	PORT1[25]	PTC12	IOMUXC_PTC12	400480E4
RGPIO[58]	PORT1[26]	PTC13	IOMUXC_PTC13	400480E8
RGPIO[59]	PORT1[27]	PTC14	IOMUXC_PTC14	400480EC
RGPIO[60]	PORT1[28]	PTC15	IOMUXC_PTC15	400480F0
RGPIO[61]	PORT1[29]	PTC16	IOMUXC_PTC16	400480F4
RGPIO[62]	PORT1[30]	PTC17	IOMUXC_PTC17	400480F8
RGPIO[63]	PORT1[31]	PTD31	IOMUXC_PTD31	400480FC
RGPIO[64]	PORT2[0]	PTD30	IOMUXC_PTD30	40048100
RGPIO[65]	PORT2[1]	PTD29	IOMUXC_PTD29	40048104
RGPIO[66]	PORT2[2]	PTD28	IOMUXC_PTD28	40048108
RGPIO[67]	PORT2[3]	PTD27	IOMUXC_PTD27	4004810C
RGPIO[68]	PORT2[4]	PTD26	IOMUXC_PTD26	40048110
RGPIO[69]	PORT2[5]	PTD25	IOMUXC_PTD25	40048114
RGPIO[70]	PORT2[6]	PTD24	IOMUXC_PTD24	40048118
RGPIO[71]	PORT2[7]	PTD23	IOMUXC_PTD23	4004811C
RGPIO[72]	PORT2[8]	PTD22	IOMUXC_PTD22	40048120
RGPIO[73]	PORT2[9]	PTD21	IOMUXC_PTD21	40048124
RGPIO[74]	PORT2[10]	PTD20	IOMUXC_PTD20	40048128
RGPIO[75]	PORT2[11]	PTD19	IOMUXC_PTD19	4004812C
RGPIO[76]	PORT2[12]	PTD18	IOMUXC_PTD18	40048130
RGPIO[77]	PORT2[13]	PTD17	IOMUXC_PTD17	40048134
RGPIO[78]	PORT2[14]	PTD16	IOMUXC_PTD16	40048138

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13 Power Supply Pins

13.1 Power Supply Pins

Table 77. Power Supply Pins

Supply Rail Name	364 MAP BGA	176 LQFP (F-series ONLY)	Comment
DECAP_V11_ LDO_OUT	V12	69	On-chip 1.1V LDO output
DECAP_V25_ LDO_OUT	T11	65	On-chip 2.5V LDO output (Intended to supply DRAM IO when required)
FA_VDD	N7	—	Factory Use Only (Connect to VDD, internally bonded in LQFP)
SDRAMC_ VDD1P5	D5, D11, E4, E7, E9, F5, H5, K5	DRAM not supported in LQFP	1.5V DDR3 DRAM Supply (1.2V for LPDDR2)
SDRAMC_ VDD2P5	E6, E10, J5	DRAM not supported in LQFP	2.5V DRAM Supply
USB_DCAP	Y10	59	On-chip 3V LDO output (Intended to be fed by external USB VBUS supply)
USB0_GND	V10	61	
USB1_GND	Y9	USB1 not supported in LQFP	
VADC_AFE_ BANDGAP	U5	Video ADC not supported in LQFP	Video ADC Bandgap Output
VBAT	V14	75	On-chip SNVS regulator battery back-up supply option
VDD	G7, G9, G11, G13, H8, H10, H12, H14, J7, J13, K8, K14, L7, L13, M8, M14, N9, N11, N13, P8, P10, P12, P14	2, 22, 48, 85, 102, 125, 136, 174	1.2V Core Supply (Internally Regulated)
VDD33	C12, C15, C18, F18, K3, K17, N3, N17, T17, U16, V8, W18	10, 25, 52, 83, 95, 108, 127, 140, 146, 158, 168	3.3V IO Supply
VDDA33_ADC	V1	38	3.3V Analog To Digital convertor supply
VDD12_AFE	T5	Video ADC not supported in LQFP	1.2V Analog Front End supply for Video ADC
VDDA33_AFE	V3	Video ADC not supported in LQFP	3.3V Analog Front End supply for Video ADC
VDD33_ LDOIN	T12	68	On-chip 2.5V LDO, 1.1V LDO and SNVS regulators input supply
VDDREG	P5	31	On-chip HPREG, LPREG, WBREG and ULPREG regulators input supply
VREFH_ADC	W1	41	ATD High Voltage Reference
VREFL_ADC	U3	40	ATD Low Voltage Reference

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Table 78. Functional Assignment Pins (continued)

Signal Name	364 MAP BGA	176 LQFP (F-series ONLY)	Power Group	Pad Type	Default Mode (Reset)	Default Function	Input/ Output	Value
DDR_A[0]	C7	—	SDRAMC_ VDD2P5	DDR	—	DDR_A[0]	—	—
DDR_A[1]	C11	—	SDRAMC_ VDD2P5	DDR	—	DDR_A[1]	—	—
DDR_A[2]	A8	—	SDRAMC_ VDD2P5	DDR	—	DDR_A[2]	—	—
DDR_A[3]	B7	—	SDRAMC_ VDD2P5	DDR	—	DDR_A[3]	—	—
DDR_A[4]	A6	—	SDRAMC_ VDD2P5	DDR	—	DDR_A[4]	—	—
DDR_A[5]	B6	—	SDRAMC_ VDD2P5	DDR	—	DDR_A[5]	—	—
DDR_A[6]	A9	—	SDRAMC_ VDD2P5	DDR	—	DDR_A[6]	—	—
DDR_A[7]	A7	—	SDRAMC_ VDD2P5	DDR	—	DDR_A[7]	—	—
DDR_A[8]	A11	—	SDRAMC_ VDD2P5	DDR	—	DDR_A[8]	—	—
DDR_A[9]	B9	—	SDRAMC_ VDD2P5	DDR	—	DDR_A[9]	—	—
DDR_A[10]	D7	—	SDRAMC_ VDD2P5	DDR	—	DDR_A[10]	—	—
DDR_A[11]	D10	—	SDRAMC_ VDD2P5	DDR	—	DDR_A[11]	—	—
DDR_A[12]	C10	—	SDRAMC_ VDD2P5	DDR	—	DDR_A[12]	—	—
DDR_A[13]	A10	—	SDRAMC_ VDD2P5	DDR	—	DDR_A[13]	—	—
DDR_A[14]	D9	—	SDRAMC_ VDD2P5	DDR	—	DDR_A[14]	—	—
DDR_A[15]	B10	—	SDRAMC_ VDD2P5	DDR	—	DDR_A[15]	—	—
DDR_BA[0]	C8	—	SDRAMC_ VDD2P5	DDR	—	DDR_BA[0]	—	—
DDR_BA[1]	C9	—	SDRAMC_ VDD2P5	DDR	—	DDR_BA[1]	—	—
DDR_BA[2]	D8	—	SDRAMC_ VDD2P5	DDR	—	DDR_BA[2]	—	—
DDR_CAS_ b	B4	—	SDRAMC_ VDD2P5	DDR	—	DDR_CAS_ b	—	—
DDR_CKE[0]	A5	—	SDRAMC_ VDD2P5	DDR	—	DDR_CKE[0]	—	—

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Table 78. Functional Assignment Pins (continued)

Signal Name	364 MAP BGA	176 LQFP (F-series ONLY)	Power Group	Pad Type	Default Mode (Reset)	Default Function	Input/ Output	Value
DDR_CLK[0]	A2	—	SDRAMC_VDD2P5	DDR	—	DDR_CLK[0]	—	—
DDR_CLK_b[0]	B2	—	SDRAMC_VDD2P5	DDR	—	DDR_CLK_b[0]	—	—
DDR_CS_b[0]	C5	—	SDRAMC_VDD2P5	DDR	—	DDR_CS_b[0]	—	—
DDR_D[0]	F4	—	SDRAMC_VDD2P5	DDR	—	DDR_D[0]	—	—
DDR_D[1]	H3	—	SDRAMC_VDD2P5	DDR	—	DDR_D[1]	—	—
DDR_D[2]	D4	—	SDRAMC_VDD2P5	DDR	—	DDR_D[2]	—	—
DDR_D[3]	G4	—	SDRAMC_VDD2P5	DDR	—	DDR_D[3]	—	—
DDR_D[4]	F3	—	SDRAMC_VDD2P5	DDR	—	DDR_D[4]	—	—
DDR_D[5]	J3	—	SDRAMC_VDD2P5	DDR	—	DDR_D[5]	—	—
DDR_D[6]	C3	—	SDRAMC_VDD2P5	DDR	—	DDR_D[6]	—	—
DDR_D[7]	G3	—	SDRAMC_VDD2P5	DDR	—	DDR_D[7]	—	—
DDR_D[8]	J1	—	SDRAMC_VDD2P5	DDR	—	DDR_D[8]	—	—
DDR_D[9]	D1	—	SDRAMC_VDD2P5	DDR	—	DDR_D[9]	—	—
DDR_D[10]	H1	—	SDRAMC_VDD2P5	DDR	—	DDR_D[10]	—	—
DDR_D[11]	E2	—	SDRAMC_VDD2P5	DDR	—	DDR_D[11]	—	—
DDR_D[12]	G1	—	SDRAMC_VDD2P5	DDR	—	DDR_D[12]	—	—
DDR_D[13]	C1	—	SDRAMC_VDD2P5	DDR	—	DDR_D[13]	—	—
DDR_D[14]	H2	—	SDRAMC_VDD2P5	DDR	—	DDR_D[14]	—	—
DDR_D[15]	D2	—	SDRAMC_VDD2P5	DDR	—	DDR_D[15]	—	—
DDR_DQM[0]	J4	—	SDRAMC_VDD2P5	DDR	—	DDR_DQM[0]	—	—
DDR_DQM[1]	G2	—	SDRAMC_VDD2P5	DDR	—	DDR_DQM[1]	—	—

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Table 79. Revision History

Rev. No.	Date	Substantial Changes
		Added Part Number Format figure Updated the Fields table as per the device part numbers Added Part Numbers table Added External NPN Ballast section In the LVD Dig Electrical Specs, minimum value of Upper Voltage Threshold and Lower Voltage threshold In the FlexBus timing specifications table, clarified the Frequency of operation In the Power consumption, filled TBDs. Updated footnotes Rewritten the EMC radiated emissions operating behaviors table In the GPIO DC Electrical characteristics table: • Vhys test condition changed • Added R_Keeper row In the DDR operating conditions, changed the Vddi Min and Max values In the Power sequencing table, rremoved some rows In the Power Supply section, removed LVDS and removed the note In the Recommended operating conditions table, updated min and max of VDD12_AFE and FA_VDD. Updated Min, Max, and Typ for VDD Added the Recommended Connections for Unused Analog Interfaces table In the 12-bit ADC Characteristics table, updated the typ and max values of TUE, DNL. INL, ZSE, FSE Added Receive and Transmit signal timing specifications for MII interfaces In the DSPI table, clarified the TBDs In PLL 4, PLL 5, PLL 6 electrical characteristics tables, added footnotes In the JTAG electrical table, clarified the TBDs In the pinouts section, added Special Signal table Added Power Supply pins section Added Functional Assignment section

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