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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-A5
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	ARM® Cortex®-M4, Multimedia; NEON™ MPE
RAM Controllers	DDR3, DRAM, LPDDR2
Graphics Acceleration	Yes
Display & Interface Controllers	DCU, GPU, LCD, VideoADC, VIU
Ethernet	10/100Mbps (2)
SATA	-
USB	USB 2.0 OTG + PHY (1)
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	ARM TZ, CAAM, HAB, RTIC, Secure JTAG, SNVS, Tamper, TZ ASC, TZ WDOG
Package / Case	364-LFBGA
Supplier Device Package	364-LFBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mvf50ns152cmk40

- Display and Video
  - Dual Display Control Unit (DCU) with support for color TFT display up to SVGA
  - Segmented LCD (3V Glass only) configurable as 40x4, 38x8, and 36x6
  - Video Interface Unit (VIU) for camera
  - Open VG Graphics Processing Unit (GPU)
  - VideoADC
- Analog
  - Dual 12-bit SAR ADC with 1MS/s
  - Dual 12-bit DAC
- Audio
  - Four Synchronous Audio Interface (SAI)
  - Enhanced Serial Audio Interface (ESAI)
  - Sony Philips Digital Interface (SPDIF), Rx and Tx
  - Asynchronous Sample Rate Converter (ASRC)
- Human-Machine Interface (HMI)
  - GPIO pins with interrupt support, DMA request capability, digital glitch filter.
  - Hysteresis and configurable pull up/down device on all input pins
  - Configurable slew rate and drive strength on all output pins
- On-Chip Memory
  - 512 KB On-chip SRAM with ECC
  - 1 MB On-chip graphics SRAM (no ECC). This depends on the part selected. Alternate configuration could be 512 KB graphics and 512 KB L2 cache.
  - 96 KB Boot ROM

6.2 Nonswitching electrical specifications

6.2.1 VREG electrical specifications

6.2.1.1 HPREG electrical characteristics

Table 2. HPREG electrical characteristics

Parameters	Min	Typ	Max	Unit	Comments
Power supply	3.0	3.3	3.6	V	-
Current Consumption	-	1.2	1.5	mA	@ no load
	-	2.0	2.5	mA	@ full load
Output current capacity	-	600	1200[1]	mA	DC load current
Output voltage @ no load		1.23	1.26	V	
Output voltage @ full load	1.20	1.21		V	
External decoupling cap	4.7		-	µF	-
	0.05		0.1	Ohms	ESR of external cap
			20	mOhms	Total effective PAD+PCB trace resistances
PSRR with 4.7uF output cap					
@ DC @noload @ DC @full load @ worst case any frequency			-48 -40 -20	dB	

1. This is peak and not continuous maximum value.

6.2.1.2 LPREG electrical characteristics

Table 3. LPREG electrical characteristics

Parameters	Min	Typ	Max	Unit	Comments
Power supply	3.0	3.3	3.6	V	
Current Consumption	350	400		µA	@ no load
	-	500	650	µA	@ full load
Output current capacity		100	200	mA	DC load current
Output voltage @ no load		1.22	1.240	V	
Output voltage @ full load	1.180			V	
External decoupling cap	4.7			µF	
	0.05		0.1	Ohms	ESR of external cap
			20	mOhms	Total PAD+PCB trace resistance

Table continues on the next page...

6.2.1.5 External NPN Ballast

The internal main regulator requires an external NPN ballast transistor to be connected as shown in the following figure as well as an external capacitance to be connected to the device in order to provide a stable 1.2V digital supply to the device. The HPREG design allows for collector voltage lower than VDDREG value. See AN4807 at www.freescale.com .

NOTE

To not overload BCTRL output, collector voltage should appear no later than VDDREG / VDD33 (3.3V).

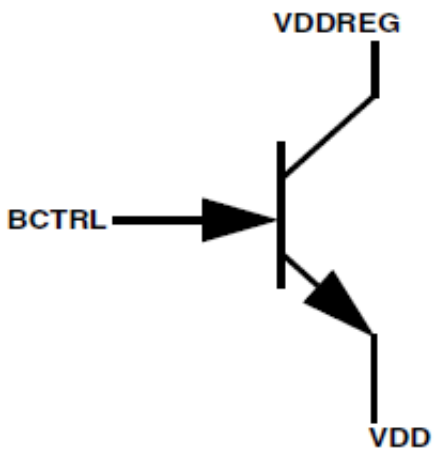

Figure 3. External NPN Ballast connections

Table 6. BCTRL OUTPUT specification

Parameter	Value	Comments
BCTRL OUTPUT specification	20mA	BCTRL driver can not drive more than 20mA current
Maximum pin voltage	VDDREG-0.5V	For Example, VDDREG =3.0V BCTRL should not exceed 2.5V.

Table 7. Assumptions For calculations

Parameter	Value
VDDREG	3.0V to 3.6V with typical value of 3.3V
Max DC Collector current	0.85A @85 °C
Emitter voltage	1.2V to 1.25V
Collector voltage	Equal to VDDREG

Table 25. DDR3 mode DC Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
Tri-state I/O supply current[3]	Icc-ovdd	Vin = ovdd or 0			5		
Tri-state vdd2p5 supply current[3]	Icc-vdd2p5	Vi = vddi or 0			1.5		
Tri-state core supply current[3]	Icc-vddi				1		
Driver unit (240 Ohm) calibration resolution	Rres				10	Ohm	

1. The single-ended signals need to be within the respective limits (Vih(dc) max, Vil(dc) min) for single-ended signals as well as the limitations for overshoot and undershoot.
2. Vtt is expected to track ovdd/2.
3. Typ condition: typ model, 1.5 V, and 25 °C. Max condition: bcs model, 1.575V, and -40 °C. Min condition: wcs model, 1.425V, and max Tj °C 125 °C junction

Table 26. LPDDR2 mode AC Electrical characteristics

Symbol	Parameter	Test condition	Min	Max	Unit	Notes
Vih(ac)	AC input logic high		Vref+0.22	ovdd	V	Note that the Jedec LPDDR2 specification (JESD209-2B) supersedes any specification in this document.
Vil(ac)	AC input logic low			Vref-0.22	V	
Vidh(ac)[1]	AC differential input high voltage		0.44	-	V	
Vidl(ac)[1]	AC differential input low voltage			0.44	V	
Vix(ac)[2]	AC differential input crosspoint voltage	Relative to ovdd/2	-0.12	0.12	V	
Vpeak	Over/undershoot peak			0.35	V	
Varea	Over/undershoot area (above ovdd or below ovss)	at 800MHz data rate		0.3	V*ns	
tsr	Single output slew rate		0.4	2	V/ns	
tskd	Skew between pad rise/fall asymmetry + skew cased by SSN			0.2	ns	

8.4 Recommended operating conditions

Table 30. Recommended operating conditions

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
USB0_VBUS	VBUS supply for USB w.r.t USB0_GND		4.4	5	5.25	V
USB1_VBUS	VBUS supply for USB w.r.t USB1_GND		4.4	5	5.25	V
USB_DCAP	USB LDO 5V->3 V Output	External DCAP (10uF termination for USBREG)		3		V
VBAT	Battery supply in case of LDOIN fails	External CAP 0.1uF	2.4	3.3	3.6	V
VDD33_LDOIN	LDO input supply		3	3.3	3.6	V
DECAP_V11_LDO_OUT	LDO 3.3V -> 1.1V Output	Recommended External DCAP: 1uF(Min) 10uF (Max)		1.1		V
DECAP_V25_LDO_OUT	LDO 3.3V -> 2.5 Output for PLL, DDR pre-driver, EFUSE	Recommended External DCAP: 1uF(Min) 10uF (Max)		2.5		V
VDD33	GPIO 3.3V IO supply	External CAP (10uF)	3	3.3	3.6	V
VDDREG	Device PMU regulator and External ballast supply	External CAP (10uF)	3	3.3	3.6	V
VDDA33_ADC	3.3V supply for ADC, DAC and IO segment	External CAP (10uF)	3	3.3	3.6	V
VREFH_ADC	High reference voltage for ADC and DAC	Relation with VDDDA33_ADC (1uF)	2.5	3.3	VDDA33_ADC	V
VREFL_ADC	Low reference voltage for ADC and DAC	External CAP (10uF)		0		V
VDDA33_AFE	3.3V supply of AFE (Video ADC)	External CAP 10uF	3	3.3	3.6	V
VDD12_AFE	1.2V supply for AFE (Video ADC)		1.16	1.23	1.26	V
FA_VDD	For testing purpose only should be shorted to VDD on board.		1.16	1.23	1.26	V
VDD[1]	1.2V core supply	4.7uF with a low ESR value (100 milliohms)	1.16	1.23	1.26	V
USB0_GND	Ground supply for USB			0		V
USB1_GND	Ground supply for USB			0		V
VSS_KEL0	USB LDO ground output			0		V
VSS	VSS ground			0		V
VSSA33_ADC	Ground supply for ADC, DAC and IO segment			0		V

Table continues on the next page...

NOTE

The ADC electrical spec would be met with the calibration enabled configuration.

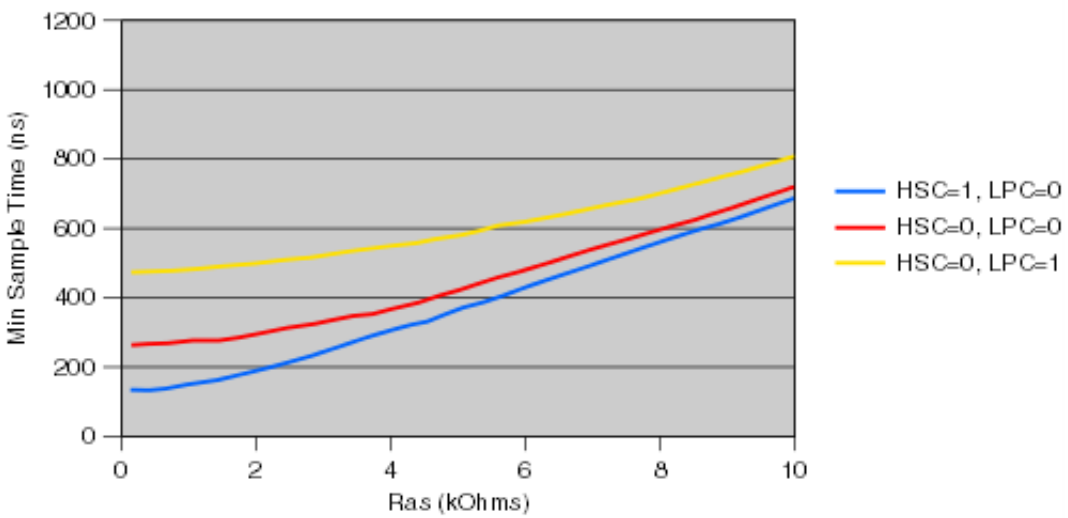

Figure 6. Minimum Sample Time Vs Ras (Cas = 2pF)

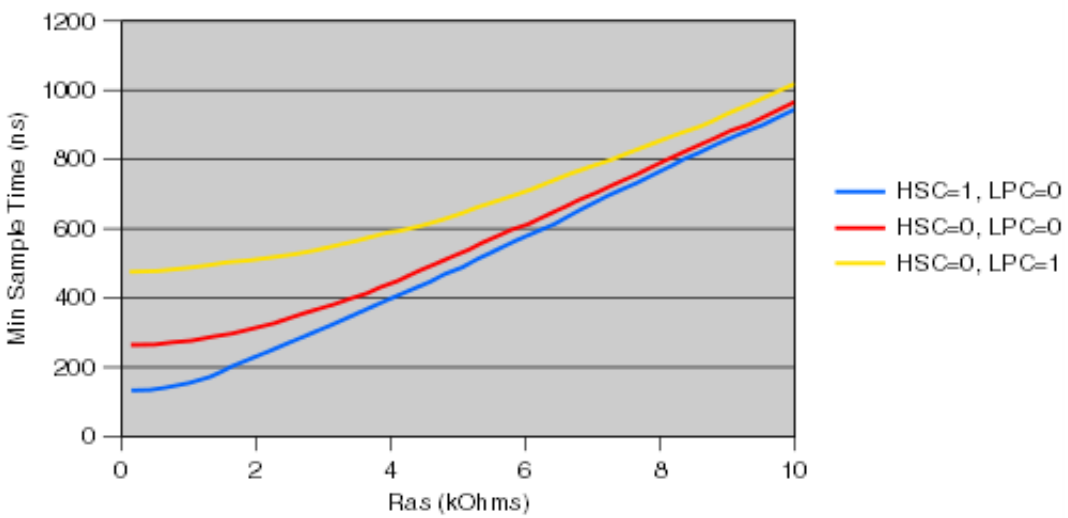

Figure 7. Minimum Sample Time Vs Ras (Cas = 5pF)

Table 34. 12-bit DAC operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{DACHP}	Full-scale settling time (0x080 to 0xF7F) — high-power mode	—	3	5	µs	1
$t_{CCDACLP}$	Code-to-code settling time (0xBF8 to 0xC08)				µs	1
	low-power mode	—	5	—		
	high-power mode	—	1	—		
$V_{dacoutl}$	DAC output voltage range low — high-speed mode, no load, DAC set to 0x000	—	—	100	mV	
$V_{dacouth}$	DAC output voltage range high — high-speed mode, no load, DAC set to 0xFFF	V_{DACR} −100	—	V_{DACR}	mV	
INL	Integral non-linearity error — high speed mode	—	—	±8	LSB	2
DNL	Differential non-linearity error — V_{DACR} = VREF_OUT	—	—	±1	LSB	3
V_{OFFSET}	Offset error	—	±0.4	±0.8	%FSR	4
E_G	Gain error	—	±0.1	±0.6	%FSR	4
PSRR	Power supply rejection ratio, V_{DDA} =3 V, T = 25 C		70		dB	
T_{CO}	Temperature coefficient offset voltage	—	3.7	—	µV/C	5
T_{GE}	Temperature coefficient gain error	—	0.000421	—	%FSR/C	
A_C	Offset aging coefficient	—	—	100	µV/yr	
Rop	Output resistance load = 3 kΩ	—	—	250	Ω	
SR	Slew rate -80h→ F7Fh→ 80h				V/µs	
	High power (SP_{HP})		1.7	3		
	Low power (SP_{LP})		0.3	0.6		
CT	Channel to channel cross talk	—	70		dB	

1. Settling within ±1 LSB
2. The INL is measured for 0+100mV to V_{DACR}−100 mV
3. The DNL is measured for 0+100mV to V_{DACR}−100 mV
4. Calculated by a best fit curve from V_{SS}+100 mV to V_{DACR}−100 mV
5. VDDA = 3.0V, reference select set for VDDA (DACx_CO:DACRFS = 1), high power mode(DACx_C0:LPEN = 0), DAC set to 0x800, Temp range from -40 °C to 85 °C

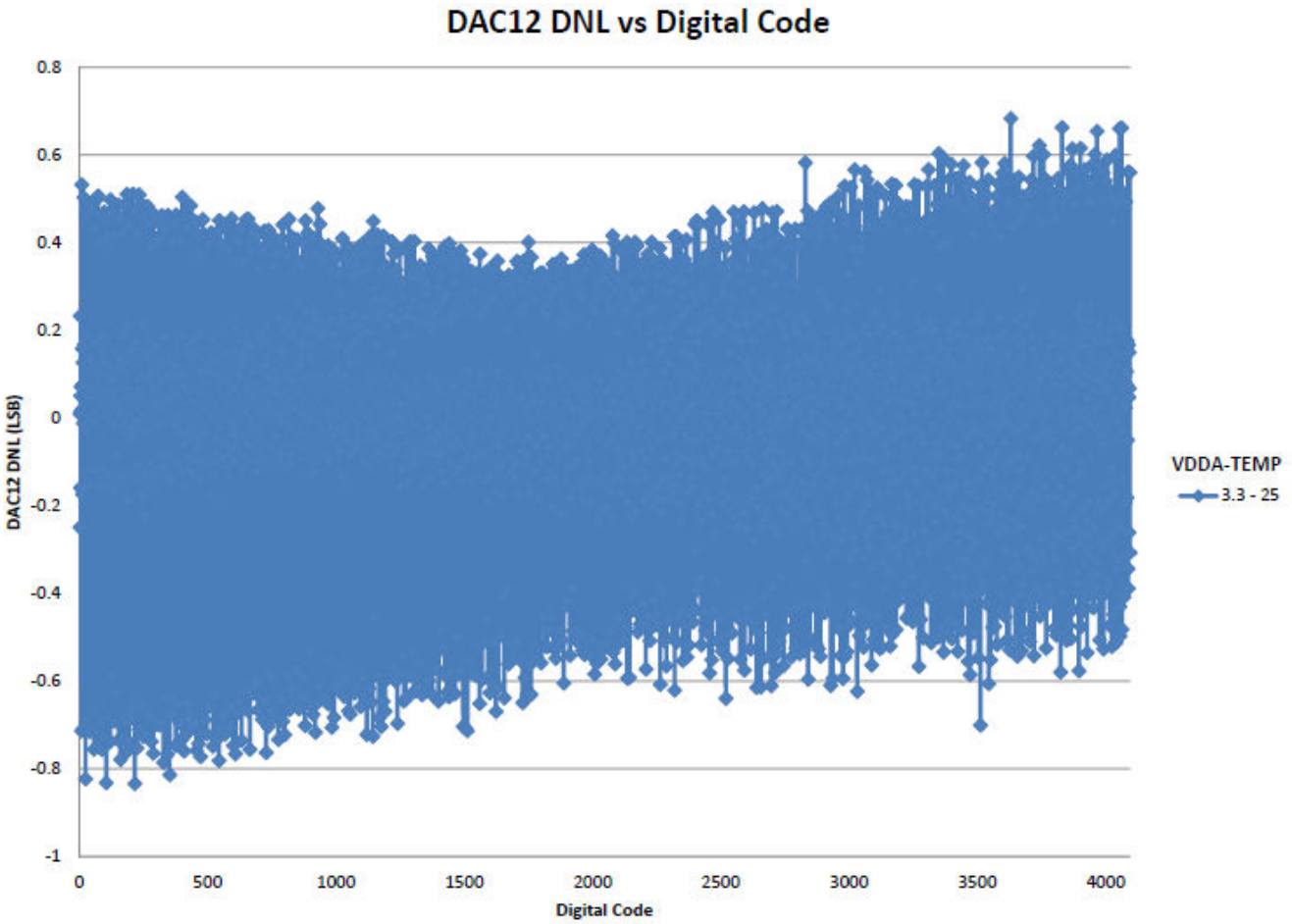

Figure 10. DNL error vs. digital code

9.2.3 LCD driver electrical characteristics

This section provides LCD driver electrical specification at V_{DD33} = 3.3 V ± 10%.

Table 39. LCD driver specifications

Symbol	Parameter	Min	Typical	Max	Unit
VLCD	Voltage on VLCD (LCD supply) pin with respect to VSS	0		VDD33 + 0.3	V
$Z_{BP/FP}$	LCD output impedance (BP[n-1:0],FP[m-1:0]) for output levels VDDE, VSS	_	_	5.0	KΩ
$I_{BP/FP}$	LCD output current (BP[n-1:0],FP[m-1:0]) for outputs charge/discharge voltage levels VDDE2/3, VDDE1/2, VDDE/3)[1]	_	25	_	µA

1. With PWR=10, BSTEN=0, and BSTAO=0

9.3 Ethernet specifications

9.3.1 Ethernet Switching Specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface. All Ethernet signals use pad type pad_fsr. The timing specifications described i the section assume a pad slew rate setting of 11 and a load of 50 pF[2].

9.3.2 Receive and Transmit signal timing specifications

This section provides timing specs that meet the requirements for RMII interfaces for a range of transceiver devices.

Table 40. Receive signal timing for RMII interfaces

	Characteristic	RMII Mode		Unit
		Min	Max	
—	EXTAL frequency (RMII input clock RMII_CLK)	—	50	MHz
E3, E7	RMII_CLK pulse width high	35%	65%	RMII_CLK period

Table continues on the next page...

2. These timing parameters are specified assuming maximum operating frequency and the fastest pad slew rate setting (11). When operating this interface at lower frequencies, increase the slew rate by using the 10, 01, or 00 setting to increase edge rise and fall times, thus reducing EMI.

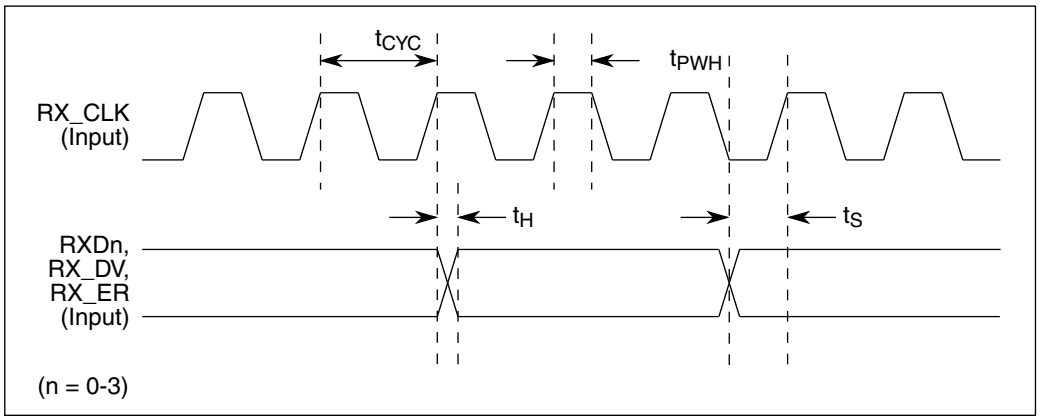

Figure 21. MII receive signal timing diagram

Table 41. Receive signal timing for MII interfaces

Characteristic		MII Mode			Unit
		Min	Typ	Max	
RX_CLK clock period (100/10 MBPS)	t_{CYC}		40/400		ns
RX_CLK duty cycle, t_{PWH}/t_{CYC}		45	50	55	%
Input setup time before RX_CLK	t_S	5			ns
Input setup time after RX_CLK	t_H	5			ns

9.3.3 Receive and Transmit signal timing specifications for MII interfaces

This section provides timing specs that meet the requirements for MII interfaces for a range of transceiver devices.

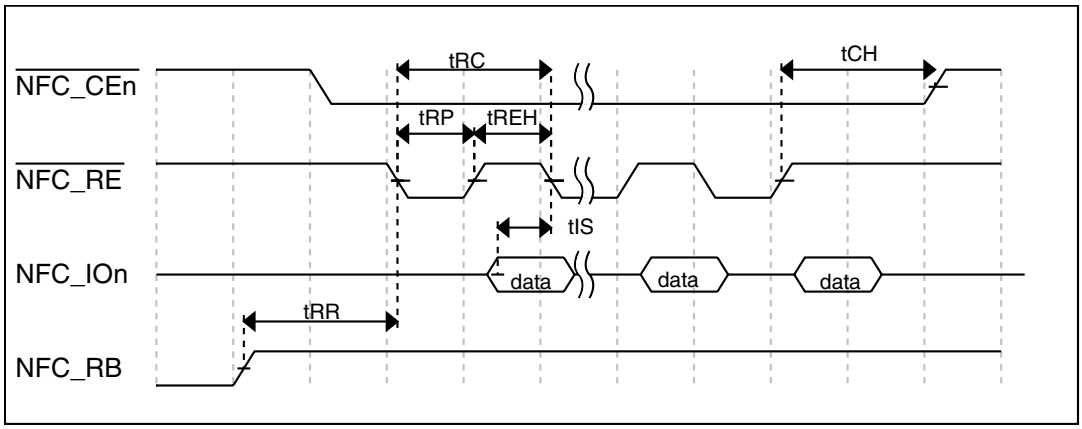

Figure 38. Read data latch cycle timing in fast mode

9.5.3 FlexBus timing specifications

This section provides FlexBus timing parameters. All processor bus timings are synchronous; input setup/hold and output delay are given in respect to the rising edge of a reference clock, FB_CLK. The FB_CLK frequency may be the same as the internal system bus frequency.

The following timing numbers indicate when data is latched or driven onto the external bus, relative to the FlexBus output clock (FB_CLK). All other timing relationships can be derived from these values.

All FlexBus signals use pad type pad_fsr. The following timing specifications assume a pad slew rate setting of 11 and a load of 50 pF[3]

Table 53. FlexBus timing specifications

Num	Characteristic	Min	Max	Unit
	Frequency of operation	—	83[1] (with Wait state)	MHz
			57[2] without Wait state , -1	
FB1	Clock Period	12	—	ns
FB4	Input setup	10.6	—	ns
FB5	Input hold	0	—	ns
FB2	Output valid	—	6.4	ns
FB3	Output hold	0	—	ns

1. Freq = 1000/(11+ access time of external memory+ trace delay for clk and data)
2. Freq = 1000/(17+access time of external memory)

3. These timing parameters are specified assuming maximum operating frequency and the fastest pad slew rate setting (11).

9.5.4 DDR controller specifications

9.5.4.1 DDR3 Timing Parameters

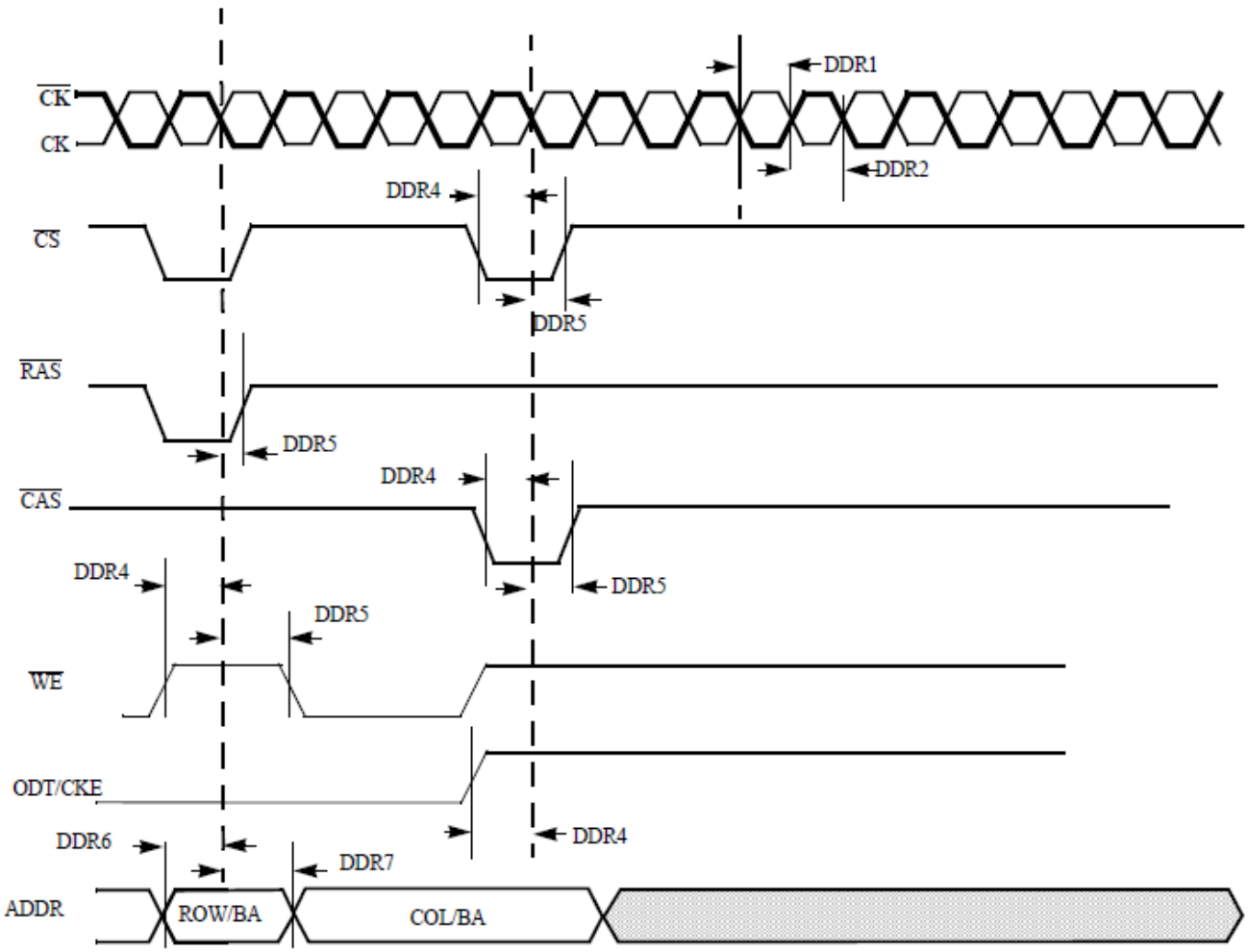

Figure 41. DDR3 Command and Address Timing Parameters

NOTE

RESET pin has a external weak pull DOWN requirement if DDR3 memory is NOT required to support content retention in the device low power modes where core voltage is off but DRAM voltage is on.

NOTE

RESET pin has a external weak pull UP requirement if DDR3 memory is required to support content retention in the device low power modes where core voltage is off but DRAM voltage is on.

NOTE

CKE pin has a external weak pull down requirement.

Table 54. DDR3 Timing Parameter

ID	Parameter	Symbol	CK = 400 MHz		Unit
			Min	Max	
DDR1	CK clock high-level width	tCH	0.47	0.53	tCK
DDR2	CK clock low-level width	tCL	0.47	0.53	tCK
DDR4	CS, RAS, CAS, CKE, WE, ODT setup time	tIS	440	-	ps
DDR5	CS, RAS, CAS, CKE, WE, ODT hold time	tIH	315	-	ps
DDR6	Address output setup time	tIS	440	-	ps
DDR7	Address output hold time	tIH	315	-	ps

NOTE

All measurements are in reference to Vref level.

NOTE

Measurements were done using balanced load and 25 ohms resistor from outputs to VDD_REF.

NOTE

Measurements were done using balanced load and 25 ohms resistor from outputs to VDD_REF.

9.5.4.5 LPDDR2 Read Cycle

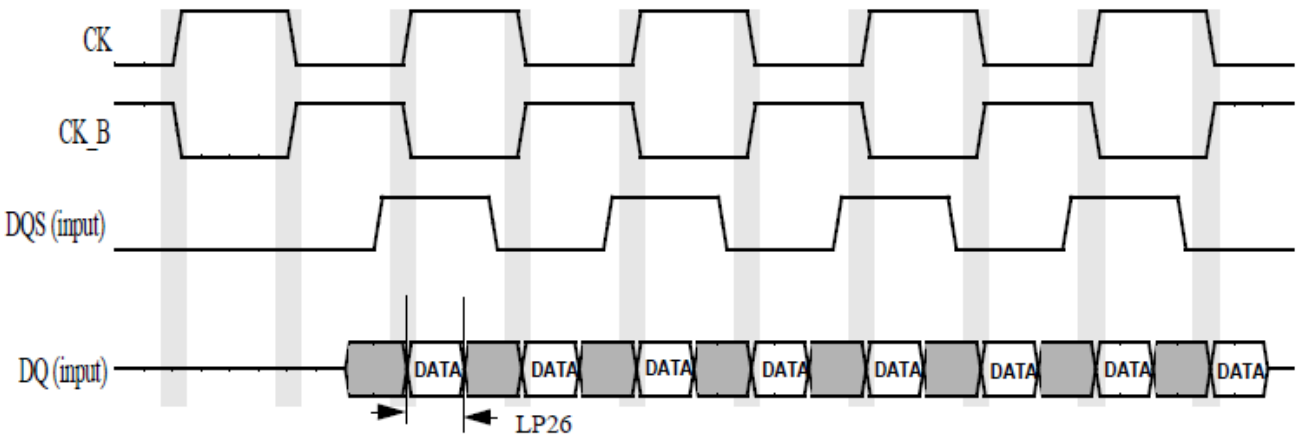

Figure 45. LPDDR2 Read cycle

Table 58. LPDDR2 Read Cycle

ID	Parameter	Symbol	CK = 400 MHz		Unit
			Min	Max	
LP26	Minimum required DQ valid window width for LPDDR2	-	270	-	ps

NOTE

To receive the reported setup and hold values, read calibration should be performed in order to locate the DQS in the middle of DQ window.

NOTE

All measurements are in reference to Vref level.

NOTE

Measurements were done using balanced load and 25 ohms resistor from outputs to VDD_REF

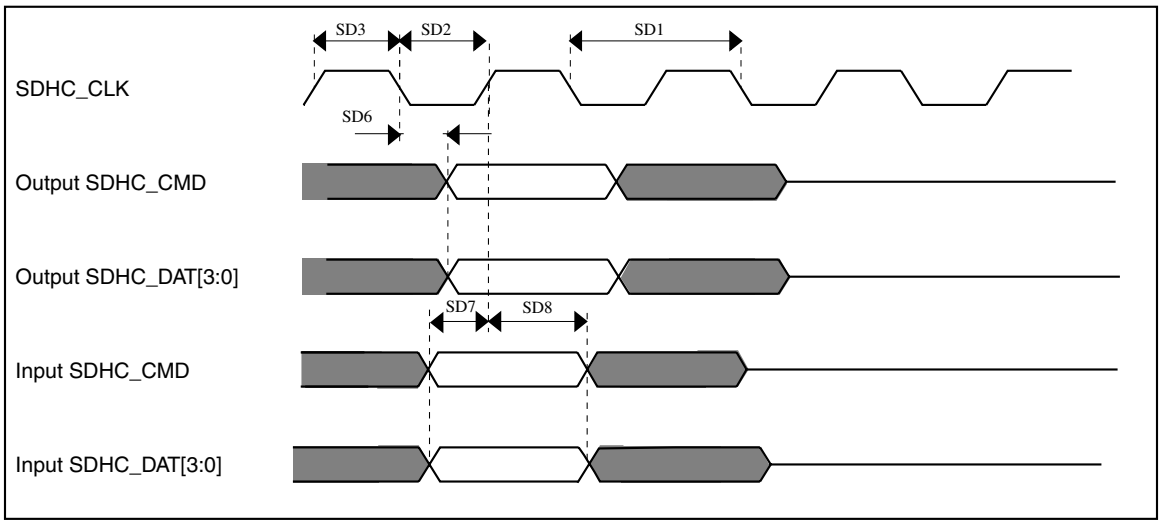

Figure 52. SDHC timing

9.6.4 USB PHY specifications

This section describes the USB-OTG PHY and the USB Host port PHY parameters.

The USB PHY meets the electrical compliance requirements defined in the Universal Serial Bus Revision 2.0 OTG, USB Host with the amendments below (On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification is not applicable to Host port).

- USB ENGINEERING CHANGE NOTICE
  - Title: 5V Short Circuit Withstand Requirement Change
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- Errata for USB Revision 2.0 April 27, 2000 as of 12/7/2000
- USB ENGINEERING CHANGE NOTICE
  - Title: Pull-up/Pull-down resistors
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- USB ENGINEERING CHANGE NOTICE
  - Title: Suspend Current Limit Changes
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification
  - Revision 2.0 plus errata and ecn June 4, 2010
- Battery Charging Specification (available from USB-IF)
  - Revision 1.2, December 7, 2010

Board type	Symbol	Description	176LQFP	Unit	Notes
		to package top (natural convection)			

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance
2. Per JEDEC JESD51-2 with the single layer board (JESD51-3) horizontal
3. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

Board type	Symbol	Description	364 MAPBGA	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	45	°C/W	1, 2
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	28	°C/W	1, 3
Single-layer (1s)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./ min. air speed)	37	°C/W	1,3
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./ min. air speed)	24	°C/W	1,3
—	$R_{\theta JB}$	Thermal resistance, junction to board	17	°C/W	4
—	$R_{\theta JC}$	Thermal resistance, junction to case	10	°C/W	5
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	2	°C/W	6

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

364 MAP BGA	176 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
V1	38	VDDA33_ ADC			VDDA33_ ADC							
V2	39	VSSA33_ ADC			VSSA33_ ADC							
U1	36	DACO0			DACO0							
U2	37	DACO1			DACO1							
Y4	—	VADCSE0			VADCSE0							
U4	—	VADCSE1			VADCSE1							
W4	—	VADCSE2			VADCSE2							
V5	—	VADCSE3			VADCSE3							
V3	—	VDDA33_ AFE			VDDA33_ AFE							
V4	—	VSSA33_AFE			VSSA33_AFE							
T5	—	VDD12_AFE			VDD12_AFE							
R5	—	VSS12_AFE			VSS12_AFE							
U5	—	VADC_AFE_ BANDGAP			VADC_AFE_ BANDGAP							
Y13	73	EXTAL			EXTAL							
W13	72	XTAL			XTAL							
Y12	70	EXTAL32			EXTAL32							
W12	71	XTAL32			XTAL32							
T4	35	RESETB/ RESET_OUT	RESETB/ RESET_OUT		RESETB/ RESET_OUT							
N5	19	PTA6		PTA6	RMII_ CLKOUT	RMII_CLKIN/ MII0_TXCLK		DCU1_ TCON11			DCU1_R2	
T3	34	TEST			TEST							
T1	30	Ext_POR			TEST2							
V12	69	DECAP_ V11_LDO_ OUT			DECAP_ V11_LDO_ OUT							
T11	65	DECAP_ V25_LDO_ OUT			DECAP_ V25_LDO_ OUT							
T2	33	BCTRL			BCTRL							
P5	31	VDDREG			VDDREG							
T12	68	VDD33_ LDOIN			VDD33_ LDOIN							
V11	67	VSS			VSS							
U11	66	VSS_KEL0			VSS_KEL0							
W14	—	LVDS0P			LVDS0P							
Y14	—	LVDS0N			LVDS0N							
K4	3	JTCLK/ SWCLK	JTCLK/ SWCLK	PTA8	JTCLK/ SWCLK			DCU0_R0			MLBCLK	

Table 77. Power Supply Pins (continued)

Supply Rail Name	364 MAP BGA	176 LQFP (F-series ONLY)	Comment
VSS	A1, A20, B3, B5, B8, B11, B13, B16, B19, C2, D17, E5, E8, E11, E14, E19, F2, G8, G10, G12, G14, G17, H4, H7, H9, H11, H13, H19, J2, J8, J9, J10, J11, J12, J14, J18, K7, K9, K10, K11, K12, K13, L8, L9, L10, L11, L12, L14, L19, M2, M4, M7, M9, M10, M11, M12, M13, M18, N8, N10, N12, N14, P7, P9, P11, P13, P19, R2, R18, U7, U19, V11, V13, V17, W6, Y1, Y20	1, 13, 24, 32, 45, 67, 82, 96, 107, 139, 144, 157, 175, 176, FLG	Ground—connect "Flag pad (FLG)" to the internal GND plane with numerous vias, for both electrical and thermal purposes.
VSSA33_ADC	V2	39	ATD Ground
VSS12_AFE	R5	Video ADC not supported in LQFP	Video ADC Ground
VSSA33_AFE	V4	Video ADC not supported in LQFP	Video ADC Ground
VSS_KEL0	U11	66	Ground (VSS and VSS_KEL0 are NOT connected internally)

14 Functional Assignment Pins

14.1 Functional Assignment Pins

Table 78. Functional Assignment Pins

Signal Name	364 MAP BGA	176 LQFP (F-series ONLY)	Power Group	Pad Type	Default Mode (Reset)	Default Function	Input/ Output	Value
ADC0SE8	Y2	—	VDDA33_ADC	Analog	—	ADC0SE8	—	—
ADC0SE9	W2	—	VDDA33_ADC	Analog	—	ADC0SE9	—	—
ADC1SE8	W3	—	VDDA33_ADC	Analog	—	ADC1SE8	—	—
ADC1SE9	Y3	—	VDDA33_ADC	Analog	—	ADC1SE9	—	—
BCTRL	T2	33	VDDREG	Analog	—	BCTRL	—	—
DACO0	U1	36	VDDA33_ADC	Analog	—	DACO0	—	—
DACO1	U2	37	VDDA33_ADC	Analog	—	DACO1	—	—

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Table 79. Revision History (continued)

Rev. No.	Date	Substantial Changes
Rev3	04/2012	Updated device name throughout the document Minor editorial updates in the feature list Updated VREG electrical specifications Updated LDO electrical specifications Updated Power consumption operating behaviors table Added USB PHY Current Consumption table Updated GPIO parameters Updated DDR parameters Updated Power sequencing Updated Power supply figure Updated Recommended operating conditions table Removed Reset specifications Updated 12-bit DAC operating requirements Added a note in 12-bit ADC operating conditions section Updated VideoADC Specifications table Updated LCD driver specifications table QuadSPI timing- Replaced VDDE with VDD33 Added notes in DDR3 Timing Parameters and LPDD2 Timing Parameters sections. Updated 24MHz external oscillator electrical characteristics table Updated OSC32K Main Characteristics table Updated Freescale Document Number for 144-pin LQFP Changed pin-name from EXT_POR to TEST2 Updated Pinouts section Updated GPIO Mapping
Rev4	08/2012	Updated Part identification Editorial changes in USB PHY Current Consumption in Normal Mode, GPIO AC Electrical Characteristics (3.3V power mode) Updated Power sequencing table

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Table 79. Revision History (continued)

Rev. No.	Date	Substantial Changes
		• In the LVD electrical specifications table, added typ. values of Upper voltage threshold (value @27oC) and Lower voltage threshold (value @27oC) • In the LVD DIG electrical specifications table, removed pretrimming values and clarified other values • Updated LVD DIG electrical specifications values • Updated LDO_1P1 tables • Updated LDO_2P5 table • Updated Power consumption operating behaviors tables • Updated Absolute maximum ratings table • Removed Temperature Voltage Monitor section to security RM • Updated VideoADC Specifications table
Rev 5	April 2013	Updated pin muxing table with the following changes: • Added MII0 including M AC0.TXDATA[2], MAC0.TXDATA[3], MAC0.RXDATA[2], MAC0.RXDATA[3] , MAC0.TXERR, MAC0.TXCLK, MAC0.RXCLK, MAC0.COL, MAC0.CRS • Following signals muxed on same RMII0 Pins : MII0_MDC, MII0_MDC, MII0_RXD[1], MII0_RXD[0], MII0_RXER, MII0_TXD[1], MII0_TXD[0], MII0_TXEN • Replaced FB_ALE with FB_MUXED_ALE, FB_CS4_b with FB_MUXED_TSIZ0, FB_TSIZ1 with FB_MUXED_TSIZ1, FB_TBST_b with FB_MUXED_TBST_b, FB_BE0_b with FB_MUXED_BE0_b • Removed RCON18,19,20 • Replaced ESAI_SDO2 with ESAI_SDO2/ESAI_SDI3 Replaced ESAI_SDO3 with ESAI_SDO3/ ESAI_SDI2 Replaced ESAI_SDI0 with ESAI_SDO5/ESAI_SDI0 Replaced ESAI_SDI1 with ESAU_SDO4/ESAI_SDI1 • CKO1 additionally muxed at PAD40
Rev 5	May 2013	In the Features, minor editorial updates

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