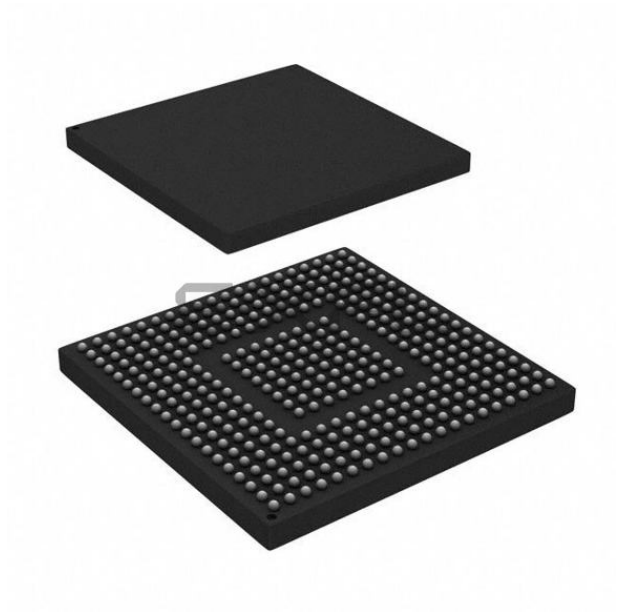


**Welcome to E-XFL.COM**

## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-A5 + Cortex®-M4 |
| Number of Cores/Bus Width | 2 Core, 32-Bit |
| Speed | 500MHz, 167MHz |
| Co-Processors/DSP | Multimedia; NEON™ MPE |
| RAM Controllers | LPDDR2, DDR3, DRAM |
| Graphics Acceleration | Yes |
| Display & Interface Controllers | DCU, GPU, LCD, VideoADC, VIU |
| Ethernet | 10/100Mbps (2) |
| SATA | - |
| USB | USB 2.0 OTG + PHY (1) |
| Voltage - I/O | 3.3V |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Security Features | - |
| Package / Case | 364-LFBGA |
| Supplier Device Package | 364-LFBGA (17x17) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/mvf60nn152cmk50 |

### 3.3.1 Example

This is an example of an attribute:

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| CIN_D | Input capacitance: digital pins | — | 7 | pF |

## 3.4 Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

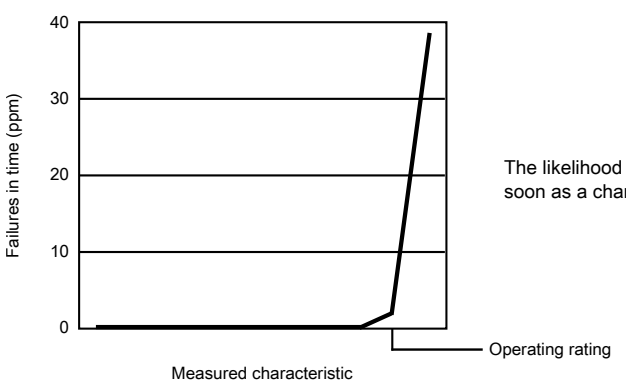
- *Operating ratings* apply during operation of the chip.
- *Handling ratings* apply when the chip is not powered.

### 3.4.1 Example

This is an example of an operating rating:

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{DD}$ | 1.0 V core supply voltage | –0.3 | 1.2 | V |

## 3.5 Result of exceeding a rating




The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.

# 6.2 Nonswitching electrical specifications

## 6.2.1 VREG electrical specifications

### 6.2.1.1 HPREG electrical characteristics

**Table 2. HPREG electrical characteristics**

| Parameters | Min | Typ | Max | Unit | Comments |
|---|---|---|---|---|---|
| Power supply | 3.0 | 3.3 | 3.6 | V | - |
| Current Consumption | - | 1.2 | 1.5 | mA | @ no load |
| | - | 2.0 | 2.5 | mA | @ full load |
| Output current capacity | - | 600 | 1200[1] | mA | DC load current |
| Output voltage @ no load | | 1.23 | 1.26 | V | |
| Output voltage @ full load | 1.20 | 1.21 | | V | |
| External decoupling cap | 4.7 | | - | µF | - |
| | 0.05 | | 0.1 | Ohms | ESR of external cap |
| | | | 20 | mOhms | Total effective PAD+PCB trace resistances |
| PSRR with 4.7uF output cap | | | | | |
| @ DC @noload<br>@ DC @full load<br>@ worst case any frequency | | | -48<br>-40<br>-20 | dB | |

1. This is peak and not continuous maximum value.

### 6.2.1.2 LPREG electrical characteristics

**Table 3. LPREG electrical characteristics**

| Parameters | Min | Typ | Max | Unit | Comments |
|---|---|---|---|---|---|
| Power supply | 3.0 | 3.3 | 3.6 | V | |
| Current Consumption | 350 | 400 | | µA | @ no load |
| | - | 500 | 650 | µA | @ full load |
| Output current capacity | | 100 | 200 | mA | DC load current |
| Output voltage @ no load | | 1.22 | 1.240 | V | |
| Output voltage @ full load | 1.180 | | | V | |
| External decoupling cap | 4.7 | | | µF | |
| | 0.05 | | 0.1 | Ohms | ESR of external cap |
| | | | 20 | mOhms | Total PAD+PCB trace resistance |

*Table continues on the next page...*

**Table 3. LPREG electrical characteristics (continued)**

| Parameters | Min | Typ | Max | Unit | Comments |
|---|---|---|---|---|---|
| PSRR with 4.7uF output cap | | | | | |
| @ DC @noload | | | -40 | dB | |
| @ DC @full load | | | -35 | | |
| Worst case @ any frequency | | | -12 | | |

### 6.2.1.3 ULPREG electrical characteristics

**Table 4. ULPREG electrical characteristics**

| Parameters | Min | Typ | Max | Unit | Comments |
|---|---|---|---|---|---|
| Power supply | 3.0 | 3.3 | 3.6 | V | |
| Current Consumption | 1.88 | 2.3 | 2.86 | µA | @ no load |
| | - | 610 | 670 | µA | @ full load |
| Output current capacity | | | 20 | mA | DC load current |
| Output voltage @ no load | | | 1.175 | V | |
| Output voltage @ full load | 1.125 | | | V | |
| PSRR with 500 pF output cap | -20 | | | dB | Worst case at any frequency across corners |
| @ DC @noload | | | -50 | dB | |
| @200KHz @noload | | | -37 | | |
| @ DC @full load | | | -42 | | |
| @200KHz @full load | | | -37 | | |
| Worst case @ any frequency @ any load | | | -15 | | |

### 6.2.1.4 WBREG electrical characteristics

**Table 5. WBREG electrical characteristics**

| Parameters | Min | Typ | Max | Unit | Comments |
|---|---|---|---|---|---|
| Power supply | 3 | 3.3 | 3.6 | V | - |
| Current Consumption | - | 2 | 5 | µA | @ no load |
| | - | 2 | 5 | µA | @ full load |
| Output current capacity | - | 1 | 2 | mA | DC load current |
| Output voltage @ no load | | 1.4 | 1.425 | V | |
| Output voltage @ full load | 1.375 | 1.398 | | V | |
| Output voltage programmability | 1.4 | 1.4 | 1.7 | V | 16 steps of 25 mV each |

## Table 25. DDR3 mode DC Electrical characteristics (continued)

| Symbol | Parameter | Test condition | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|---|
| Tri-state I/O supply current[3] | Icc-ovdd | Vin = ovdd or 0 | | | 5 | | |
| Tri-state vdd2p5 supply current[3] | Icc-vdd2p5 | Vi = vddi or 0 | | | 1.5 | | |
| Tri-state core supply current[3] | Icc-vddi | | | | 1 | | |
| Driver unit (240 Ohm) calibration resolution | Rres | | | | 10 | Ohm | |

1. The single-ended signals need to be within the respective limits (Vih(dc) max, Vil(dc) min) for single-ended signals as well as the limitations for overshoot and undershoot.
2. Vtt is expected to track ovdd/2.
3. Typ condition: typ model, 1.5 V, and 25 °C. Max condition: bcs model, 1.575V, and -40 °C. Min condition: wcs model, 1.425V, and max Tj °C 125 °C junction

## Table 26. LPDDR2 mode AC Electrical characteristics

| Symbol | Parameter | Test condition | Min | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| Vih(ac) | AC input logic high | | Vref+0.22 | ovdd | V | Note that the Jedec LPDDR2 specification (JESD209-2B) supersedes any specification in this document. |
| Vil(ac) | AC input logic low | | | Vref-0.22 | V | |
| Vidh(ac)[1] | AC differential input high voltage | | 0.44 | - | V | |
| Vidl(ac)[1] | AC differential input low voltage | | | 0.44 | V | |
| Vix(ac)[2] | AC differential input crosspoint voltage | Relative to ovdd/2 | -0.12 | 0.12 | V | |
| Vpeak | Over/undershoot peak | | | 0.35 | V | |
| Varea | Over/undershoot area (above ovdd or below ovss) | at 800MHz data rate | | 0.3 | V*ns | |
| tsr | Single output slew rate | | 0.4 | 2 | V/ns | |
| tskd | Skew between pad rise/fall asymmetry + skew cased by SSN | | | 0.2 | ns | |

## Table 32. 12-bit ADC Characteristics ($V_{REFH}$ = $V_{DDAD}$, $V_{REFL}$ = $V_{SSAD}$) (continued)

| Characteristic | Conditions[1] | Symb | Min | Typ [2] | Max | Unit | Comment |
|---|---|---|---|---|---|---|---|
| | ADLSMP=0 ADSTS=10 | | | 0.8 | | | |
| | ADLSMP=0 ADSTS=11 | | | 0.85 | | | |
| | ADLSMP=1 ADSTS=00 | | | 0.95 | | | |
| | ADLSMP=1 ADSTS=01 | | | 1.05 | | | |
| | ADLSMP=1 ADSTS=10 | | | 1.15 | | | |
| | ADLSMP=1, ADSTS=11 | | | 1.25 | | | |
| Total Unadjusted Error | 12 bit mode | TUE | -2 | - | +5 | LSB[3] | With Max Averaging |
| | 10 bit mode | | -0.5 | - | +2 | | |
| | 8 bit mode | | -0.25 | - | +1.5 | | |
| Differential Non-Linearity | 12 bit mode | DNL | - | ±0.6 | ±1.5 | LSB[3] | Waiting for histogram method confirmation |
| | 10bit mode | | - | ±0.5 | ±1 | | |
| | 8 bit mode | | - | ±0.25 | ±0.5 | | |
| Integral Non-Linearity | 12 bit mode | INL | - | ±2 | ±4 | LSB[3] | Waiting for histogram method confirmation |
| | 10bit mode | | - | ±1 | ±2 | | |
| | 8 bit mode | | - | ±0.5 | ±1 | | |
| Zero-Scale Error | 12 bit mode | $E_{ZS}$ | - | +1.0 | ±1.6 | LSB[3] | VADIN = $V_{REFL}$ With Max Averaging |
| | 10bit mode | | - | ±0.4 | ±0.8 | | |
| | 8 bit mode | | - | ±0.1 | ±0.4 | | |
| Full-Scale Error | 12 bit mode | $E_{FS}$ | - | ±2 | ±3.5 | LSB[3] | VADIN = $V_{REFH}$ With Max Averaging |
| | 10bit mode | | - | ±0.5 | ±1 | | |
| | 8 bit mode | | - | ±0.25 | ±0.75 | | |
| Quantization Error | 12 bit mode | $E_Q$ | - | ±1 to 0 | | LSB[3] | |
| | 10bit mode | | - | ±0.5 | | | |
| | 8 bit mode | | - | ±0.5 | | | |
| Effective Number of Bits | 12 bit mode | ENOB | 10.1 | 10.7 | - | Bits | Fin = 100Hz |
| Signal to Noise plus Distortion | See ENOB | SINAD | SINAD = 6.02 x ENOB + 1.76 | | | dB | |
| Input Leakage Error | all modes | EIL | $I_{In}$ x RAS | | | mV | $I_{In}$ = 400 nA leakage current |
| Temp Sensor Slope | Across the full temperature range of the device | m | -- | 1.84 | -- | mV/°C | |
| Temp Sensor Voltage | 25°C | $V_{TEMP25}$ | - | 696 | - | mV | |

1. All accuracy numbers assume the ADC is calibrated with $V_{REFH}$=$V_{DDAD}$
2. Typical values assume $V_{DDAD}$ = 3.0 V, Temp = 25°C, $F_{adck}$=20 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
3. 1 LSB = ($V_{REFH}$ - $V_{REFL}$)/2N

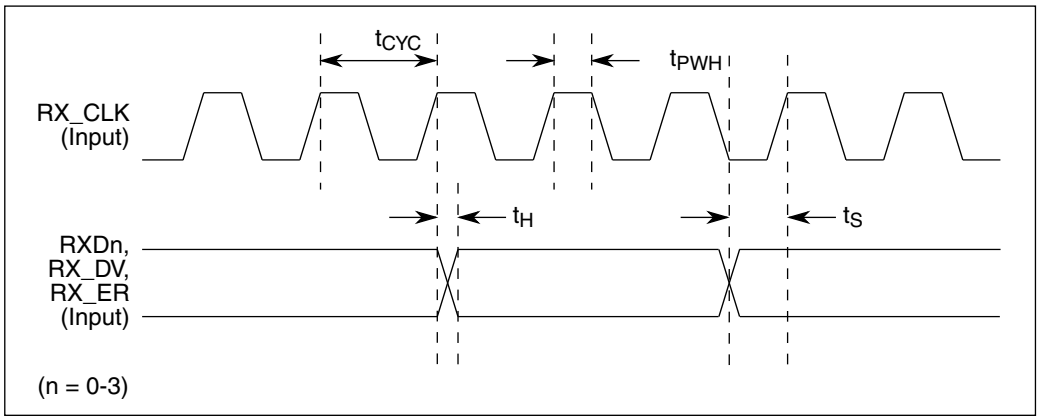



**Figure 22. MII receive signal timing diagram**

**Table 42. Receive signal timing for MII interfaces**

| Characteristic | | MII Mode | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| RX_CLK clock period (100/10 MBPS) | $t_{CYC}$ | | 40/400 | | ns |
| RX_CLK duty cycle, $t_{PWH}/t_{CYC}$ | | 45 | 50 | 55 | % |
| Input setup time before RX_CLK | $t_s$ | 5 | | | ns |
| Input hold time after RX_CLK | $t_h$ | 5 | | | ns |

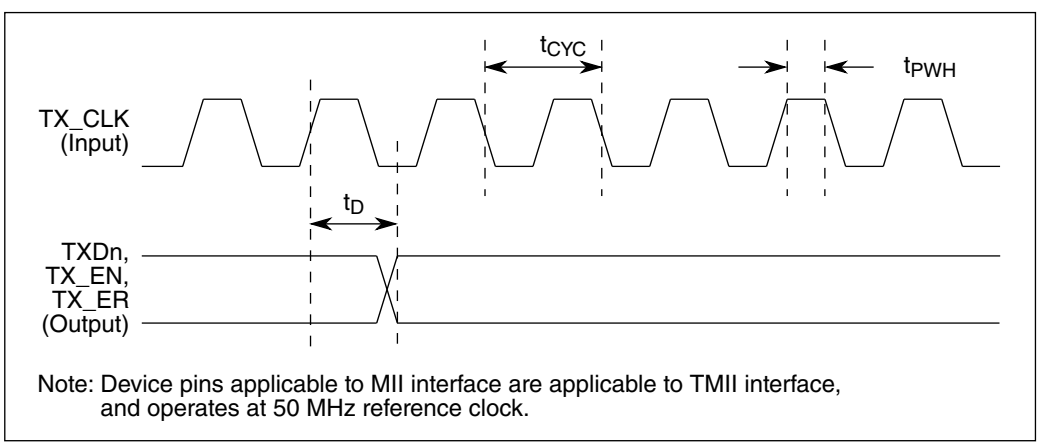



**Figure 23. MII transmit signal timing diagram**

**Table 43. Transmit signal timing for MII interfaces**

| Characteristic | | MII Mode | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| TX_CLK clock period (100/10 MBPS) | $t_{CYC}$ | | 40/400 | | ns |
| TX_CLK duty cycle, $t_{PWH}/t_{CYC}$ | | 45 | 50 | 55 | % |
| Out delay from TX_CLK | $t_D$ | 2 | | 25 | ns |

# 9.5 Memory interfaces

## 9.5.1 QuadSPI timing

- All data is based on a negative edge data launch from the device and a negative edge data capture, as shown in the timing diagrams in this section. This corresponds to the N/1 sample point as shown in the reference manual QSPI section "Internal Sampling of Serial Flash Input Data."
- Measurements are with a load of 35 pF on output pins. I/P Slew : 1ns
- Timings assume a setting of 0x0000_000x for QSPI_SMPR register (see the reference manual for details).

### SDR mode

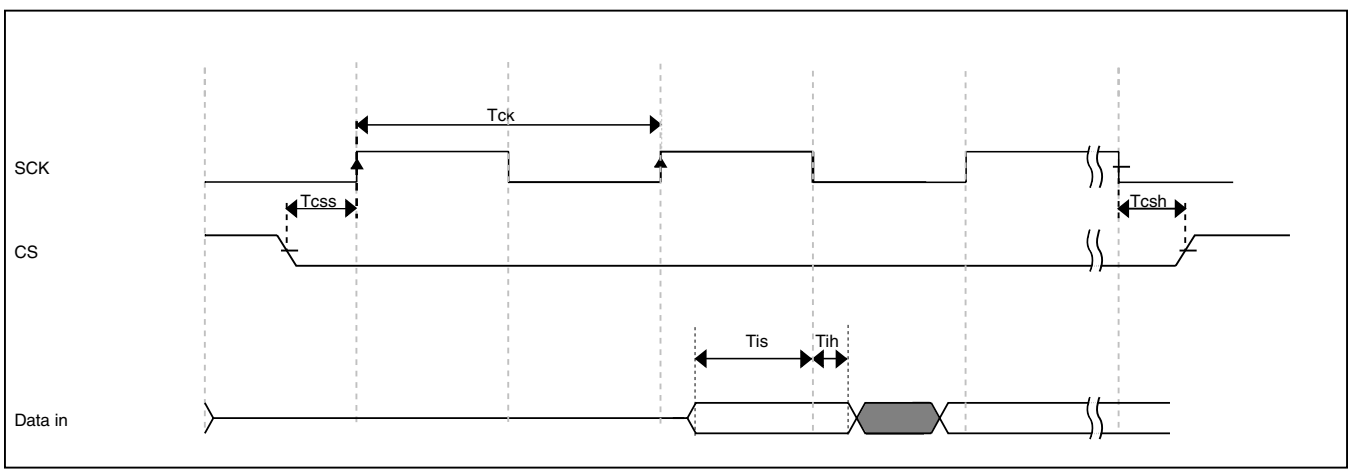



**Figure 30. QuadSPI Input/Read timing (SDR mode)**

**Table 48. QuadSPI Input/Read timing (SDR mode)**

| Symbol | Parameter | Value | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| $T_{is}$ | Setup time for incoming data | 4.5 | — | ns |
| $T_{ih}$ | Hold time requirement for incoming data | 0 | — | ns |

## Table 52. NFC specifications

| Num | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $t_{CLS}$ | NFC_CLE setup time | $2T_H + T_L - 1$ | — | ns |
| $t_{CLH}$ | NFC_CLE hold time | $T_H + T_L - 1$ | — | ns |
| $t_{CS}$ | $\overline{\text{NFC\_CEn}}$ setup time | $2T_H + T_L - 1$ | — | ns |
| $t_{CH}$ | $\overline{\text{NFC\_CEn}}$ hold time | $T_H + T_L$ | — | ns |
| $t_{WP}$ | $\overline{\text{NFC\_WP}}$ pulse width | $T_L - 1$ | — | ns |
| $t_{ALS}$ | NFC_ALE setup time | $2T_H + T_L$ | — | ns |
| $t_{ALH}$ | NFC_ALE hold time | $T_H + T_L$ | — | ns |
| $t_{DS}$ | Data setup time | $T_L - 1$ | — | ns |
| $t_{DH}$ | Data hold time | $T_H - 1$ | — | ns |
| $t_{WC}$ | Write cycle time | $T_H + T_L - 1$ | — | ns |
| $t_{WH}$ | $\overline{\text{NFC\_WE}}$ hold time | $T_H - 1$ | — | ns |
| $t_{RR}$ | Ready to $\overline{\text{NFC\_RE}}$ low | $4T_H + 3T_L + 90$ | — | ns |
| $t_{RP}$ | $\overline{\text{NFC\_RE}}$ pulse width | $T_L + 1$ | — | ns |
| $t_{RC}$ | Read cycle time | $T_L + T_H - 1$ | — | ns |
| $t_{REH}$ | $\overline{\text{NFC\_RE}}$ high hold time | $T_H - 1$ | — | ns |
| $t_{IS}$ | Data input setup time | 11 | — | ns |

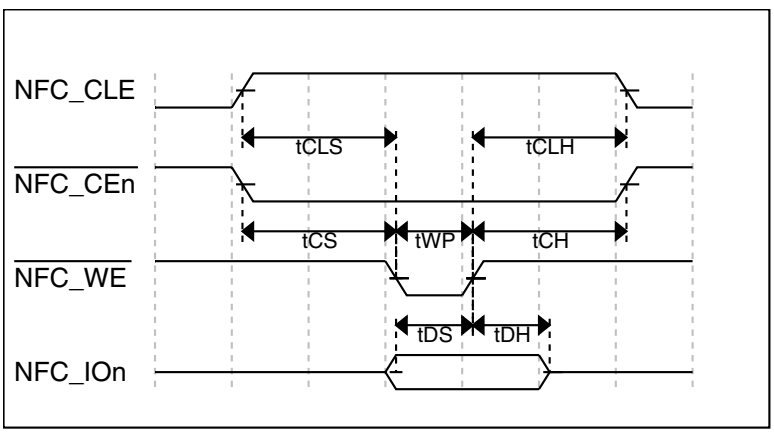



**Figure 34. Command latch cycle timing**

### 9.5.4.2 DDR3 Read Cycle

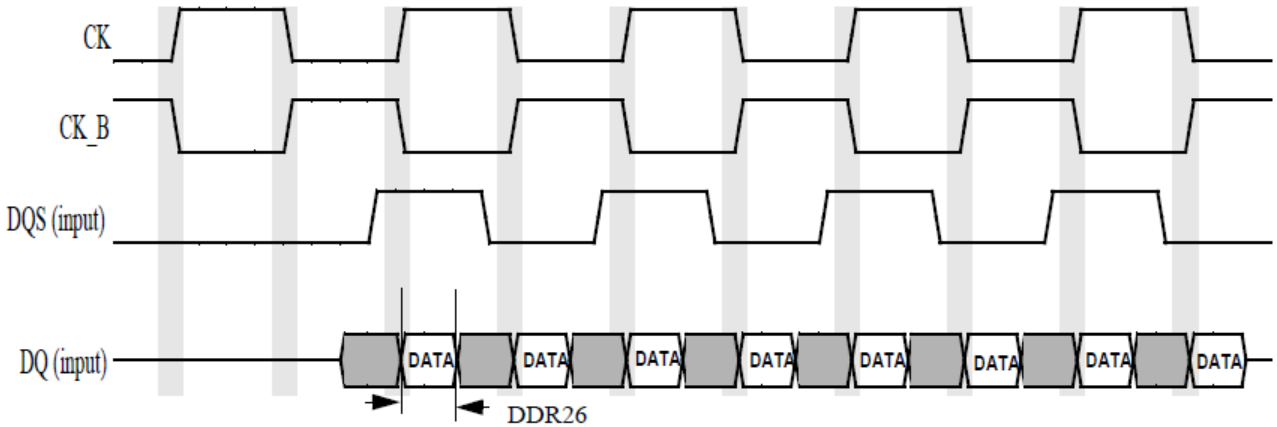



**Figure 42. DDR3 Read Cycle**

**Table 55. DDR3 Read Cycle**

| ID | Parameter | Symbol | CK = 400 MHz | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| DDR26 | Minimum required DQ valid window width | - | 750 | - | ps |

**NOTE**

To receive the reported setup and hold values, read calibration should be performed in order to locate the DQS in the middle of DQ window.

**NOTE**

All measurements are in reference to Vref level.

**NOTE**

Measurements were done using balanced load and 25 ohms resistor from outputs to VDD_REF

### 9.5.4.3 DDR3 Write cycle

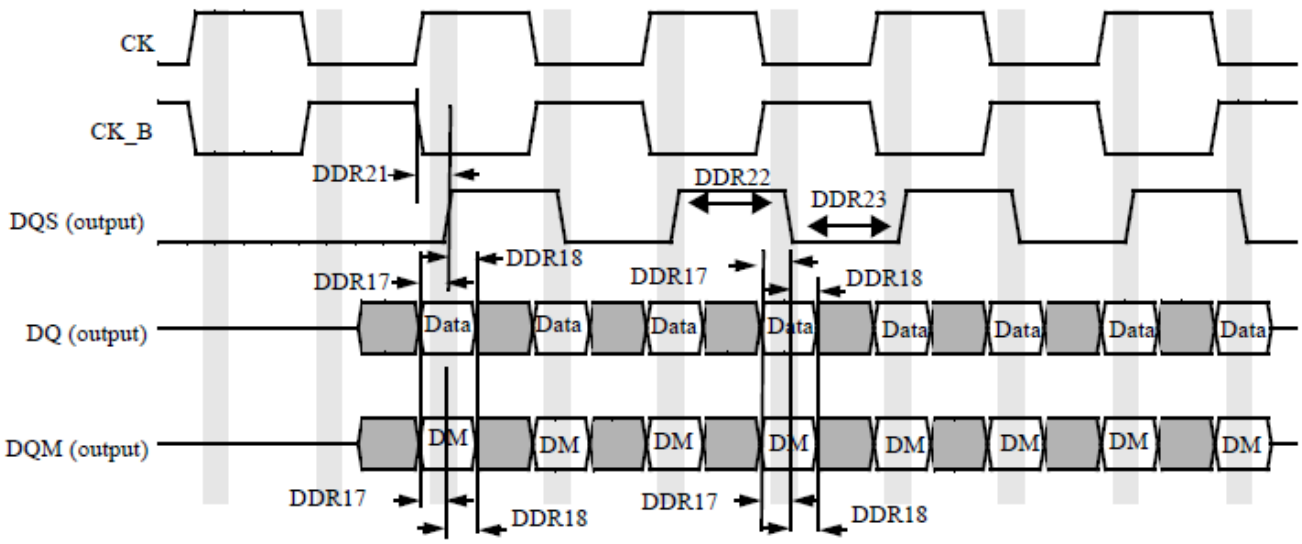



**Figure 43. DDR3 Write cycle**

**Table 56. DDR3 Write cycle**

| ID | Parameter | Symbol | CK = 400 MHz | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| DDR17 | DQ and DQM setup time to DQS (differential strobe) | tDS | 240 | — | ps |
| DDR18 | DQ and DQM hold time to DQS (differential strobe) | tDH | 215 | — | ps |
| DDR21 | DQS latching rising transitions to associated clock edges | tDQSS | -0.25 | +0.25 | tCK |
| DDR22 | DQS high level width | tDQSH | 0.45 | 0.55 | tCK |
| DDR22 | DQS low level width | tDQSL | 0.45 | 0.55 | tCK |

**NOTE**

To receive the reported setup and hold values, write calibration should be performed in order to locate the DQS in the middle of DQ window.

**NOTE**

All measurements are in reference to Vref level.

**NOTE**

Measurements were done using balanced load and 25 ohms resistor from outputs to VDD_REF.

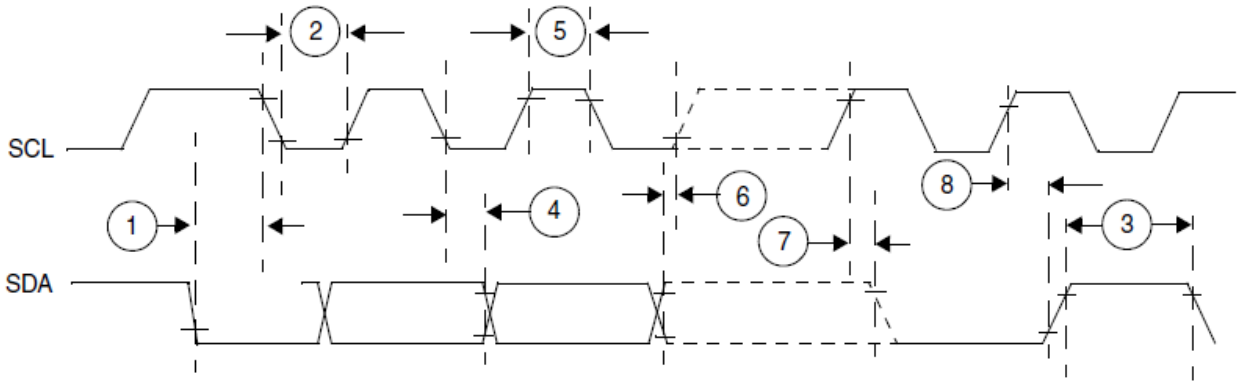



**Figure 51. I2C input/output timing**

## 9.6.3 SDHC specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface. A load of 50 pF is assumed.

**Table 63. SDHC switching specifications**

| Num | Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|---|
| | | Operating voltage | 1.71 | 3.6 | V |
| | **Card input clock** | | | | |
| SD1 | fpp | Clock frequency (low speed) | 0 | 400 | kHz |
| | fpp | Clock frequency (SD\SDIO full speed\high speed) | 0 | 25\50 | MHz |
| | fpp | Clock frequency (MMC full speed\high speed) | 0 | 20\50 | MHz |
| | $f_{OD}$ | Clock frequency (identification mode) | 0 | 400 | kHz |
| SD2 | $t_{WL}$ | Clock low time | 7 | — | ns |
| SD3 | $t_{WH}$ | Clock high time | 7 | — | ns |
| SD4 | $t_{TLH}$ | Clock rise time | — | 3 | ns |
| SD5 | $t_{THL}$ | Clock fall time | — | 3 | ns |
| | **SDHC output / card inputs SDHC_CMD, SDHC_DAT (reference to SDHC_CLK)** | | | | |
| SD6 | $t_{OD}$ | SDHC output delay (output valid) | -5 | 4 | ns |
| | **SDHC input / card inputs SDHC_CMD, SDHC_DAT (reference to SDHC_CLK)** | | | | |
| SD7 | $t_{ISU}$ | SDHC input setup time | 5 | — | ns |
| SD8 | $t_{IH}$ | SDHC input hold time | 0 | — | ns |

**Table 66. Fast internal oscillator electrical characteristics (continued)**

| Symbol | Parameter | Condition[1] | Value | | | |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Unit |
| RCMVAR | RC oscillator variation in temperature and supply with respect to $f_{RC}$ at $T_A$ = 55 °C in high frequency configuration | | -5 | | +5 | % |

1. $V_{DD}$ = 1.2 V , $T_A$ = -40 to +85 °C, unless otherwise specified.

## 9.7.4 Slow internal RC oscillator (128 KHz) electrical characteristics

This section describes a slow internal RC oscillator (SIRC). This can be used as the reference clock for the RTC module.

**Table 67. Slow internal RC oscillator electrical characteristics**

| Symbol | Parameter | Condition[1] | Value | | | |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Unit |
| $f_{RCL}$ | RC oscillator low frequency | $T_A$= 25 °C, trimmed | — | 128 | — | kHz |
| $I_{RCL}$ | RC oscillator low frequency current | $T_A$= 25 °C, trimmed | — | 3.1 | | µA |
| RCLTRIM | RC oscillator precision after trimming of $f_{RCL}$ | $T_A$= 25 °C | -1 | — | +1 | % |
| RCLVAR 3 | RC oscillator variation in temperature and supply with respect to $f_{RC}$ at $T_A$ = 55 °C in high frequency configuration | High frequency configuration | -5 | — | +5 | % |

1. $V_{DD}$ = 1.2 V , $T_A$ = -40 to +85 °C, unless otherwise specified.

## 9.7.5 PLL1 and PLL2 (528 MHz System PLL) Electrical Parameters

**Table 68. PLL1 and PLL2 Electrical Parameters**

| Parameter | Value |
|---|---|
| Clock output range | 528 MHz PLL output |
| Reference clock | 24 MHz |
| Lock time | <7500 reference cycles |
| Period jitter(p2p) | <140ps |
| Duty Cycle | 48.9%~51.7% PLL output |

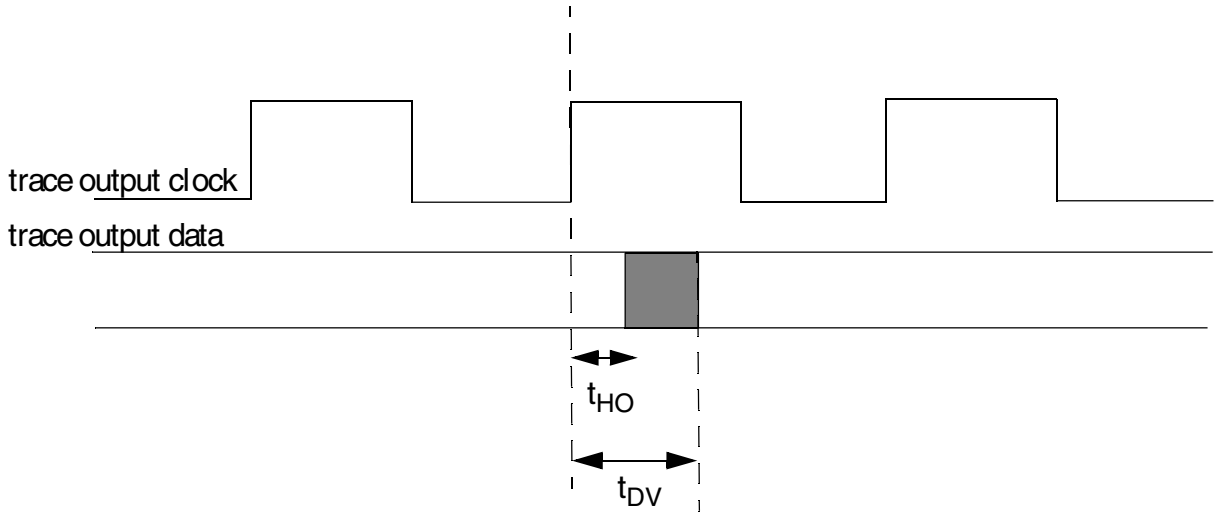



**Figure 57. Trace data specifications**

# 10 Thermal attributes

## 10.1 Thermal attributes

| Board type | Symbol | Description | 176LQFP | Unit | Notes |
|---|---|---|---|---|---|
| Single-layer (1s) | $R_{\theta JA}$ | Thermal resistance, junction to ambient (natural convection) | 50 | °C/W | 1, 2 |
| Four-layer (2s2p) | $R_{\theta JA}$ | Thermal resistance, junction to ambient (natural convection) | 32 | °C/W | 1,3 |
| Single-layer (1s) | $R_{\theta JMA}$ | Thermal resistance, junction to ambient (200 ft./ min. air speed) | 40 | °C/W | 1, 3 |
| Four-layer (2s2p) | $R_{\theta JMA}$ | Thermal resistance, junction to ambient (200 ft./ min. air speed) | 25 | °C/W | 1, 3 |
| — | $R_{\theta JB}$ | Thermal resistance, junction to board | 21 | °C/W | 4 |
| — | $R_{\theta JCtop}$ | Thermal resistance, junction to case top | 12 | °C/W | 5 |
| — | $\Psi_{JT}$ | Thermal characterization parameter, junction | 3 | °C/W | 6 |

5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

# 11 Dimensions

## 11.1 Obtaining package dimensions

Package dimensions are provided in package drawing.

To find a package drawing, go to www.freescale.com and perform a keyword search for the drawing's document number:

| Package | Freescale Document Number |
|---|---|
| 176-pin LQFP | 98ASA00452D |
| 364 MAPBGA | 98ASA00418D |

# 12 Pinouts

## 12.1 Pinouts

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The IOMUX Controller (IOMUXC) Module is responsible for selecting which ALT functionality is available on each pin.

**NOTE**

The 176 LQFP parts are not pin compatible between the F-Series and R-Series families.

| 364 MAP BGA | 176 LQFP | Pin Name | Default | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 | EzPort |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Y2 | — | ADC0SE8 | N/A | | ADC0_SE8 | | | | | | | |
| W2 | — | ADC0SE9 | | | ADC0_SE9 | | | | | | | |
| W3 | — | ADC1SE8 | | | ADC1_SE8 | | | | | | | |
| Y3 | — | ADC1SE9 | | | ADC1_SE9 | | | | | | | |
| W1 | 41 | VREFH_ADC | | | VREFH_ADC | | | | | | | |
| U3 | 40 | VREFL_ADC | | | VREFL_ADC | | | | | | | |

| 364 MAP BGA | 176 LQFP | Pin Name | Default | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 | EzPort |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| U14 | 74 | EXT_ TAMPER1 | | | EXT_ TAMPER1 | | | | | | | |
| T13 | — | EXT_ TAMPER2/ EXT_WM0_ TAMPER_IN | | | EXT_ TAMPER2/ EXT_WM0_ TAMPER_IN | | | | | | | |
| U13 | — | EXT_ TAMPER3/ EXT_WM0_ TAMPER_ OUT | | | EXT_ TAMPER3/ EXT_WM0_ TAMPER_ OUT | | | | | | | |
| U12 | — | EXT_ TAMPER4/ EXT_WM1_ TAMPER_IN | | | EXT_ TAMPER4/ EXT_WM1_ TAMPER_IN | | | | | | | |
| U10 | — | EXT_ TAMPER5/ EXT_WM1_ TAMPER_ OUT | | | EXT_ TAMPER5/ EXT_WM1_ TAMPER_ OUT | | | | | | | |
| G7 | 2 | VDD | | | VDD | | | | | | | |
| J7 | — | VDD | | | VDD | | | | | | | |
| L7 | 22 | VDD | | | VDD | | | | | | | |
| H8 | 48 | VDD | | | VDD | | | | | | | |
| K8 | 85 | VDD | | | VDD | | | | | | | |
| M8 | 102 | VDD | | | VDD | | | | | | | |
| P8 | 125 | VDD | | | VDD | | | | | | | |
| G9 | 136 | VDD | | | VDD | | | | | | | |
| N9 | 174 | VDD | | | VDD | | | | | | | |
| H10 | — | VDD | | | VDD | | | | | | | |
| P10 | — | VDD | | | VDD | | | | | | | |
| G11 | — | VDD | | | VDD | | | | | | | |
| N11 | — | VDD | | | VDD | | | | | | | |
| H12 | — | VDD | | | VDD | | | | | | | |
| P12 | — | VDD | | | VDD | | | | | | | |
| G13 | — | VDD | | | VDD | | | | | | | |
| J13 | — | VDD | | | VDD | | | | | | | |
| L13 | — | VDD | | | VDD | | | | | | | |
| N13 | — | VDD | | | VDD | | | | | | | |
| H14 | — | VDD | | | VDD | | | | | | | |
| K14 | — | VDD | | | VDD | | | | | | | |
| M14 | — | VDD | | | VDD | | | | | | | |
| P14 | — | VDD | | | VDD | | | | | | | |
| A1 | 1 | VSS | | | VSS | | | | | | | |
| A20 | 13 | VSS | | | VSS | | | | | | | |

## Table 78. Functional Assignment Pins (continued)

| Signal Name | 364 MAP BGA | 176 LQFP (F-series ONLY) | Power Group | Pad Type | Default Mode (Reset) | Default Function | Input/ Output | Value |
|---|---|---|---|---|---|---|---|---|
| PTC7 | N2 | 17 | VDD33 | GPIO | ALT0 | GPIO | Disabled | |
| PTC8 | N4 | 18 | VDD33 | GPIO | ALT0 | GPIO | Disabled | |
| PTC9 | T15 | 77 | VDD33 | GPIO | ALT0 | GPIO | Disabled | |
| PTC10 | U15 | 78 | VDD33 | GPIO | ALT0 | GPIO | Disabled | |
| PTC11 | P4 | 20 | VDD33 | GPIO | ALT0 | GPIO | Disabled | |
| PTC12 | P3 | 21 | VDD33 | GPIO | ALT0 | GPIO | Disabled | |
| PTC13 | P1 | 23 | VDD33 | GPIO | ALT0 | GPIO | Disabled | |
| PTC14 | R1 | 26 | VDD33 | GPIO | ALT0 | GPIO | Disabled | |
| PTC15 | P2 | 27 | VDD33 | GPIO | ALT0 | GPIO | Disabled | |
| PTC16 | R3 | 29 | VDD33 | GPIO | ALT0 | GPIO | Disabled | |
| PTC17 | R4 | 28 | VDD33 | GPIO | ALT0 | GPIO | Disabled | |
| PTC26 | D16 | 153 | VDD33 | GPIO | ALT3 | RCON24 | Input | Disabled |
| PTC27 | E16 | 154 | VDD33 | GPIO | ALT3 | RCON25 | Input | Disabled |
| PTC28 | E15 | 155 | VDD33 | GPIO | ALT3 | RCON26 | Input | Disabled |
| PTC29 | C16 | 152 | VDD33 | GPIO | ALT3 | RCON27 | Input | Disabled |
| PTC30 | T8 | 58 | VDD33 | GPIO | ALT3 | RCON28 | Input | Disabled |
| PTC31 | W5 | 42 | VDD33 | GPIO | ALT3 | RCON29 | Input | Disabled |
| PTD0 | Y17 | 86 | VDD33 | GPIO | ALT0 | GPIO | Disabled | |
| PTD1 | Y18 | 87 | VDD33 | GPIO | ALT0 | GPIO | Disabled | |
| PTD2 | V18 | 88 | VDD33 | GPIO | ALT0 | GPIO | Disabled | |
| PTD3 | Y19 | 89 | VDD33 | GPIO | ALT0 | GPIO | Disabled | |
| PTD4 | W19 | 90 | VDD33 | GPIO | ALT0 | GPIO | Disabled | |
| PTD5 | W20 | 91 | VDD33 | GPIO | ALT0 | GPIO | Disabled | |
| PTD6 | V20 | 92 | VDD33 | GPIO | ALT0 | GPIO | Disabled | |
| PTD7 | V19 | 93 | VDD33 | GPIO | ALT0 | GPIO | Disabled | |
| PTD8 | U17 | 94 | VDD33 | GPIO | ALT0 | GPIO | Disabled | |
| PTD9 | U18 | 97 | VDD33 | GPIO | ALT0 | GPIO | Disabled | |
| PTD10 | U20 | 98 | VDD33 | GPIO | ALT0 | GPIO | Disabled | |
| PTD11 | T20 | 99 | VDD33 | GPIO | ALT0 | GPIO | Disabled | |
| PTD12 | T19 | 100 | VDD33 | GPIO | ALT0 | GPIO | Disabled | |
| PTD13 | T18 | 101 | VDD33 | GPIO | ALT0 | GPIO | Disabled | |
| PTD16 | D20 | 133 | VDD33 | GPIO | ALT0 | GPIO | Disabled | |
| PTD17 | E20 | 132 | VDD33 | GPIO | ALT0 | GPIO | Disabled | |
| PTD18 | E18 | 131 | VDD33 | GPIO | ALT0 | GPIO | Disabled | |
| PTD19 | F16 | 130 | VDD33 | GPIO | ALT0 | GPIO | Disabled | |
| PTD20 | F17 | 129 | VDD33 | GPIO | ALT0 | GPIO | Disabled | |
| PTD21 | F19 | 128 | VDD33 | GPIO | ALT0 | GPIO | Disabled | |

*Table continues on the next page...*

## Table 78. Functional Assignment Pins (continued)

| Signal Name | 364 MAP BGA | 176 LQFP (F-series ONLY) | Power Group | Pad Type | Default Mode (Reset) | Default Function | Input/ Output | Value |
|---|---|---|---|---|---|---|---|---|
| PTD22 | F20 | 126 | VDD33 | GPIO | ALT0 | GPIO | Disabled | |
| PTD23 | G20 | 124 | VDD33 | GPIO | ALT0 | GPIO | Disabled | |
| PTD24 | G19 | — | VDD33 | GPIO | ALT0 | GPIO | Disabled | |
| PTD25 | G18 | — | VDD33 | GPIO | ALT0 | GPIO | Disabled | |
| PTD26 | G16 | — | VDD33 | GPIO | ALT0 | GPIO | Disabled | |
| PTD27 | H16 | — | VDD33 | GPIO | ALT0 | GPIO | Disabled | |
| PTD28 | H17 | — | VDD33 | GPIO | ALT0 | GPIO | Disabled | |
| PTD29 | H18 | — | VDD33 | GPIO | ALT0 | GPIO | Disabled | |
| PTD30 | H20 | — | VDD33 | GPIO | ALT0 | GPIO | Disabled | |
| PTD31 | J20 | — | VDD33 | GPIO | ALT0 | GPIO | Disabled | |
| PTE0 | N16 | 103 | VDD33 | GPIO | ALT2 | BMODE1 | Input | Disabled |
| PTE1 | N18 | 104 | VDD33 | GPIO | ALT2 | BMODE0 | Input | Disabled |
| PTE2 | N19 | 105 | VDD33 | GPIO | ALT0 | GPIO | Disabled | |
| PTE3 | Y15 | 80 | VDD33 | GPIO | ALT0 | GPIO | Disabled | |
| PTE4 | N20 | 106 | VDD33 | GPIO | ALT0 | GPIO | Disabled | |
| PTE5 | T16 | — | VDD33 | GPIO | ALT0 | GPIO | Disabled | |
| PTE6 | W16 | — | VDD33 | GPIO | ALT0 | GPIO | Disabled | |
| PTE7 | M20 | 109 | VDD33 | GPIO | ALT3 | RCON0 | Input | Disabled |
| PTE8 | M19 | 110 | VDD33 | GPIO | ALT3 | RCON1 | Input | Disabled |
| PTE9 | M17 | 111 | VDD33 | GPIO | ALT3 | RCON2 | Input | Disabled |
| PTE10 | M16 | 112 | VDD33 | GPIO | ALT3 | RCON3 | Input | Disabled |
| PTE11 | L16 | 113 | VDD33 | GPIO | ALT3 | RCON4 | Input | Disabled |
| PTE12 | L17 | 114 | VDD33 | GPIO | ALT3 | RCON5 | Input | Disabled |
| PTE13 | Y16 | — | VDD33 | GPIO | ALT0 | GPIO | Disabled | |
| PTE14 | W15 | — | VDD33 | GPIO | ALT0 | GPIO | Disabled | |
| PTE15 | L18 | 115 | VDD33 | GPIO | ALT3 | RCON6 | Input | Disabled |
| PTE16 | L20 | 116 | VDD33 | GPIO | ALT3 | RCON7 | Input | Disabled |
| PTE17 | K20 | 117 | VDD33 | GPIO | ALT3 | RCON8 | Input | Disabled |
| PTE18 | K19 | 118 | VDD33 | GPIO | ALT3 | RCON9 | Input | Disabled |
| PTE19 | K18 | 119 | VDD33 | GPIO | ALT3 | RCON10 | Input | Disabled |
| PTE20 | A12 | 170 | VDD33 | GPIO | ALT3 | RCON11 | Input | Disabled |
| PTE21 | V16 | 81 | VDD33 | GPIO | ALT0 | GPIO | Disabled | |
| PTE22 | W17 | 84 | VDD33 | GPIO | ALT0 | GPIO | Disabled | |
| PTE23 | J17 | 122 | VDD33 | GPIO | ALT3 | RCON12 | Input | Disabled |
| PTE24 | D19 | 134 | VDD33 | GPIO | ALT3 | RCON13 | Input | Disabled |
| PTE25 | C19 | 135 | VDD33 | GPIO | ALT3 | RCON14 | Input | Disabled |
| PTE26 | C20 | 137 | VDD33 | GPIO | ALT3 | RCON15 | Input | Disabled |

*Table continues on the next page...*

## Table 79. Revision History

| Rev. No. | Date | Substantial Changes |
|---|---|---|
| | | Added Part Number Format figure<br>Updated the Fields table as per the device part numbers<br>Added Part Numbers table<br>Added External NPN Ballast section<br>In the LVD Dig Electrical Specs, minimum value of Upper Voltage Threshold and Lower Voltage threshold<br>In the FlexBus timing specifications table, clarified the Frequency of operation<br>In the Power consumption, filled TBDs. Updated footnotes<br>Rewritten the EMC radiated emissions operating behaviors table<br>In the GPIO DC Electrical characteristics table:<br>• Vhys test condition changed<br>• Added R_Keeper row<br>In the DDR operating conditions, changed the Vddi Min and Max values<br>In the Power sequencing table, rremoved some rows<br>In the Power Supply section, removed LVDS and removed the note<br>In the Recommended operating conditions table, updated min and max of VDD12_AFE and FA_VDD. Updated Min, Max, and Typ for VDD<br>Added the Recommended Connections for Unused Analog Interfaces table<br>In the 12-bit ADC Characteristics table, updated the typ and max values of TUE, DNL. INL, ZSE, FSE<br>Added Receive and Transmit signal timing specifications for MII interfaces<br>In the DSPI table, clarified the TBDs<br>In PLL 4, PLL 5, PLL 6 electrical characteristics tables, added footnotes<br>In the JTAG electrical table, clarified the TBDs<br>In the pinouts section, added Special Signal table<br>Added Power Supply pins section<br>Added Functional Assignment section |

*Table continues on the next page...*

## Table 79. Revision History (continued)

| Rev. No. | Date | Substantial Changes |
|---|---|---|
| | | in 12-bit ADC operating conditions section<br>• Updated figures for clarity in "12-bit DAC operating behaviors" section<br>• Updated figure "VideoADC supply scheme" in "VideoADC Specifications" section<br>• Editorial updates thorughout |
| Rev 8 | November 2014 | • In "Part number format" figure, updated explanation for '1'.<br>• In "Fields" table, updated definition of 'R'.<br>• In "External NPN ballast" section, updated recommendations for transistor selection.<br>• In "DDR parameters" section, updated table footnotes regarding typical condition.<br>• In "Power sequencing" table, added comment regarding SDRAMC_VDD1P5: "In case the Ballast transistor's collector is connected to the 1.5 V DRAM supply (instead of the 3.3 V supply), turn this 1.5 V supply on before turning on the 3.3V."<br>• In "VideoADC specifications" table, added supply current values.<br>• In "Receive and Transmit signal timing specifications," added the following note: "See the most current errata document when using the internally generated RXCLK and TXCLK clocks."<br>• Updated "QuadSPI timing" section, presenting data based on a negative edge data launch from the device and a negative edge data capture; updated the figure, "QuadSPI Input/Read timing (SDR mode)"; updated the table, "QuadSPI Input/Read timing (SDR mode)."<br>• For the "SDHC switching specifcations" table, added the statement, "A load of 50 pF is assumed"; updated max value for SD6, SDHC output delay (output valid).<br>• In the "24 MHz oscillator specifications" section, added the statement, "The crystal must be rated for a drive level of 250 µW or higher. An ESR (equivalent series |

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