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## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-A5 + Cortex®-M4 |
| Number of Cores/Bus Width | 2 Core, 32-Bit |
| Speed | 400MHz, 167MHz |
| Co-Processors/DSP | Multimedia; NEON™ MPE |
| RAM Controllers | LPDDR2, DDR3, DRAM |
| Graphics Acceleration | Yes |
| Display & Interface Controllers | DCU, GPU, LCD, VideoADC, VIU |
| Ethernet | 10/100Mbps (2) |
| SATA | - |
| USB | USB 2.0 OTG + PHY (1) |
| Voltage - I/O | 3.3V |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Security Features | ARM TZ, CAAM, HAB, RTIC, Secure JTAG, SNVS, Tamper, TZ ASC, TZ WDOG |
| Package / Case | 364-LFBGA |
| Supplier Device Package | 364-LFBGA (17x17) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/mvf60ns151cmk40 |

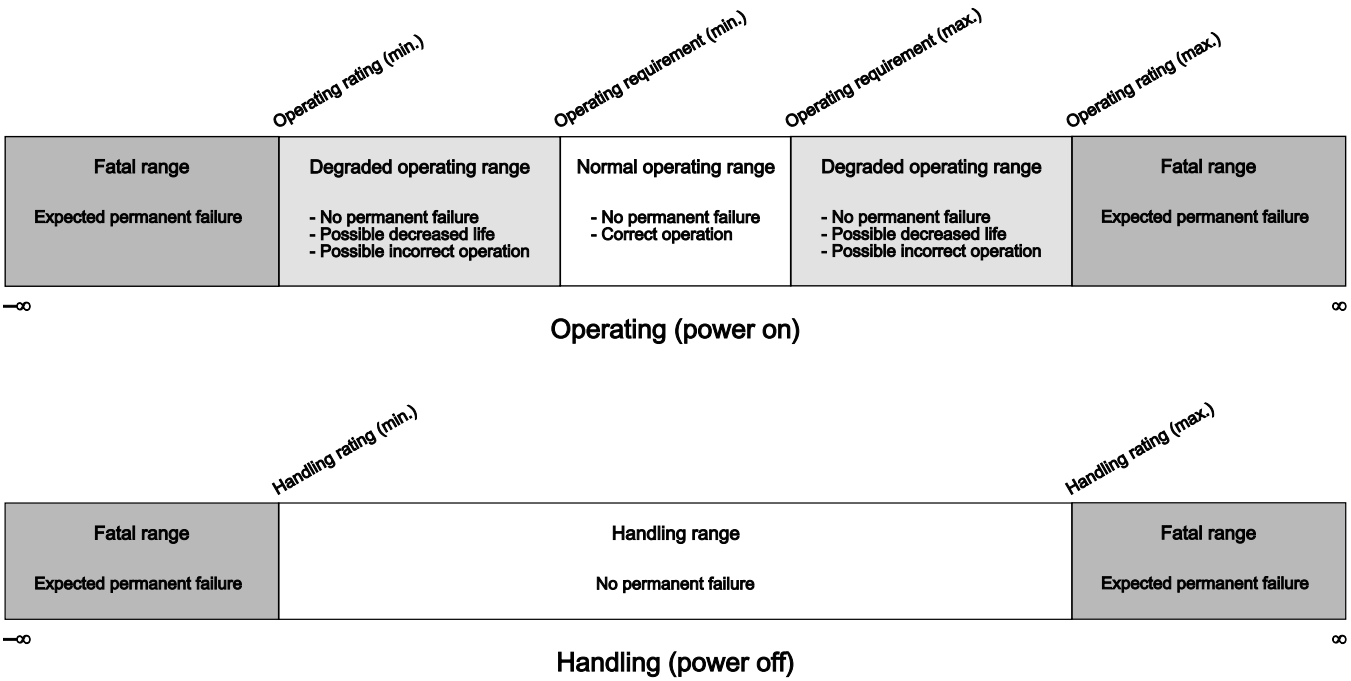
| Field | Description | Values |
|---|---|---|
| R | Revision | • 1 = Rev 1.x |
| T | Temperature range (°C) | • C = -40 °C to +85 °C $T_a$ |
| PP | Package type | • KU = 176LQFP<br>• MK = 364 MAPBGA |
| S | Speed | • Speed A5 Core<br>• 26 = 266MHz<br>• 40 = 400MHz<br>• 50 = 500MHz |

## 2.4 Part Numbers

This table lists the part numbers on the device.

| Part Number | Package | Description |
|---|---|---|
| MVF30NN151CKU26 | LQFP-EP 176 24*24*1.6 | A5-266, No Security, 176LQFP |
| MVF30NS151CKU26 | LQFP-EP 176 24*24*1.6 | A5-266, Security, 176LQFP |
| MVF50NN151CMK40 | MAP 364 17*17*1.5 P0.8 | A5-400, No Security, 364BGA |
| MVF50NS151CMK40 | MAP 364 17*17*1.5 P0.8 | A5-400, Security, 364BGA |
| MVF50NN151CMK50 | MAP 364 17*17*1.5 P0.8 | A5-500, No Security, 364BGA |
| MVF50NS151CMK50 | MAP 364 17*17*1.5 P0.8 | A5-500, Security, 364BGA |
| MVF51NN151CMK50 | MAP 364 17*17*1.5 P0.8 | A5-500, L2 Cache, No Security, 364BGA |
| MVF51NS151CMK50 | MAP 364 17*17*1.5 P0.8 | A5-500, L2 Cache, Security, 364BGA |
| MVF60NN151CMK40 | MAP 364 17*17*1.5 P0.8 | A5-400, M4, No Security, 364BGA |
| MVF60NS151CMK40 | MAP 364 17*17*1.5 P0.8 | A5-400, M4, Security, 364BGA |
| MVF60NN151CMK50 | MAP 364 17*17*1.5 P0.8 | A5-500, M4, No Security, 364BGA |
| MVF60NS151CMK50 | MAP 364 17*17*1.5 P0.8 | A5-500, M4, Security, 364BGA |
| MVF61NN151CMK50 | MAP 364 17*17*1.5 P0.8 | A5-500, M4, L2 Cache, No Security, 364BGA |
| MVF61NS151CMK50 | MAP 364 17*17*1.5 P0.8 | A5-500, M4, L2 Cache, Security, 364BGA |
| MVF62NN151CMK40 | MAP 364 17*17*1.5 P0.8 | A5-400, M4 Primary, No Security, 364BGA |

## 3.6 Relationship between ratings and operating requirements




## 3.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

## 3.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:

- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.

# 6.2 Nonswitching electrical specifications

## 6.2.1 VREG electrical specifications

### 6.2.1.1 HPREG electrical characteristics

**Table 2. HPREG electrical characteristics**

| Parameters | Min | Typ | Max | Unit | Comments |
|---|---|---|---|---|---|
| Power supply | 3.0 | 3.3 | 3.6 | V | - |
| Current Consumption | - | 1.2 | 1.5 | mA | @ no load |
| | - | 2.0 | 2.5 | mA | @ full load |
| Output current capacity | - | 600 | 1200[1] | mA | DC load current |
| Output voltage @ no load | | 1.23 | 1.26 | V | |
| Output voltage @ full load | 1.20 | 1.21 | | V | |
| External decoupling cap | 4.7 | | - | µF | - |
| | 0.05 | | 0.1 | Ohms | ESR of external cap |
| | | | 20 | mOhms | Total effective PAD+PCB trace resistances |
| PSRR with 4.7uF output cap | | | | | |
| @ DC @noload<br>@ DC @full load<br>@ worst case any frequency | | | -48<br>-40<br>-20 | dB | |

1. This is peak and not continuous maximum value.

### 6.2.1.2 LPREG electrical characteristics

**Table 3. LPREG electrical characteristics**

| Parameters | Min | Typ | Max | Unit | Comments |
|---|---|---|---|---|---|
| Power supply | 3.0 | 3.3 | 3.6 | V | |
| Current Consumption | 350 | 400 | | µA | @ no load |
| | - | 500 | 650 | µA | @ full load |
| Output current capacity | | 100 | 200 | mA | DC load current |
| Output voltage @ no load | | 1.22 | 1.240 | V | |
| Output voltage @ full load | 1.180 | | | V | |
| External decoupling cap | 4.7 | | | µF | |
| | 0.05 | | 0.1 | Ohms | ESR of external cap |
| | | | 20 | mOhms | Total PAD+PCB trace resistance |

*Table continues on the next page...*

## 6.2.2 LVD electrical specifications

### 6.2.2.1 Main Supply electrical characteristics

**Table 9. LVD_MAIN supply electrical characteristics**

| Main Supply LVD Parameters | Min | Typ | Max | Unit | Comments |
|---|---|---|---|---|---|
| Power supply | 3.0 | 3.3 | 3.6 | V | |
| Upper voltage threshold (value @27°C) | | 2.76 | 2.915 | V | |
| Lower voltage threshold (value @27°C) | 2.656 | 2.73 | | V | |
| Time constant of RC filter at LVD input (0.69*RC) | 3.3 | | | µs | 3.3 V noise rejection at LVD comparator input |

### 6.2.2.2 LVD DIG characteristics

**Table 10. LVD DIG electrical specifications [HPREG(RUN MODE) and LPREG(STOP MODE)]**

| LVD DIG Parameters | Min | Typ | Max | Unit | Comments |
|---|---|---|---|---|---|
| Power supply | 3.0 | 3.3 | 3.6 | V | |
| Upper voltage threshold | 1.135 | 1.16 | 1.185 | V | |
| Lower voltage threshold | 1.105 | 1.13 | 1.155 | V | |
| Time constant of RC filter at LVD input | 200 | | | ns | 1.2V noise rejection at the input of LVD comparator |

**Table 11. LVD DIG electrical specifications [ULPREG(STANDBY MODE)]**

| LVD DIG Parameters | Min | Typ | Max | Unit | Comments |
|---|---|---|---|---|---|
| Power supply | 3.0 | 3.3 | 3.6 | V | |
| Upper voltage threshold | 1.105 | 1.13 | 1.155 | V | |
| Lower voltage threshold | 1.075 | 1.10 | 1.125 | V | |
| Time constant of RC filter at LVD input | 200 | | | ns | 1.2V noise rejection at the input of LVD comparator |

## Table 24. LPDDR2 mode DC Electrical characteristics (continued)

| Symbol | Parameter | Test condition | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|---|
| Iin[2] | Input current (no pull-up/ down) | Vin = ovdd or 0 | | | 2.5 | uA | |
| Tri-state I/O supply current[2] | Icc-ovdd | Vin = ovdd or 0 | | | 4 | | |
| Tri-state vdd2p5 supply current[2] | Icc-vdd2p5 | Vi = vddi or 0 | | | 1.5 | | |
| Tri-state core supply current[2] | Icc-vddi | | | | 1 | | |
| Driver unit (240 Ohm) calibration resolution | Rres | | | | 10 | Ohm | |

1. The single-ended signals need to be within the respective limits (Vih(dc) max, Vil(dc) min) for single-ended signals as well as the limitations for overshoot and undershoot.
2. Typ condition: typ model, 1.2 V, and 25 °C junction. Max condition: bcs model, 1.26V, and -40 °C. Min condition: wcs model, 1.14V, and Tj 125 °C.

## Table 25. DDR3 mode DC Electrical characteristics

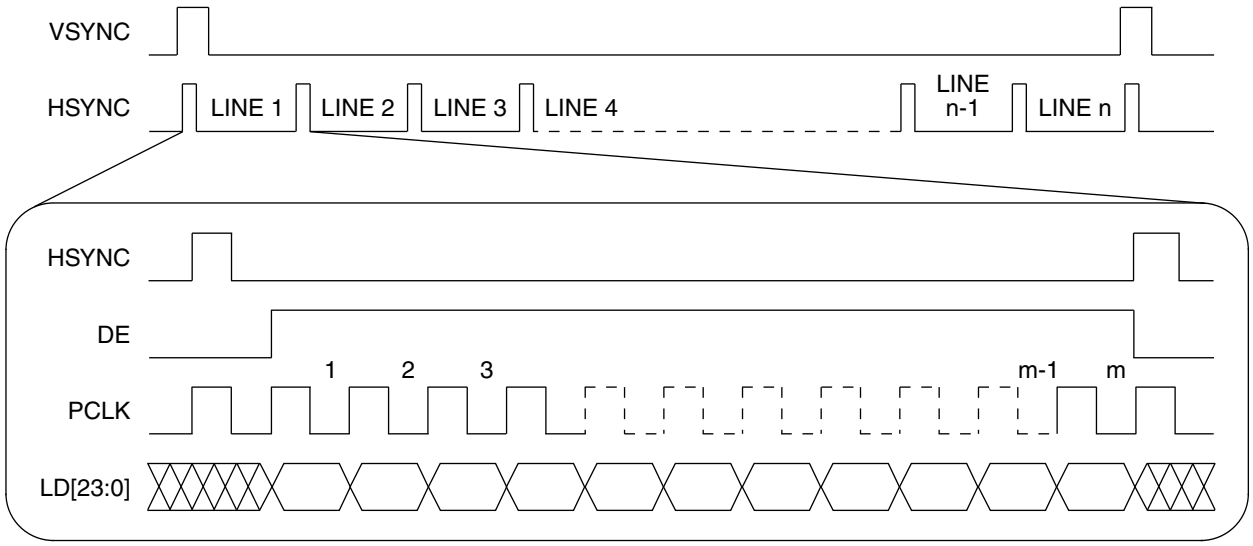
| Symbol | Parameter | Test condition | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|---|
| Voh | High-level output voltage | | 0.8*ovdd | | | V | Note that the JEDEC JESD79_3E specification supersedes any specification in this document |
| Vol | Low-level output voltage | Iol= 1mA | | | 0.2*ovdd | V | |
| Vref | Input reference voltage | | 0.49*ovdd | 0.5*ovdd | 0.51*ovdd | V | |
| Vih(dc) | DC input high voltage | | Vref+0.1 | | ovdd | V | |
| Vil(dc) | DC input low voltage | | ovss | | Vref-0.1 | V | |
| Vih(diff) | DC differential input logic high | | 0.2 | | Note[1] | V | |
| Vil(diff) | DC differential input logic low | | Note[1] | | -0.2 | V | |
| Vtt[2] | Termination voltage | Vin = ovdd or 0 | 0.49*ovdd | 0.5*ovdd | 0.51*ovdd | | |
| Iin[3] | Input current (no pullup/ pulldown) | Vi = 0 Vi = ovdd | | | 3 | uA | |

*Table continues on the next page...*

## Table 32. 12-bit ADC Characteristics ($V_{REFH}$ = $V_{DDAD}$, $V_{REFL}$ = $V_{SSAD}$) (continued)

| Characteristic | Conditions[1] | Symb | Min | Typ [2] | Max | Unit | Comment |
|---|---|---|---|---|---|---|---|
| | ADLSMP=0 ADSTS=10 | | | 0.8 | | | |
| | ADLSMP=0 ADSTS=11 | | | 0.85 | | | |
| | ADLSMP=1 ADSTS=00 | | | 0.95 | | | |
| | ADLSMP=1 ADSTS=01 | | | 1.05 | | | |
| | ADLSMP=1 ADSTS=10 | | | 1.15 | | | |
| | ADLSMP=1, ADSTS=11 | | | 1.25 | | | |
| Total Unadjusted Error | 12 bit mode | TUE | -2 | - | +5 | LSB[3] | With Max Averaging |
| | 10 bit mode | | -0.5 | - | +2 | | |
| | 8 bit mode | | -0.25 | - | +1.5 | | |
| Differential Non-Linearity | 12 bit mode | DNL | - | ±0.6 | ±1.5 | LSB[3] | Waiting for histogram method confirmation |
| | 10bit mode | | - | ±0.5 | ±1 | | |
| | 8 bit mode | | - | ±0.25 | ±0.5 | | |
| Integral Non-Linearity | 12 bit mode | INL | - | ±2 | ±4 | LSB[3] | Waiting for histogram method confirmation |
| | 10bit mode | | - | ±1 | ±2 | | |
| | 8 bit mode | | - | ±0.5 | ±1 | | |
| Zero-Scale Error | 12 bit mode | $E_{ZS}$ | - | +1.0 | ±1.6 | LSB[3] | VADIN = $V_{REFL}$ With Max Averaging |
| | 10bit mode | | - | ±0.4 | ±0.8 | | |
| | 8 bit mode | | - | ±0.1 | ±0.4 | | |
| Full-Scale Error | 12 bit mode | $E_{FS}$ | - | ±2 | ±3.5 | LSB[3] | VADIN = $V_{REFH}$ With Max Averaging |
| | 10bit mode | | - | ±0.5 | ±1 | | |
| | 8 bit mode | | - | ±0.25 | ±0.75 | | |
| Quantization Error | 12 bit mode | $E_Q$ | - | ±1 to 0 | | LSB[3] | |
| | 10bit mode | | - | ±0.5 | | | |
| | 8 bit mode | | - | ±0.5 | | | |
| Effective Number of Bits | 12 bit mode | ENOB | 10.1 | 10.7 | - | Bits | Fin = 100Hz |
| Signal to Noise plus Distortion | See ENOB | SINAD | SINAD = 6.02 x ENOB + 1.76 | | | dB | |
| Input Leakage Error | all modes | EIL | $I_{In}$ x RAS | | | mV | $I_{In}$ = 400 nA leakage current |
| Temp Sensor Slope | Across the full temperature range of the device | m | -- | 1.84 | -- | mV/°C | |
| Temp Sensor Voltage | 25°C | $V_{TEMP25}$ | - | 696 | - | mV | |

1. All accuracy numbers assume the ADC is calibrated with $V_{REFH}$=$V_{DDAD}$
2. Typical values assume $V_{DDAD}$ = 3.0 V, Temp = 25°C, $F_{adck}$=20 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
3. 1 LSB = ($V_{REFH}$ - $V_{REFL}$)/2N




### 9.2.1.2 Interface to TFT LCD Panels—Pixel Level Timings

This section provides the horizontal timing (timing of one line), including both the horizontal sync pulse and data. All parameters shown in the figure below are programmable. This timing diagram corresponds to positive polarity of the PCLK signal (meaning the data and sync signals change on the rising edge) and active-high polarity of the HSYNC, VSYNC and DE signals. The user can select the polarity of the HSYNC and VSYNC signals via the SYN_POL register, whether active-high or active-low. The default is active-high. The DE signal is always active-high. Pixel clock inversion and a flexible programmable pixel clock delay are also supported. They are programmed via the clock divide . The DELTA_X and DELTA_Y parameters are programmed via the DISP_SIZE register. The PW_H, BP_H and FP_H parameters are programmed via the HSYN PARA register. The PW_V, BP_V and FP_V parameters are programmed via the VSYN_PARA register.

**Table 36. LCD interface timing parameters—horizontal and vertical**

| Symbol | Characteristic | | Unit |
|---|---|---|---|
| $t_{PCP}$ | Display pixel clock period | 11.2 | ns |
| $t_{PWH}$ | HSYNC pulse width | PW_H * $t_{PCP}$ | ns |
| $t_{BPH}$ | HSYNC back porch width | BP_H * $t_{PCP}$ | ns |
| $t_{FPH}$ | HSYNC front porch width | FP_H * $t_{PCP}$ | ns |
| $t_{SW}$ | Screen width | DELTA_X * $t_{PCP}$ | ns |
| $t_{HSP}$ | HSYNC (line) period | (PW_H + BP_H + FP_H + DELTA_X ) * $t_{PCP}$ | ns |
| $t_{PWV}$ | VSYNC pulse width | PWV * $t_{HSP}$ | ns |
| $t_{BPV}$ | VSYNC back porch width | BP_V * $t_{HSP}$ | ns |
| $t_{FPV}$ | VSYNC front porch width | FP_V * $t_{HSP}$ | ns |
| $t_{SH}$ | Screen height | DELTA_Y * $t_{HSP}$ | ns |
| $t_{VSP}$ | VSYNC (frame) period | (PW_V + BP_V + FP_V + DELTA_Y ) * $t_{HSP}$ | ns |

## Table 52. NFC specifications

| Num | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $t_{CLS}$ | NFC_CLE setup time | $2T_H + T_L - 1$ | — | ns |
| $t_{CLH}$ | NFC_CLE hold time | $T_H + T_L - 1$ | — | ns |
| $t_{CS}$ | $\overline{\text{NFC\_CEn}}$ setup time | $2T_H + T_L - 1$ | — | ns |
| $t_{CH}$ | $\overline{\text{NFC\_CEn}}$ hold time | $T_H + T_L$ | — | ns |
| $t_{WP}$ | $\overline{\text{NFC\_WP}}$ pulse width | $T_L - 1$ | — | ns |
| $t_{ALS}$ | NFC_ALE setup time | $2T_H + T_L$ | — | ns |
| $t_{ALH}$ | NFC_ALE hold time | $T_H + T_L$ | — | ns |
| $t_{DS}$ | Data setup time | $T_L - 1$ | — | ns |
| $t_{DH}$ | Data hold time | $T_H - 1$ | — | ns |
| $t_{WC}$ | Write cycle time | $T_H + T_L - 1$ | — | ns |
| $t_{WH}$ | $\overline{\text{NFC\_WE}}$ hold time | $T_H - 1$ | — | ns |
| $t_{RR}$ | Ready to $\overline{\text{NFC\_RE}}$ low | $4T_H + 3T_L + 90$ | — | ns |
| $t_{RP}$ | $\overline{\text{NFC\_RE}}$ pulse width | $T_L + 1$ | — | ns |
| $t_{RC}$ | Read cycle time | $T_L + T_H - 1$ | — | ns |
| $t_{REH}$ | $\overline{\text{NFC\_RE}}$ high hold time | $T_H - 1$ | — | ns |
| $t_{IS}$ | Data input setup time | 11 | — | ns |

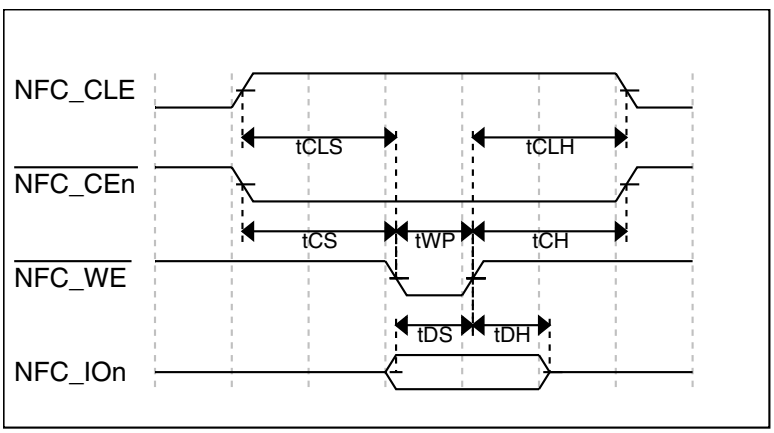



**Figure 34. Command latch cycle timing**

**NOTE**

Measurements were done using balanced load and 25 ohms resistor from outputs to VDD_REF.

### 9.5.4.5 LPDDR2 Read Cycle

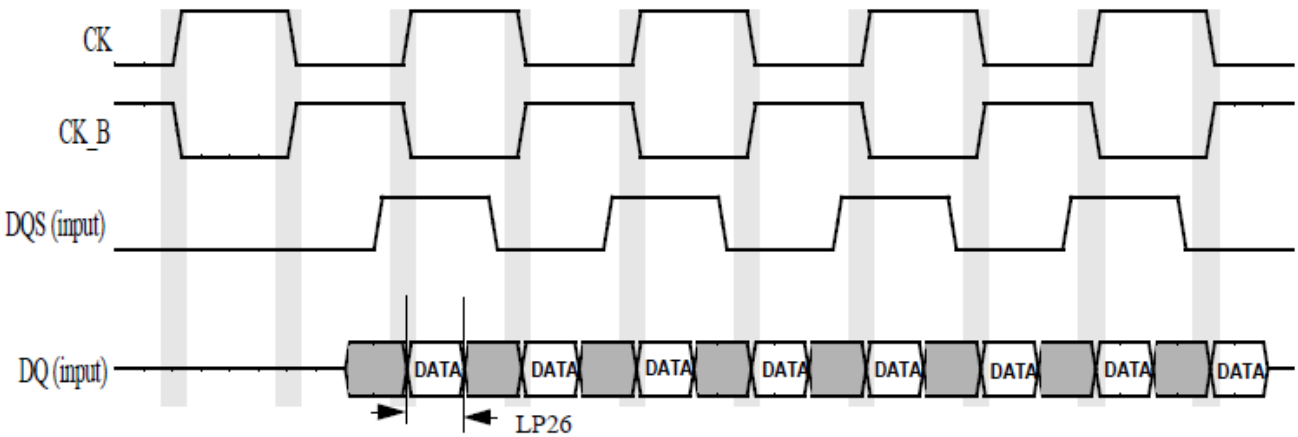



**Figure 45. LPDDR2 Read cycle**

**Table 58. LPDDR2 Read Cycle**

| ID | Parameter | Symbol | CK = 400 MHz | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| LP26 | Minimum required DQ valid window width for LPDDR2 | - | 270 | - | ps |

**NOTE**

To receive the reported setup and hold values, read calibration should be performed in order to locate the DQS in the middle of DQ window.

**NOTE**

All measurements are in reference to Vref level.

**NOTE**

Measurements were done using balanced load and 25 ohms resistor from outputs to VDD_REF

# 9.7 Clocks and PLL Specifications

## 9.7.1 24 MHz Oscillator Specifications

The system crystal oscillator consists of a Pierce-type structure running off the digital supply. A straight forward biased-inverter implementation is used. The crystal must be rated for a drive level of 250 µW or higher. An ESR (equivalent series resistance) of 80 Ω or less is recommended to achieve a gain margin of 5.

**Table 64. 24MHz external oscillator electrical characteristics**

| Symbol | Parameter | Condition | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $f_{osc}$ | Crystal oscillator range | — | — | 24 | — | MHz |
| $I_{osc}$ | Startup current | — | — | < 5 | — | mA |
| $t_{uposc}$ | Oscillator startup time | — | — | < 5 | — | ms |
| $C_{IN}$ | Input Capacitance | EXTAL and XTAL pins | — | 9 | — | pF |
| VIH | XTAL pin input high voltage | — | 0.8 x Vdd[1] | — | Vdd +0.3 | V |
| VIL | XTAL pin input low voltage | — | Vss -0.3 | — | 0.2 x Vdd | V |

1. $V_{DD}$ =1.1 V ± 10%, TA = -40 to +85 °C, unless otherwise specified.

## 9.7.2 32 KHz Oscillator Specifications

This block implements an amplifier that when combined with a suitable quartz crystal and external load capacitors implements a low power oscillator. It also implements a power mux such that it can be powered from either a ~3 V backup battery or VDDIO such as the oscillator consumes power from VDDIO when that supply is available and transitions to the back up battery when VDDIO is lost.

In addition, if the clock monitor determines that the OSC32K is not present, then the source of the 32 K will automatically switch to the 128kHz internal RC clock divided by 4.

The OSC32k runs from vdd_rtc supply, generated inside OSC32k itself from VDDIO/ VBAT. The target battery is a ~3 V coin cell. Proper choice of coin cell type is necessary for chosen VDDIO range. Appropriate series resistor (Rs) must be used when connecting the coin cell. Rs depends on the charge current limit that depends on the chosen coin cell.

For example:

## 9.7.6 PLL3 and PLL7 (480 MHz USB PLL) Electrical Parameters

**Table 69. PLL3 and PLL7 Electrical Parameters**

| Parameter | Value |
|---|---|
| Clock output range | 480 MHz PLL output |
| Reference clock | 24 MHz |
| Lock time | <425 reference cycles |
| Period jitter(p2p) | <140 ps |
| Duty Cycle | 48.9%~51.7% PLL output |

## 9.7.7 PLL5 (Ethernet PLL) Electrical Parameters

**Table 70. PLL5 Electrical Parameters**

| Parameter | Value |
|---|---|
| Clock output range | 500 MHz |
| Reference clock | 24 MHz |
| Lock time | <7500 reference cycles |
| Cycle to cycle jitter (p2p)[1] | <400ps @ 50 MHz |
| Duty Cycle | 45%~55% |

1. Jitter numbers are measured at divided PLL clock because high frequency cannot be brought-out IO pad.

## 9.7.8 PLL4 (Audio PLL) Electrical Parameters

**Table 71. PLL4 Electrical Parameters**

| Parameter | Value |
|---|---|
| Clock output range | 650 MHz ~1.3 GHz |
| Reference clock | 24 MHz |
| Lock time | <7500 reference cycles |
| Long term jitter(RMS) | <42ps @1128MHz |
| Period jitter(p2p)[1] | <115ps@1128MHz |
| Duty Cycle | 43%~57% |

1. Jitter numbers are measured at divided PLL clock because high frequency cannot be brought-out on IO pad.

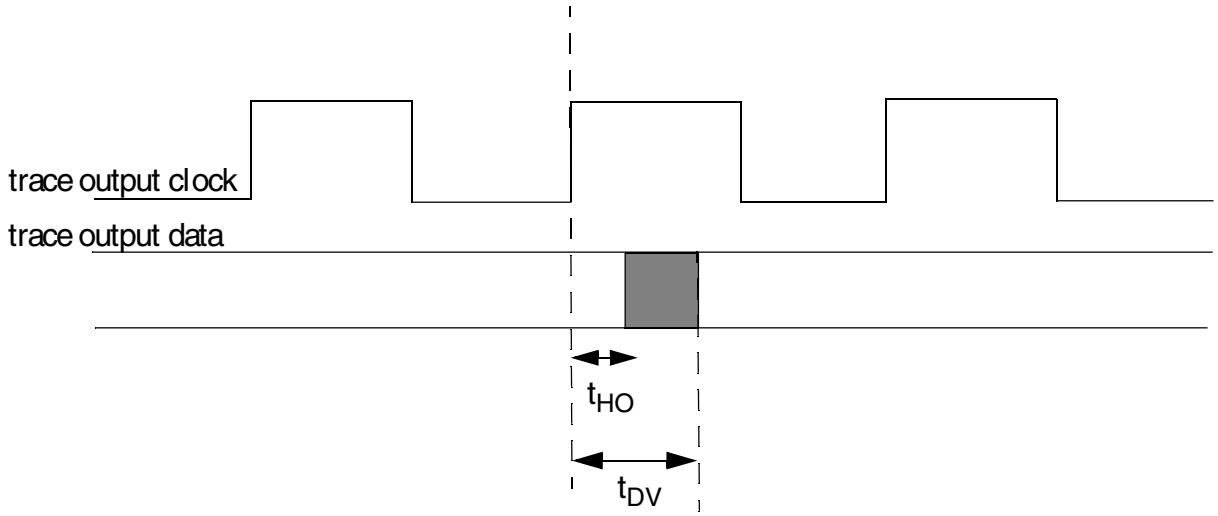



**Figure 57. Trace data specifications**

# 10 Thermal attributes

## 10.1 Thermal attributes

| Board type | Symbol | Description | 176LQFP | Unit | Notes |
|---|---|---|---|---|---|
| Single-layer (1s) | $R_{\theta JA}$ | Thermal resistance, junction to ambient (natural convection) | 50 | °C/W | 1, 2 |
| Four-layer (2s2p) | $R_{\theta JA}$ | Thermal resistance, junction to ambient (natural convection) | 32 | °C/W | 1,3 |
| Single-layer (1s) | $R_{\theta JMA}$ | Thermal resistance, junction to ambient (200 ft./ min. air speed) | 40 | °C/W | 1, 3 |
| Four-layer (2s2p) | $R_{\theta JMA}$ | Thermal resistance, junction to ambient (200 ft./ min. air speed) | 25 | °C/W | 1, 3 |
| — | $R_{\theta JB}$ | Thermal resistance, junction to board | 21 | °C/W | 4 |
| — | $R_{\theta JCtop}$ | Thermal resistance, junction to case top | 12 | °C/W | 5 |
| — | $\Psi_{JT}$ | Thermal characterization parameter, junction | 3 | °C/W | 6 |

| 364 MAP BGA | 176 LQFP | Pin Name | Default | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 | EzPort |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| V1 | 38 | VDDA33_ ADC | | | VDDA33_ ADC | | | | | | | |
| V2 | 39 | VSSA33_ ADC | | | VSSA33_ ADC | | | | | | | |
| U1 | 36 | DACO0 | | | DACO0 | | | | | | | |
| U2 | 37 | DACO1 | | | DACO1 | | | | | | | |
| Y4 | — | VADCSE0 | | | VADCSE0 | | | | | | | |
| U4 | — | VADCSE1 | | | VADCSE1 | | | | | | | |
| W4 | — | VADCSE2 | | | VADCSE2 | | | | | | | |
| V5 | — | VADCSE3 | | | VADCSE3 | | | | | | | |
| V3 | — | VDDA33_ AFE | | | VDDA33_ AFE | | | | | | | |
| V4 | — | VSSA33_AFE | | | VSSA33_AFE | | | | | | | |
| T5 | — | VDD12_AFE | | | VDD12_AFE | | | | | | | |
| R5 | — | VSS12_AFE | | | VSS12_AFE | | | | | | | |
| U5 | — | VADC_AFE_ BANDGAP | | | VADC_AFE_ BANDGAP | | | | | | | |
| Y13 | 73 | EXTAL | | | EXTAL | | | | | | | |
| W13 | 72 | XTAL | | | XTAL | | | | | | | |
| Y12 | 70 | EXTAL32 | | | EXTAL32 | | | | | | | |
| W12 | 71 | XTAL32 | | | XTAL32 | | | | | | | |
| T4 | 35 | RESETB/ RESET_OUT | RESETB/ RESET_OUT | | RESETB/ RESET_OUT | | | | | | | |
| N5 | 19 | PTA6 | | PTA6 | RMII_ CLKOUT | RMII_CLKIN/ MII0_TXCLK | | DCU1_ TCON11 | | | DCU1_R2 | |
| T3 | 34 | TEST | | | TEST | | | | | | | |
| T1 | 30 | Ext_POR | | | TEST2 | | | | | | | |
| V12 | 69 | DECAP_ V11_LDO_ OUT | | | DECAP_ V11_LDO_ OUT | | | | | | | |
| T11 | 65 | DECAP_ V25_LDO_ OUT | | | DECAP_ V25_LDO_ OUT | | | | | | | |
| T2 | 33 | BCTRL | | | BCTRL | | | | | | | |
| P5 | 31 | VDDREG | | | VDDREG | | | | | | | |
| T12 | 68 | VDD33_ LDOIN | | | VDD33_ LDOIN | | | | | | | |
| V11 | 67 | VSS | | | VSS | | | | | | | |
| U11 | 66 | VSS_KEL0 | | | VSS_KEL0 | | | | | | | |
| W14 | — | LVDS0P | | | LVDS0P | | | | | | | |
| Y14 | — | LVDS0N | | | LVDS0N | | | | | | | |
| K4 | 3 | JTCLK/ SWCLK | JTCLK/ SWCLK | PTA8 | JTCLK/ SWCLK | | | DCU0_R0 | | | MLBCLK | |

| 364 MAP BGA | 176 LQFP | Pin Name | Default | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 | EzPort |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A10 | — | DDR_A[13] | | | DDR_A13 | | | | | | | |
| C10 | — | DDR_A[12] | | | DDR_A12 | | | | | | | |
| D10 | — | DDR_A[11] | | | DDR_A11 | | | | | | | |
| D7 | — | DDR_A[10] | | | DDR_A10 | | | | | | | |
| B9 | — | DDR_A[9] | | | DDR_A9 | | | | | | | |
| A11 | — | DDR_A[8] | | | DDR_A8 | | | | | | | |
| A7 | — | DDR_A[7] | | | DDR_A7 | | | | | | | |
| A9 | — | DDR_A[6] | | | DDR_A6 | | | | | | | |
| B6 | — | DDR_A[5] | | | DDR_A5 | | | | | | | |
| A6 | — | DDR_A[4] | | | DDR_A4 | | | | | | | |
| B7 | — | DDR_A[3] | | | DDR_A3 | | | | | | | |
| A8 | — | DDR_A[2] | | | DDR_A2 | | | | | | | |
| C11 | — | DDR_A[1] | | | DDR_A1 | | | | | | | |
| C7 | — | DDR_A[0] | | | DDR_A0 | | | | | | | |
| D8 | — | DDR_BA[2] | | | DDR_BA2 | | | | | | | |
| C9 | — | DDR_BA[1] | | | DDR_BA1 | | | | | | | |
| C8 | — | DDR_BA[0] | | | DDR_BA0 | | | | | | | |
| B4 | — | DDR_CAS_b | | | DDR_CAS_b | | | | | | | |
| A5 | — | DDR_CKE[0] | | | DDR_CKE0 | | | | | | | |
| A2 | — | DDR_CLK[0] | | | DDR_CLK0 | | | | | | | |
| B2 | — | DDR_CLK_ b[0] | | | DDR_CLK_ b0 | | | | | | | |
| C5 | — | DDR_CS_ b[0] | | | DDR_CS_b0 | | | | | | | |
| D2 | — | DDR_D[15] | | | DDR_D15 | | | | | | | |
| H2 | — | DDR_D[14] | | | DDR_D14 | | | | | | | |
| C1 | — | DDR_D[13] | | | DDR_D13 | | | | | | | |
| G1 | — | DDR_D[12] | | | DDR_D12 | | | | | | | |
| E2 | — | DDR_D[11] | | | DDR_D11 | | | | | | | |
| H1 | — | DDR_D[10] | | | DDR_D10 | | | | | | | |
| D1 | — | DDR_D[9] | | | DDR_D9 | | | | | | | |
| J1 | — | DDR_D[8] | | | DDR_D8 | | | | | | | |
| G3 | — | DDR_D[7] | | | DDR_D7 | | | | | | | |
| C3 | — | DDR_D[6] | | | DDR_D6 | | | | | | | |
| J3 | — | DDR_D[5] | | | DDR_D5 | | | | | | | |
| F3 | — | DDR_D[4] | | | DDR_D4 | | | | | | | |
| G4 | — | DDR_D[3] | | | DDR_D3 | | | | | | | |
| D4 | — | DDR_D[2] | | | DDR_D2 | | | | | | | |
| H3 | — | DDR_D[1] | | | DDR_D1 | | | | | | | |
| F4 | — | DDR_D[0] | | | DDR_D0 | | | | | | | |
| G2 | — | DDR_DQM[1] | | | DDR_DQM1 | | | | | | | |

| 364 MAP BGA | 176 LQFP | Pin Name | Default | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 | EzPort |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| E4 | — | SDRAMC_ VDD1P5 | | | SDRAMC_ VDD1P5 | | | | | | | |
| D5 | — | SDRAMC_ VDD1P5 | | | SDRAMC_ VDD1P5 | | | | | | | |
| F5 | — | SDRAMC_ VDD1P5 | | | SDRAMC_ VDD1P5 | | | | | | | |
| H5 | — | SDRAMC_ VDD1P5 | | | SDRAMC_ VDD1P5 | | | | | | | |
| K5 | — | SDRAMC_ VDD1P5 | | | SDRAMC_ VDD1P5 | | | | | | | |
| E7 | — | SDRAMC_ VDD1P5 | | | SDRAMC_ VDD1P5 | | | | | | | |
| E9 | — | SDRAMC_ VDD1P5 | | | SDRAMC_ VDD1P5 | | | | | | | |
| D11 | — | SDRAMC_ VDD1P5 | | | SDRAMC_ VDD1P5 | | | | | | | |
| K3 | 10 | VDD33 | | | VDD33 | | | | | | | |
| N3 | 25 | VDD33 | | | VDD33 | | | | | | | |
| V8 | 52 | VDD33 | | | VDD33 | | | | | | | |
| C12 | 83 | VDD33 | | | VDD33 | | | | | | | |
| C15 | — | VDD33 | | | VDD33 | | | | | | | |
| U16 | 95 | VDD33 | | | VDD33 | | | | | | | |
| K17 | 108 | VDD33 | | | VDD33 | | | | | | | |
| N17 | 127 | VDD33 | | | VDD33 | | | | | | | |
| T17 | 140 | VDD33 | | | VDD33 | | | | | | | |
| C18 | 146 | VDD33 | | | VDD33 | | | | | | | |
| F18 | 158 | VDD33 | | | VDD33 | | | | | | | |
| W18 | 168 | VDD33 | | | VDD33 | | | | | | | |
| H7 | — | VSS | | | VSS | | | | | | | |
| K7 | 45 | VSS | | | VSS | | | | | | | |
| M7 | 82 | VSS | | | VSS | | | | | | | |
| P7 | — | VSS | | | VSS | | | | | | | |
| G8 | 96 | VSS | | | VSS | | | | | | | |
| J8 | 107 | VSS | | | VSS | | | | | | | |
| L8 | — | VSS | | | VSS | | | | | | | |
| N8 | 139 | VSS | | | VSS | | | | | | | |
| H9 | 144 | VSS | | | VSS | | | | | | | |
| J9 | 157 | VSS | | | VSS | | | | | | | |
| K9 | 175 | VSS | | | VSS | | | | | | | |
| L9 | 176 | VSS | | | VSS | | | | | | | |
| M9 | — | VSS | | | VSS | | | | | | | |
| P9 | — | VSS | | | VSS | | | | | | | |
| G10 | — | VSS | | | VSS | | | | | | | |

| 364 MAP BGA | 176 LQFP | Pin Name | Default | ALT0 | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 | EzPort |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| J10 | — | VSS | | | VSS | | | | | | | |
| K10 | — | VSS | | | VSS | | | | | | | |
| L10 | — | VSS | | | VSS | | | | | | | |
| M10 | — | VSS | | | VSS | | | | | | | |
| N10 | — | VSS | | | VSS | | | | | | | |
| H11 | — | VSS | | | VSS | | | | | | | |
| J11 | — | VSS | | | VSS | | | | | | | |
| K11 | — | VSS | | | VSS | | | | | | | |
| L11 | — | VSS | | | VSS | | | | | | | |
| M11 | — | VSS | | | VSS | | | | | | | |
| P11 | — | VSS | | | VSS | | | | | | | |
| G12 | — | VSS | | | VSS | | | | | | | |
| J12 | — | VSS | | | VSS | | | | | | | |
| K12 | — | VSS | | | VSS | | | | | | | |
| L12 | — | VSS | | | VSS | | | | | | | |
| M12 | — | VSS | | | VSS | | | | | | | |
| N12 | — | VSS | | | VSS | | | | | | | |
| H13 | — | VSS | | | VSS | | | | | | | |
| K13 | — | VSS | | | VSS | | | | | | | |
| M13 | — | VSS | | | VSS | | | | | | | |
| P13 | — | VSS | | | VSS | | | | | | | |
| G14 | — | VSS | | | VSS | | | | | | | |
| J14 | — | VSS | | | VSS | | | | | | | |
| L14 | — | VSS | | | VSS | | | | | | | |
| N14 | — | VSS | | | VSS | | | | | | | |
| N7 | — | FA_VDD | | | FA_VDD | | | | | | | |
| V14 | 75 | VBAT | | | VBAT | | | | | | | |
| — | FLG | VSS | | | VSS | | | | | | | |

## 12.2 Pinout diagrams

**NOTE**

The 176 LQFP parts are not pin compatible between the F and R series families devices.

**NOTE**

If tamper detection is not required, the tamper pins must be tied to ground.

## Table 75. RGPIO versus Pins (continued)

| RGPIO | In GPIO module | Corresponding Pin on the chip | IOMUX register name | IOMUX register address |
|---|---|---|---|---|
| RGPIO[40] | PORT1[8] | PTB18 | IOMUXC_PTB18 | 400480A0 |
| RGPIO[41] | PORT1[9] | PTB19 | IOMUXC_PTB19 | 400480A4 |
| RGPIO[42] | PORT1[10] | PTB20 | IOMUXC_PTB20 | 400480A8 |
| RGPIO[43] | PORT1[11] | PTB21 | IOMUXC_PTB21 | 400480AC |
| RGPIO[44] | PORT1[12] | PTB22 | IOMUXC_PTB22 | 400480B0 |
| RGPIO[45] | PORT1[13] | PTC0 | IOMUXC_PTC0 | 400480B4 |
| RGPIO[46] | PORT1[14] | PTC1 | IOMUXC_PTC1 | 400480B8 |
| RGPIO[47] | PORT1[15] | PTC2 | IOMUXC_PTC2 | 400480BC |
| RGPIO[48] | PORT1[16] | PTC3 | IOMUXC_PTC3 | 400480C0 |
| RGPIO[49] | PORT1[17] | PTC4 | IOMUXC_PTC4 | 400480C4 |
| RGPIO[50] | PORT1[18] | PTC5 | IOMUXC_PTC5 | 400480C8 |
| RGPIO[51] | PORT1[19] | PTC6 | IOMUXC_PTC6 | 400480CC |
| RGPIO[52] | PORT1[20] | PTC7 | IOMUXC_PTC7 | 400480D0 |
| RGPIO[53] | PORT1[21] | PTC8 | IOMUXC_PTC8 | 400480D4 |
| RGPIO[54] | PORT1[22] | PTC9 | IOMUXC_PTC9 | 400480D8 |
| RGPIO[55] | PORT1[23] | PTC10 | IOMUXC_PTC10 | 400480DC |
| RGPIO[56] | PORT1[24] | PTC11 | IOMUXC_PTC11 | 400480E0 |
| RGPIO[57] | PORT1[25] | PTC12 | IOMUXC_PTC12 | 400480E4 |
| RGPIO[58] | PORT1[26] | PTC13 | IOMUXC_PTC13 | 400480E8 |
| RGPIO[59] | PORT1[27] | PTC14 | IOMUXC_PTC14 | 400480EC |
| RGPIO[60] | PORT1[28] | PTC15 | IOMUXC_PTC15 | 400480F0 |
| RGPIO[61] | PORT1[29] | PTC16 | IOMUXC_PTC16 | 400480F4 |
| RGPIO[62] | PORT1[30] | PTC17 | IOMUXC_PTC17 | 400480F8 |
| RGPIO[63] | PORT1[31] | PTD31 | IOMUXC_PTD31 | 400480FC |
| RGPIO[64] | PORT2[0] | PTD30 | IOMUXC_PTD30 | 40048100 |
| RGPIO[65] | PORT2[1] | PTD29 | IOMUXC_PTD29 | 40048104 |
| RGPIO[66] | PORT2[2] | PTD28 | IOMUXC_PTD28 | 40048108 |
| RGPIO[67] | PORT2[3] | PTD27 | IOMUXC_PTD27 | 4004810C |
| RGPIO[68] | PORT2[4] | PTD26 | IOMUXC_PTD26 | 40048110 |
| RGPIO[69] | PORT2[5] | PTD25 | IOMUXC_PTD25 | 40048114 |
| RGPIO[70] | PORT2[6] | PTD24 | IOMUXC_PTD24 | 40048118 |
| RGPIO[71] | PORT2[7] | PTD23 | IOMUXC_PTD23 | 4004811C |
| RGPIO[72] | PORT2[8] | PTD22 | IOMUXC_PTD22 | 40048120 |
| RGPIO[73] | PORT2[9] | PTD21 | IOMUXC_PTD21 | 40048124 |
| RGPIO[74] | PORT2[10] | PTD20 | IOMUXC_PTD20 | 40048128 |
| RGPIO[75] | PORT2[11] | PTD19 | IOMUXC_PTD19 | 4004812C |
| RGPIO[76] | PORT2[12] | PTD18 | IOMUXC_PTD18 | 40048130 |
| RGPIO[77] | PORT2[13] | PTD17 | IOMUXC_PTD17 | 40048134 |
| RGPIO[78] | PORT2[14] | PTD16 | IOMUXC_PTD16 | 40048138 |

*Table continues on the next page...*

## Table 79. Revision History (continued)

| Rev. No. | Date | Substantial Changes |
|---|---|---|
| | | Updated Power supply diagram<br>Updated AC electrical specification of following modules: DCU, 12-bit DAC, Ethernet, Enhanced Serial Audio Interface (ESAI), SAI/I2S, Flexbus, MLB, DSPI, 24MHz External Oscillator, JTAG, Debug, ESAI, QSPI<br>Updated Thermal Attributes for 364 MAPBGA<br>Updated Freescale document number for 176-pin LQFP and 364 MAPBGA<br>Updated VREG specifications<br>Added WBREG specifications<br>Updated Recommended operating conditions table<br>Updated DAC INL and DNL charts<br>Updated Pinouts |
| Rev 4.1 | 12/2012 | Editorial updates: Removed instances of VF7xx and VF4xx. |
| Rev 5 | April 2013 | • Removed references to VF1xxR and refernces to F100 and 144 LQFP and 256 MAPBGA<br>• Replaced references to Auto and IMM by R-series and F-series respectively<br>• In the feature list, the ARM Core frequency changed to 500 MHz for F-series<br>• In the feature list, changed the DRAM controller frequency<br>• Updated Part Nummbering format<br>• Clarified the Fields table as per Marketing<br>• Sample numbers updated<br>• From the VREG electrical specifications tables, deleted pre-trimming rows and comments<br>• .In the HPREG electrical characteristics table, add footnote on maximum Output Current Capacity<br>• In the ULPREG electrical characteristics table, clarified max value of Output voltage @ no load and min value of Output voltage @ full load<br>• In the WBREG electrical characteristics table, clarified max value of Output voltage @ no load and min value of Output voltage @ full load |

*Table continues on the next page...*

## Table 79. Revision History (continued)

| Rev. No. | Date | Substantial Changes |
|---|---|---|
| | | • In the LVD electrical specifications table, added typ. values of Upper voltage threshold (value @27oC) and Lower voltage threshold (value @27oC)<br>• In the LVD DIG electrical specifications table, removed pretrimming values and clarified other values<br>• Updated LVD DIG electrical specifications values<br>• Updated LDO_1P1 tables<br>• Updated LDO_2P5 table<br>• Updated Power consumption operating behaviors tables<br>• Updated Absolute maximum ratings table<br>• Removed Temperature Voltage Monitor section to security RM<br>• Updated VideoADC Specifications table |
| Rev 5 | April 2013 | Updated pin muxing table with the following changes:<br>• Added MII0 including M AC0.TXDATA[2], MAC0.TXDATA[3], MAC0.RXDATA[2], MAC0.RXDATA[3] , MAC0.TXERR, MAC0.TXCLK, MAC0.RXCLK, MAC0.COL, MAC0.CRS<br>• Following signals muxed on same RMII0 Pins : MII0_MDC, MII0_MDC, MII0_RXD[1], MII0_RXD[0], MII0_RXER, MII0_TXD[1], MII0_TXD[0], MII0_TXEN<br>• Replaced FB_ALE with FB_MUXED_ALE, FB_CS4_b with FB_MUXED_TSIZ0, FB_TSIZ1 with FB_MUXED_TSIZ1, FB_TBST_b with FB_MUXED_TBST_b, FB_BE0_b with FB_MUXED_BE0_b<br>• Removed RCON18,19,20<br>• Replaced ESAI_SDO2 with ESAI_SDO2/ESAI_SDI3 Replaced ESAI_SDO3 with ESAI_SDO3/ ESAI_SDI2 Replaced ESAI_SDI0 with ESAI_SDO5/ESAI_SDI0 Replaced ESAI_SDI1 with ESAU_SDO4/ESAI_SDI1<br>• CKO1 additionally muxed at PAD40 |
| Rev 5 | May 2013 | In the Features, minor editorial updates |

*Table continues on the next page...*