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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A5 + Cortex®-M4
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	500MHz, 167MHz
Co-Processors/DSP	Multimedia; NEON™ MPE
RAM Controllers	LPDDR2, DDR3, DRAM
Graphics Acceleration	Yes
Display & Interface Controllers	DCU, GPU, LCD, VideoADC, VIU
Ethernet	10/100Mbps (2)
SATA	-
USB	USB 2.0 OTG + PHY (1)
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	-
Package / Case	364-LFBGA
Supplier Device Package	364-LFBGA (17x17)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mvf61nn151cmk50

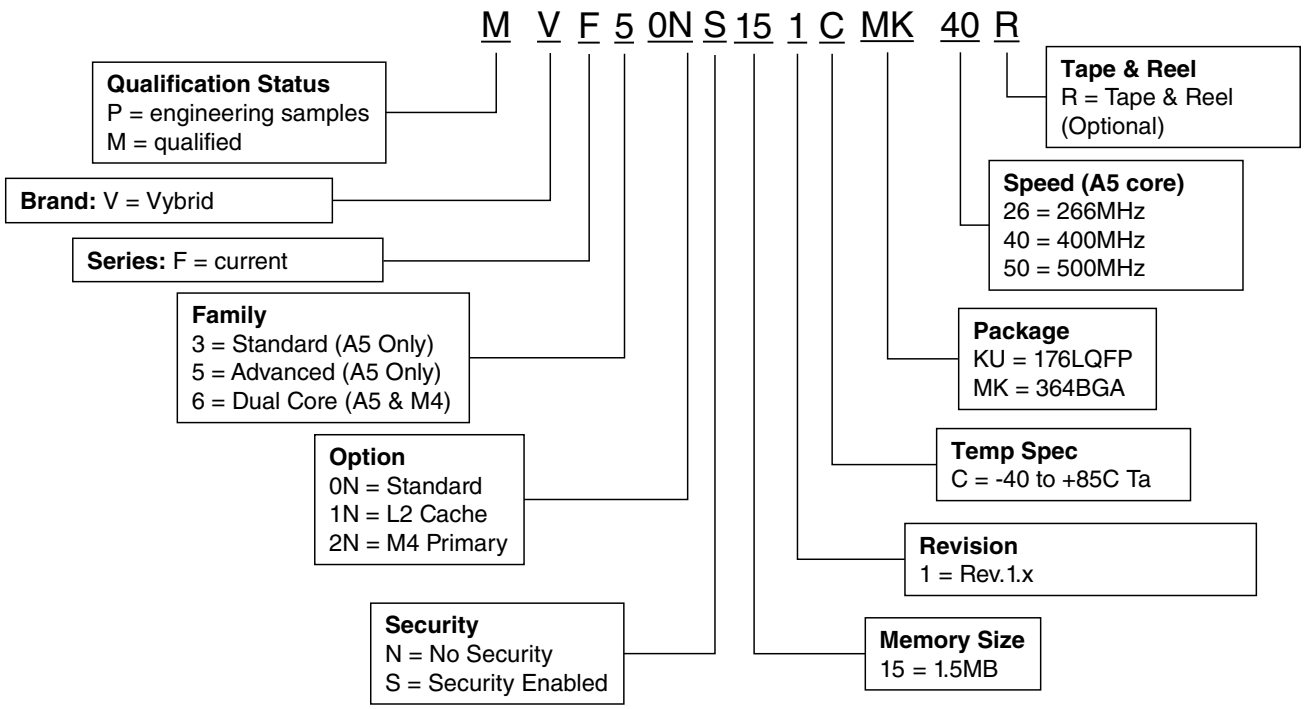


Figure 1. Part Number Format

2.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
Q	Qualification status	• P = Engineering samples • M = Qualified
B	Brand	• V = Vybrid
S	Series	• F = current
F	Family	• 3 = Standard (A5 Only) • 5 = Advanced (A5 Only) • 6 = Dual Core (A5 & M4)
O	Option	• 0N = Standard • 1N = L2 Cache • 2N = M4 Primary
S	Security	• N = No Security • S = Security Enabled
MM	Memory size	• 15 = 1.5 MB

Table continues on the next page...

6.2 Nonswitching electrical specifications

6.2.1 VREG electrical specifications

6.2.1.1 HPREG electrical characteristics

Table 2. HPREG electrical characteristics

Parameters	Min	Typ	Max	Unit	Comments
Power supply	3.0	3.3	3.6	V	-
Current Consumption	-	1.2	1.5	mA	@ no load
	-	2.0	2.5	mA	@ full load
Output current capacity	-	600	1200[1]	mA	DC load current
Output voltage @ no load		1.23	1.26	V	
Output voltage @ full load	1.20	1.21		V	
External decoupling cap	4.7		-	µF	-
	0.05		0.1	Ohms	ESR of external cap
			20	mOhms	Total effective PAD+PCB trace resistances
PSRR with 4.7uF output cap					
@ DC @noload @ DC @full load @ worst case any frequency			-48 -40 -20	dB	

1. This is peak and not continuous maximum value.

6.2.1.2 LPREG electrical characteristics

Table 3. LPREG electrical characteristics

Parameters	Min	Typ	Max	Unit	Comments
Power supply	3.0	3.3	3.6	V	
Current Consumption	350	400		µA	@ no load
	-	500	650	µA	@ full load
Output current capacity		100	200	mA	DC load current
Output voltage @ no load		1.22	1.240	V	
Output voltage @ full load	1.180			V	
External decoupling cap	4.7			µF	
	0.05		0.1	Ohms	ESR of external cap
			20	mOhms	Total PAD+PCB trace resistance

Table continues on the next page...

Table 8. General guidelines for selection of NPN ballast

Symbol	Parameters	Value	Unit	Comments
Hfe	Minimum DC current gain (Beta)	42.5		As BCTRL pin can not drive more than 20mA Minimum value of beta for a collector current of 0.85A comes out to be 42.5.
PD (Junction to ambient)	Minimum power dissipation @ TA=85 °C	2.04	W	Assuming 0.85A collector current with Collector voltage of Ballast 3.6V(max) we get VCE= 3.6V-1.2V=2.4V So power dissipated is 2.4V*0.85A=2.04W . This should be met for junction to ambient power dissipation spec of ballast
IcmaxDC peak	Maximum peak DC collector current	0.85	A	1.2A and above capacity device preferable
VBE	Maximum voltage that BCTRL pin can drive	1.25V for 0.85A @ 85 °C	V	For a VDDREG of 3.0 V (min.), BCTRL pin can drive voltage up to VDDREG - 0.5 V = 2.5 V. Since emitter of ballast is fixed at 1.25 V (max) if chosen ballast can supply 0.85 A collector current @ 85 °C with a base-to-emitter voltage of 1.25 V or lower, it is suitable for application.
Ft	Unity current gain Frequency of Ballast	50	MHz	

Reducing the collector-to-emitter voltage drop lowers the ballast transistor heat dissipation. This can be implemented in two ways:

1. By introducing series resistor or diode(s) between the collector and VDDREG (placed far enough from the transistor for proper cooling)
2. By connecting the collector to a separate lower-voltage supply

In both of the above cases the transistor has to stay away from the deep saturation region; otherwise, due to significant Hfe degradation, its base current exceeds the BCTRL output maximum value.

In general, the transistor must be selected such that its Vce saturation voltage is lower than the expected minimum Collector-Emitter voltage, and at the same time, the base current is less than 20 mA for the maximum expected collector current. More information can be found in collateral documentation at http://www.freescale.com

Table 20. GPIO DC Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
		VOH/VOL values are with respect to DSE=001[1]				
Vol	Low-level output voltage	Iol= 1mA			0.15	V
Vih [2]	High-Level DC input voltage		0.7*ovdd		ovdd	V
Vil[2]	Low-Level DC input voltage		0		0.3*ovdd	V
Vhys	Input Hysteresis	ovdd=3.3 V	250			mV
Vt+[2, 3]	Schmitt trigger VT+		0.5*ovdd			V
Vt-[2, 3]	Schmitt trigger VT-				0.5*ovdd	V
Iin[4]	Input current (no pull-up/down)	Vin = ovdd or 0	-1		1	uA
Iin_22pu	Input current (22KOhm PU)	Vin = 0			212	uA
		Vin = ovdd			1	
Iin_47pu	Input current (47KOhm PU)	Vin = 0			100	
		Vin = ovdd			1	
Iin_100pu	Input current (100KOhm PU)	Vin = 0			50	
		Vin = ovdd			1	
Iin_100pd	Input current (100KOhm PD)	Vin = 0			1	
		Vin = ovdd			50	
R_Keeper	Keeper Circuit Resistance	Vin = 0.3 x OVDD VI = 0.7 x OVDD	105		175	Ohm
Issod	Sink current in open drain mode	Vin = ovdd			7	mA
Issop	Sink/source current in Push Pull mode	Vin = ovdd			7	mA

1. For details about Software MUX Pad Control Register DSE bit, see IOMUX Controller chapter of the device reference manual.
2. To maintain a valid level, the transitioning edge of the input must sustain a constant slew rate (monotonic) from the current DC level through to the target DC level, VIL or VIH. Monotonic input transition time is from 0.1ns to 1s. Vil and Vih do not apply when hysteresis is enabled.
3. Hysteresis of 250 mV is guaranteed over all operating conditions when hysteresis is enabled.
4. Typ condition: typ model, 3.3V, and 25°C. Max condition: bcs model, 3.6V, and -40°C. Min condition: wcs model, 3.0V and 85 °C. These values are for digital IO buffer cells.

1. Vid(ac) specifies the input differential voltage |Vtr-Vcp| required for switching, where Vtr is the “true” input signal and Vcp is the “complementary” input signal. The Minimum value is equal to Vih(ac)-Vil(ac).
2. The typical value of Vix(ac) is expected to be about 0.5*ovdd, and Vix(ac) is expected to track variation of ovdd. Vix(ac) indicates the voltage at which differential input signal must cross.

Table 27. DDR3 mode AC Electrical characteristics

Symbol	Parameter	Test condition	Min	Max	Unit	Notes
Vih(ac)	AC input logic high		Vref+0.175	ovdd	V	Note that the JEDEC JESD79_3E specification supersedes any specification in this document
Vil(ac)	AC input logic low		ovss	Vref-0.175	V	
Vidh(ac)[1]	AC differential input high voltage		0.35	-	V	
Vidl(ac)[1]	AC differential input low voltage		0.35		V	
Vix(ac)[2]	AC differential input crosspoint voltage	relative to ovdd/2	Vref-0.15	Vref+0.15	V	
Vpeak	Over/undershoot peak			0.4	V	
Varea	Over/undershoot area (above ovdd or below ovss)	at 800 MHz data rate		0.5	V*ns	
tsr	Single output slew rate		0.4	2	V/ns	
tskd	Skew between pad rise/fall asymmetry + skew cased by SSN			0.2	ns	

1. Vid(ac) specifies the input differential voltage |Vtr-Vcp| required for switching, where Vtr is the “true” input signal and Vcp is the “complementary” input signal. The Minimum value is equal to Vih(ac)-Vil(ac).
2. The typical value of Vix(ac) is expected to be about 0.5*ovdd, and Vix(ac) is expected to track variation of ovdd. Vix(ac) indicates the voltage at which differential input signal must cross.

8 Power supplies and sequencing

8.1 Power sequencing

Table 28. Power sequencing

Power Supply (PKG Level)	Board Level Power Nets	Parameters	Power Order	Comment
VBAT	VBAT	Battery supply in case of LDOIN fails	NA	

Table continues on the next page...

Table 28. Power sequencing (continued)

Power Supply (PKG Level)	Board Level Power Nets	Parameters	Power Order	Comment
VDD33_LDOIN	VDD33	LDO input supply (LDO1P1, LDO2P5, LDO1P1_RTC)	1	VDD33_LDOIN,VDDREG and VDD33 should come from a common supply source (represented as 3.3V SMPS in the Figure 4)
VDDREG	VDD33	Device PMU regulator and External ballast supply	1	
VDD33	VDD33	GPIO 3.3V IO supply, LCD Supply	1	
SDRAMC_VDD1P5	SDRAMC_VDD1P5	1.2/1.5 DDR Main IO supply	NA	In case the Ballast transistor's collector is connected to the 1.5V DRAM supply (instead of the 3.3V supply), turn this 1.5V supply on before turning on the 3.3V.
VDDA33_ADC	VDDA33_ADC	3.3V supply for ADC, DAC and IO segment	1	
VREFH_ADC	VREFH_ADC	High Reference of ADC, DAC	1	
VDDA33_AFE	VDDA33_AFE	3.3V supply of AFE (Video ADC)	1	
VDD12_AFE	VDD	1.2V supply for AFE (Video ADC)	2	
FA_VDD	VDD	Shorted with VDD at Board Level in 364BGA (Test pin only)	NA	
VDD	VDD	1.2V core supply from External ballast	2	
USB0_VBUS 1	USB_VBUS	VBUS supply for USB	NA	
USB1_VBUS 2	USB_VBUS	VBUS supply for USB	NA	

1. Power sequencing of USB0_VBUS is independent of any other power supply.
2. Power sequencing of USB1_VBUS is independent of any other power supply.

NOTE

NA stands for no sequencing needs, for example, the supply can come in any order.

NOTE

All supplies grouped together e.g. 1,2, others. These have no power sequencing restriction in between them.

NOTE

If none of the SDRAMC pins are connected on the board, the SDRAMC supply could be left floating.

NOTE

At power up, 1.2V supply will follow 3.3V supply. At power down, it should be checked that 1.2V falls before 3.3V.

NOTE

The standby current on USBx_VBUS is 300 - 500 uA. This is well below the 2.5 mA limit set by the USB 2.0 specification.

8.4 Recommended operating conditions

Table 30. Recommended operating conditions

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
USB0_VBUS	VBUS supply for USB w.r.t USB0_GND		4.4	5	5.25	V
USB1_VBUS	VBUS supply for USB w.r.t USB1_GND		4.4	5	5.25	V
USB_DCAP	USB LDO 5V->3 V Output	External DCAP (10uF termination for USBREG)		3		V
VBAT	Battery supply in case of LDOIN fails	External CAP 0.1uF	2.4	3.3	3.6	V
VDD33_LDOIN	LDO input supply		3	3.3	3.6	V
DECAP_V11_LDO_OUT	LDO 3.3V -> 1.1V Output	Recommended External DCAP: 1uF(Min) 10uF (Max)		1.1		V
DECAP_V25_LDO_OUT	LDO 3.3V -> 2.5 Output for PLL, DDR pre-driver, EFUSE	Recommended External DCAP: 1uF(Min) 10uF (Max)		2.5		V
VDD33	GPIO 3.3V IO supply	External CAP (10uF)	3	3.3	3.6	V
VDDREG	Device PMU regulator and External ballast supply	External CAP (10uF)	3	3.3	3.6	V
VDDA33_ADC	3.3V supply for ADC, DAC and IO segment	External CAP (10uF)	3	3.3	3.6	V
VREFH_ADC	High reference voltage for ADC and DAC	Relation with VDDDA33_ADC (1uF)	2.5	3.3	VDDA33_ADC	V
VREFL_ADC	Low reference voltage for ADC and DAC	External CAP (10uF)		0		V
VDDA33_AFE	3.3V supply of AFE (Video ADC)	External CAP 10uF	3	3.3	3.6	V
VDD12_AFE	1.2V supply for AFE (Video ADC)		1.16	1.23	1.26	V
FA_VDD	For testing purpose only should be shorted to VDD on board.		1.16	1.23	1.26	V
VDD[1]	1.2V core supply	4.7uF with a low ESR value (100 milliohms)	1.16	1.23	1.26	V
USB0_GND	Ground supply for USB			0		V
USB1_GND	Ground supply for USB			0		V
VSS_KEL0	USB LDO ground output			0		V
VSS	VSS ground			0		V
VSSA33_ADC	Ground supply for ADC, DAC and IO segment			0		V

Table continues on the next page...

Table 34. 12-bit DAC operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{DACHP}	Full-scale settling time (0x080 to 0xF7F) — high-power mode	—	3	5	µs	1
$t_{CCDACLP}$	Code-to-code settling time (0xBF8 to 0xC08)				µs	1
	low-power mode	—	5	—		
	high-power mode	—	1	—		
$V_{dacoutl}$	DAC output voltage range low — high-speed mode, no load, DAC set to 0x000	—	—	100	mV	
$V_{dacouth}$	DAC output voltage range high — high-speed mode, no load, DAC set to 0xFFF	V_{DACR} −100	—	V_{DACR}	mV	
INL	Integral non-linearity error — high speed mode	—	—	±8	LSB	2
DNL	Differential non-linearity error — V_{DACR} = VREF_OUT	—	—	±1	LSB	3
V_{OFFSET}	Offset error	—	±0.4	±0.8	%FSR	4
E_G	Gain error	—	±0.1	±0.6	%FSR	4
PSRR	Power supply rejection ratio, V_{DDA} =3 V, T = 25 C		70		dB	
T_{CO}	Temperature coefficient offset voltage	—	3.7	—	µV/C	5
T_{GE}	Temperature coefficient gain error	—	0.000421	—	%FSR/C	
A_C	Offset aging coefficient	—	—	100	µV/yr	
Rop	Output resistance load = 3 kΩ	—	—	250	Ω	
SR	Slew rate -80h→ F7Fh→ 80h				V/µs	
	High power (SP_{HP})		1.7	3		
	Low power (SP_{LP})		0.3	0.6		
CT	Channel to channel cross talk	—	70		dB	

1. Settling within ±1 LSB
2. The INL is measured for 0+100mV to V_{DACR}−100 mV
3. The DNL is measured for 0+100mV to V_{DACR}−100 mV
4. Calculated by a best fit curve from V_{SS}+100 mV to V_{DACR}−100 mV
5. VDDA = 3.0V, reference select set for VDDA (DACx_CO:DACRFS = 1), high power mode(DACx_C0:LPEN = 0), DAC set to 0x800, Temp range from -40 °C to 85 °C

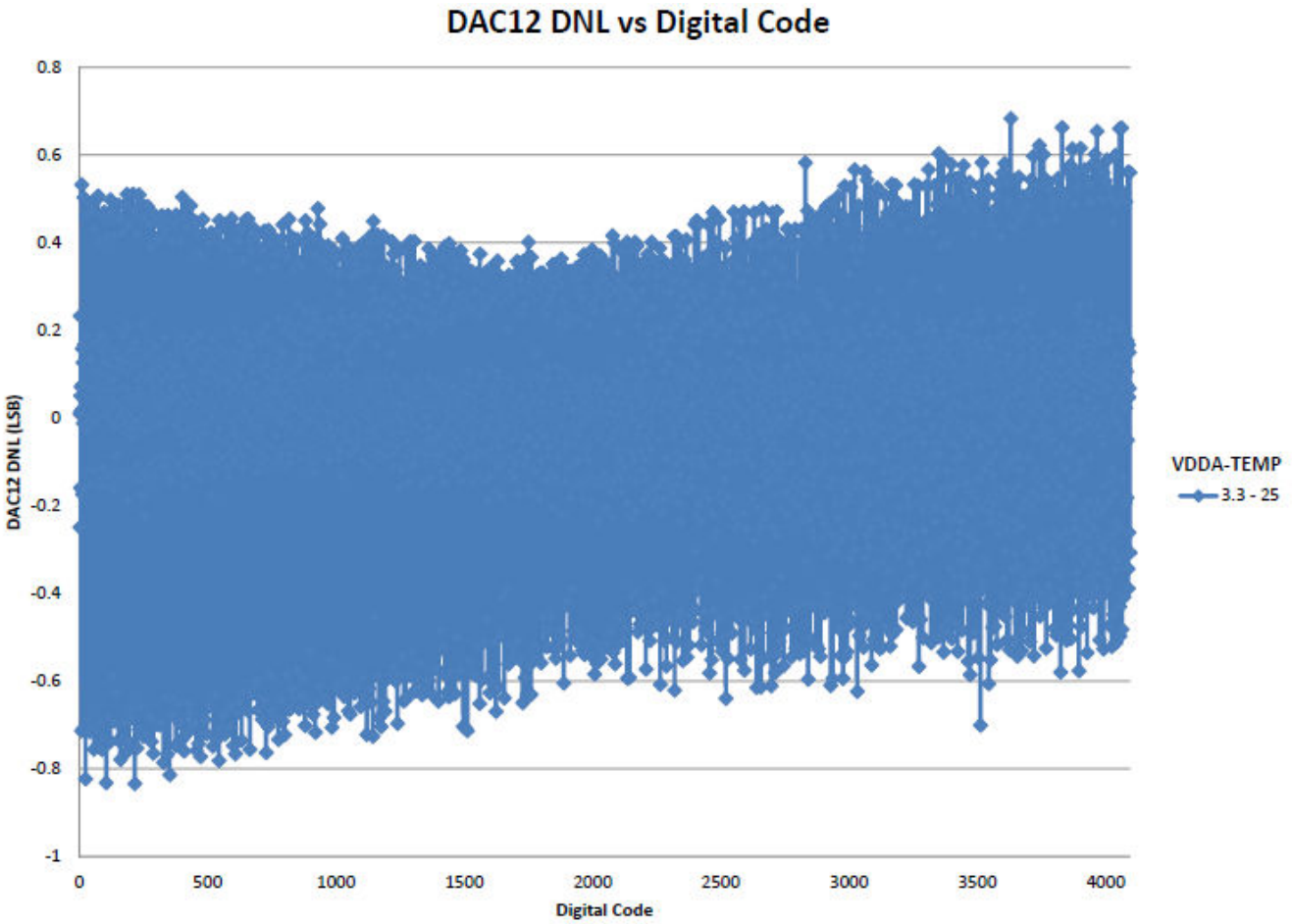


Figure 10. DNL error vs. digital code

Table 35. VideoADC Specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{BG}	Bandgap voltage	—	0.6	—	V	Bandgap voltage on VADC_AFE_BANDGAP pin. Pin should be decoupled with a 100nF capacitor

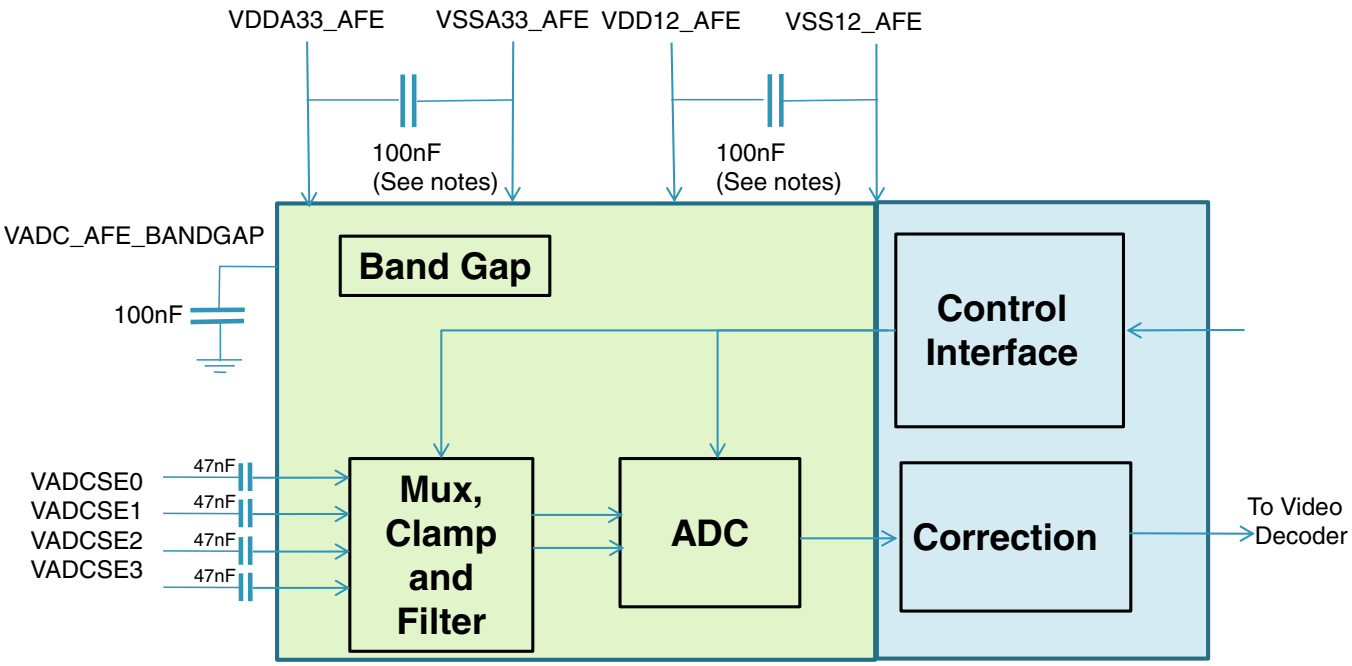


Figure 12. VideoADC supply scheme

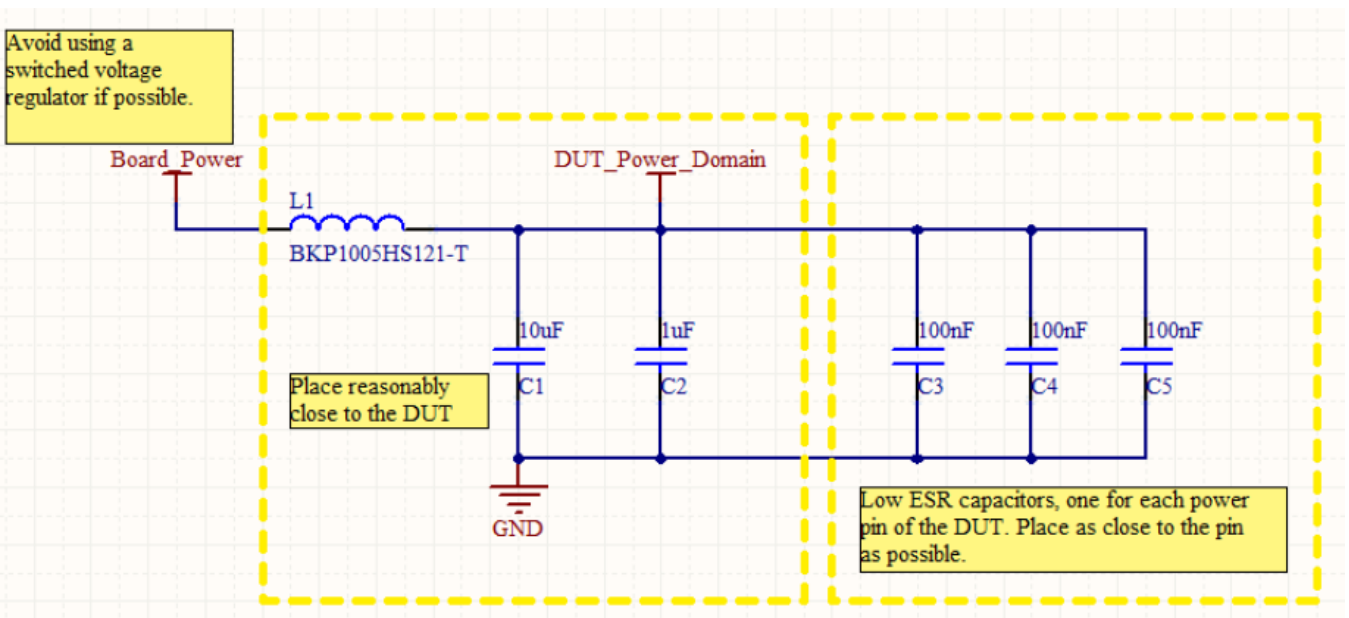


Figure 13. VideoADC supply decoupling

Table 40. Receive signal timing for RMII interfaces (continued)

	Characteristic	RMII Mode		Unit
		Min	Max	
E4, E8	RMII_CLK pulse width low	35%	65%	RMII_CLK period
E1	RXD[1:0], CVS_DV, RXER to RMII_CLK setup	4	—	ns
E2	RMII_CLK to RXD[1:0], CRS_DV, RXER hold	2	—	ns
E6	RMII_CLK to TXD[1:0], TXEN valid	—	14	ns
E5	RMII_CLK to TXD[1:0], TXEN invalid	4	—	ns

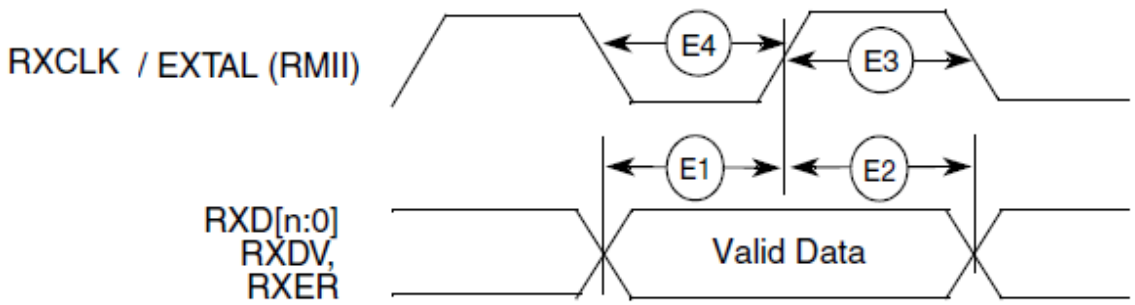


Figure 19. RMII receive signal timing diagram

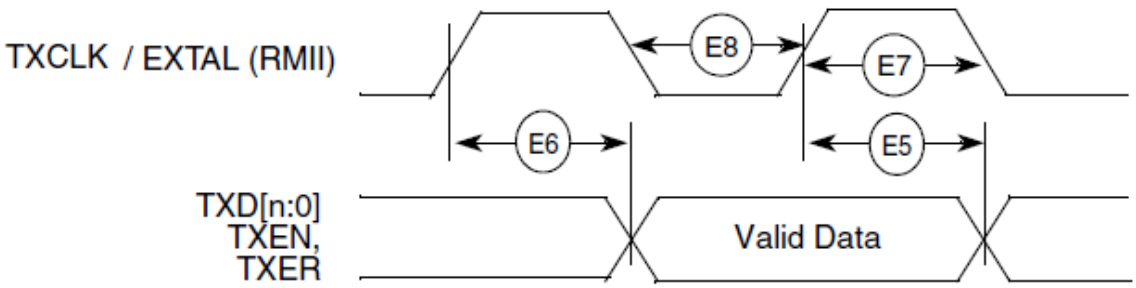


Figure 20. RMII transmit signal timing diagram

NOTE

See the most current device errata document when using the internally generated RXCLK and TXCLK clocks.

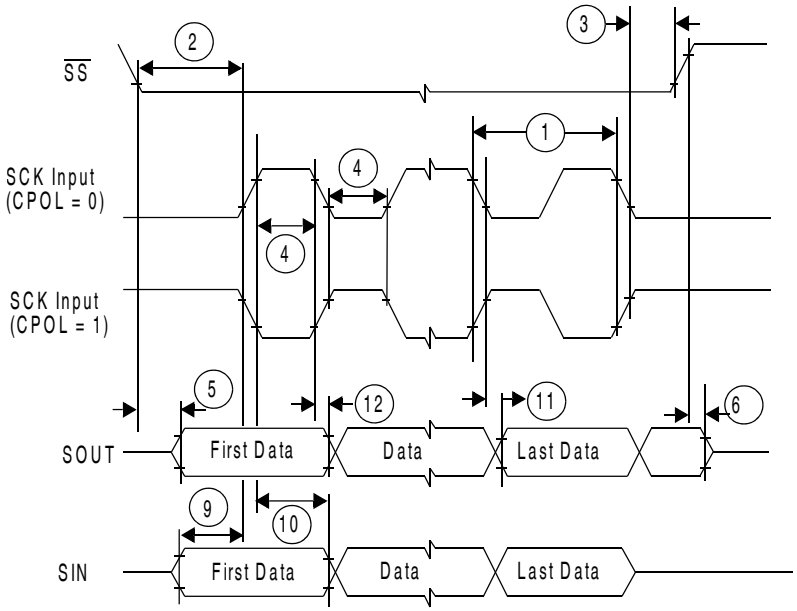


Figure 49. DSPI classic SPI timing slave, CPHA=0

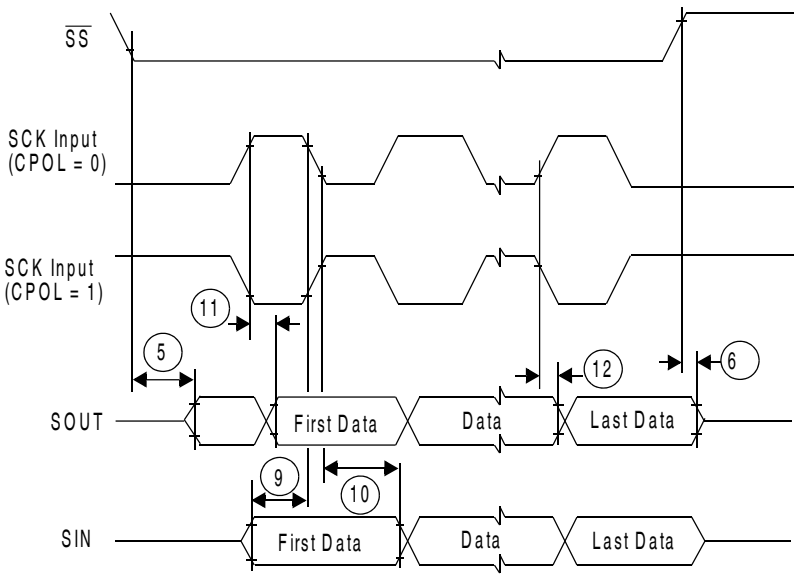


Figure 50. DSPI classic SPI timing slave, CPHA=1

9.6.2 I2C timing

Table 61. I2C input timing specifications — SCL and SDA[1]

No.	Parameter	Min.	Max.	Unit
1	Start condition hold time	2	—	PER_CLK Cycle[2]
2	Clock low time	8	—	PER_CLK Cycle

Table continues on the next page...

Table 66. Fast internal oscillator electrical characteristics (continued)

Symbol	Parameter	Condition[1]	Value			
			Min	Typ	Max	Unit
RCMVAR	RC oscillator variation in temperature and supply with respect to f_{RC} at T_A = 55 °C in high frequency configuration		-5		+5	%

1. V_{DD} = 1.2 V , T_A = -40 to +85 °C, unless otherwise specified.

9.7.4 Slow internal RC oscillator (128 KHz) electrical characteristics

This section describes a slow internal RC oscillator (SIRC). This can be used as the reference clock for the RTC module.

Table 67. Slow internal RC oscillator electrical characteristics

Symbol	Parameter	Condition[1]	Value			
			Min	Typ	Max	Unit
f_{RCL}	RC oscillator low frequency	T_A= 25 °C, trimmed	—	128	—	kHz
I_{RCL}	RC oscillator low frequency current	T_A= 25 °C, trimmed	—	3.1		µA
RCLTRIM	RC oscillator precision after trimming of f_{RCL}	T_A= 25 °C	-1	—	+1	%
RCLVAR 3	RC oscillator variation in temperature and supply with respect to f_{RC} at T_A = 55 °C in high frequency configuration	High frequency configuration	-5	—	+5	%

1. V_{DD} = 1.2 V , T_A = -40 to +85 °C, unless otherwise specified.

9.7.5 PLL1 and PLL2 (528 MHz System PLL) Electrical Parameters

Table 68. PLL1 and PLL2 Electrical Parameters

Parameter	Value
Clock output range	528 MHz PLL output
Reference clock	24 MHz
Lock time	<7500 reference cycles
Period jitter(p2p)	<140ps
Duty Cycle	48.9%~51.7% PLL output

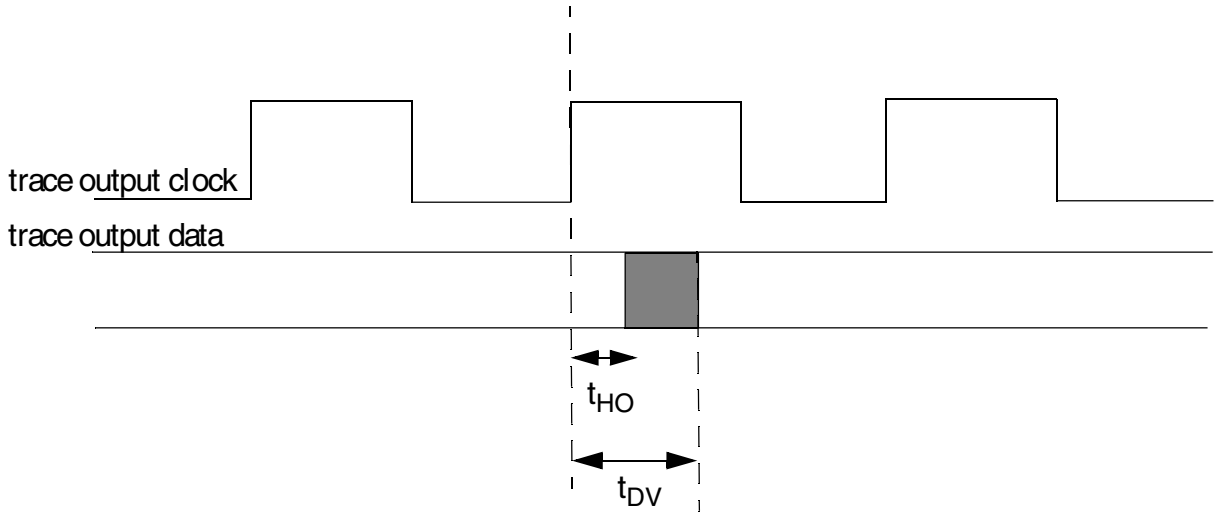


Figure 57. Trace data specifications

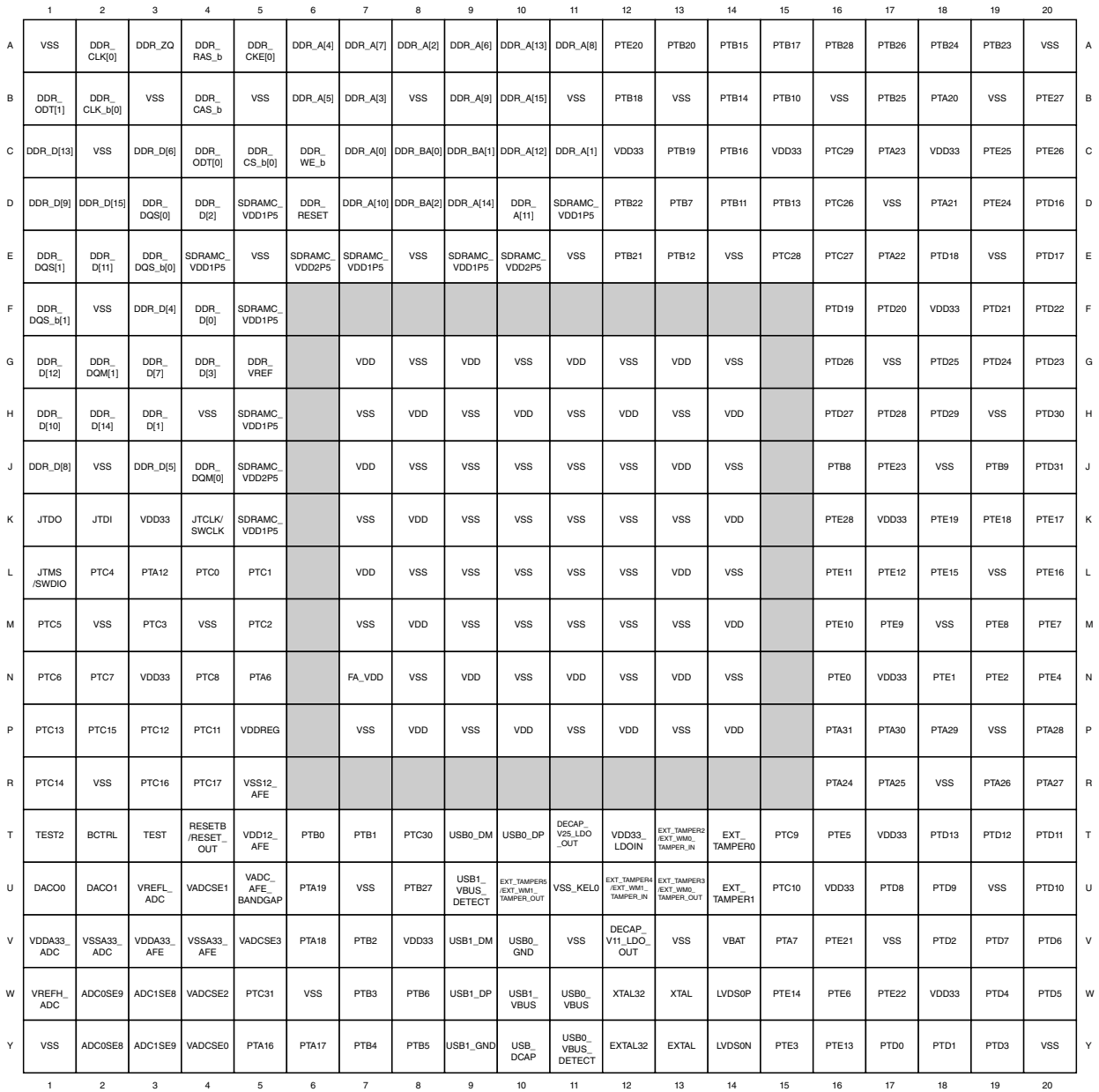
10 Thermal attributes

10.1 Thermal attributes

Board type	Symbol	Description	176LQFP	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	50	°C/W	1, 2
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	32	°C/W	1,3
Single-layer (1s)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./ min. air speed)	40	°C/W	1, 3
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./ min. air speed)	25	°C/W	1, 3
—	$R_{\theta JB}$	Thermal resistance, junction to board	21	°C/W	4
—	$R_{\theta JCtop}$	Thermal resistance, junction to case top	12	°C/W	5
—	Ψ_{JT}	Thermal characterization parameter, junction	3	°C/W	6

364 MAP BGA	176 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
J4	—	DDR_DQM[0]			DDR_DQM0							
E1	—	DDR_DQS[1]			DDR_DQS1							
D3	—	DDR_DQS[0]			DDR_DQS0							
F1	—	DDR_DQS_b[1]			DDR_DQS_b1							
E3	—	DDR_DQS_b[0]			DDR_DQS_b0							
A4	—	DDR_RAS_b			DDR_RAS_b							
C6	—	DDR_WE_b			DDR_WE_b							
C4	—	DDR_ODT[0]			DDR_ODT0							
B1	—	DDR_ODT[1]			DDR_ODT1							
G5	—	DDR_VREF			DDR_VREF							
A3	—	DDR_ZQ			DDR_ZQ							
D6	—	DDR_RESET			DDR_RESET							
J20	—	PTD31		PTD31	FB_AD31	NF_IO15		FTM3_CH0	SPI2_PCS1			
H20	—	PTD30		PTD30	FB_AD30	NF_IO14		FTM3_CH1	SPI2_PCS0			
H18	—	PTD29		PTD29	FB_AD29	NF_IO13		FTM3_CH2	SPI2_SIN			
H17	—	PTD28		PTD28	FB_AD28	NF_IO12	I2C2_SCL	FTM3_CH3	SPI2_SOUT			
H16	—	PTD27		PTD27	FB_AD27	NF_IO11	I2C2_SDA	FTM3_CH4	SPI2_SCK			
G16	—	PTD26		PTD26	FB_AD26	NF_IO10		FTM3_CH5	SDHC1_WP			
G18	—	PTD25		PTD25	FB_AD25	NF_IO9		FTM3_CH6				
G19	—	PTD24		PTD24	FB_AD24	NF_IO8		FTM3_CH7				
G20	124	PTD23		PTD23/ MII0_ RXDATA[3]	FB_AD23	NF_IO7	FTM2CH0	ENET0_ 1588_TMR0	SDHC0_ DAT4	SCI2_TX	DCU1_R3	
F20	126	PTD22		PTD22/ MII0_ RXDATA[2]	FB_AD22	NF_IO6	FTM2CH1	ENET0_ 1588_TMR1	SDHC0_ DAT5	SCI2_RX	DCU1_R4	
F19	128	PTD21		PTD21/ MII0_CRS	FB_AD21	NF_IO5		ENET0_ 1588_TMR2	SDHC0_ DAT6	SCI2_RTS	DCU1_R5	
F17	129	PTD20		PTD20/ MII0_COL	FB_AD20	NF_IO4		ENET0_ 1588_TMR3	SDHC0_ DAT7	SCI2_CTS	DCU1_R0	
F16	130	PTD19		PTD19	FB_AD19	NF_IO3	ESAI_SCKR	I2C0_SCL	FTM2_QD_ PHA	MII0_ TXDATA[3]	DCU1_R1	
E18	131	PTD18		PTD18	FB_AD18	NF_IO2	ESAI_FSR	I2C0_SDA	FTM2_QD_ PHB	MII0_ TXDATA[2]	DCU1_G0	
E20	132	PTD17		PTD17	FB_AD17	NF_IO1	ESAI_HCKR	I2C1_SCL		MII0_TXERR	DCU1_G1	
D20	133	PTD16		PTD16	FB_AD16	NF_IO0	ESAI_HCKT	I2C1_SDA			DCU1_G2	
Y17	86	PTD0		PTD0	QSPI0_A_ SCK	SCI2_TX		FB_AD15	SPDIF_ EXTCLK			
Y18	87	PTD1		PTD1	QSPI0_A_ CS0	SCI2_RX		FB_AD14	SPDIF_IN1			
V18	88	PTD2		PTD2	QSPI0_A_ DATA3	SCI2_RTS	SPI1_PCS3	FB_AD13	SPDIF_OUT1			

364 MAP BGA	176 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
N16	103	PTE0	BOOTMOD1	PTE0	DCU0_ HSYNC/ DCU0_ TCON1	BOOTMOD1		LCD0				
N18	104	PTE1	BOOTMOD0	PTE1	DCU0_ VSYNC/ DCU0_ TCON2	BOOTMOD0		LCD1				
N19	105	PTE2		PTE2	DCU0_PCLK			LCD2				
Y15	80	PTE3		PTE3	DCU0_TAG/ DCU0_ TCON0			LCD3				
N20	106	PTE4		PTE4	DCU0_DE/ DCU0_ TCON3			LCD4				
T16	—	PTE5		PTE5	DCU0_R0			LCD5				
W16	—	PTE6		PTE6	DCU0_R1			LCD6				
M20	109	PTE7	RCON0	PTE7	DCU0_R2		RCON0	LCD7				
M19	110	PTE8	RCON1	PTE8	DCU0_R3		RCON1	LCD8				
M17	111	PTE9	RCON2	PTE9	DCU0_R4		RCON2	LCD9				
M16	112	PTE10	RCON3	PTE10	DCU0_R5		RCON3	LCD10				
L16	113	PTE11	RCON4	PTE11	DCU0_R6		RCON4	LCD11				
L17	114	PTE12	RCON5	PTE12	DCU0_R7	SPI1_PCS3	RCON5	LCD12			LPT_ALT0	
Y16	—	PTE13		PTE13	DCU0_G0			LCD13				
W15	—	PTE14		PTE14	DCU0_G1			LCD14				
L18	115	PTE15	RCON6	PTE15	DCU0_G2		RCON6	LCD15				
L20	116	PTE16	RCON7	PTE16	DCU0_G3		RCON7	LCD16				
K20	117	PTE17	RCON8	PTE17	DCU0_G4		RCON8	LCD17				
K19	118	PTE18	RCON9	PTE18	DCU0_G5		RCON9	LCD18				
K18	119	PTE19	RCON10	PTE19	DCU0_G6		RCON10	LCD19	I2C0_SCL			
A12	170	PTE20	RCON11	PTE20	DCU0_G7		RCON11	LCD20	I2C0_SDA		EWM_in	
V16	81	PTE21		PTE21	DCU0_B0			LCD21				
W17	84	PTE22		PTE22	DCU0_B1			LCD22				
J17	122	PTE23	RCON12	PTE23	DCU0_B2		RCON12	LCD23				
D19	134	PTE24	RCON13	PTE24	DCU0_B3		RCON13	LCD24				
C19	135	PTE25	RCON14	PTE25	DCU0_B4		RCON14	LCD25				
C20	137	PTE26	RCON15	PTE26	DCU0_B5		RCON15	LCD26				
B20	138	PTE27	RCON16	PTE27	DCU0_B6		RCON16	LCD27	I2C1_SCL			
K16	120	PTE28	RCON17	PTE28	DCU0_B7		RCON17	LCD28	I2C1_SDA		EWM_out	
V15	79	PTA7		PTA7	VIU_PIX_ CLK							
T14	76	EXT_ TAMPER0			EXT_ TAMPER0							



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A	VSS	DDR_ CLK[0]	DDR_ZQ	DDR_ RAS_b	DDR_ CKE[0]	DDR_A[4]	DDR_A[7]	DDR_A[2]	DDR_A[6]	DDR_A[13]	DDR_A[8]	PTE20	PTB20	PTB15	PTB17	PTB28	PTB26	PTB24	PTB23	VSS	A
B	DDR_ ODT[1]	DDR_ CLK_b[0]	VSS	DDR_ CAS_b	VSS	DDR_A[5]	DDR_A[3]	VSS	DDR_A[9]	DDR_A[15]	VSS	PTB18	VSS	PTB14	PTB10	VSS	PTB25	PTA20	VSS	PTE27	B
C	DDR_D[13]	VSS	DDR_D[6]	DDR_ ODT[0]	DDR_ CS_b[0]	DDR_ WE_b	DDR_A[0]	DDR_BA[0]	DDR_BA[1]	DDR_A[12]	DDR_A[1]	VDD33	PTB19	PTB16	VDD33	PTC29	PTA23	VDD33	PTE25	PTE26	C
D	DDR_D[9]	DDR_D[15]	DDR_ DQS[0]	DDR_ D[2]	SDRAMC_ VDD1P5	DDR_ RESET	DDR_A[10]	DDR_BA[2]	DDR_A[14]	DDR_ A[11]	SDRAMC_ VDD1P5	PTB22	PTB7	PTB11	PTB13	PTC26	VSS	PTA21	PTE24	PTD16	D
E	DDR_ DQS[1]	DDR_ D[11]	DDR_ DQS_b[0]	SDRAMC_ VDD1P5	VSS	SDRAMC_ VDD2P5	SDRAMC_ VDD1P5	VSS	SDRAMC_ VDD1P5	SDRAMC_ VDD2P5	VSS	PTB21	PTB12	VSS	PTC28	PTC27	PTA22	PTD18	VSS	PTD17	E
F	DDR_ DQS_b[1]	VSS	DDR_D[4]	DDR_ D[0]	SDRAMC_ VDD1P5											PTD19	PTD20	VDD33	PTD21	PTD22	F
G	DDR_ D[12]	DDR_ DQM[1]	DDR_ D[7]	DDR_ D[3]	DDR_ VREF		VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS		PTD26	VSS	PTD25	PTD24	PTD23	G
H	DDR_ D[10]	DDR_ D[14]	DDR_ D[1]	VSS	SDRAMC_ VDD1P5		VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD		PTD27	PTD28	PTD29	VSS	PTD30	H
J	DDR_D[8]	VSS	DDR_D[5]	DDR_ DQM[0]	SDRAMC_ VDD2P5		VDD	VSS	VSS	VSS	VSS	VSS	VDD	VSS		PTB8	PTE23	VSS	PTB9	PTD31	J
K	JTDO	JTDI	VDD33	JTCLK/ SWCLK	SDRAMC_ VDD1P5		VSS	VDD	VSS	VSS	VSS	VSS	VSS	VDD		PTE28	VDD33	PTE19	PTE18	PTE17	K
L	JTMS /SWDIO	PTC4	PTA12	PTC0	PTC1		VDD	VSS	VSS	VSS	VSS	VSS	VDD	VSS		PTE11	PTE12	PTE15	VSS	PTE16	L
M	PTC5	VSS	PTC3	VSS	PTC2		VSS	VDD	VSS	VSS	VSS	VSS	VSS	VDD		PTE10	PTE9	VSS	PTE8	PTE7	M
N	PTC6	PTC7	VDD33	PTC8	PTA6		FA_VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS		PTE0	VDD33	PTE1	PTE2	PTE4	N
P	PTC13	PTC15	PTC12	PTC11	VDDREG		VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD		PTA31	PTA30	PTA29	VSS	PTA28	P
R	PTC14	VSS	PTC16	PTC17	VSS12_ AFE											PTA24	PTA25	VSS	PTA26	PTA27	R
T	TEST2	BCTRL	TEST	RESETB /RESET_ OUT	VDD12_ AFE	PTB0	PTB1	PTC30	USB0_DM	USB0_DP	DECAP_ V25_LDO _OUT	VDD33_ LDOIN	EXT_TAMPER2 /EXT_WM0_ TAMPER_IN	EXT_ TAMPER0	PTC9	PTE5	VDD33	PTD13	PTD12	PTD11	T
U	DACO0	DACO1	VREFL_ ADC	VADCSE1	VADC_ AFE_ BANDGAP	PTA19	VSS	PTB27	USB1_ VBUS_ DETECT	EXT_TAMPER5 /EXT_WM1_ TAMPER_OUT	VSS_KEL0	EXT_TAMPER4 /EXT_WM1_ TAMPER_IN	EXT_TAMPER3 /EXT_WM0_ TAMPER_OUT	EXT_ TAMPER1	PTC10	VDD33	PTD8	PTD9	VSS	PTD10	U
V	VDDA33_ ADC	VSSA33_ ADC	VDDA33_ AFE	VSSA33_ AFE	VADCSE3	PTA18	PTB2	VDD33	USB1_DM	USB0_ GND	VSS	DECAP_ V11_LDO_ OUT	VSS	VBAT	PTA7	PTE21	VSS	PTD2	PTD7	PTD6	V
W	VREFH_ ADC	ADC0SE9	ADC1SE8	VADCSE2	PTC31	VSS	PTB3	PTB6	USB1_DP	USB1_ VBUS	USB0_ VBUS	XTAL32	XTAL	LVDS0P	PTE14	PTE6	PTE22	VDD33	PTD4	PTD5	W
Y	VSS	ADC0SE8	ADC1SE9	VADCSE0	PTA16	PTA17	PTB4	PTB5	USB1_GND	USB_ DCAP	USB0_ VBUS_ DETECT	EXTAL32	EXTAL	LVDS0N	PTE3	PTE13	PTD0	PTD1	PTD3	VSS	Y
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	

Figure 59. 364-pin BGA package ballmap

12.2.1 GPIO Mapping

Table 75. RGPIO versus Pins

RGPIO	In GPIO module	Corresponding Pin on the chip	IOMUX register name	IOMUX register address
RGPIO[0]	PORT0[0]	PTA6	IOMUXC_PTA6	40048000

Table continues on the next page...

13 Power Supply Pins

13.1 Power Supply Pins

Table 77. Power Supply Pins

Supply Rail Name	364 MAP BGA	176 LQFP (F-series ONLY)	Comment
DECAP_V11_ LDO_OUT	V12	69	On-chip 1.1V LDO output
DECAP_V25_ LDO_OUT	T11	65	On-chip 2.5V LDO output (Intended to supply DRAM IO when required)
FA_VDD	N7	—	Factory Use Only (Connect to VDD, internally bonded in LQFP)
SDRAMC_ VDD1P5	D5, D11, E4, E7, E9, F5, H5, K5	DRAM not supported in LQFP	1.5V DDR3 DRAM Supply (1.2V for LPDDR2)
SDRAMC_ VDD2P5	E6, E10, J5	DRAM not supported in LQFP	2.5V DRAM Supply
USB_DCAP	Y10	59	On-chip 3V LDO output (Intended to be fed by external USB VBUS supply)
USB0_GND	V10	61	
USB1_GND	Y9	USB1 not supported in LQFP	
VADC_AFE_ BANDGAP	U5	Video ADC not supported in LQFP	Video ADC Bandgap Output
VBAT	V14	75	On-chip SNVS regulator battery back-up supply option
VDD	G7, G9, G11, G13, H8, H10, H12, H14, J7, J13, K8, K14, L7, L13, M8, M14, N9, N11, N13, P8, P10, P12, P14	2, 22, 48, 85, 102, 125, 136, 174	1.2V Core Supply (Internally Regulated)
VDD33	C12, C15, C18, F18, K3, K17, N3, N17, T17, U16, V8, W18	10, 25, 52, 83, 95, 108, 127, 140, 146, 158, 168	3.3V IO Supply
VDDA33_ADC	V1	38	3.3V Analog To Digital convertor supply
VDD12_AFE	T5	Video ADC not supported in LQFP	1.2V Analog Front End supply for Video ADC
VDDA33_AFE	V3	Video ADC not supported in LQFP	3.3V Analog Front End supply for Video ADC
VDD33_ LDOIN	T12	68	On-chip 2.5V LDO, 1.1V LDO and SNVS regulators input supply
VDDREG	P5	31	On-chip HPREG, LPREG, WBREG and ULPREG regulators input supply
VREFH_ADC	W1	41	ATD High Voltage Reference
VREFL_ADC	U3	40	ATD Low Voltage Reference

Table continues on the next page...

Table 79. Revision History (continued)

Rev. No.	Date	Substantial Changes
Rev 6	Jan 2014	• Added QuadSPI electricals • Changed VBB references to VBAT • In the feature list, clarified that ECC supported for 8-bit mode only, not 16-bit. • Revised the part number format • Revised the field table • Added Absolute Maximum Rating table, which was madde non_cust in the previous version • In the Power Consumption Operating Behavior table, Revised min and max value of IDD_LPS3 and IDD_LPS2. Removed IDD_LPS1 row • In the USB PHY Current Consumption table, removed the Normal Mode • In the Power Sequence table, revised the Power UP/ Down Order column for USB0_VBUs and USB1_VBUS • In the Recommended operating conditions table, revised the min value of VBAT. Revised the min value of VREFH_ADC Revised the min and max values of SDRAMC_VDD1P5 • In the Recommended Connections for Unused Analog Interfaces section, added the notes. Revised the Recommendation if Unused column • In the 12-bit ADC operating conditions, revised Conditions for Ground voltage. Revised min Ref High Voltage • In the 12-bit DAC operating requirements, revised the min and max value of VREFH_ADC • In the SDHC switching specifications, revised the max value of SD6 • In the 24MHz external oscillator electrical characteristics table, revised the min value of VIH and max value of VIL
Rev 7	April 2014	• Updated Note in "Power supply" section. • Updated Absolute maximum ratings section: solute maximum ratings Table - FA_VDD row: Min and Max column • Updated figure "12-bit ADC Input Impedance Equivalency Diagram"

Table continues on the next page...

Table 79. Revision History (continued)

Rev. No.	Date	Substantial Changes
		in 12-bit ADC operating conditions section • Updated figures for clarity in "12-bit DAC operating behaviors" section • Updated figure "VideoADC supply scheme" in "VideoADC Specifications" section • Editorial updates thorughout
Rev 8	November 2014	• In "Part number format" figure, updated explanation for '1'. • In "Fields" table, updated definition of 'R'. • In "External NPN ballast" section, updated recommendations for transistor selection. • In "DDR parameters" section, updated table footnotes regarding typical condition. • In "Power sequencing" table, added comment regarding SDRAMC_VDD1P5: "In case the Ballast transistor's collector is connected to the 1.5 V DRAM supply (instead of the 3.3 V supply), turn this 1.5 V supply on before turning on the 3.3V." • In "VideoADC specifications" table, added supply current values. • In "Receive and Transmit signal timing specifications," added the following note: "See the most current errata document when using the internally generated RXCLK and TXCLK clocks." • Updated "QuadSPI timing" section, presenting data based on a negative edge data launch from the device and a negative edge data capture; updated the figure, "QuadSPI Input/Read timing (SDR mode)"; updated the table, "QuadSPI Input/Read timing (SDR mode)." • For the "SDHC switching specifcations" table, added the statement, "A load of 50 pF is assumed"; updated max value for SD6, SDHC output delay (output valid). • In the "24 MHz oscillator specifications" section, added the statement, "The crystal must be rated for a drive level of 250 µW or higher. An ESR (equivalent series