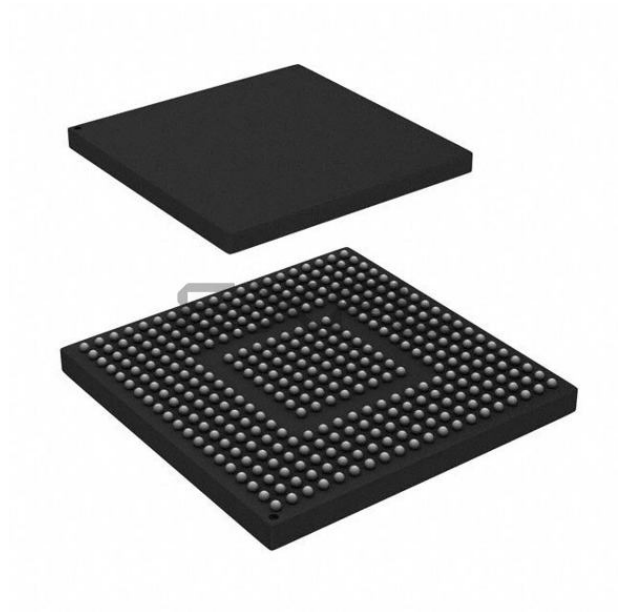

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-A5 + Cortex®-M4
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	400MHz, 167MHz
Co-Processors/DSP	Multimedia; NEON™ MPE
RAM Controllers	LPDDR2, DDR3, DRAM
Graphics Acceleration	Yes
Display & Interface Controllers	DCU, GPU, LCD, VideoADC, VIU
Ethernet	10/100Mbps (2)
SATA	-
USB	USB 2.0 OTG + PHY (1)
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	-
Package / Case	364-LFBGA
Supplier Device Package	364-LFBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mvf62nn151cmk4

3 Terminology and guidelines

3.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

3.1.1 Example

This is an example of an operating requirement:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	0.9	1.1	V

3.2 Definition: Operating behavior

Unless otherwise specified, an *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

3.2.1 Example

This is an example of an operating behavior:

Symbol	Description	Min.	Max.	Unit
I_{WP}	Digital I/O weak pullup/ pulldown current	10	130	µA

3.3 Definition: Attribute

An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

5 Operating Requirements

5.1 Thermal operating requirements

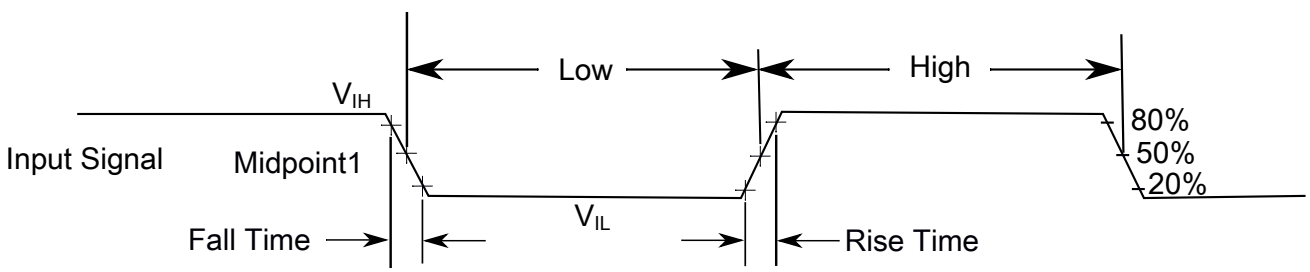
Table 1. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit
T_A	Ambient temperature	–40	85	°C
T_J	Junction temperature		105	°C

6 General

6.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.



The midpoint is $V_{IL} + (V_{IH} - V_{IL}) / 2$

Figure 2. Input signal measurement reference

NOTE

WBREG is the Well Bias Regulator. Supplies PD1 WELL during well bias modes.

8.3 Absolute maximum ratings

NOTE

These are the values above which device can get damaged. Refer to the recommended operating conditions table for intended use case values

Table 29. Absolute maximum ratings

Symbol	Parameters	Min	Max	Unit
USB0_VBUS	VBUS supply for USB	-	5.25	V
USB1_VBUS	VBUS supply for USB	-	5.25	V
USB_DCAP	USB LDO 5V->3.3V Outpu	-0.3	3.6	V
VBAT	Battery supply in case of LDOIN fails	-0.3	3.6	V
VDD33_LDOIN	LDO input supply	-0.3	3.6	V
DECAP_V11_LDO_OUT	LDO 3.3V -> 1.1V Output	-0.3	1.3	V
DECAP_V25_LDO_OUT	LDO 3.3V -> 2.5 Output for PLL, DDR, EFUSE	-0.3	3.6	V
VDD33	GPIO 3.3V IO supply	-0.3	3.6	V
VDDREG	Device PMU regulator and External ballast supply	-0.3	3.6	V
VDDA33_ADC	3.3V supply for ADC, DAC and IO segment	-0.3	3.6	V
VREFH_ADC	3.3V supply of AFE (Video ADC)	-0.3	3.6	V
VDDA33_AFE	3.3V supply of AFE (Video ADC)	-0.3	3.6	V
VDD12_AFE	1.2V supply for AFE (Video ADC)	-0.3	1.3	V
FA_VDD	Test purpose only	-0.3	1.3	V
VDD	1.2V core supply	-0.3	1.3	V
SDRAMC_VDD1P5	1.2/1.5 DDR Main IO supply	-0.3	1.975	V
SDRAMC_VDD2P5	2.5V DDR pre-drive supply DD2P5_LDO_OUT	-0.3	3.6	V

Table 32. 12-bit ADC Characteristics (V_{REFH} = V_{DDAD}, V_{REFL} = V_{SSAD}) (continued)

Characteristic	Conditions[1]	Symb	Min	Typ [2]	Max	Unit	Comment
	ADLSMP=0 ADSTS=10			0.8			
	ADLSMP=0 ADSTS=11			0.85			
	ADLSMP=1 ADSTS=00			0.95			
	ADLSMP=1 ADSTS=01			1.05			
	ADLSMP=1 ADSTS=10			1.15			
	ADLSMP=1, ADSTS=11			1.25			
Total Unadjusted Error	12 bit mode	TUE	-2	-	+5	LSB[3]	With Max Averaging
	10 bit mode		-0.5	-	+2		
	8 bit mode		-0.25	-	+1.5		
Differential Non-Linearity	12 bit mode	DNL	-	±0.6	±1.5	LSB[3]	Waiting for histogram method confirmation
	10bit mode		-	±0.5	±1		
	8 bit mode		-	±0.25	±0.5		
Integral Non-Linearity	12 bit mode	INL	-	±2	±4	LSB[3]	Waiting for histogram method confirmation
	10bit mode		-	±1	±2		
	8 bit mode		-	±0.5	±1		
Zero-Scale Error	12 bit mode	E_{ZS}	-	+1.0	±1.6	LSB[3]	VADIN = V_{REFL} With Max Averaging
	10bit mode		-	±0.4	±0.8		
	8 bit mode		-	±0.1	±0.4		
Full-Scale Error	12 bit mode	E_{FS}	-	±2	±3.5	LSB[3]	VADIN = V_{REFH} With Max Averaging
	10bit mode		-	±0.5	±1		
	8 bit mode		-	±0.25	±0.75		
Quantization Error	12 bit mode	E_Q	-	±1 to 0		LSB[3]	
	10bit mode		-	±0.5			
	8 bit mode		-	±0.5			
Effective Number of Bits	12 bit mode	ENOB	10.1	10.7	-	Bits	Fin = 100Hz
Signal to Noise plus Distortion	See ENOB	SINAD	SINAD = 6.02 x ENOB + 1.76			dB	
Input Leakage Error	all modes	EIL	I_{In} x RAS			mV	I_{In} = 400 nA leakage current
Temp Sensor Slope	Across the full temperature range of the device	m	--	1.84	--	mV/°C	
Temp Sensor Voltage	25°C	V_{TEMP25}	-	696	-	mV	

1. All accuracy numbers assume the ADC is calibrated with V_{REFH}=V_{DDAD}
2. Typical values assume V_{DDAD} = 3.0 V, Temp = 25°C, F_{adck}=20 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
3. 1 LSB = (V_{REFH} - V_{REFL})/2N

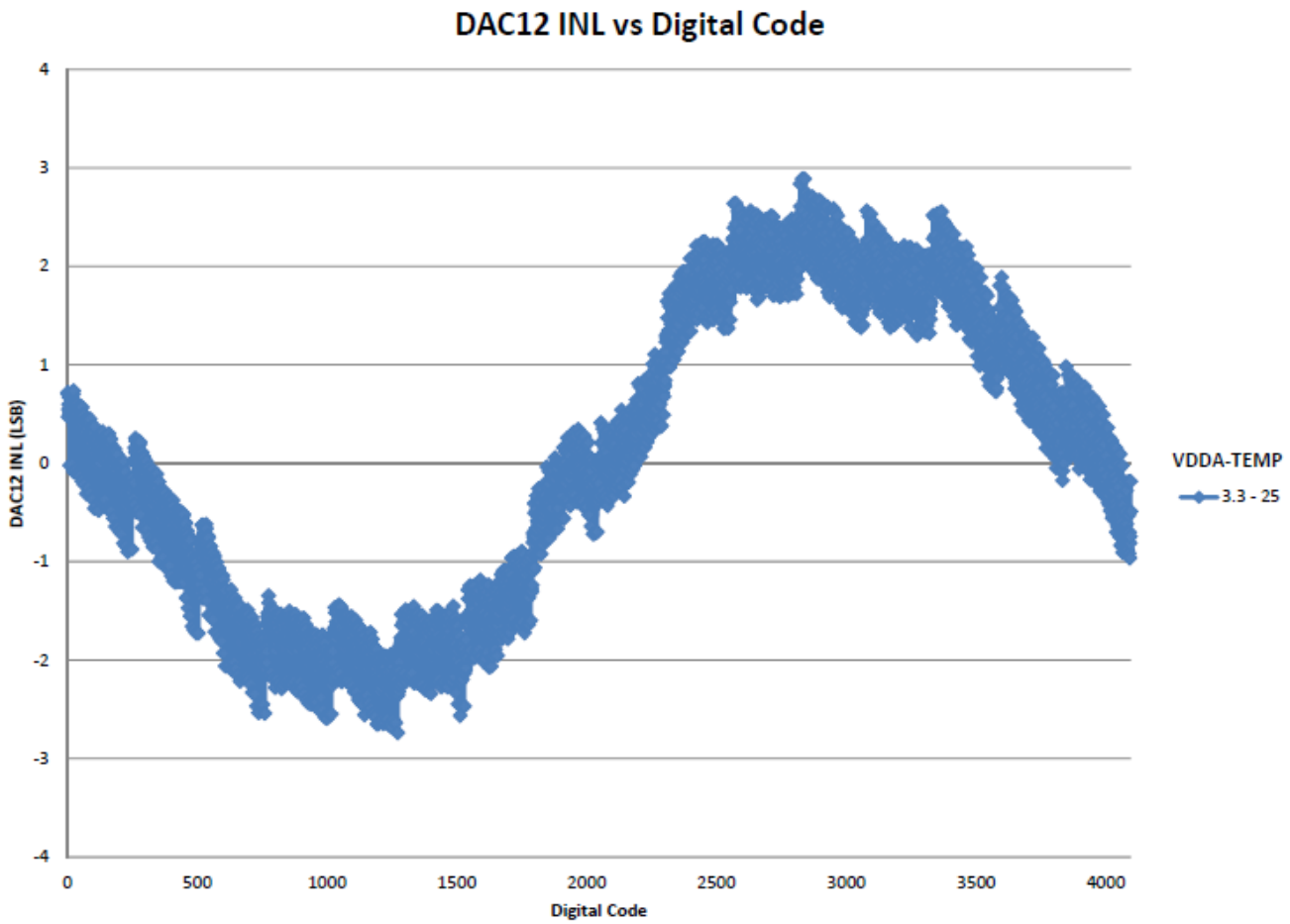


Figure 9. INL error vs. digital code

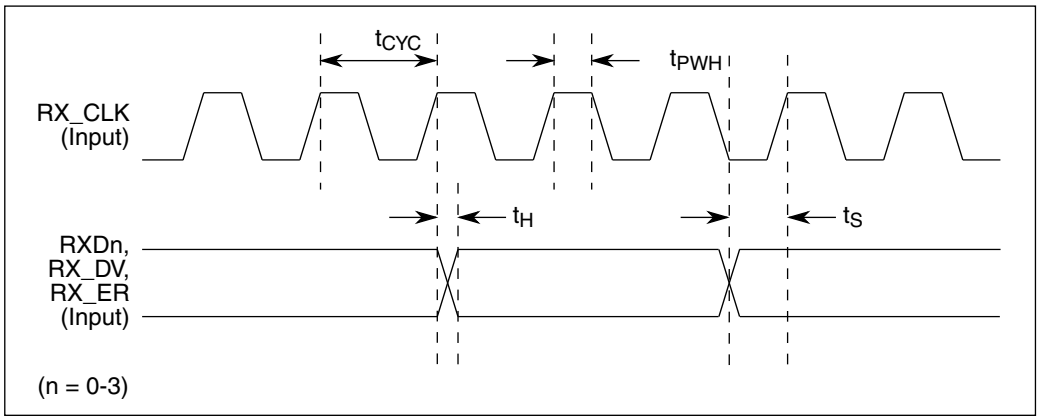


Figure 22. MII receive signal timing diagram

Table 42. Receive signal timing for MII interfaces

Characteristic		MII Mode			Unit
		Min	Typ	Max	
RX_CLK clock period (100/10 MBPS)	t_{CYC}		40/400		ns
RX_CLK duty cycle, t_{PWH}/t_{CYC}		45	50	55	%
Input setup time before RX_CLK	t_s	5			ns
Input hold time after RX_CLK	t_h	5			ns

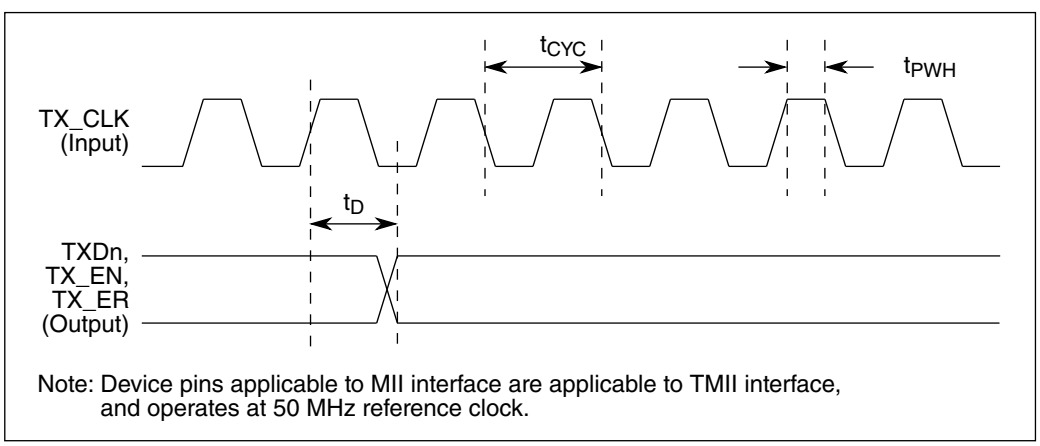


Figure 23. MII transmit signal timing diagram

Table 43. Transmit signal timing for MII interfaces

Characteristic		MII Mode			Unit
		Min	Typ	Max	
TX_CLK clock period (100/10 MBPS)	t_{CYC}		40/400		ns
TX_CLK duty cycle, t_{PWH}/t_{CYC}		45	50	55	%
Out delay from TX_CLK	t_D	2		25	ns

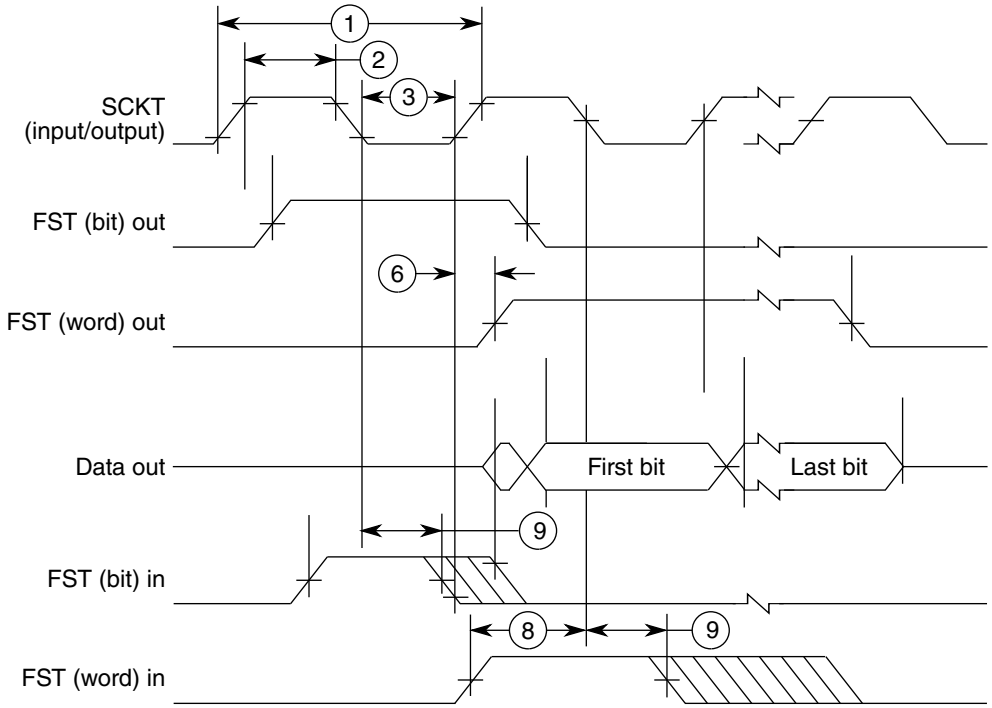


Figure 24. ESAI Transmitter Timing

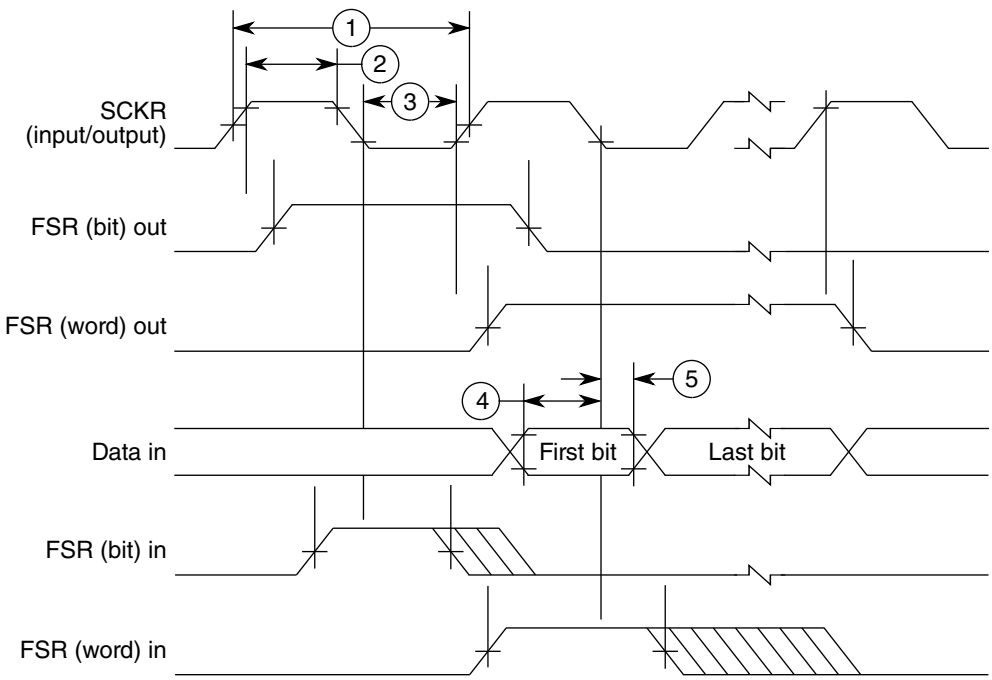


Figure 25. ESAI Receiver Timing

9.5 Memory interfaces

9.5.1 QuadSPI timing

- All data is based on a negative edge data launch from the device and a negative edge data capture, as shown in the timing diagrams in this section. This corresponds to the N/1 sample point as shown in the reference manual QSPI section "Internal Sampling of Serial Flash Input Data."
- Measurements are with a load of 35 pF on output pins. I/P Slew : 1ns
- Timings assume a setting of 0x0000_000x for QSPI_SMPR register (see the reference manual for details).

SDR mode

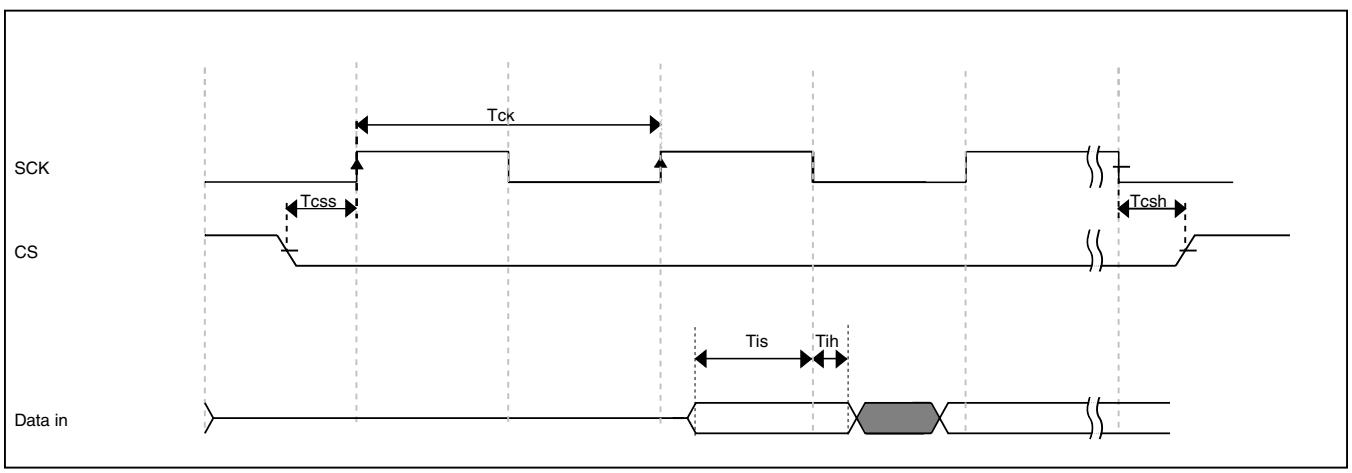


Figure 30. QuadSPI Input/Read timing (SDR mode)

Table 48. QuadSPI Input/Read timing (SDR mode)

Symbol	Parameter	Value		Unit
		Min	Max	
T_{is}	Setup time for incoming data	4.5	—	ns
T_{ih}	Hold time requirement for incoming data	0	—	ns

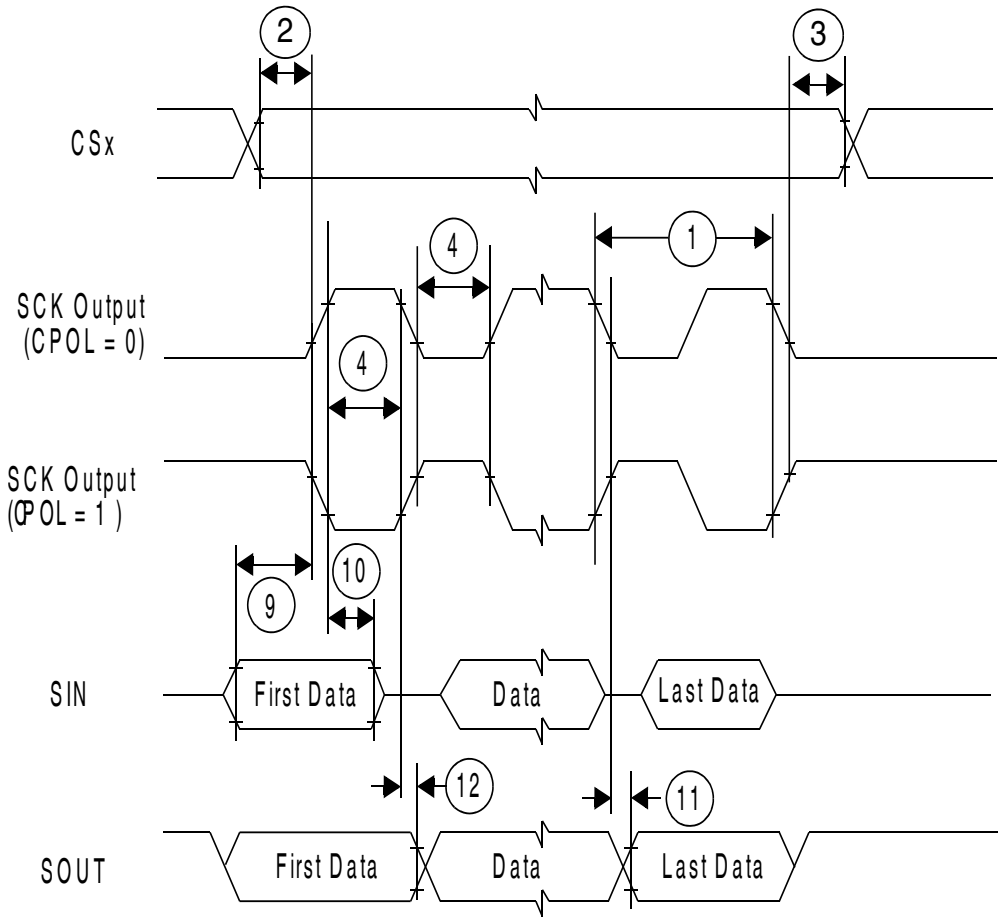


Figure 47. DSPI classic SPI timing master, CPHA=0

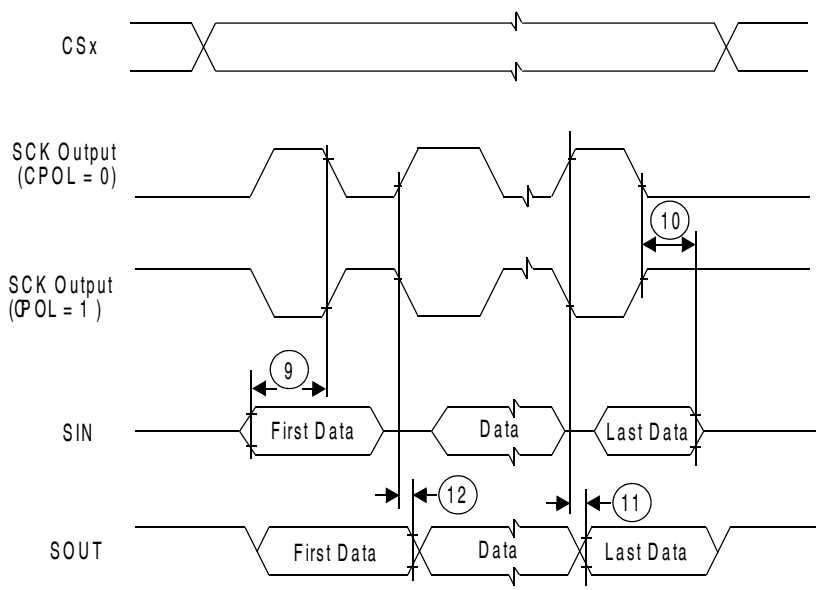


Figure 48. DSPI classic SPI timing master, CPHA=1

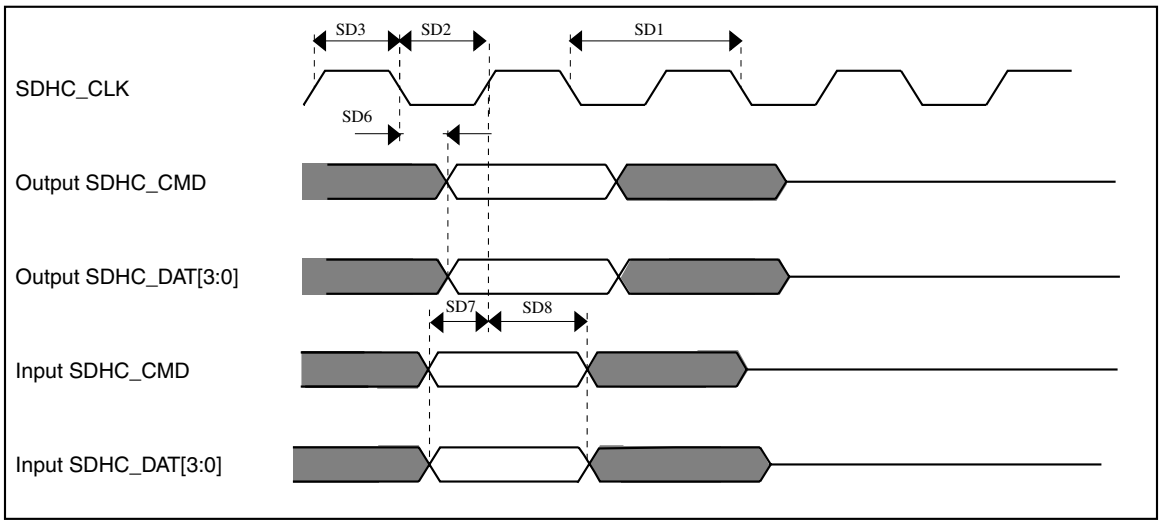


Figure 52. SDHC timing

9.6.4 USB PHY specifications

This section describes the USB-OTG PHY and the USB Host port PHY parameters.

The USB PHY meets the electrical compliance requirements defined in the Universal Serial Bus Revision 2.0 OTG, USB Host with the amendments below (On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification is not applicable to Host port).

- USB ENGINEERING CHANGE NOTICE
  - Title: 5V Short Circuit Withstand Requirement Change
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- Errata for USB Revision 2.0 April 27, 2000 as of 12/7/2000
- USB ENGINEERING CHANGE NOTICE
  - Title: Pull-up/Pull-down resistors
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- USB ENGINEERING CHANGE NOTICE
  - Title: Suspend Current Limit Changes
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification
  - Revision 2.0 plus errata and ecn June 4, 2010
- Battery Charging Specification (available from USB-IF)
  - Revision 1.2, December 7, 2010

Board type	Symbol	Description	176LQFP	Unit	Notes
		to package top (natural convection)			

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance
2. Per JEDEC JESD51-2 with the single layer board (JESD51-3) horizontal
3. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

Board type	Symbol	Description	364 MAPBGA	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	45	°C/W	1, 2
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	28	°C/W	1, 3
Single-layer (1s)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./ min. air speed)	37	°C/W	1,3
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./ min. air speed)	24	°C/W	1,3
—	$R_{\theta JB}$	Thermal resistance, junction to board	17	°C/W	4
—	$R_{\theta JC}$	Thermal resistance, junction to case	10	°C/W	5
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	2	°C/W	6

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

364 MAP BGA	176 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
B3	24	VSS			VSS							
B5	32	VSS			VSS							
B8	—	VSS			VSS							
B11	—	VSS			VSS							
B13	—	VSS			VSS							
B16	—	VSS			VSS							
B19	—	VSS			VSS							
C2	—	VSS			VSS							
D17	—	VSS			VSS							
E5	—	VSS			VSS							
E8	—	VSS			VSS							
E11	—	VSS			VSS							
E14	—	VSS			VSS							
E19	—	VSS			VSS							
F2	—	VSS			VSS							
G17	—	VSS			VSS							
H4	—	VSS			VSS							
J2	—	VSS			VSS							
J18	—	VSS			VSS							
M2	—	VSS			VSS							
M4	—	VSS			VSS							
M18	—	VSS			VSS							
R2	—	VSS			VSS							
R18	—	VSS			VSS							
U7	—	VSS			VSS							
U19	—	VSS			VSS							
V13	—	VSS			VSS							
W6	—	VSS			VSS							
V17	—	VSS			VSS							
Y1	—	VSS			VSS							
Y20	—	VSS			VSS							
H19	—	VSS			VSS							
L19	—	VSS			VSS							
P19	—	VSS			VSS							
J5	—	SDRAMC_ VDD2P5			SDRAMC_ VDD2P5							
E6	—	SDRAMC_ VDD2P5			SDRAMC_ VDD2P5							
E10	—	SDRAMC_ VDD2P5			SDRAMC_ VDD2P5							

Table 75. RGPIO versus Pins (continued)

RGPIO	In GPIO module	Corresponding Pin on the chip	IOMUX register name	IOMUX register address
RGPIO[1]	PORT0[1]	PTA8	IOMUXC_PTA8	40048004
RGPIO[2]	PORT0[2]	PTA9	IOMUXC_PTA9	40048008
RGPIO[3]	PORT0[3]	PTA10	IOMUXC_PTA10	4004800C
RGPIO[4]	PORT0[4]	PTA11	IOMUXC_PTA11	40048010
RGPIO[5]	PORT0[5]	PTA12	IOMUXC_PTA12	40048014
RGPIO[6]	PORT0[6]	PTA16	IOMUXC_PTA16	40048018
RGPIO[7]	PORT0[7]	PTA17	IOMUXC_PTA17	4004801C
RGPIO[8]	PORT0[8]	PTA18	IOMUXC_PTA18	40048020
RGPIO[9]	PORT0[9]	PTA19	IOMUXC_PTA19	40048024
RGPIO[10]	PORT0[10]	PTA20	IOMUXC_PTA20	40048028
RGPIO[11]	PORT0[11]	PTA21	IOMUXC_PTA21	4004802C
RGPIO[12]	PORT0[12]	PTA22	IOMUXC_PTA22	40048030
RGPIO[13]	PORT0[13]	PTA23	IOMUXC_PTA23	40048034
RGPIO[14]	PORT0[14]	PTA24	IOMUXC_PTA24	40048038
RGPIO[15]	PORT0[15]	PTA25	IOMUXC_PTA25	4004803C
RGPIO[16]	PORT0[16]	PTA26	IOMUXC_PTA26	40048040
RGPIO[17]	PORT0[17]	PTA27	IOMUXC_PTA27	40048044
RGPIO[18]	PORT0[18]	PTA28	IOMUXC_PTA28	40048048
RGPIO[19]	PORT0[19]	PTA29	IOMUXC_PTA29	4004804C
RGPIO[20]	PORT0[20]	PTA30	IOMUXC_PTA30	40048050
RGPIO[21]	PORT0[21]	PTA31	IOMUXC_PTA31	40048054
RGPIO[22]	PORT0[22]	PTB0	IOMUXC_PTB0	40048058
RGPIO[23]	PORT0[23]	PTB1	IOMUXC_PTB1	4004805C
RGPIO[24]	PORT0[24]	PTB2	IOMUXC_PTB2	40048060
RGPIO[25]	PORT0[25]	PTB3	IOMUXC_PTB3	40048064
RGPIO[26]	PORT0[26]	PTB4	IOMUXC_PTB4	40048068
RGPIO[27]	PORT0[27]	PTB5	IOMUXC_PTB5	4004806C
RGPIO[28]	PORT0[28]	PTB6	IOMUXC_PTB6	40048070
RGPIO[29]	PORT0[29]	PTB7	IOMUXC_PTB7	40048074
RGPIO[30]	PORT0[30]	PTB8	IOMUXC_PTB8	40048078
RGPIO[31]	PORT0[31]	PTB9	IOMUXC_PTB9	4004807C
RGPIO[32]	PORT1[0]	PTB10	IOMUXC_PTB10	40048080
RGPIO[33]	PORT1[1]	PTB11	IOMUXC_PTB11	40048084
RGPIO[34]	PORT1[2]	PTB12	IOMUXC_PTB12	40048088
RGPIO[35]	PORT1[3]	PTB13	IOMUXC_PTB13	4004808C
RGPIO[36]	PORT1[4]	PTB14	IOMUXC_PTB14	40048090
RGPIO[37]	PORT1[5]	PTB15	IOMUXC_PTB15	40048094
RGPIO[38]	PORT1[6]	PTB16	IOMUXC_PTB16	40048098
RGPIO[39]	PORT1[7]	PTB17	IOMUXC_PTB17	4004809C

Table continues on the next page...

Table 75. RGPIO versus Pins (continued)

RGPIO	In GPIO module	Corresponding Pin on the chip	IOMUX register name	IOMUX register address
RGPIO[40]	PORT1[8]	PTB18	IOMUXC_PTB18	400480A0
RGPIO[41]	PORT1[9]	PTB19	IOMUXC_PTB19	400480A4
RGPIO[42]	PORT1[10]	PTB20	IOMUXC_PTB20	400480A8
RGPIO[43]	PORT1[11]	PTB21	IOMUXC_PTB21	400480AC
RGPIO[44]	PORT1[12]	PTB22	IOMUXC_PTB22	400480B0
RGPIO[45]	PORT1[13]	PTC0	IOMUXC_PTC0	400480B4
RGPIO[46]	PORT1[14]	PTC1	IOMUXC_PTC1	400480B8
RGPIO[47]	PORT1[15]	PTC2	IOMUXC_PTC2	400480BC
RGPIO[48]	PORT1[16]	PTC3	IOMUXC_PTC3	400480C0
RGPIO[49]	PORT1[17]	PTC4	IOMUXC_PTC4	400480C4
RGPIO[50]	PORT1[18]	PTC5	IOMUXC_PTC5	400480C8
RGPIO[51]	PORT1[19]	PTC6	IOMUXC_PTC6	400480CC
RGPIO[52]	PORT1[20]	PTC7	IOMUXC_PTC7	400480D0
RGPIO[53]	PORT1[21]	PTC8	IOMUXC_PTC8	400480D4
RGPIO[54]	PORT1[22]	PTC9	IOMUXC_PTC9	400480D8
RGPIO[55]	PORT1[23]	PTC10	IOMUXC_PTC10	400480DC
RGPIO[56]	PORT1[24]	PTC11	IOMUXC_PTC11	400480E0
RGPIO[57]	PORT1[25]	PTC12	IOMUXC_PTC12	400480E4
RGPIO[58]	PORT1[26]	PTC13	IOMUXC_PTC13	400480E8
RGPIO[59]	PORT1[27]	PTC14	IOMUXC_PTC14	400480EC
RGPIO[60]	PORT1[28]	PTC15	IOMUXC_PTC15	400480F0
RGPIO[61]	PORT1[29]	PTC16	IOMUXC_PTC16	400480F4
RGPIO[62]	PORT1[30]	PTC17	IOMUXC_PTC17	400480F8
RGPIO[63]	PORT1[31]	PTD31	IOMUXC_PTD31	400480FC
RGPIO[64]	PORT2[0]	PTD30	IOMUXC_PTD30	40048100
RGPIO[65]	PORT2[1]	PTD29	IOMUXC_PTD29	40048104
RGPIO[66]	PORT2[2]	PTD28	IOMUXC_PTD28	40048108
RGPIO[67]	PORT2[3]	PTD27	IOMUXC_PTD27	4004810C
RGPIO[68]	PORT2[4]	PTD26	IOMUXC_PTD26	40048110
RGPIO[69]	PORT2[5]	PTD25	IOMUXC_PTD25	40048114
RGPIO[70]	PORT2[6]	PTD24	IOMUXC_PTD24	40048118
RGPIO[71]	PORT2[7]	PTD23	IOMUXC_PTD23	4004811C
RGPIO[72]	PORT2[8]	PTD22	IOMUXC_PTD22	40048120
RGPIO[73]	PORT2[9]	PTD21	IOMUXC_PTD21	40048124
RGPIO[74]	PORT2[10]	PTD20	IOMUXC_PTD20	40048128
RGPIO[75]	PORT2[11]	PTD19	IOMUXC_PTD19	4004812C
RGPIO[76]	PORT2[12]	PTD18	IOMUXC_PTD18	40048130
RGPIO[77]	PORT2[13]	PTD17	IOMUXC_PTD17	40048134
RGPIO[78]	PORT2[14]	PTD16	IOMUXC_PTD16	40048138

Table continues on the next page...

Table 75. RGPIO versus Pins (continued)

RGPIO	In GPIO module	Corresponding Pin on the chip	IOMUX register name	IOMUX register address
RGPIO[79]	PORT2[15]	PTD0	IOMUXC_PTD0	4004813C
RGPIO[80]	PORT2[16]	PTD1	IOMUXC_PTD1	40048140
RGPIO[81]	PORT2[17]	PTD2	IOMUXC_PTD2	40048144
RGPIO[82]	PORT2[18]	PTD3	IOMUXC_PTD3	40048148
RGPIO[83]	PORT2[19]	PTD4	IOMUXC_PTD4	4004814C
RGPIO[84]	PORT2[20]	PTD5	IOMUXC_PTD5	40048150
RGPIO[85]	PORT2[21]	PTD6	IOMUXC_PTD6	40048154
RGPIO[86]	PORT2[22]	PTD7	IOMUXC_PTD7	40048158
RGPIO[87]	PORT2[23]	PTD8	IOMUXC_PTD8	4004815C
RGPIO[88]	PORT2[24]	PTD9	IOMUXC_PTD9	40048160
RGPIO[89]	PORT2[25]	PTD10	IOMUXC_PTD10	40048164
RGPIO[90]	PORT2[26]	PTD11	IOMUXC_PTD11	40048168
RGPIO[91]	PORT2[27]	PTD12	IOMUXC_PTD12	4004816C
RGPIO[92]	PORT2[28]	PTD13	IOMUXC_PTD13	40048170
RGPIO[93]	PORT2[29]	PTB23	IOMUXC_PTB23	40048174
RGPIO[94]	PORT2[30]	PTB24	IOMUXC_PTB24	40048178
RGPIO[95]	PORT2[31]	PTB25	IOMUXC_PTB25	4004817C
RGPIO[96]	PORT3[0]	PTB26	IOMUXC_PTB26	40048180
RGPIO[97]	PORT3[1]	PTB27	IOMUXC_PTB27	40048184
RGPIO[98]	PORT3[2]	PTB28	IOMUXC_PTB28	40048188
RGPIO[99]	PORT3[3]	PTC26	IOMUXC_PTC26	4004818C
RGPIO[100]	PORT3[4]	PTC27	IOMUXC_PTC27	40048190
RGPIO[101]	PORT3[5]	PTC28	IOMUXC_PTC28	40048194
RGPIO[102]	PORT3[6]	PTC29	IOMUXC_PTC29	40048198
RGPIO[103]	PORT3[7]	PTC30	IOMUXC_PTC30	4004819C
RGPIO[104]	PORT3[8]	PTC31	IOMUXC_PTC31	400481A0
RGPIO[105]	PORT3[9]	PTE0	IOMUXC_PTE0	400481A4
RGPIO[106]	PORT3[10]	PTE1	IOMUXC_PTE1	400481A8
RGPIO[107]	PORT3[11]	PTE2	IOMUXC_PTE2	400481AC
RGPIO[108]	PORT3[12]	PTE3	IOMUXC_PTE3	400481B0
RGPIO[109]	PORT3[13]	PTE4	IOMUXC_PTE4	400481B4
RGPIO[110]	PORT3[14]	PTE5	IOMUXC_PTE5	400481B8
RGPIO[111]	PORT3[15]	PTE6	IOMUXC_PTE6	400481BC
RGPIO[112]	PORT3[16]	PTE7	IOMUXC_PTE7	400481C0
RGPIO[113]	PORT3[17]	PTE8	IOMUXC_PTE8	400481C4
RGPIO[114]	PORT3[18]	PTE9	IOMUXC_PTE9	400481C8
RGPIO[115]	PORT3[19]	PTE10	IOMUXC_PTE10	400481CC
RGPIO[116]	PORT3[20]	PTE11	IOMUXC_PTE11	400481D0
RGPIO[117]	PORT3[21]	PTE12	IOMUXC_PTE12	400481D4

Table continues on the next page...

Table 75. RGPIO versus Pins (continued)

RGPIO	In GPIO module	Corresponding Pin on the chip	IOMUX register name	IOMUX register address
RGPIO[118]	PORT3[22]	PTE13	IOMUXC_PTE13	400481D8
RGPIO[119]	PORT3[23]	PTE14	IOMUXC_PTE14	400481DC
RGPIO[120]	PORT3[24]	PTE15	IOMUXC_PTE15	400481E0
RGPIO[121]	PORT3[25]	PTE16	IOMUXC_PTE16	400481E4
RGPIO[122]	PORT3[26]	PTE17	IOMUXC_PTE17	400481E8
RGPIO[123]	PORT3[27]	PTE18	IOMUXC_PTE18	400481EC
RGPIO[124]	PORT3[28]	PTE19	IOMUXC_PTE19	400481F0
RGPIO[125]	PORT3[29]	PTE20	IOMUXC_PTE20	400481F4
RGPIO[126]	PORT3[30]	PTE21	IOMUXC_PTE21	400481F8
RGPIO[127]	PORT3[31]	PTE22	IOMUXC_PTE22	400481FC
RGPIO[128]	PORT4[0]	PTE23	IOMUXC_PTE23	40048200
RGPIO[129]	PORT4[1]	PTE24	IOMUXC_PTE24	40048204
RGPIO[130]	PORT4[2]	PTE25	IOMUXC_PTE25	40048208
RGPIO[131]	PORT4[3]	PTE26	IOMUXC_PTE26	4004820C
RGPIO[132]	PORT4[4]	PTE27	IOMUXC_PTE27	40048210
RGPIO[133]	PORT4[5]	PTE28	IOMUXC_PTE28	40048214
RGPIO[134]	PORT4[6]	PTA7	IOMUXC_PTA7	40048218

12.2.2 Special Signal

Table 76. Special Signal Considerations

Special Signal	Comments
DDR_VREF	When using DDR_VREF with DDR I/O, the nominal reference voltage must be half of the SDRAMC_VDD1P5 supply. The user must tie DDR_VREF to a precision external resistor divider. Shunt each resistor with a closely-mounted 0.1 µF capacitor.
DDR_ZQ	DRAM calibration resistor 240 Ω 1% used as reference during DRAM output buffer driver calibration should be connected between this pad and GND
DECAP_V25_LDO_OUT	DCAP_V25_LDO_OUT can be tied to SDRAMC_VDD2P5 to provide the predriver supply for the DDR I/O segment. SDRAMC_VDD1P5 requires an external regulated supply. If SDRAMC_VDD2P5 uses an external 2.5V supply, do NOT tie it to DCAP_V25_LDO_OUT.
EXT_POR, TEST	Factory use only, tie to ground..
EXT_TAMPER0, EXT_TAMPER1, EXT_TAMPER2, EXT_TAMPER3, EXT_TAMPER4, EXT_TAMPER5	Security related tamper detection inputs, if not in use they must be tied to ground.
FA_VDD	Factory use only, tie to VDD.

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Table 76. Special Signal Considerations (continued)

Special Signal	Comments
JTCLK, JTDI, JTDO, JTMS	For JTAG the use of external resistors is unnecessary. However, if external resistors are used, the user must ensure that the on-chip pull-up/down configuration is matched. For example, do not use an external pull down on an input that has on-chip pull-up. JTDO is configured with a keeper circuit such that the floating condition is eliminated if an external pull resistor is not present. An external pull resistor on JTDO is detrimental and should be avoided.
LVDS0N, LVDS0P	Not recommended for application use, intended for clock observation purposes during debug only.
RESETB/RESET_OUT	Active low input used to generate a system wide reset (except the SRTC). A glitch filter is include to help prevent unexpected resets, a minimum pulse width of 125 nsecs is required to guarantee a reset is detected.
XTAL, EXTAL	A 24.0 MHz fundamental mode crystal should be connected between XTAL and EXTAL. The crystal must be rated for a drive level of 250 µW or higher. An ESR (equivalent series resistance) of 80 Ω or less is recommended. This clock is used as a reference for USB, so there are strict frequency tolerance and jitter requirements. The crystal can be eliminated if an external 24 MHz oscillator is available in the system. In this case, XTAL must be directly driven by the external oscillator and EXTAL floated. The XTAL signal level must swing from ~0.8 x DECAP_V11_ LDO_OUT to ~0.2 V.
XTAL32, EXTAL32	If the user wishes to configure XTAL32 and EXTAL32 as an RTC oscillator, a 32.768 kHz crystal, (≤50 kΩ ESR, 10 pF load) should be connected between XTAL32 and EXTAL32. Keep in mind the capacitors implemented on either side of the crystal are about twice the crystal load capacitor. To hit the exact oscillation frequency, the board capacitors need to be reduced to account for board and chip parasitics. The integrated oscillation amplifier is self biasing, but relatively weak. Care must be taken to limit parasitic leakage from XTAL32 and EXTAL32 to either power or ground (>100 MΩ). This will debias the amplifier and cause a reduction of startup margin. Typically XTAL32 and EXTAL32 should bias to approximately 0.5 V. If it is desired to feed an external low frequency clock into XTAL32 the EXTAL32 pin should be left floating or driven with a complimentary signal. The logic level of this forcing clock should not exceed DECAP_V11_ LDO_OUT level and the frequency should be <100 kHz under typical conditions. In the case where the SIRC is used, it is recommended to connect XTAL32 to ground and leave EXTAL32 floating.

Table 78. Functional Assignment Pins (continued)

Signal Name	364 MAP BGA	176 LQFP (F-series ONLY)	Power Group	Pad Type	Default Mode (Reset)	Default Function	Input/ Output	Value
PTA31	P16	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB0	T6	49	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB1	T7	50	VDD33	GPIO	ALT3	RCON30	Input	Disabled
PTB2	V7	51	VDD33	GPIO	ALT3	RCON31	Input	Disabled
PTB3	W7	53	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB4	Y7	54	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB5	Y8	55	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB6	W8	56	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB7	D13	166	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB8	J16	121	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB9	J19	123	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB10	B15	159	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB11	D14	164	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB12	E13	165	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB13	D15	156	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB14	B14	162	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB15	A14	161	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB16	C14	163	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB17	A15	160	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB18	B12	171	VDD33	GPIO	ALT0	GPIO	Input	Disabled
PTB19	C13	167	VDD33	GPIO	ALT0	GPIO	Input	Disabled
PTB20	A13	169	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB21	E12	173	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB22	D12	172	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB23	A19	141	VDD33	GPIO	ALT3	GPIO	Disabled	
PTB24	A18	142	VDD33	GPIO	ALT3	GPIO	Disabled	
PTB25	B17	149	VDD33	GPIO	ALT3	GPIO	Disabled	
PTB26	A17	150	VDD33	GPIO	ALT3	RCON21	Input	Disabled
PTB27	U8	57	VDD33	GPIO	ALT3	RCON22	Input	Disabled
PTB28	A16	151	VDD33	GPIO	ALT3	RCON23	Input	Disabled
PTC0	L4	8	VDD33	GPIO	ALT7	RCON18	Input	Disabled
PTC1	L5	9	VDD33	GPIO	ALT7	RCON19	Input	Disabled
PTC2	M5	11	VDD33	GPIO	ALT7	RCON20	Input	Disabled
PTC3	M3	12	VDD33	GPIO	ALT0	GPIO	Disabled	
PTC4	L2	14	VDD33	GPIO	ALT0	GPIO	Disabled	
PTC5	M1	15	VDD33	GPIO	ALT0	GPIO	Disabled	
PTC6	N1	16	VDD33	GPIO	ALT0	GPIO	Disabled	

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Table 78. Functional Assignment Pins (continued)

Signal Name	364 MAP BGA	176 LQFP (F-series ONLY)	Power Group	Pad Type	Default Mode (Reset)	Default Function	Input/ Output	Value
PTC7	N2	17	VDD33	GPIO	ALT0	GPIO	Disabled	
PTC8	N4	18	VDD33	GPIO	ALT0	GPIO	Disabled	
PTC9	T15	77	VDD33	GPIO	ALT0	GPIO	Disabled	
PTC10	U15	78	VDD33	GPIO	ALT0	GPIO	Disabled	
PTC11	P4	20	VDD33	GPIO	ALT0	GPIO	Disabled	
PTC12	P3	21	VDD33	GPIO	ALT0	GPIO	Disabled	
PTC13	P1	23	VDD33	GPIO	ALT0	GPIO	Disabled	
PTC14	R1	26	VDD33	GPIO	ALT0	GPIO	Disabled	
PTC15	P2	27	VDD33	GPIO	ALT0	GPIO	Disabled	
PTC16	R3	29	VDD33	GPIO	ALT0	GPIO	Disabled	
PTC17	R4	28	VDD33	GPIO	ALT0	GPIO	Disabled	
PTC26	D16	153	VDD33	GPIO	ALT3	RCON24	Input	Disabled
PTC27	E16	154	VDD33	GPIO	ALT3	RCON25	Input	Disabled
PTC28	E15	155	VDD33	GPIO	ALT3	RCON26	Input	Disabled
PTC29	C16	152	VDD33	GPIO	ALT3	RCON27	Input	Disabled
PTC30	T8	58	VDD33	GPIO	ALT3	RCON28	Input	Disabled
PTC31	W5	42	VDD33	GPIO	ALT3	RCON29	Input	Disabled
PTD0	Y17	86	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD1	Y18	87	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD2	V18	88	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD3	Y19	89	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD4	W19	90	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD5	W20	91	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD6	V20	92	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD7	V19	93	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD8	U17	94	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD9	U18	97	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD10	U20	98	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD11	T20	99	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD12	T19	100	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD13	T18	101	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD16	D20	133	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD17	E20	132	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD18	E18	131	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD19	F16	130	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD20	F17	129	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD21	F19	128	VDD33	GPIO	ALT0	GPIO	Disabled	

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