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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A5 + Cortex®-M4
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	400MHz, 167MHz
Co-Processors/DSP	Multimedia; NEON™ MPE
RAM Controllers	LPDDR2, DDR3, DRAM
Graphics Acceleration	Yes
Display & Interface Controllers	DCU, GPU, LCD, VideoADC, VIU
Ethernet	10/100Mbps (2)
SATA	-
USB	USB 2.0 OTG + PHY (1)
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	-
Package / Case	364-LFBGA
Supplier Device Package	364-LFBGA (17x17)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mvf62nn151cmk40

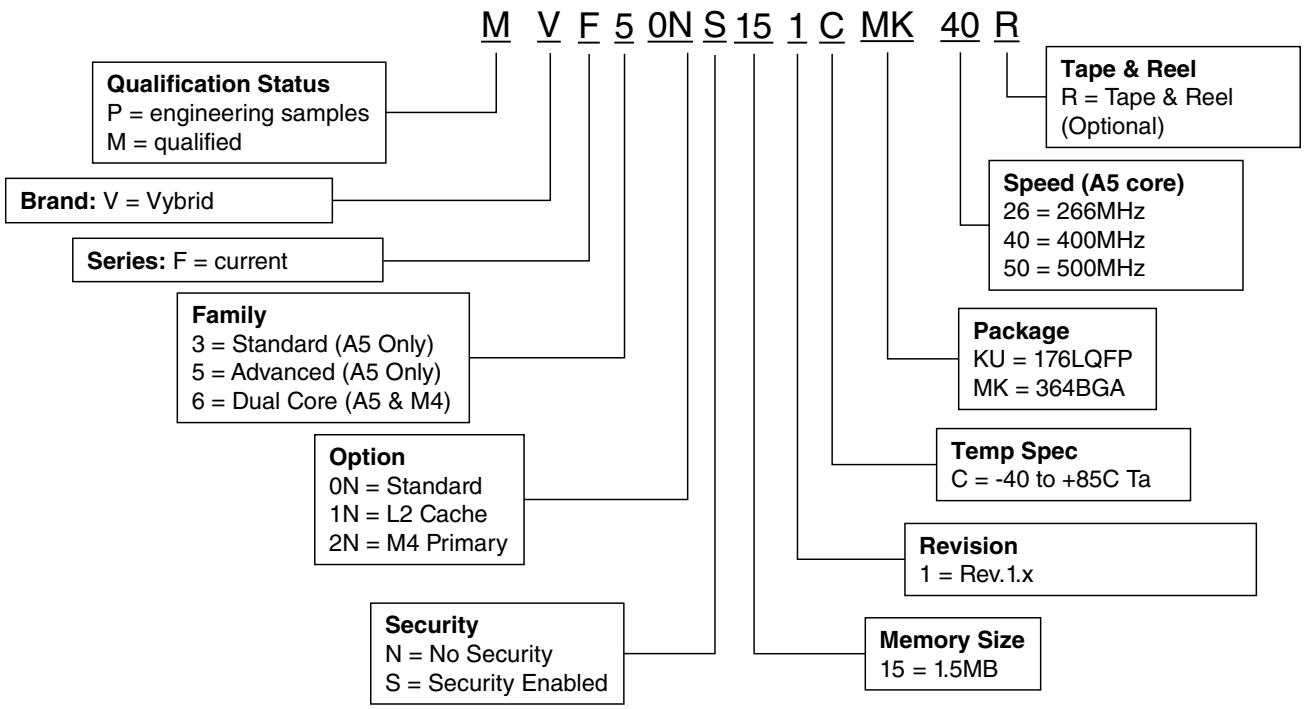


Figure 1. Part Number Format

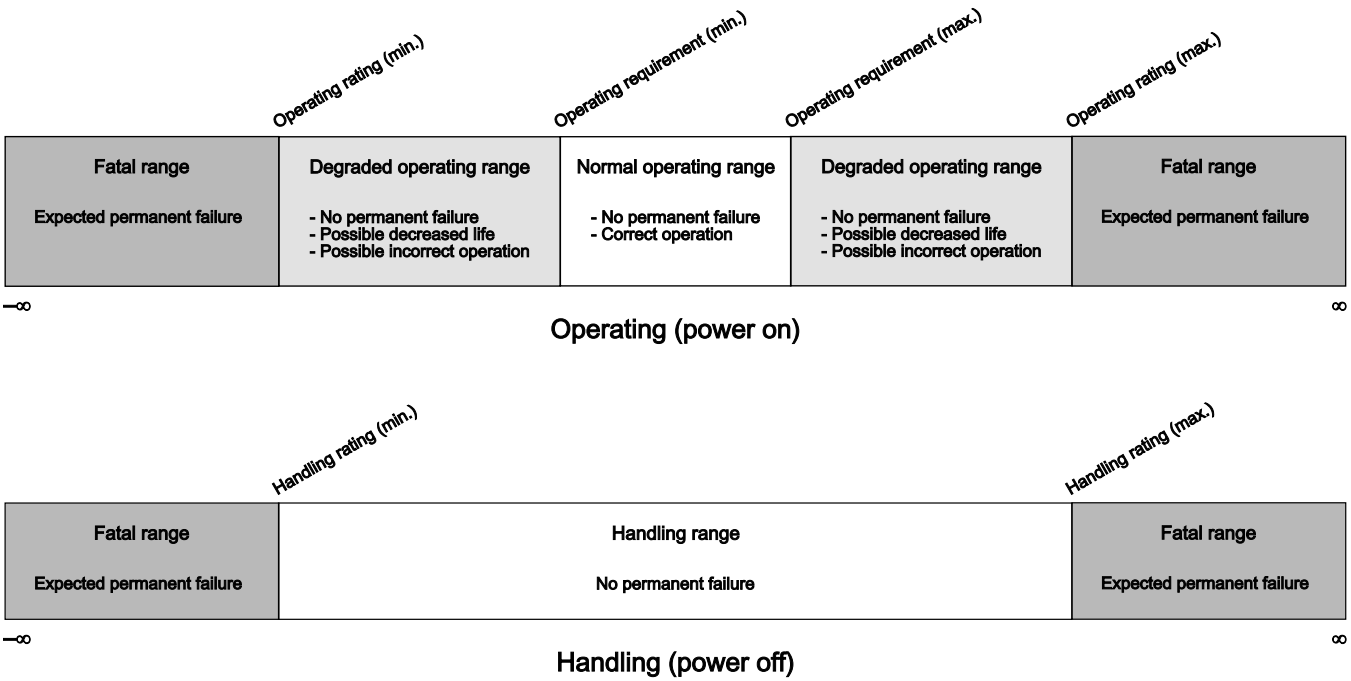
2.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
Q	Qualification status	• P = Engineering samples • M = Qualified
B	Brand	• V = Vybrid
S	Series	• F = current
F	Family	• 3 = Standard (A5 Only) • 5 = Advanced (A5 Only) • 6 = Dual Core (A5 & M4)
O	Option	• 0N = Standard • 1N = L2 Cache • 2N = M4 Primary
S	Security	• N = No Security • S = Security Enabled
MM	Memory size	• 15 = 1.5 MB

Table continues on the next page...

3.6 Relationship between ratings and operating requirements



3.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

3.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:

- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.

Table 8. General guidelines for selection of NPN ballast

Symbol	Parameters	Value	Unit	Comments
Hfe	Minimum DC current gain (Beta)	42.5		As BCTRL pin can not drive more than 20mA Minimum value of beta for a collector current of 0.85A comes out to be 42.5.
PD (Junction to ambient)	Minimum power dissipation @ TA=85 °C	2.04	W	Assuming 0.85A collector current with Collector voltage of Ballast 3.6V(max) we get VCE= 3.6V-1.2V=2.4V So power dissipated is 2.4V*0.85A=2.04W . This should be met for junction to ambient power dissipation spec of ballast
IcmaxDC peak	Maximum peak DC collector current	0.85	A	1.2A and above capacity device preferable
VBE	Maximum voltage that BCTRL pin can drive	1.25V for 0.85A @ 85 °C	V	For a VDDREG of 3.0 V (min.), BCTRL pin can drive voltage up to VDDREG - 0.5 V = 2.5 V. Since emitter of ballast is fixed at 1.25 V (max) if chosen ballast can supply 0.85 A collector current @ 85 °C with a base-to-emitter voltage of 1.25 V or lower, it is suitable for application.
Ft	Unity current gain Frequency of Ballast	50	MHz	

Reducing the collector-to-emitter voltage drop lowers the ballast transistor heat dissipation. This can be implemented in two ways:

1. By introducing series resistor or diode(s) between the collector and VDDREG (placed far enough from the transistor for proper cooling)
2. By connecting the collector to a separate lower-voltage supply

In both of the above cases the transistor has to stay away from the deep saturation region; otherwise, due to significant Hfe degradation, its base current exceeds the BCTRL output maximum value.

In general, the transistor must be selected such that its Vce saturation voltage is lower than the expected minimum Collector-Emitter voltage, and at the same time, the base current is less than 20 mA for the maximum expected collector current. More information can be found in collateral documentation at http://www.freescale.com

Table 40. Receive signal timing for RMII interfaces (continued)

	Characteristic	RMII Mode		Unit
		Min	Max	
E4, E8	RMII_CLK pulse width low	35%	65%	RMII_CLK period
E1	RXD[1:0], CVS_DV, RXER to RMII_CLK setup	4	—	ns
E2	RMII_CLK to RXD[1:0], CRS_DV, RXER hold	2	—	ns
E6	RMII_CLK to TXD[1:0], TXEN valid	—	14	ns
E5	RMII_CLK to TXD[1:0], TXEN invalid	4	—	ns

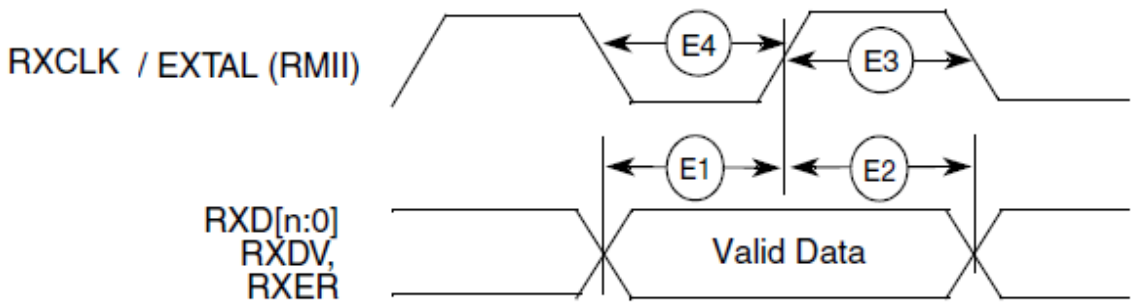


Figure 19. RMII receive signal timing diagram

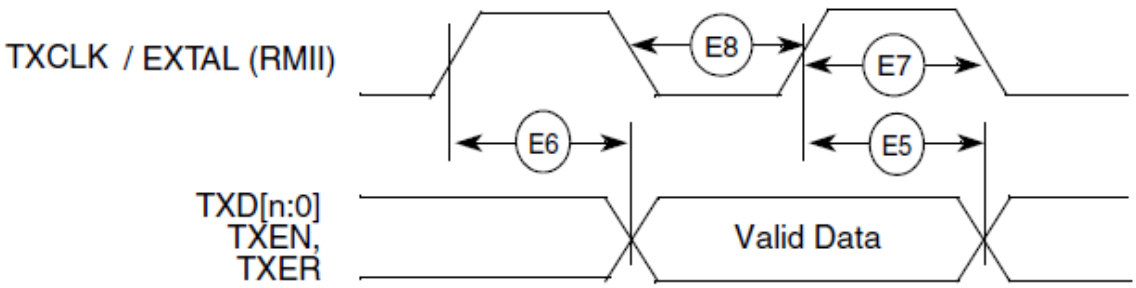


Figure 20. RMII transmit signal timing diagram

NOTE

See the most current device errata document when using the internally generated RXCLK and TXCLK clocks.

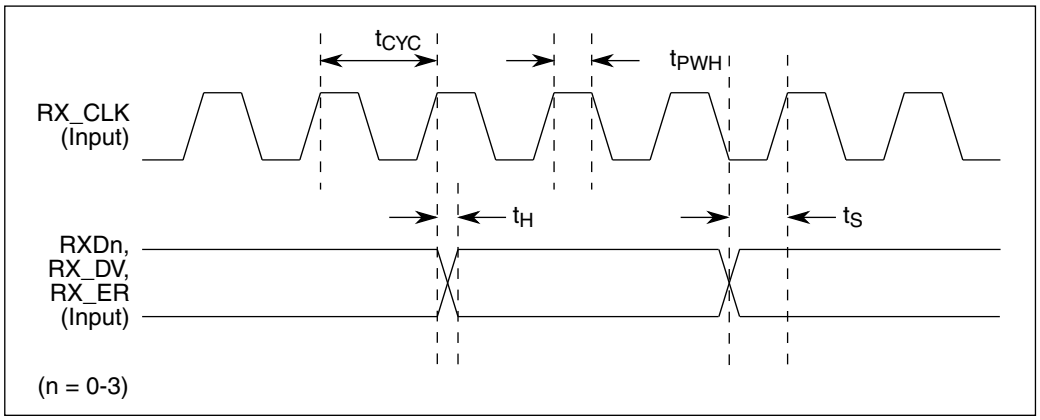


Figure 22. MII receive signal timing diagram

Table 42. Receive signal timing for MII interfaces

Characteristic		MII Mode			Unit
		Min	Typ	Max	
RX_CLK clock period (100/10 MBPS)	t_{CYC}		40/400		ns
RX_CLK duty cycle, t_{PWH}/t_{CYC}		45	50	55	%
Input setup time before RX_CLK	t_s	5			ns
Input hold time after RX_CLK	t_h	5			ns

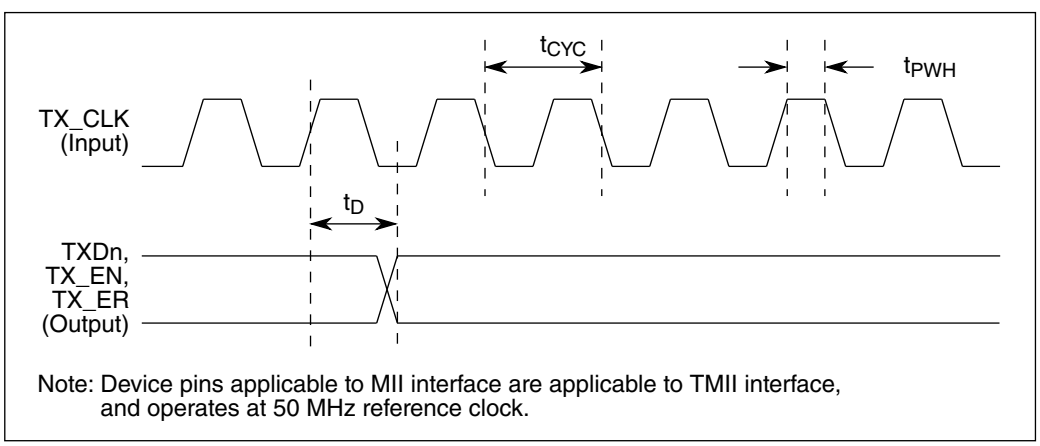


Figure 23. MII transmit signal timing diagram

Table 43. Transmit signal timing for MII interfaces

Characteristic		MII Mode			Unit
		Min	Typ	Max	
TX_CLK clock period (100/10 MBPS)	t_{CYC}		40/400		ns
TX_CLK duty cycle, t_{PWH}/t_{CYC}		45	50	55	%
Out delay from TX_CLK	t_D	2		25	ns

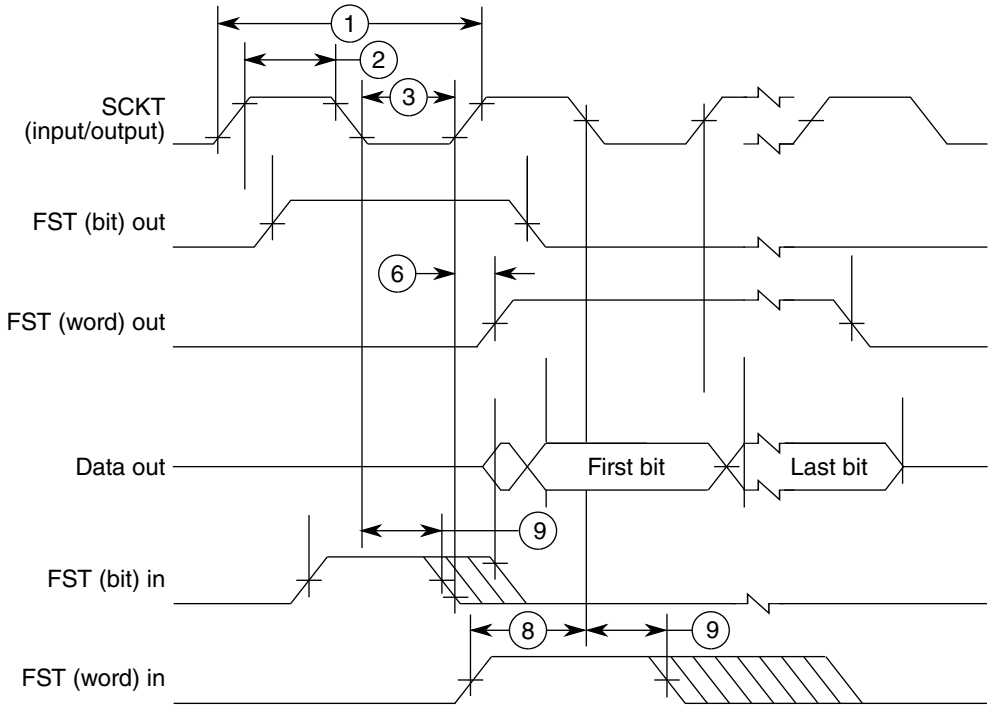


Figure 24. ESAI Transmitter Timing

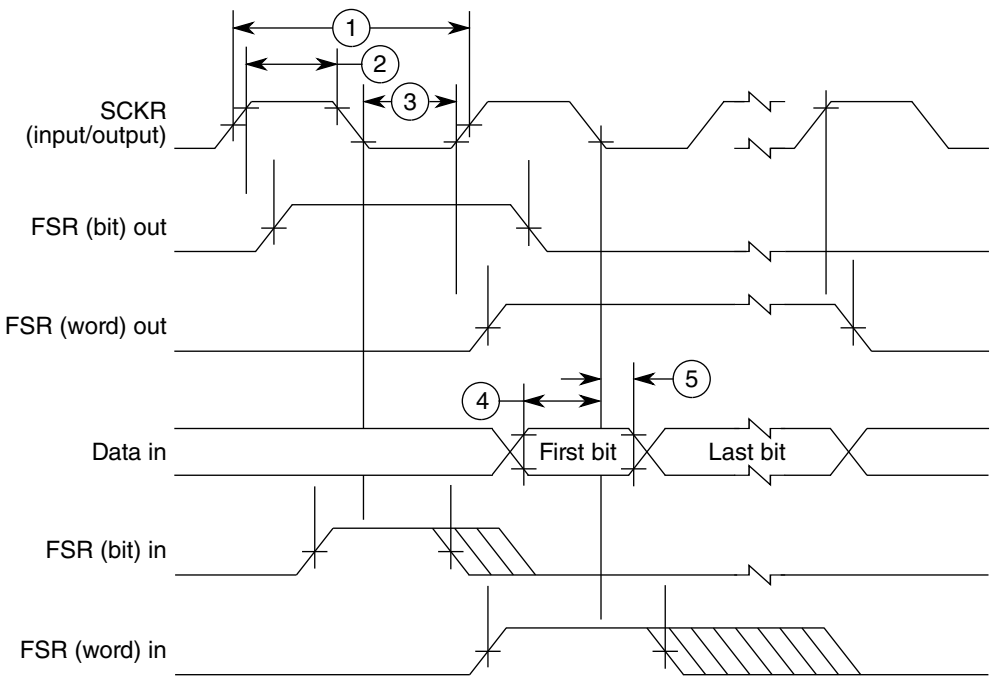


Figure 25. ESAI Receiver Timing

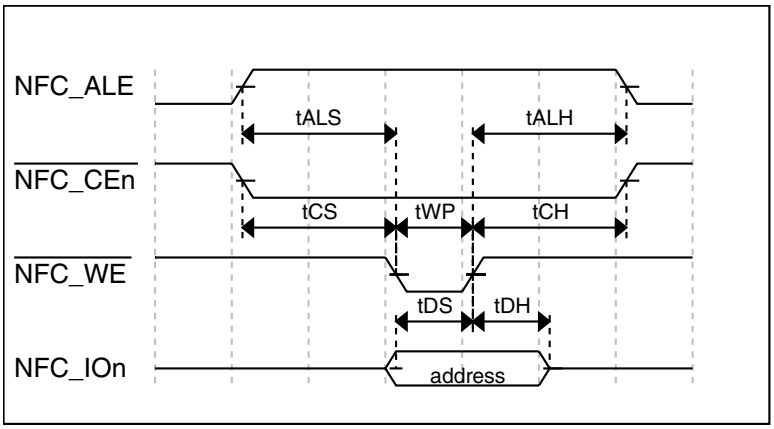


Figure 35. Address latch cycle timing

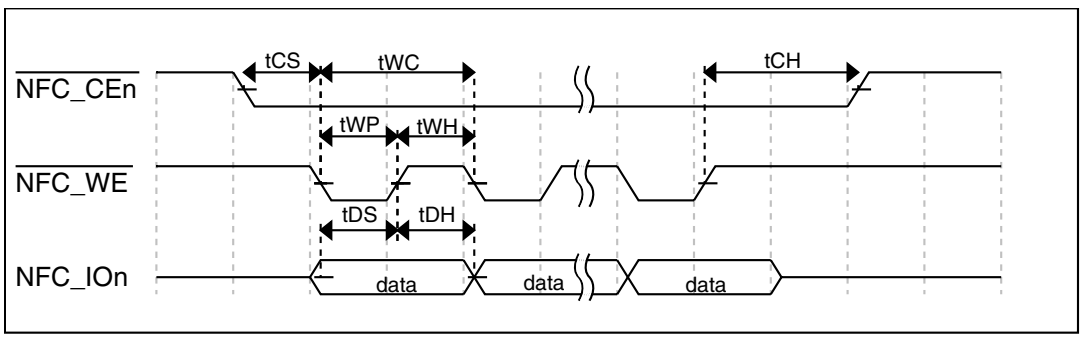


Figure 36. Write data latch cycle timing

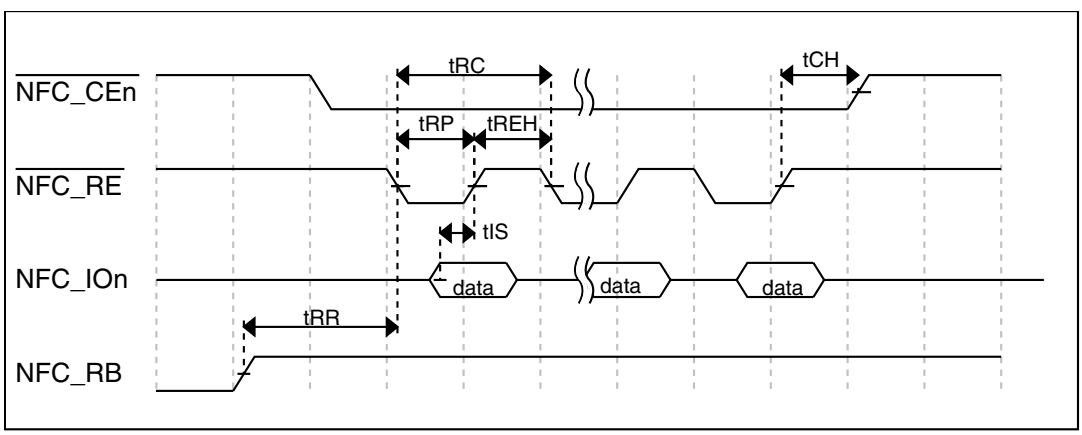


Figure 37. Read data latch cycle timing in non-fast mode

9.5.4.4 LPDDR2 Timing Parameter

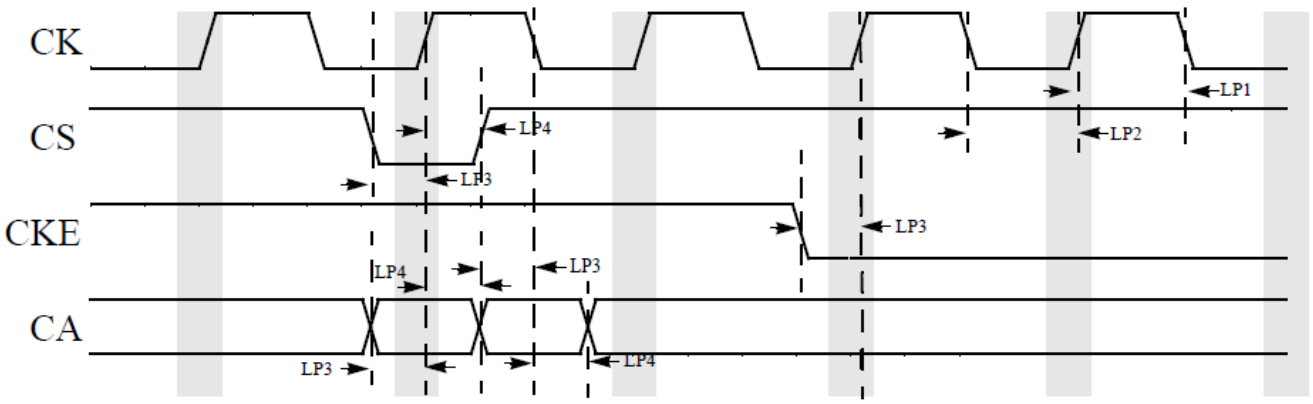


Figure 44. LPDDR2 Command and Address timing parameter

NOTE

RESET pin has a external weak pull DOWN requirement if LPDDR2 memory is NOT required to support content retention in the device low power modes where core voltage is off but DRAM voltage is on.

NOTE

RESET pin has a external weak pull UP requirement if LPDDR2 memory is required to support content retention in the device low power modes where core voltage is off but DRAM voltage is on.

NOTE

CKE pin has a external weak pull down requirement.

Table 57. LPDDR2 Timing Parameter

ID	Parameter	Symbol	CK = 400 MHz		Unit
			Min	Max	
LP1	SDRAM clock high-level width	tCH	0.45	0.55	tCK
LP2	SDRAM clock LOW-level width	tCL	0.45	0.55	tCK
LP3	CS, CKE setup time	tIS	230	-	ps
LP4	CS, CKE hold time	tIH	230	-	ps
LP3	CA setup time	tIS	230	-	ps
LP4	CA hold time	tIH	230	-	ps

NOTE

All measurements are in reference to Vref level.

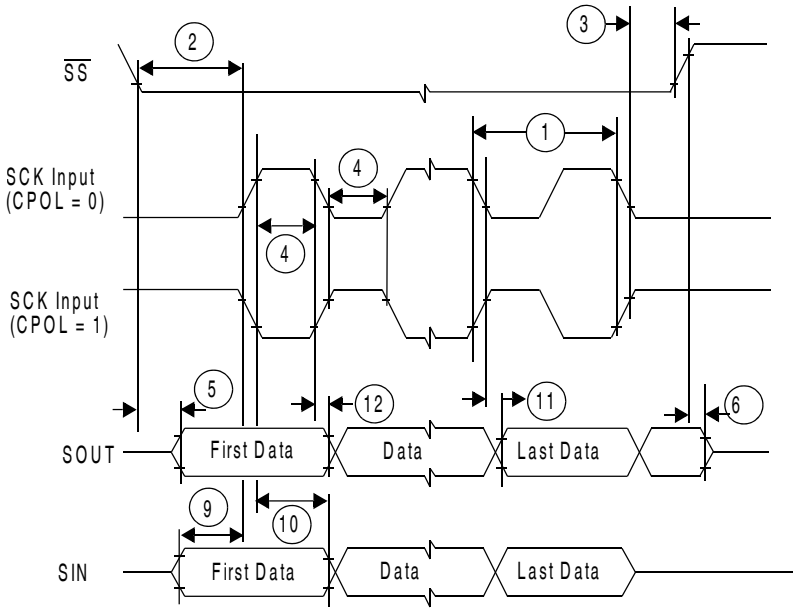


Figure 49. DSPI classic SPI timing slave, CPHA=0

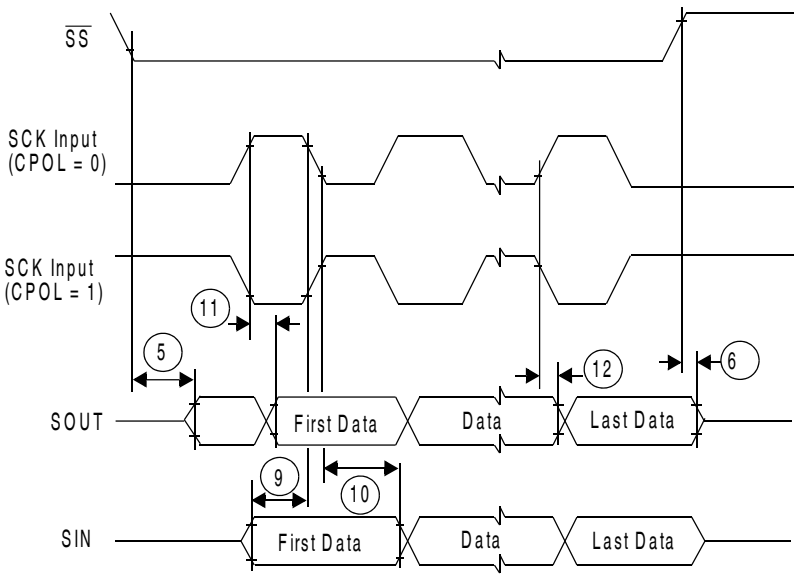


Figure 50. DSPI classic SPI timing slave, CPHA=1

9.6.2 I2C timing

Table 61. I2C input timing specifications — SCL and SDA[1]

No.	Parameter	Min.	Max.	Unit
1	Start condition hold time	2	—	PER_CLK Cycle[2]
2	Clock low time	8	—	PER_CLK Cycle

Table continues on the next page...

9.7 Clocks and PLL Specifications

9.7.1 24 MHz Oscillator Specifications

The system crystal oscillator consists of a Pierce-type structure running off the digital supply. A straight forward biased-inverter implementation is used. The crystal must be rated for a drive level of 250 µW or higher. An ESR (equivalent series resistance) of 80 Ω or less is recommended to achieve a gain margin of 5.

Table 64. 24MHz external oscillator electrical characteristics

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
f_{osc}	Crystal oscillator range	—	—	24	—	MHz
I_{osc}	Startup current	—	—	< 5	—	mA
t_{uposc}	Oscillator startup time	—	—	< 5	—	ms
C_{IN}	Input Capacitance	EXTAL and XTAL pins	—	9	—	pF
VIH	XTAL pin input high voltage	—	0.8 x Vdd[1]	—	Vdd +0.3	V
VIL	XTAL pin input low voltage	—	Vss -0.3	—	0.2 x Vdd	V

1. V_{DD} =1.1 V ± 10%, TA = -40 to +85 °C, unless otherwise specified.

9.7.2 32 KHz Oscillator Specifications

This block implements an amplifier that when combined with a suitable quartz crystal and external load capacitors implements a low power oscillator. It also implements a power mux such that it can be powered from either a ~3 V backup battery or VDDIO such as the oscillator consumes power from VDDIO when that supply is available and transitions to the back up battery when VDDIO is lost.

In addition, if the clock monitor determines that the OSC32K is not present, then the source of the 32 K will automatically switch to the 128kHz internal RC clock divided by 4.

The OSC32k runs from vdd_rtc supply, generated inside OSC32k itself from VDDIO/ VBAT. The target battery is a ~3 V coin cell. Proper choice of coin cell type is necessary for chosen VDDIO range. Appropriate series resistor (Rs) must be used when connecting the coin cell. Rs depends on the charge current limit that depends on the chosen coin cell.

For example:

- Average Discharge Voltage is 2.5 V
- Maximum Charge Current is 0.6 mA

For a charge voltage of 3.2 V, Rs = (3.2-2.5)/0.6 m = 1.17 k

Table 65. OSC32K Main Characteristics

	Notes	Min	Typ	Max
F_{OSC}	This frequency is nominal and determined mainly by the crystal selected. 32.0 K would work as well.		32.768 KHz	
Current consumption	The 4 µA is the consumption of the oscillator alone (OSC32k). Total supply consumption will depend on what the digital portion of the RTC consumes. The ring oscillator consumes 1 µA when ring oscillator is inactive, 20 µA when the ring oscillator is running. Another 1.5 µA is drawn from vdd_rtc in the power_detect block. So, the total current is 6.5 µA on vdd_rtc when the ring oscillator is not running.		4 µA	
Bias resistor	This the integrated bias resistor that sets the amplifier into a high gain state. Any leakage through the ESD network, external board leakage, or even a scope probe that is significant relative to this value will debias the amp. The debiasing will result in low gain, and will impact the circuit's ability to start up and maintain oscillations.		14 MΩ	
Crystal Properties				
Cload	Usually crystals can be purchased tuned for different Cloads. This Cload value is typically 1/2 of the capacitances realized on the PCB on either side of the quartz. A higher Cload will decrease oscillation margin, but increases current oscillating through the crystal		12.5 pF	
ESR	Equivalent series resistance of the crystal. Choosing a crystal with a higher value will decrease the oscillating margin.		50 kΩ	

9.7.3 Fast internal RC oscillator (24 MHz) electrical characteristics

This section describes a fast internal RC oscillator (FIRC). This is used as the default clock at the power-up of the device.

Table 66. Fast internal oscillator electrical characteristics

Symbol	Parameter	Condition[1]	Value			
			Min	Typ	Max	Unit
f_{RCM}	RC oscillator high frequency	T_A= 25 °C, trimmed	—	24	—	MHz
I_{RCMRUN}	RC oscillator high frequency current in running mode	T_A= 25 °C, trimmed	—	55		µA
I_{RCMPWD}	RC oscillator high frequency current in power down mode	T_A= 25 °C		100		nA
RCMTRIM	RC oscillator precision after trimming of f_{RC}	T_A= 25 °C	-1	—	+1	%

Table continues on the next page...

9.7.6 PLL3 and PLL7 (480 MHz USB PLL) Electrical Parameters

Table 69. PLL3 and PLL7 Electrical Parameters

Parameter	Value
Clock output range	480 MHz PLL output
Reference clock	24 MHz
Lock time	<425 reference cycles
Period jitter(p2p)	<140 ps
Duty Cycle	48.9%~51.7% PLL output

9.7.7 PLL5 (Ethernet PLL) Electrical Parameters

Table 70. PLL5 Electrical Parameters

Parameter	Value
Clock output range	500 MHz
Reference clock	24 MHz
Lock time	<7500 reference cycles
Cycle to cycle jitter (p2p)[1]	<400ps @ 50 MHz
Duty Cycle	45%~55%

1. Jitter numbers are measured at divided PLL clock because high frequency cannot be brought-out IO pad.

9.7.8 PLL4 (Audio PLL) Electrical Parameters

Table 71. PLL4 Electrical Parameters

Parameter	Value
Clock output range	650 MHz ~1.3 GHz
Reference clock	24 MHz
Lock time	<7500 reference cycles
Long term jitter(RMS)	<42ps @1128MHz
Period jitter(p2p)[1]	<115ps@1128MHz
Duty Cycle	43%~57%

1. Jitter numbers are measured at divided PLL clock because high frequency cannot be brought-out on IO pad.

Board type	Symbol	Description	176LQFP	Unit	Notes
		to package top (natural convection)			

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance
2. Per JEDEC JESD51-2 with the single layer board (JESD51-3) horizontal
3. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

Board type	Symbol	Description	364 MAPBGA	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	45	°C/W	1, 2
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	28	°C/W	1, 3
Single-layer (1s)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./ min. air speed)	37	°C/W	1,3
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./ min. air speed)	24	°C/W	1,3
—	$R_{\theta JB}$	Thermal resistance, junction to board	17	°C/W	4
—	$R_{\theta JC}$	Thermal resistance, junction to case	10	°C/W	5
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	2	°C/W	6

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

364 MAP BGA	176 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
K2	4	JTDI	JTDI	PTA9	JTDI	RMII_ CLKOUT	RMII_CLKIN/ MII0_TXCLK	DCU0_R1		WDOG_b		
K1	5	JTDO	JTDO/ TRACESWO	PTA10	JTDO	EXT_AUDIO_ MCLK		DCU0_G0		ENET_TS_ CLKIN	MLBSIGNAL	
L1	6	JTMS/ SWDIO	JTMS/ SWDIO	PTA11	JTMS/ SWDIO			DCU0_G1			MLBDATA	
L3	7	PTA12		PTA12	TRACECK	EXT_AUDIO_ MCLK				VIU_DATA13	I2C0_SCL	
Y5	43	PTA16		PTA16	TRACED0	USB0_ VBUS_EN	ADC1_SE0	LCD29	SAI2_TX_ BCLK	VIU_DATA14	I2C0_SDA	
Y6	44	PTA17		PTA17	TRACED1	USB0_ VBUS_OC	ADC1_SE1	LCD30	USB0_SOF_ PULSE	VIU_DATA15	I2C1_SCL	
V6	46	PTA18		PTA18	TRACED2	ADC0_SE0	FTM1_QD_ PHA	LCD31	SAI2_TX_ DATA	VIU_DATA16	I2C1_SDA	
U6	47	PTA19		PTA19	TRACED3	ADC0_SE1	FTM1_QD_ PHB	LCD32	SAI2_TX_ SYNC	VIU_DATA17	QSPI1_A_ SCK	
B18	143	PTA20		PTA20	TRACED4			LCD33		SCI3_TX	DCU1_ HSYNC/ DCU1_ TCON1	
D18	145	PTA21		PTA21/ MII0_RXCLK	TRACED5				SAI2_RX_ BCLK	SCI3_RX	DCU1_ VSYNC/ DCU1_ TCON2	
E17	147	PTA22		PTA22	TRACED6				SAI2_RX_ DATA	I2C2_SCL	DCU1_TAG/ DCU1_ TCON0	
C17	148	PTA23		PTA23	TRACED7				SAI2_RX_ SYNC	I2C2_SDA	DCU1_DE/ DCU1_ TCON3	
R16	—	PTA24		PTA24	TRACED8	USB1_ VBUS_EN			SDHC1_CLK	DCU1_ TCON4		
R17	—	PTA25		PTA25	TRACED9	USB1_ VBUS_OC			SDHC1_CMD	DCU1_ TCON5		
R19	—	PTA26		PTA26	TRACED10	SAI3_TX_ BCLK			SDHC1_ DAT0	DCU1_ TCON6		
R20	—	PTA27		PTA27	TRACED11	SAI3_RX_ BCLK			SDHC1_ DAT1	DCU1_ TCON7		
P20	—	PTA28		PTA28	TRACED12	SAI3_RX_ DATA	ENET1_ 1588_TMR0	SCI4_TX	SDHC1_ DAT2	DCU1_ TCON8		
P18	—	PTA29		PTA29	TRACED13	SAI3_TX_ DATA	ENET1_ 1588_TMR1	SCI4_RX	SDHC1_ DAT3	DCU1_ TCON9		
P17	—	PTA30		PTA30	TRACED14	SAI3_RX_ SYNC	ENET1_ 1588_TMR2	SCI4_RTS	I2C3_SCL		SCI3_TX	
P16	—	PTA31		PTA31	TRACED15	SAI3_TX_ SYNC	ENET1_ 1588_TMR3	SCI4_CTS	I2C3_SDA		SCI3_RX	
T6	49	PTB0		PTB0	FTM0_CH0	ADC0_SE2	TRACECTL	LCD34	SAI2_RX_ BCLK	VIU_DATA18	QSPI1_A_ CS0	

364 MAP BGA	176 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
A10	—	DDR_A[13]			DDR_A13							
C10	—	DDR_A[12]			DDR_A12							
D10	—	DDR_A[11]			DDR_A11							
D7	—	DDR_A[10]			DDR_A10							
B9	—	DDR_A[9]			DDR_A9							
A11	—	DDR_A[8]			DDR_A8							
A7	—	DDR_A[7]			DDR_A7							
A9	—	DDR_A[6]			DDR_A6							
B6	—	DDR_A[5]			DDR_A5							
A6	—	DDR_A[4]			DDR_A4							
B7	—	DDR_A[3]			DDR_A3							
A8	—	DDR_A[2]			DDR_A2							
C11	—	DDR_A[1]			DDR_A1							
C7	—	DDR_A[0]			DDR_A0							
D8	—	DDR_BA[2]			DDR_BA2							
C9	—	DDR_BA[1]			DDR_BA1							
C8	—	DDR_BA[0]			DDR_BA0							
B4	—	DDR_CAS_b			DDR_CAS_b							
A5	—	DDR_CKE[0]			DDR_CKE0							
A2	—	DDR_CLK[0]			DDR_CLK0							
B2	—	DDR_CLK_ b[0]			DDR_CLK_ b0							
C5	—	DDR_CS_ b[0]			DDR_CS_b0							
D2	—	DDR_D[15]			DDR_D15							
H2	—	DDR_D[14]			DDR_D14							
C1	—	DDR_D[13]			DDR_D13							
G1	—	DDR_D[12]			DDR_D12							
E2	—	DDR_D[11]			DDR_D11							
H1	—	DDR_D[10]			DDR_D10							
D1	—	DDR_D[9]			DDR_D9							
J1	—	DDR_D[8]			DDR_D8							
G3	—	DDR_D[7]			DDR_D7							
C3	—	DDR_D[6]			DDR_D6							
J3	—	DDR_D[5]			DDR_D5							
F3	—	DDR_D[4]			DDR_D4							
G4	—	DDR_D[3]			DDR_D3							
D4	—	DDR_D[2]			DDR_D2							
H3	—	DDR_D[1]			DDR_D1							
F4	—	DDR_D[0]			DDR_D0							
G2	—	DDR_DQM[1]			DDR_DQM1							

364 MAP BGA	176 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
Y19	89	PTD3		PTD3	QSPI0_A_DATA2	SCI2_CTS	SPI1_PCS2	FB_AD12	SPDIF_PLOCK			
W19	90	PTD4		PTD4	QSPI0_A_DATA1		SPI1_PCS1	FB_AD11	SPDIF_SRCLK			
W20	91	PTD5		PTD5	QSPI0_A_DATA0		SPI1_PCS0	FB_AD10				
V20	92	PTD6		PTD6	QSPI0_A_DQS		SPI1_SIN	FB_AD9				
V19	93	PTD7		PTD7	QSPI0_B_SCK		SPI1_SOUT	FB_AD8				
U17	94	PTD8		PTD8	QSPI0_B_CS0	FB_CLKOUT	SPI1_SCK	FB_AD7				
U18	97	PTD9		PTD9	QSPI0_B_DATA3	SPI3_PCS1		FB_AD6		SAI1_TX_SYNC	DCU1_B0	
U20	98	PTD10		PTD10	QSPI0_B_DATA2	SPI3_PCS0		FB_AD5			DCU1_B1	
T20	99	PTD11		PTD11	QSPI0_B_DATA1	SPI3_SIN		FB_AD4				
T19	100	PTD12		PTD12	QSPI0_B_DATA0	SPI3_SOUT		FB_AD3				
T18	101	PTD13		PTD13	QSPI0_B_DQS	SPI3_SCK		FB_AD2				
A19	141	PTB23		PTB23	SAI0_TX_BCLK	SCI1_TX		FB_MUXED_ALE	FB_TS_b	SCI3_RTS	DCU1_G3	
A18	142	PTB24		PTB24	SAI0_RX_BCLK	SCI1_RX		FB_MUXED_TSIZ0	NF_WE_b	SCI3_CTS	DCU1_G4	
B17	149	PTB25		PTB25	SAI0_RX_DATA	SCI1_RTS		FB_CS1_b	NF_CE0_b		DCU1_G5	
A17	150	PTB26	RCON21	PTB26	SAI0_TX_DATA	SCI1_CTS	RCON21	FB_CS0_b	NF_CE1_b		DCU1_G6	
U8	57	PTB27	RCON22	PTB27	SAI0_RX_SYNC		RCON22	FB_OE_b	FB_MUXED_TBST_b	NF_RE_b	DCU1_G7	
A16	151	PTB28	RCON23	PTB28	SAI0_TX_SYNC		RCON23	FB_RW_b			DCU1_B6	
D16	153	PTC26	RCON24	PTC26	SAI1_TX_BCLK	SPI0_PCS5	RCON24	FB_TA_b	NF_RB_b		DCU1_B7	
E16	154	PTC27	RCON25	PTC27	SAI1_RX_BCLK	SPI0_PCS4	RCON25	FB_BE3_b	FB_CS3_b	NF_ALE	DCU1_B2	
E15	155	PTC28	RCON26	PTC28	SAI1_RX_DATA	SPI0_PCS3	RCON26	FB_BE2_b	FB_CS2_b	NF_CLE	DCU1_B3	
C16	152	PTC29	RCON27	PTC29	SAI1_TX_DATA	SPI0_PCS2	RCON27	FB_BE1_b	FB_MUXED_TSIZ1		DCU1_B4	
T8	58	PTC30	RCON28	PTC30	SAI1_RX_SYNC	SPI1_PCS2	RCON28	FB_MUXED_BE0_b	FB_TSIZ0	ADC0_SE5	DCU1_B5	
W5	42	PTC31	RCON29	PTC31	SAI1_TX_SYNC		RCON29			ADC1_SE5	DCU1_B6	

364 MAP BGA	176 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
U14	74	EXT_ TAMPER1			EXT_ TAMPER1							
T13	—	EXT_ TAMPER2/ EXT_WM0_ TAMPER_IN			EXT_ TAMPER2/ EXT_WM0_ TAMPER_IN							
U13	—	EXT_ TAMPER3/ EXT_WM0_ TAMPER_ OUT			EXT_ TAMPER3/ EXT_WM0_ TAMPER_ OUT							
U12	—	EXT_ TAMPER4/ EXT_WM1_ TAMPER_IN			EXT_ TAMPER4/ EXT_WM1_ TAMPER_IN							
U10	—	EXT_ TAMPER5/ EXT_WM1_ TAMPER_ OUT			EXT_ TAMPER5/ EXT_WM1_ TAMPER_ OUT							
G7	2	VDD			VDD							
J7	—	VDD			VDD							
L7	22	VDD			VDD							
H8	48	VDD			VDD							
K8	85	VDD			VDD							
M8	102	VDD			VDD							
P8	125	VDD			VDD							
G9	136	VDD			VDD							
N9	174	VDD			VDD							
H10	—	VDD			VDD							
P10	—	VDD			VDD							
G11	—	VDD			VDD							
N11	—	VDD			VDD							
H12	—	VDD			VDD							
P12	—	VDD			VDD							
G13	—	VDD			VDD							
J13	—	VDD			VDD							
L13	—	VDD			VDD							
N13	—	VDD			VDD							
H14	—	VDD			VDD							
K14	—	VDD			VDD							
M14	—	VDD			VDD							
P14	—	VDD			VDD							
A1	1	VSS			VSS							
A20	13	VSS			VSS							

364 MAP BGA	176 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
B3	24	VSS			VSS							
B5	32	VSS			VSS							
B8	—	VSS			VSS							
B11	—	VSS			VSS							
B13	—	VSS			VSS							
B16	—	VSS			VSS							
B19	—	VSS			VSS							
C2	—	VSS			VSS							
D17	—	VSS			VSS							
E5	—	VSS			VSS							
E8	—	VSS			VSS							
E11	—	VSS			VSS							
E14	—	VSS			VSS							
E19	—	VSS			VSS							
F2	—	VSS			VSS							
G17	—	VSS			VSS							
H4	—	VSS			VSS							
J2	—	VSS			VSS							
J18	—	VSS			VSS							
M2	—	VSS			VSS							
M4	—	VSS			VSS							
M18	—	VSS			VSS							
R2	—	VSS			VSS							
R18	—	VSS			VSS							
U7	—	VSS			VSS							
U19	—	VSS			VSS							
V13	—	VSS			VSS							
W6	—	VSS			VSS							
V17	—	VSS			VSS							
Y1	—	VSS			VSS							
Y20	—	VSS			VSS							
H19	—	VSS			VSS							
L19	—	VSS			VSS							
P19	—	VSS			VSS							
J5	—	SDRAMC_ VDD2P5			SDRAMC_ VDD2P5							
E6	—	SDRAMC_ VDD2P5			SDRAMC_ VDD2P5							
E10	—	SDRAMC_ VDD2P5			SDRAMC_ VDD2P5							

Table 78. Functional Assignment Pins (continued)

Signal Name	364 MAP BGA	176 LQFP (F-series ONLY)	Power Group	Pad Type	Default Mode (Reset)	Default Function	Input/ Output	Value
EXT_TAMPER5/ EXT_WM1_TAMPER_OUT	U10	—	VBAT	Analog	—	EXT_TAMPER5/ EXT_WM1_TAMPER_OUT	—	—
EXTAL	Y13	73	DECAP_V11_LDO_OUT	Analog	—	EXTAL	—	—
EXTAL32	Y12	70	DECAP_V11_LDO_OUT	Analog	—	EXTAL32	—	—
JTCLK/ SWCLK	K4	3	VDD33	GPIO	ALT1	JTAG	Input	100K PU
JTDI	K2	4	VDD33	GPIO	ALT1	JTAG	Input	100K PU
JTDO	K1	5	VDD33	GPIO	ALT1	JTAG	Disabled	—
JTMS/ SWDIO	L1	6	VDD33	GPIO	ALT1	JTAG	Input	100K PU
LVDS0P	W14	—	DECAP_V25_LDO_OUT	Analog	—	LVDS0P	—	—
LVDS0N	Y14	—	DECAP_V25_LDO_OUT	Analog	—	LVDS0N	—	—
PTA6	N5	19	VDD33	GPIO	ALT0	GPIO	Disabled	
PTA7	V15	79	VDD33	GPIO	ALT0	GPIO	Disabled	
PTA12	L3	7	VDD33	GPIO	ALT0	GPIO	Disabled	
PTA16	Y5	43	VDD33	GPIO	ALT0	GPIO	Disabled	
PTA17	Y6	44	VDD33	GPIO	ALT0	GPIO	Disabled	
PTA18	V6	46	VDD33	GPIO	ALT0	GPIO	Disabled	
PTA19	U6	47	VDD33	GPIO	ALT0	GPIO	Disabled	
PTA20	B18	143	VDD33	GPIO	ALT0	GPIO	Disabled	
PTA21	D18	145	VDD33	GPIO	ALT0	GPIO	Disabled	
PTA22	E17	147	VDD33	GPIO	ALT0	GPIO	Disabled	
PTA23	C17	148	VDD33	GPIO	ALT0	GPIO	Disabled	
PTA24	R16	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTA25	R17	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTA26	R19	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTA27	R20	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTA28	P20	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTA29	P18	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTA30	P17	—	VDD33	GPIO	ALT0	GPIO	Disabled	

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Table 78. Functional Assignment Pins (continued)

Signal Name	364 MAP BGA	176 LQFP (F-series ONLY)	Power Group	Pad Type	Default Mode (Reset)	Default Function	Input/ Output	Value
XTAL	W13	72	DECAP_V11_LDO_OUT	Analog	—	XTAL	—	—
XTAL32	W12	71	DECAP_V11_LDO_OUT	Analog	—	XTAL32	—	—

15 Revision History

The following table provides a revision history for this document.

Table 79. Revision History

Rev. No.	Date	Substantial Changes
Rev1	12/2011	Initial release
Rev2	02/2012	Updated feature list Updated VREG electrical specifications Updated LDO_1P1, LDO2P5 tables Updated DDR IO parameters Added DDR memory controller parameters Updated Power sequencing table Added Power supply diagram Updated Recommended operating conditions Replaced DryIce Tamper Electrical Specifications with Voltage and temperature monitor electrical specifications Updated VideoADC electricals. Updated VideoADC supply scheme diagram. Added VideoADC supply_decoupling diagram Added QuadSPI DDR mode electrical specifications Updated Fast internal RC oscillator table Updated Slow internal RC oscillator table Updated Pinouts section

Table continues on the next page...