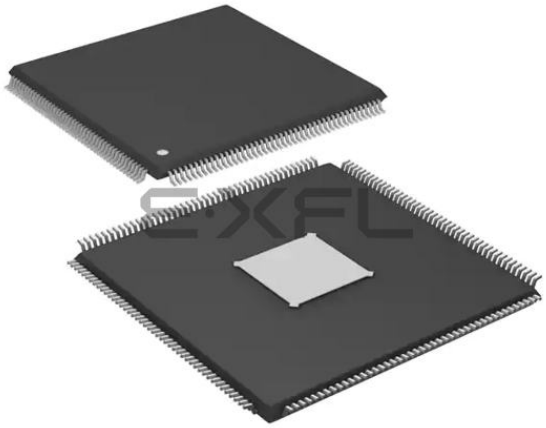


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-A5
Core Size	32-Bit Single-Core
Speed	266MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, SCI, SD, SPI, UART/USART, USB OTG
Peripherals	DMA, LVD, WDT
Number of I/O	-
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	1.5MB
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 12bit SAR; D/A 12bit
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	176-LQFP Exposed Pad
Supplier Device Package	176-HLQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/pvf30nn151cku26

- Display and Video
  - Dual Display Control Unit (DCU) with support for color TFT display up to SVGA
  - Segmented LCD (3V Glass only) configurable as 40x4, 38x8, and 36x6
  - Video Interface Unit (VIU) for camera
  - Open VG Graphics Processing Unit (GPU)
  - VideoADC
- Analog
  - Dual 12-bit SAR ADC with 1MS/s
  - Dual 12-bit DAC
- Audio
  - Four Synchronous Audio Interface (SAI)
  - Enhanced Serial Audio Interface (ESAI)
  - Sony Philips Digital Interface (SPDIF), Rx and Tx
  - Asynchronous Sample Rate Converter (ASRC)
- Human-Machine Interface (HMI)
  - GPIO pins with interrupt support, DMA request capability, digital glitch filter.
  - Hysteresis and configurable pull up/down device on all input pins
  - Configurable slew rate and drive strength on all output pins
- On-Chip Memory
  - 512 KB On-chip SRAM with ECC
  - 1 MB On-chip graphics SRAM (no ECC). This depends on the part selected. Alternate configuration could be 512 KB graphics and 512 KB L2 cache.
  - 96 KB Boot ROM

Field	Description	Values
R	Revision	• 1 = Rev 1.x
T	Temperature range (°C)	• C = -40 °C to +85 °C T_a
PP	Package type	• KU = 176LQFP • MK = 364 MAPBGA
S	Speed	• Speed A5 Core • 26 = 266MHz • 40 = 400MHz • 50 = 500MHz

2.4 Part Numbers

This table lists the part numbers on the device.

Part Number	Package	Description
MVF30NN151CKU26	LQFP-EP 176 24*24*1.6	A5-266, No Security, 176LQFP
MVF30NS151CKU26	LQFP-EP 176 24*24*1.6	A5-266, Security, 176LQFP
MVF50NN151CMK40	MAP 364 17*17*1.5 P0.8	A5-400, No Security, 364BGA
MVF50NS151CMK40	MAP 364 17*17*1.5 P0.8	A5-400, Security, 364BGA
MVF50NN151CMK50	MAP 364 17*17*1.5 P0.8	A5-500, No Security, 364BGA
MVF50NS151CMK50	MAP 364 17*17*1.5 P0.8	A5-500, Security, 364BGA
MVF51NN151CMK50	MAP 364 17*17*1.5 P0.8	A5-500, L2 Cache, No Security, 364BGA
MVF51NS151CMK50	MAP 364 17*17*1.5 P0.8	A5-500, L2 Cache, Security, 364BGA
MVF60NN151CMK40	MAP 364 17*17*1.5 P0.8	A5-400, M4, No Security, 364BGA
MVF60NS151CMK40	MAP 364 17*17*1.5 P0.8	A5-400, M4, Security, 364BGA
MVF60NN151CMK50	MAP 364 17*17*1.5 P0.8	A5-500, M4, No Security, 364BGA
MVF60NS151CMK50	MAP 364 17*17*1.5 P0.8	A5-500, M4, Security, 364BGA
MVF61NN151CMK50	MAP 364 17*17*1.5 P0.8	A5-500, M4, L2 Cache, No Security, 364BGA
MVF61NS151CMK50	MAP 364 17*17*1.5 P0.8	A5-500, M4, L2 Cache, Security, 364BGA
MVF62NN151CMK40	MAP 364 17*17*1.5 P0.8	A5-400, M4 Primary, No Security, 364BGA

3 Terminology and guidelines

3.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

3.1.1 Example

This is an example of an operating requirement:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	0.9	1.1	V

3.2 Definition: Operating behavior

Unless otherwise specified, an *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

3.2.1 Example

This is an example of an operating behavior:

Symbol	Description	Min.	Max.	Unit
I_{WP}	Digital I/O weak pullup/ pulldown current	10	130	µA

3.3 Definition: Attribute

An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

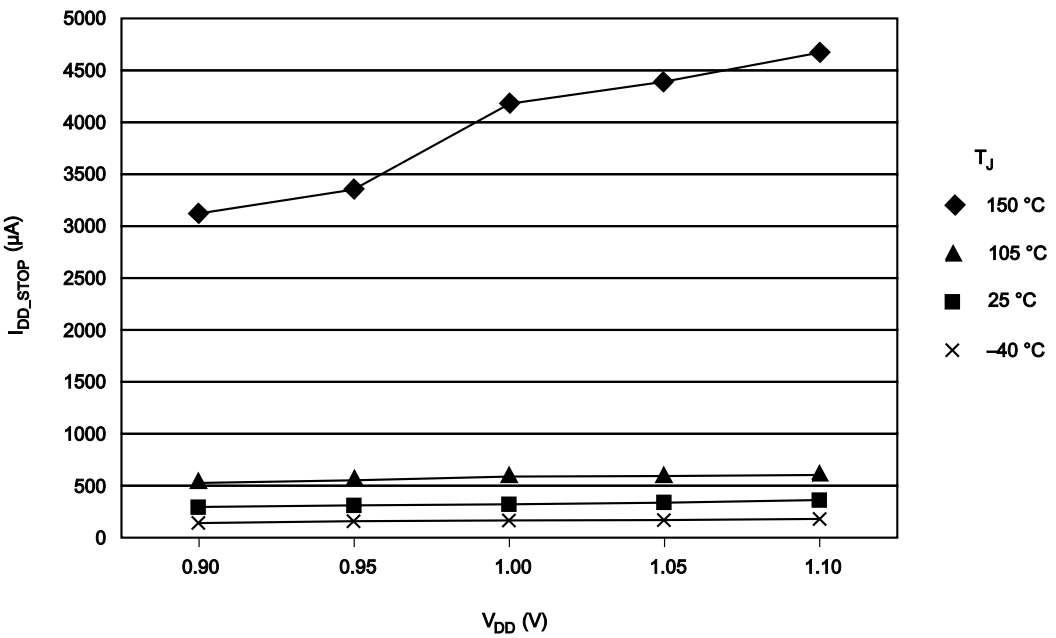
3.8.1 Example 1

This is an example of an operating behavior that includes a typical value:

Symbol	Description	Min.	Typ.	Max.	Unit
I_{WP}	Digital I/O weak pullup/pulldown current	10	70	130	µA

3.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions:



3.9 Typical Value Conditions

Typical values assume you meet the following conditions (or other conditions as specified):

Symbol	Description	Value	Unit
T_A	Ambient temperature	25	°C
V_{DD}	3.3 V supply voltage	3.3	V

4 Handling ratings

4.1 ESD Handling Ratings Table [JEDEC]

Symbol	Description	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model	2000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model	Corner pins: 750 Other pins: 500	V	2

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.

4.2 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	–55	150	°C	1
T_{SDR}	Solder temperature, lead-free	—	260	°C	2
	Solder temperature, leaded	—	245		

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

4.3 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

6.2.1.5 External NPN Ballast

The internal main regulator requires an external NPN ballast transistor to be connected as shown in the following figure as well as an external capacitance to be connected to the device in order to provide a stable 1.2V digital supply to the device. The HPREG design allows for collector voltage lower than VDDREG value. See AN4807 at www.freescale.com .

NOTE

To not overload BCTRL output, collector voltage should appear no later than VDDREG / VDD33 (3.3V).

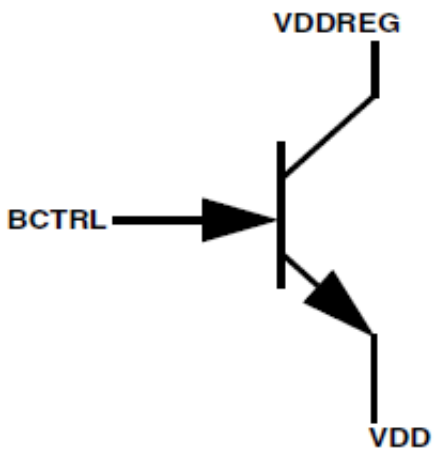


Figure 3. External NPN Ballast connections

Table 6. BCTRL OUTPUT specification

Parameter	Value	Comments
BCTRL OUTPUT specification	20mA	BCTRL driver can not drive more than 20mA current
Maximum pin voltage	VDDREG-0.5V	For Example, VDDREG =3.0V BCTRL should not exceed 2.5V.

Table 7. Assumptions For calculations

Parameter	Value
VDDREG	3.0V to 3.6V with typical value of 3.3V
Max DC Collector current	0.85A @85 °C
Emitter voltage	1.2V to 1.25V
Collector voltage	Equal to VDDREG

3. The reported emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.
4. IEC Level Maximums: N ≤ 12dBmV, M ≤ 18dBmV, L ≤ 24dBmV, K ≤ 30dBmV, I ≤ 36dBmV, H ≤ 42dBmV

6.2.7 EMC Radiated Emissions Web Search Procedure boilerplate

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to www.freescale.com.
2. Perform a keyword search for "EMC design."

6.2.8 Capacitance attributes

Table 18. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C_{IN_A}	Input capacitance: analog pins	—	7	pF
C_{IN_D}	Input capacitance: digital pins	—	7	pF

7 I/O parameters

7.1 GPIO parameters

Table 19. GPIO DC operating conditions

Symbol	Parameter	Min	Typ	Max	Unit
vddi[1]	Core internal supply voltage		1.2		V
ovdd	I/O output supply voltage	3	3.3	3.6	V

1. This is internally controlled.

Table 20. GPIO DC Electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
Voh	High-level output voltage	Ioh= -1mA	ovdd-0.15			V

Table continues on the next page...

Table 20. GPIO DC Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
		VOH/VOL values are with respect to DSE=001[1]				
Vol	Low-level output voltage	Iol= 1mA			0.15	V
Vih [2]	High-Level DC input voltage		0.7*ovdd		ovdd	V
Vil[2]	Low-Level DC input voltage		0		0.3*ovdd	V
Vhys	Input Hysteresis	ovdd=3.3 V	250			mV
Vt+[2, 3]	Schmitt trigger VT+		0.5*ovdd			V
Vt-[2, 3]	Schmitt trigger VT-				0.5*ovdd	V
Iin[4]	Input current (no pull-up/down)	Vin = ovdd or 0	-1		1	uA
Iin_22pu	Input current (22KOhm PU)	Vin = 0			212	uA
		Vin = ovdd			1	
Iin_47pu	Input current (47KOhm PU)	Vin = 0			100	
		Vin = ovdd			1	
Iin_100pu	Input current (100KOhm PU)	Vin = 0			50	
		Vin = ovdd			1	
Iin_100pd	Input current (100KOhm PD)	Vin = 0			1	
		Vin = ovdd			50	
R_Keeper	Keeper Circuit Resistance	Vin = 0.3 x OVDD VI = 0.7 x OVDD	105		175	Ohm
Issod	Sink current in open drain mode	Vin = ovdd			7	mA
Issop	Sink/source current in Push Pull mode	Vin = ovdd			7	mA

1. For details about Software MUX Pad Control Register DSE bit, see IOMUX Controller chapter of the device reference manual.
2. To maintain a valid level, the transitioning edge of the input must sustain a constant slew rate (monotonic) from the current DC level through to the target DC level, VIL or VIH. Monotonic input transition time is from 0.1ns to 1s. Vil and Vih do not apply when hysteresis is enabled.
3. Hysteresis of 250 mV is guaranteed over all operating conditions when hysteresis is enabled.
4. Typ condition: typ model, 3.3V, and 25°C. Max condition: bcs model, 3.6V, and -40°C. Min condition: wcs model, 3.0V and 85 °C. These values are for digital IO buffer cells.

Table 21. GPIO AC Electrical Characteristics (3.3V power mode)

Symbol	Parameter	Drive strength[1]	Slew rate	Test conditions	Min	Max	Unit
tpr	IO Output Transition Times (PA1), rise/fall	Max 1 1 1	slow	15pF Cload on pad, input edge rate 200ps	1.70	1.81	ns
			fast		1.04	1.18	
		High 1 0 1	slow		2.30	2.44	
			fast		1.69	1.79	
		Medium 1 0 0	slow		3.07	3.31	
			fast		2.45	2.61	
		Low 0 1 1	slow		5.13	5.44	
			fast		4.79	5.18	
tpo	IO Output Propagation Delay (PA2), rise/fall	Max 1 1 1	slow	15pF Cload on pad, input edge rate 200ps	5.01	5.04	ns
			fast		3.06	3.10	
		High 1 0 1	slow		5.55	5.68	
			fast		3.52	3.55	
		Medium 1 0 0	slow		6.37	6.67	
			fast		4.04	4.11	
		Low 0 1 1	slow		7.39	7.60	
			fast		5.54	6.10	
tpv	Output Enable to Output Valid Delay, rise/fall	Max 1 1 1	slow	15pF Cload on pad, input edge rate 200ps, 0->1, 1->0 pad transitions	5.12	5.21	ns
			fast		3.18	3.28	
		High 1 0 1	slow		5.72	5.80	
			fast		3.67	3.71	
		Medium 1 0 0	slow		6.55	6.80	
			fast		4.06	4.09	
		Low 0 1 1	slow		7.80	8.19	
			fast		5.72	6.22	
tpi	Input Pad Propagation Delay rise/fall	without hysteresis	-	150f Cload on, input edge rate from pad =1.2ns	1.06	1.31	ns
		with hysteresis	-		1.22	1.41	

1. The drive strengths are controlled by the DSE bit of the Software MUX Pad Control Register. For details, see IOMUX Controller chapter of the device reference manual.

7.1.1 Output Buffer Impedance measurement

Table 22. Output Buffer Average Impedance (3.3V power mode)

Symbol	Parameter	Drive strength[1]	Min	Typ	Max	Unit
Rdrv	Output driver impedance	0 0 1	116	150	220	Ohm
		0 1 0	58	75	110	
		0 1 1	39	50	73	

Table continues on the next page...

1. Vid(ac) specifies the input differential voltage |Vtr-Vcp| required for switching, where Vtr is the “true” input signal and Vcp is the “complementary” input signal. The Minimum value is equal to Vih(ac)-Vil(ac).
2. The typical value of Vix(ac) is expected to be about 0.5*ovdd, and Vix(ac) is expected to track variation of ovdd. Vix(ac) indicates the voltage at which differential input signal must cross.

Table 27. DDR3 mode AC Electrical characteristics

Symbol	Parameter	Test condition	Min	Max	Unit	Notes
Vih(ac)	AC input logic high		Vref+0.175	ovdd	V	Note that the JEDEC JESD79_3E specification supersedes any specification in this document
Vil(ac)	AC input logic low		ovss	Vref-0.175	V	
Vidh(ac)[1]	AC differential input high voltage		0.35	-	V	
Vidl(ac)[1]	AC differential input low voltage		0.35		V	
Vix(ac)[2]	AC differential input crosspoint voltage	relative to ovdd/2	Vref-0.15	Vref+0.15	V	
Vpeak	Over/undershoot peak			0.4	V	
Varea	Over/undershoot area (above ovdd or below ovss)	at 800 MHz data rate		0.5	V*ns	
tsr	Single output slew rate		0.4	2	V/ns	
tskd	Skew between pad rise/fall asymmetry + skew cased by SSN			0.2	ns	

1. Vid(ac) specifies the input differential voltage |Vtr-Vcp| required for switching, where Vtr is the “true” input signal and Vcp is the “complementary” input signal. The Minimum value is equal to Vih(ac)-Vil(ac).
2. The typical value of Vix(ac) is expected to be about 0.5*ovdd, and Vix(ac) is expected to track variation of ovdd. Vix(ac) indicates the voltage at which differential input signal must cross.

8 Power supplies and sequencing

8.1 Power sequencing

Table 28. Power sequencing

Power Supply (PKG Level)	Board Level Power Nets	Parameters	Power Order	Comment
VBAT	VBAT	Battery supply in case of LDOIN fails	NA	

Table continues on the next page...

Module	Name	Recommendation if Unused
USB	USB_DCAP, USB0_VBUS, USB1_VBUS	Connect USBx_VBUS and USB_DCAP together and tie to ground through a 10K ohm resistor. Do NOT tie directly to ground, latch-up risk.
	USB0_GND, USB1_GND	Ground
	USB0_VBUS_DETECT, USB1_VBUS_DETECT	Float
	USB0_DM, USB0_DP, USB1_DM, USB1_DP	Float
Video ADC	VDDA33_AFE	3.3V or Float
	VDD12_AFE	1.2V or Float
	VADC_AFE_BANDGAP	Float
	VADCSE0, VADCSE1, VADCSE2, VADCSE3	Ground or Float

9 Peripheral operating requirements and behaviours

9.1 Analog

9.1.1 12-bit ADC electrical characteristics

9.1.1.1 12-bit ADC operating conditions

Table 31. 12-bit ADC Operating Conditions

Characteristic	Conditions	Symb	Min	Typ [1]	Max	Unit	Comment
Supply voltage	Absolute	V_{DDAD}	2.5	-	3.6	V	-
	Delta to V_{DDAD} (VDD-VDDAD) [2]	ΔVDDAD	-100	0	100	mV	-
Ground voltage	Delta to V_{SSAD} (VSS-VSSAD) [2]	ΔVSSAD	-100	0	100	mV	-
Ref Voltage High	-	V_{REFH}	1.5	V_{DDAD}	V_{DDAD}	V	-
Ref Voltage Low	-	V_{REFL}	V_{SSAD}	V_{SSAD}	V_{SSAD}	V	-
Input Voltage	-	V_{ADIN}	V_{REFL}	-	V_{REFH}	V	-
Input Capacitance	8/10/12 bit modes	C_{ADIN}	-	1.5	2	pF	-
Input Resistance	ADLPC=0, ADHSC=1	R_{ADIN}	-	5	7	kohms	-
	ADLPC=0, ADHSC=0		-	12.5	15	kohms	-
	ADLPC=1, ADHSC=0		-	25	30	kohms	-

Table continues on the next page...

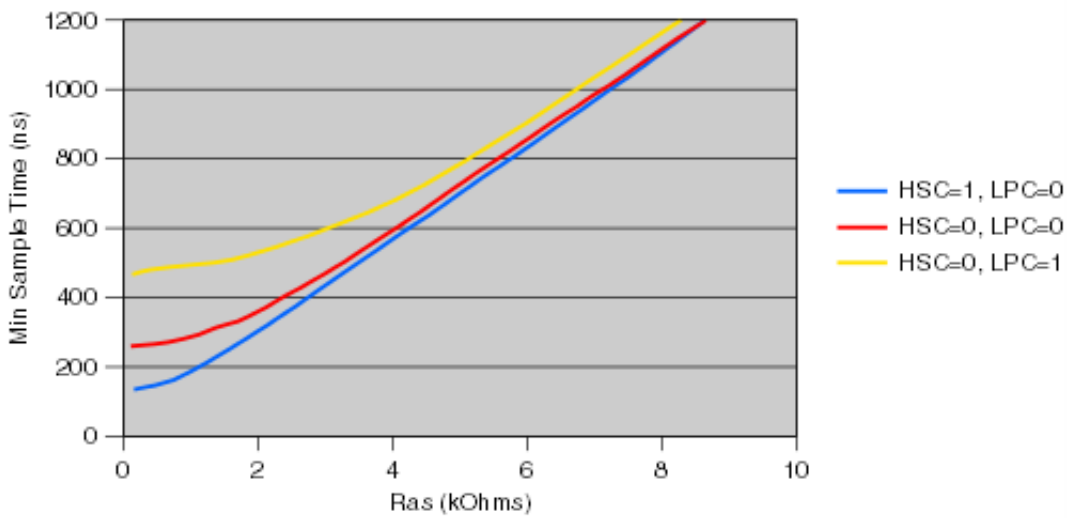


Figure 8. Minimum Sample Time Vs Ras (Cas = 10pF)

9.1.2 12-bit DAC electrical characteristics

9.1.2.1 12-bit DAC operating requirements

Table 33. 12-bit DAC operating requirements

Symbol	Desciption	Min.	Typ	Max.	Unit	Notes
VDDA33_ADC	Supply voltage	3.0	3.3	3.6	V	
VREFH_ADC	Reference voltage	2.5	3.3	VDDA33_ADC	V	1
C_L	Output load capacitance	—		100	pF	2
I_L	Output load current	—		1	mA	

1. User will need to set up DACx_STATCTRL [DACRFS]=1 to select the valid VREFH_ADC reference. When DACx_STATCTRL [DACRFS]=0, the DAC reference is connected to an internal ground node and is not a valid voltage reference. Note that the DAC and ADC share the VREFH_ADC reference simultaneously.)
2. A small load capacitance (47 pF) can improve the bandwidth performance of the DAC

9.1.2.2 12-bit DAC operating behaviors

Table 34. 12-bit DAC operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDA_DACLP}	Supply current — low-power mode	—	—	100	µA	
I_{DDA_DACHP}	Supply current — high-power mode	—	—	500	µA	
t_{DACLP}	Full-scale settling time (0x080 to 0xF7F) — low-power mode	—	10	15	µs	1

Table continues on the next page...

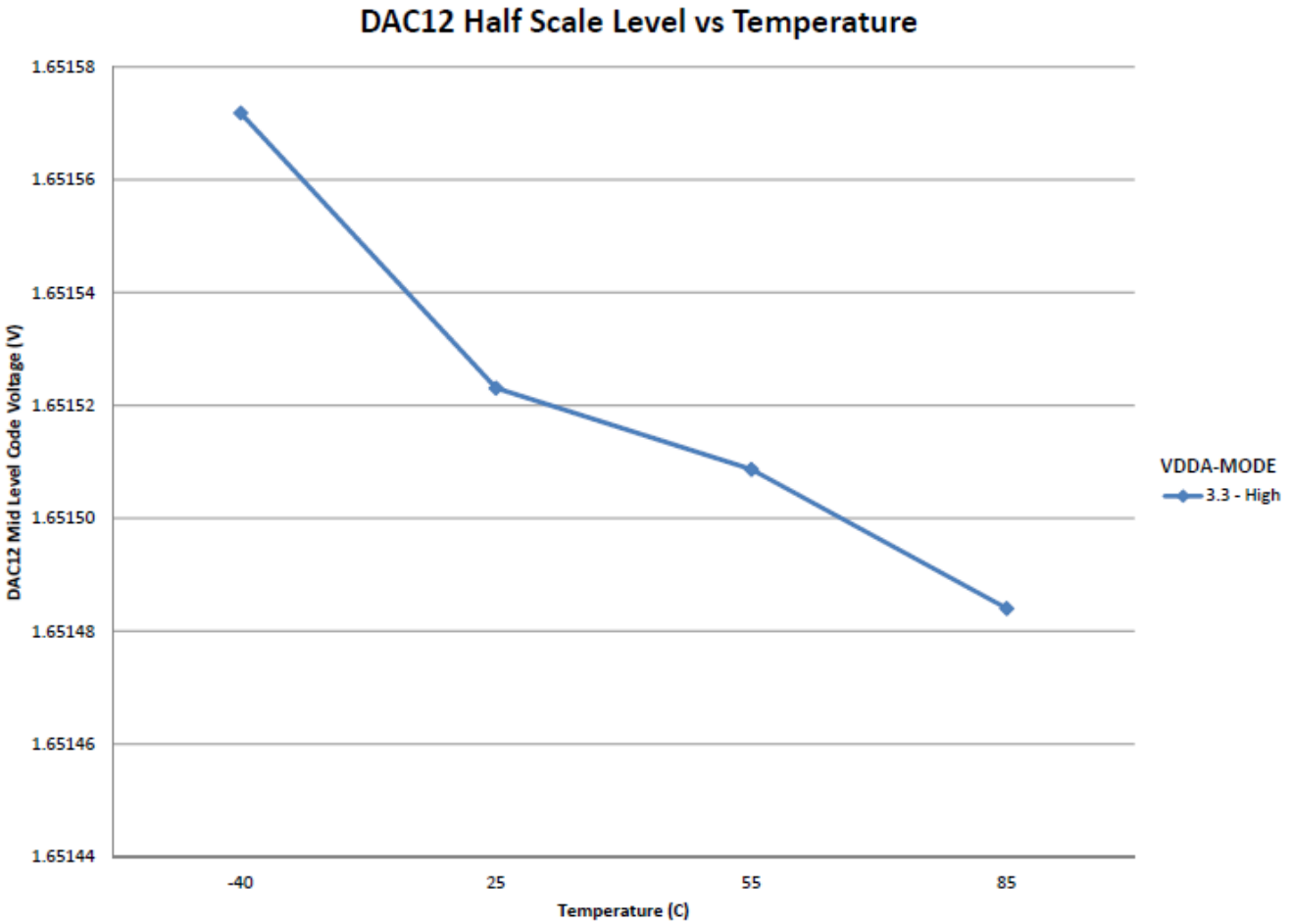


Figure 11. Offset at half scale vs. temperature

9.1.3 VideoADC Specifications

This section describes the electrical specification and characteristics of the VideoADC Analog Front End.

Table 35. VideoADC Specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
VDDA33_AFE	Supply voltage	3.0	3.3	3.6	V	—
	Supply current	—	—	41	mA	—
VDDA12_AFE	Supply voltage	1.1	1.2	1.26	V	—
	Supply current	—	—	14	mA	—
V_{in}	Input signal voltage range	0	0.5	1.4	V	—
	External AC coupling	10	47		nF	The external AC coupling capacitance cannot be too large.

Table continues on the next page...

9.2.3 LCD driver electrical characteristics

This section provides LCD driver electrical specification at V_{DD33} = 3.3 V ± 10%.

Table 39. LCD driver specifications

Symbol	Parameter	Min	Typical	Max	Unit
VLCD	Voltage on VLCD (LCD supply) pin with respect to VSS	0		VDD33 + 0.3	V
$Z_{BP/FP}$	LCD output impedance (BP[n-1:0],FP[m-1:0]) for output levels VDDE, VSS	_	_	5.0	KΩ
$I_{BP/FP}$	LCD output current (BP[n-1:0],FP[m-1:0]) for outputs charge/discharge voltage levels VDDE2/3, VDDE1/2, VDDE/3)[1]	_	25	_	µA

1. With PWR=10, BSTEN=0, and BSTAO=0

9.3 Ethernet specifications

9.3.1 Ethernet Switching Specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface. All Ethernet signals use pad type pad_fsr. The timing specifications described i the section assume a pad slew rate setting of 11 and a load of 50 pF[2].

9.3.2 Receive and Transmit signal timing specifications

This section provides timing specs that meet the requirements for RMII interfaces for a range of transceiver devices.

Table 40. Receive signal timing for RMII interfaces

	Characteristic	RMII Mode		Unit
		Min	Max	
—	EXTAL frequency (RMII input clock RMII_CLK)	—	50	MHz
E3, E7	RMII_CLK pulse width high	35%	65%	RMII_CLK period

Table continues on the next page...

2. These timing parameters are specified assuming maximum operating frequency and the fastest pad slew rate setting (11). When operating this interface at lower frequencies, increase the slew rate by using the 10, 01, or 00 setting to increase edge rise and fall times, thus reducing EMI.

Table 40. Receive signal timing for RMII interfaces (continued)

	Characteristic	RMII Mode		Unit
		Min	Max	
E4, E8	RMII_CLK pulse width low	35%	65%	RMII_CLK period
E1	RXD[1:0], CVS_DV, RXER to RMII_CLK setup	4	—	ns
E2	RMII_CLK to RXD[1:0], CRS_DV, RXER hold	2	—	ns
E6	RMII_CLK to TXD[1:0], TXEN valid	—	14	ns
E5	RMII_CLK to TXD[1:0], TXEN invalid	4	—	ns

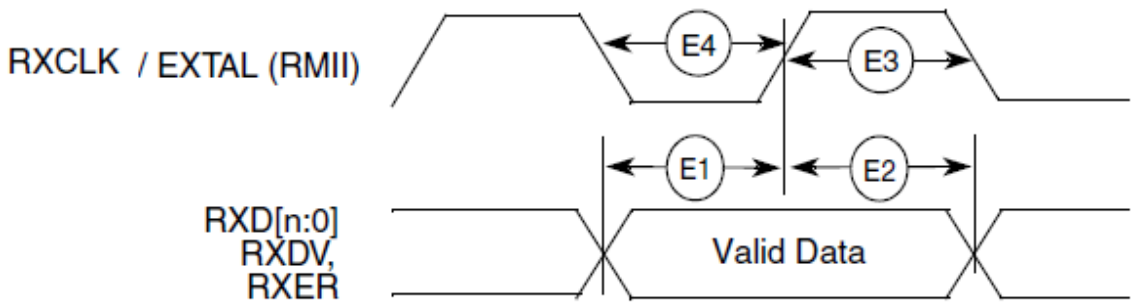


Figure 19. RMII receive signal timing diagram

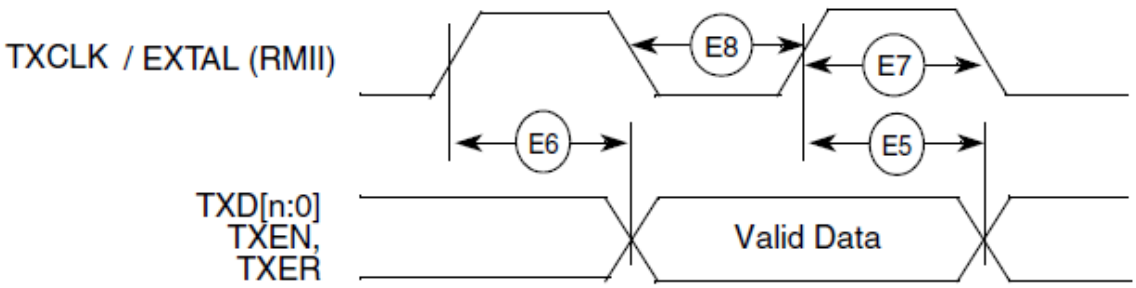


Figure 20. RMII transmit signal timing diagram

NOTE

See the most current device errata document when using the internally generated RXCLK and TXCLK clocks.

Table 61. I2C input timing specifications — SCL and SDA[1] (continued)

No.	Parameter	Min.	Max.	Unit
3	Bus free time between Start and Stop condition	4.7	—	µs
4	Data hold time	0.0	—	µs
5	Clock high time	4	—	PER_CLK Cycle
6	Data setup time	0.0	—	ns
7	Start condition setup time (for repeated start condition only)	2	—	PER_CLK Cycle
8	Stop condition setup time	2	—	PER_CLKCycle

1. I2C input timing is valid for Automotive and TTL inputs levels, hysteresis enabled, and an input edge rate no slower than 1 ns (10% – 90%).
2. PER_CLK is the IPG Clock which drive the I2C BIU and module clock inputs. Typically this is 83Mhz. See the Clocking Overview chapter in the device reference manual for more details.

Table 62. I2C output timing specifications — SCL and SDA[1234]

No.	Parameter	Min	Max	Unit
1	Start condition hold time	6	—	PER_CLK Cycle[5]
2	Clock low time	10	—	PER_CLK Cycle
3	Bus free time between Start and Stop condition	4.7	—	µs
4	Data hold time	7	—	PER_CLK Cycle
5	Clock high time	10	—	PER_CLK Cycle
6	Data setup time	2	—	PER_CLK Cycle
7	Start condition setup time (for repeated start condition only)	20	—	PER_CLK Cycle
8	Stop condition setup time	10	—	PER_CLK Cycle

1. All output timing is worst case and includes the mismatching of rise and fall times of the output pads.
2. Output parameters are valid for CL = 25 pF, where CL is the external load to the device (lumped). The internal package capacitance is accounted for, and does not need to be subtracted from the 25 pF value.
3. Timing is guaranteed to same drive capabilities for all signals, mixing of pad drives may reduce operating speedsand may cause incorrect operation.
4. Programming the IBFD register (I2C bus Frequency Divider) with the maximum frequency results in the minimum output timings listed. The I2C interface is designed to scale the data transition time, moving it to the middle of the SCL low period. The actual position is affected by the pre-scale and division values programmed in the IBC field of the IBFD register.
5. PER_CLK is the IPG Clock which drive the I2C BIU and module clock inputs. Typically this is 83Mhz. See the Clocking Overview chapter in the device reference manual for more details.

9.7.6 PLL3 and PLL7 (480 MHz USB PLL) Electrical Parameters

Table 69. PLL3 and PLL7 Electrical Parameters

Parameter	Value
Clock output range	480 MHz PLL output
Reference clock	24 MHz
Lock time	<425 reference cycles
Period jitter(p2p)	<140 ps
Duty Cycle	48.9%~51.7% PLL output

9.7.7 PLL5 (Ethernet PLL) Electrical Parameters

Table 70. PLL5 Electrical Parameters

Parameter	Value
Clock output range	500 MHz
Reference clock	24 MHz
Lock time	<7500 reference cycles
Cycle to cycle jitter (p2p)[1]	<400ps @ 50 MHz
Duty Cycle	45%~55%

1. Jitter numbers are measured at divided PLL clock because high frequency cannot be brought-out IO pad.

9.7.8 PLL4 (Audio PLL) Electrical Parameters

Table 71. PLL4 Electrical Parameters

Parameter	Value
Clock output range	650 MHz ~1.3 GHz
Reference clock	24 MHz
Lock time	<7500 reference cycles
Long term jitter(RMS)	<42ps @1128MHz
Period jitter(p2p)[1]	<115ps@1128MHz
Duty Cycle	43%~57%

1. Jitter numbers are measured at divided PLL clock because high frequency cannot be brought-out on IO pad.

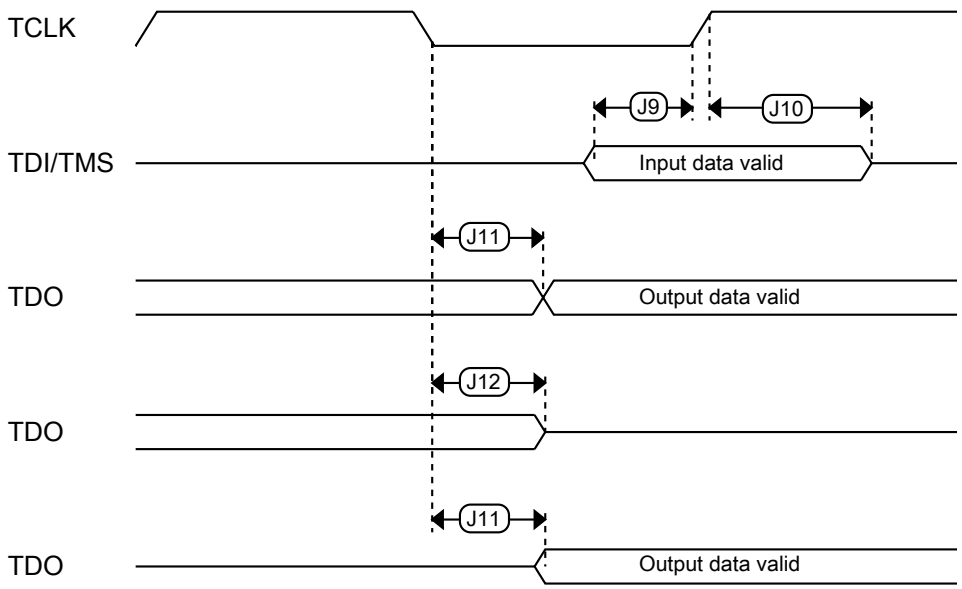


Figure 55. Test Access Port timing

9.8.2 Debug trace timing specifications

Table 74. Debug trace operating behaviors

Symbol	Description	Min.	Max.	Unit
T_{cyc}	Clock period	50		MHz
T_{wl}	Low pulse width	2	—	ns
T_{wh}	High pulse width	2	—	ns
T_r	Clock and data rise time	Refer Table 21		ns
T_f	Clock and data fall time Refer			ns
tDV	Data output valid	3	—	ns
tHO	Data output hold	1	—	ns

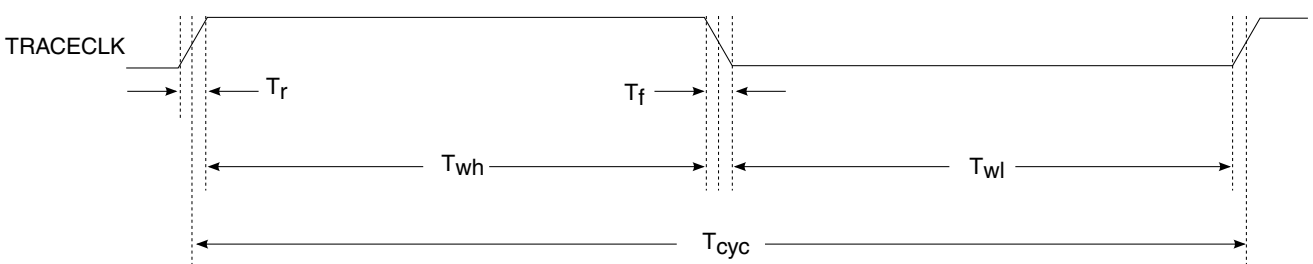


Figure 56. TRACE_CLKOUT specifications

364 MAP BGA	176 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
Y11	64	USB0_ VBUS_ DETECT			USB0_ VBUS_ DETECT							
Y9	—	USB1_GND			USB1_GND							
W9	—	USB1_DP			USB1_DP							
V9	—	USB1_DM			USB1_DM							
W10	—	USB1_VBUS			USB1_VBUS							
U9	—	USB1_ VBUS_ DETECT			USB1_ VBUS_ DETECT							
L4	8	PTC0		PTC0	RMII0_MDC/ MII0_MDC	FTM1CH0	SPI0_PCS3	ESAI_SCKT	SDHC0_CLK	VIU_DATA0	RCON18	
L5	9	PTC1		PTC1	RMII0_MDIO/ MII0_MDC	FTM1CH1	SPI0_PCS2	ESAI_FST	SDHC0_CMD	VIU_DATA1	RCON19	
M5	11	PTC2		PTC2	RMII0_CRS_ DV	SCI1_TX		ESAI_SDO0	SDHC0_ DAT0	VIU_DATA2	RCON20	
M3	12	PTC3		PTC3	RMII0_RXD1/ MII0_RXD[1]	SCI1_RX		ESAI_SDO1	SDHC0_ DAT1	VIU_DATA3	DCU0_R0	
L2	14	PTC4		PTC4	RMII0_RXD0/ MII0_RXD[0]	SCI1_RTS	SPI1_PCS1	ESAI_SDO2/ ESAI_SDI3	SDHC0_ DAT2	VIU_DATA4	DCU0_R1	
M1	15	PTC5		PTC5	RMII0_RXER/ MII0_RXER	SCI1_CTS	SPI1_PCS0	ESAI_SDO3/ ESAI_SDI2	SDHC0_ DAT3	VIU_DATA5	DCU0_G0	
N1	16	PTC6		PTC6	RMII0_TXD1/ MII0_TXD[1]		SPI1_SIN	ESAI_SDO5/ ESAI_SDI0	SDHC0_WP	VIU_DATA6	DCU0_G1	
N2	17	PTC7		PTC7	RMII0_TXD0/ MII0_TXD[0]		SPI1_SOUT	ESAI_SDO4/ ESAI_SDI1		VIU_DATA7	DCU0_B0	
N4	18	PTC8		PTC8	RMII0_TXEN/ MII0_TXEN		SPI1_SCK			VIU_DATA8	DCU0_B1	
T15	77	PTC9		PTC9	RMII1_MDC		ESAI_SCKT			MLBCLK		
U15	78	PTC10		PTC10	RMII1_MDIO		ESAI_FST			MLBSIGNAL		
P4	20	PTC11		PTC11	RMII1_CRS_ DV		ESAI_SDO0			MLBDATA		
P3	21	PTC12		PTC12	RMII1_RXD1		ESAI_SDO1		SAI2_TX_ BCLK			
P1	23	PTC13		PTC13	RMII1_RXD0		ESAI_SDO2/ ESAI_SDI3		SAI2_RX_ BCLK			
R1	26	PTC14		PTC14	RMII1_RXER		ESAI_SDO3/ ESAI_SDI2	SCI5_TX	SAI2_RX_ DATA	ADC0_SE6		
P2	27	PTC15		PTC15	RMII1_TXD1		ESAI_SDI0	SCI5_RX	SAI2_TX_ DATA	ADC0_SE7		
R3	29	PTC16		PTC16	RMII1_TXD0		ESAI_SDO4/ ESAI_SDI1	SCI5_RTS	SAI2_RX_ SYNC	ADC1_SE6		
R4	28	PTC17		PTC17	RMII1_TXEN		ADC1_SE7	SCI5_CTS	SAI2_TX_ SYNC	USB1_SOF_ PULSE		
B10	—	DDR_A[15]			DDR_A15							
D9	—	DDR_A[14]			DDR_A14							

Table 78. Functional Assignment Pins (continued)

Signal Name	364 MAP BGA	176 LQFP (F-series ONLY)	Power Group	Pad Type	Default Mode (Reset)	Default Function	Input/ Output	Value
PTA31	P16	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB0	T6	49	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB1	T7	50	VDD33	GPIO	ALT3	RCON30	Input	Disabled
PTB2	V7	51	VDD33	GPIO	ALT3	RCON31	Input	Disabled
PTB3	W7	53	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB4	Y7	54	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB5	Y8	55	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB6	W8	56	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB7	D13	166	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB8	J16	121	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB9	J19	123	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB10	B15	159	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB11	D14	164	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB12	E13	165	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB13	D15	156	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB14	B14	162	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB15	A14	161	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB16	C14	163	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB17	A15	160	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB18	B12	171	VDD33	GPIO	ALT0	GPIO	Input	Disabled
PTB19	C13	167	VDD33	GPIO	ALT0	GPIO	Input	Disabled
PTB20	A13	169	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB21	E12	173	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB22	D12	172	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB23	A19	141	VDD33	GPIO	ALT3	GPIO	Disabled	
PTB24	A18	142	VDD33	GPIO	ALT3	GPIO	Disabled	
PTB25	B17	149	VDD33	GPIO	ALT3	GPIO	Disabled	
PTB26	A17	150	VDD33	GPIO	ALT3	RCON21	Input	Disabled
PTB27	U8	57	VDD33	GPIO	ALT3	RCON22	Input	Disabled
PTB28	A16	151	VDD33	GPIO	ALT3	RCON23	Input	Disabled
PTC0	L4	8	VDD33	GPIO	ALT7	RCON18	Input	Disabled
PTC1	L5	9	VDD33	GPIO	ALT7	RCON19	Input	Disabled
PTC2	M5	11	VDD33	GPIO	ALT7	RCON20	Input	Disabled
PTC3	M3	12	VDD33	GPIO	ALT0	GPIO	Disabled	
PTC4	L2	14	VDD33	GPIO	ALT0	GPIO	Disabled	
PTC5	M1	15	VDD33	GPIO	ALT0	GPIO	Disabled	
PTC6	N1	16	VDD33	GPIO	ALT0	GPIO	Disabled	

Table continues on the next page...