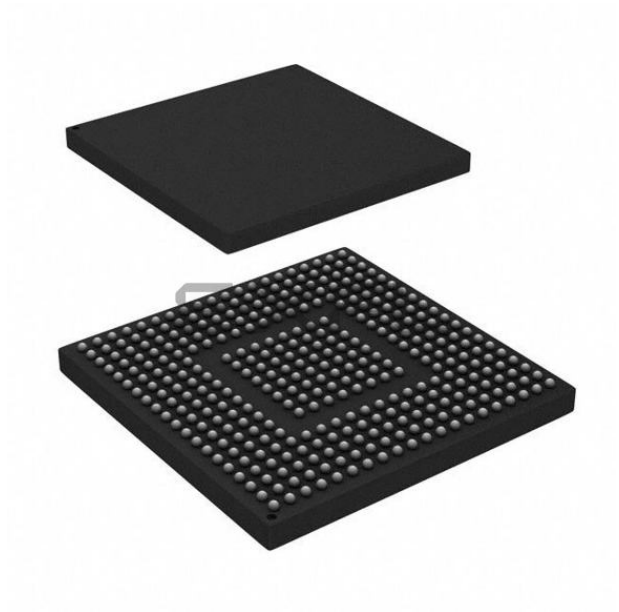

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What is "Embedded - Microcontrollers"?

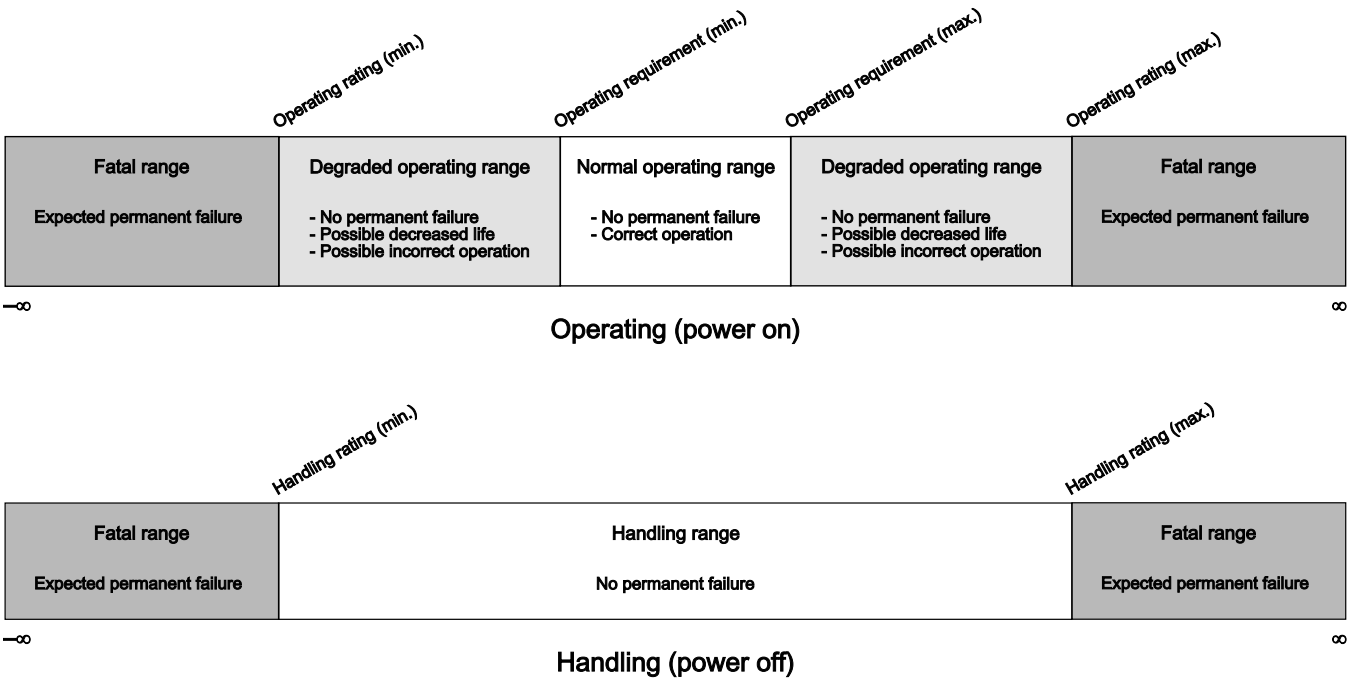
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-A5/M4
Core Size	32-Bit Dual-Core
Speed	500MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, SCI, SD, SPI, UART/USART, USB OTG
Peripherals	DMA, LVD, WDT
Number of I/O	-
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	1.5MB
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 12bit SAR; D/A 12bit
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	364-LFBGA
Supplier Device Package	364-LFBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/pvf61ns151cmk50

- Display and Video
  - Dual Display Control Unit (DCU) with support for color TFT display up to SVGA
  - Segmented LCD (3V Glass only) configurable as 40x4, 38x8, and 36x6
  - Video Interface Unit (VIU) for camera
  - Open VG Graphics Processing Unit (GPU)
  - VideoADC
- Analog
  - Dual 12-bit SAR ADC with 1MS/s
  - Dual 12-bit DAC
- Audio
  - Four Synchronous Audio Interface (SAI)
  - Enhanced Serial Audio Interface (ESAI)
  - Sony Philips Digital Interface (SPDIF), Rx and Tx
  - Asynchronous Sample Rate Converter (ASRC)
- Human-Machine Interface (HMI)
  - GPIO pins with interrupt support, DMA request capability, digital glitch filter.
  - Hysteresis and configurable pull up/down device on all input pins
  - Configurable slew rate and drive strength on all output pins
- On-Chip Memory
  - 512 KB On-chip SRAM with ECC
  - 1 MB On-chip graphics SRAM (no ECC). This depends on the part selected. Alternate configuration could be 512 KB graphics and 512 KB L2 cache.
  - 96 KB Boot ROM

3.6 Relationship between ratings and operating requirements



3.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

3.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:

- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.

6.2.2 LVD electrical specifications

6.2.2.1 Main Supply electrical characteristics

Table 9. LVD_MAIN supply electrical characteristics

Main Supply LVD Parameters	Min	Typ	Max	Unit	Comments
Power supply	3.0	3.3	3.6	V	
Upper voltage threshold (value @27°C)		2.76	2.915	V	
Lower voltage threshold (value @27°C)	2.656	2.73		V	
Time constant of RC filter at LVD input (0.69*RC)	3.3			µs	3.3 V noise rejection at LVD comparator input

6.2.2.2 LVD DIG characteristics

Table 10. LVD DIG electrical specifications [HPREG(RUN MODE) and LPREG(STOP MODE)]

LVD DIG Parameters	Min	Typ	Max	Unit	Comments
Power supply	3.0	3.3	3.6	V	
Upper voltage threshold	1.135	1.16	1.185	V	
Lower voltage threshold	1.105	1.13	1.155	V	
Time constant of RC filter at LVD input	200			ns	1.2V noise rejection at the input of LVD comparator

Table 11. LVD DIG electrical specifications [ULPREG(STANDBY MODE)]

LVD DIG Parameters	Min	Typ	Max	Unit	Comments
Power supply	3.0	3.3	3.6	V	
Upper voltage threshold	1.105	1.13	1.155	V	
Lower voltage threshold	1.075	1.10	1.125	V	
Time constant of RC filter at LVD input	200			ns	1.2V noise rejection at the input of LVD comparator

Table 31. 12-bit ADC Operating Conditions (continued)

Characteristic	Conditions	Symb	Min	Typ [1]	Max	Unit	Comment
Analog Source Resistance	12 bit mode f_{ADCK} = 40MHz ADLSMP=0, ADSTS=10, ADHSC=1	R_{AS}	-	-	1	kohms	T_{samp}=150 ns
R_{AS} depends on Sample Time Setting (ADLSMP, ADSTS) and ADC Power Mode (ADHSC, ADLPC). See charts for Minimum Sample Time vs R_{AS}							
ADC Conversion Clock Frequency	ADLPC=0, ADHSC=1 12 bit mode	f_{ADCK}	4	-	40	MHz	-
	ADLPC=0, ADHSC=0 12 bit mode		4	-	30	MHz	-
	ADLPC=1, ADHSC=0 12 bit mode		4	-	20	MHz	-

1. Typical values assume VDDAD = 3.3 V, Temp = 25°C, f_{ADCK}=20 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
2. DC potential difference

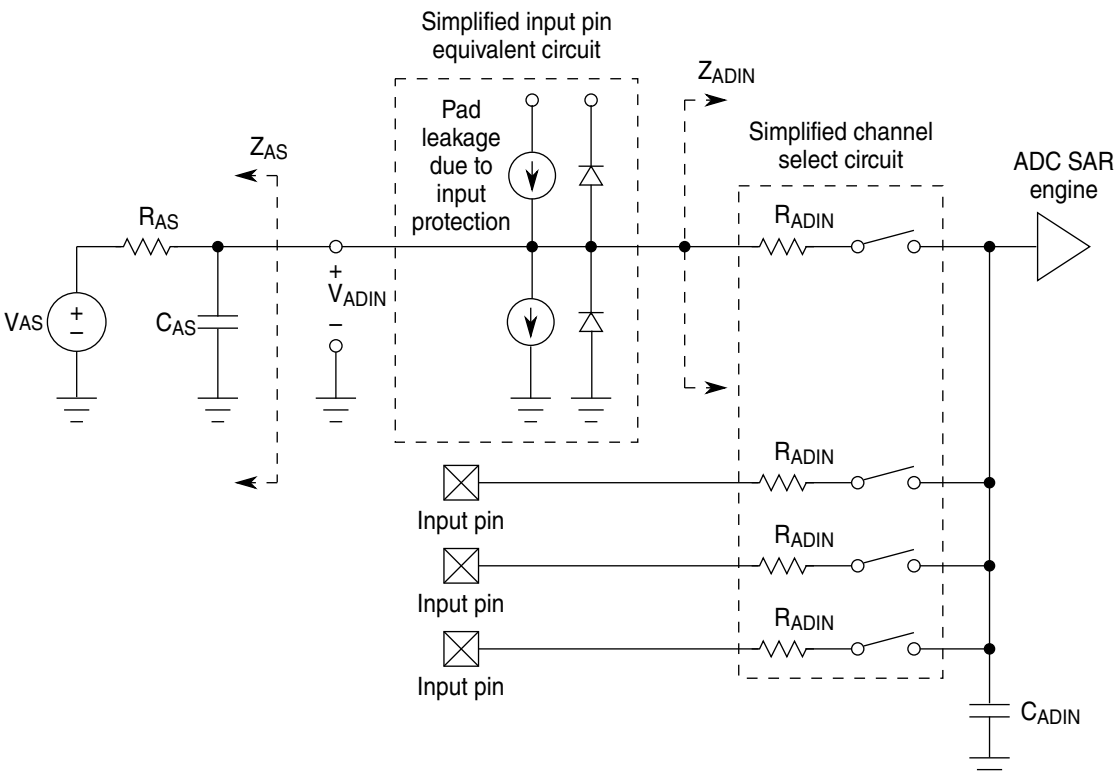


Figure 5. 12-bit ADC Input Impedance Equivalency Diagram

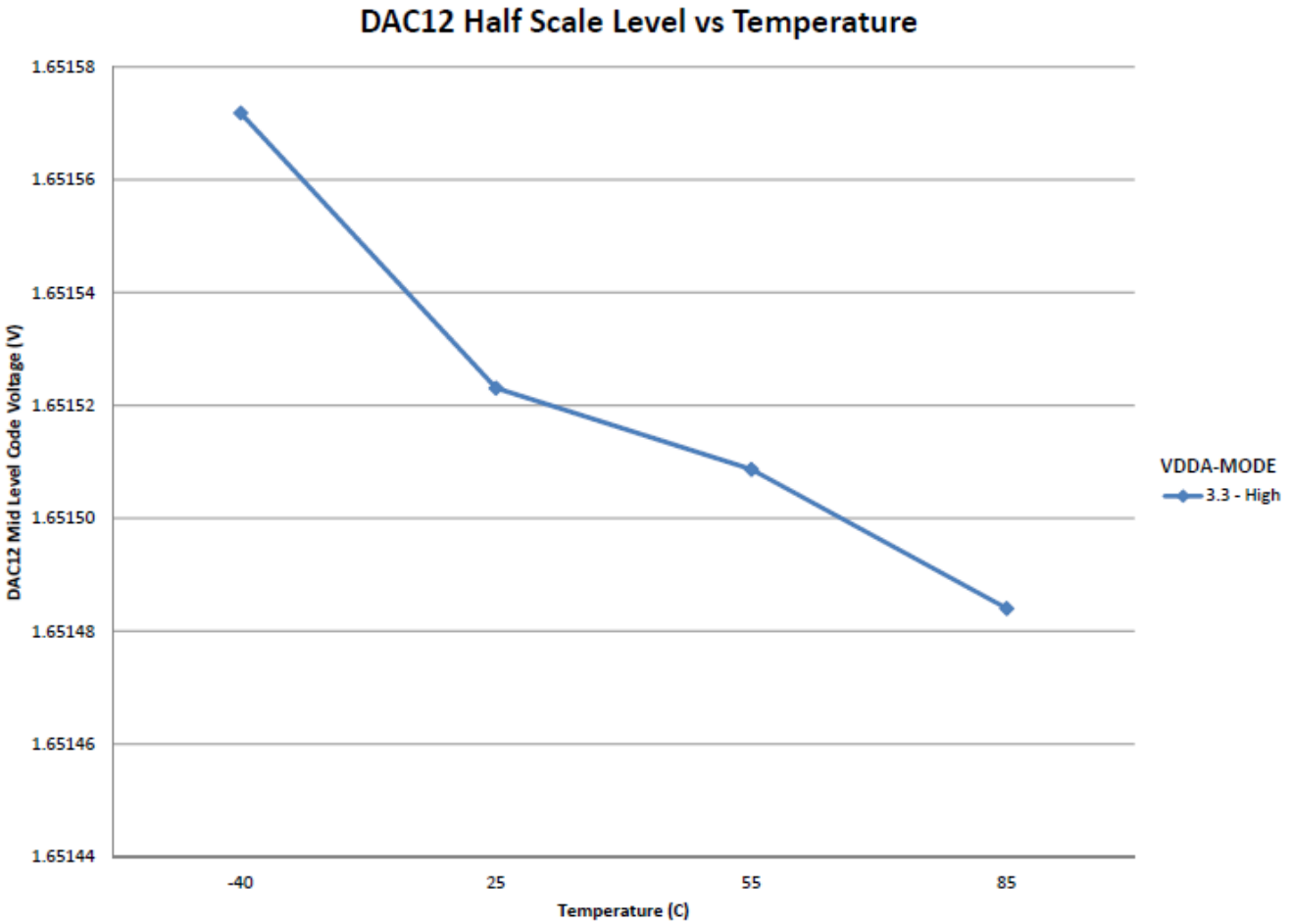


Figure 11. Offset at half scale vs. temperature

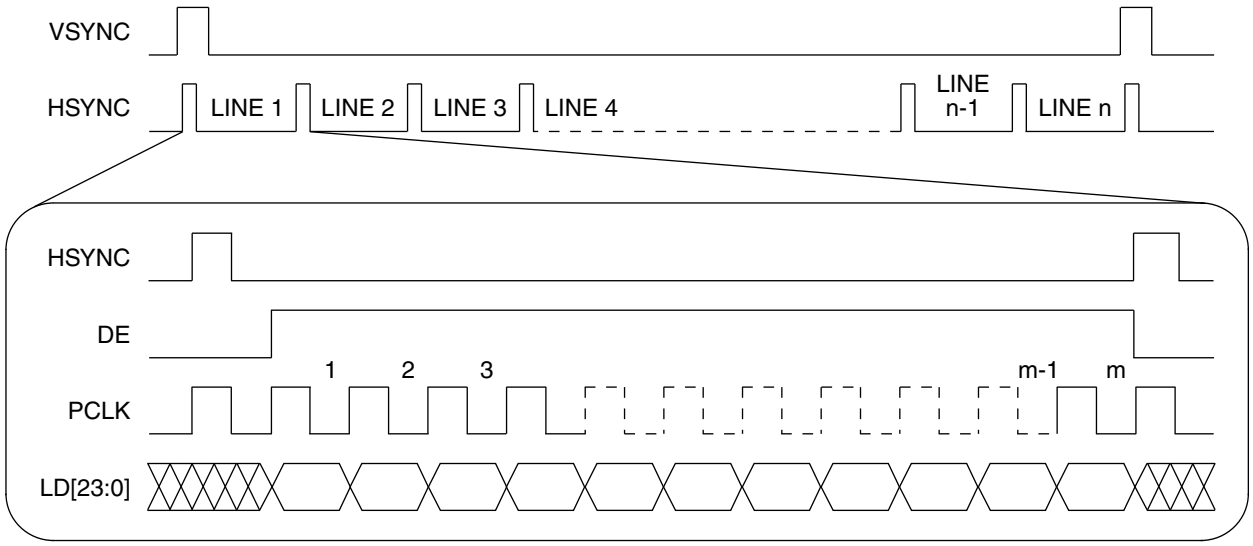
9.1.3 VideoADC Specifications

This section describes the electrical specification and characteristics of the VideoADC Analog Front End.

Table 35. VideoADC Specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
VDDA33_AFE	Supply voltage	3.0	3.3	3.6	V	—
	Supply current	—	—	41	mA	—
VDDA12_AFE	Supply voltage	1.1	1.2	1.26	V	—
	Supply current	—	—	14	mA	—
V_{in}	Input signal voltage range	0	0.5	1.4	V	—
	External AC coupling	10	47		nF	The external AC coupling capacitance cannot be too large.

Table continues on the next page...



9.2.1.2 Interface to TFT LCD Panels—Pixel Level Timings

This section provides the horizontal timing (timing of one line), including both the horizontal sync pulse and data. All parameters shown in the figure below are programmable. This timing diagram corresponds to positive polarity of the PCLK signal (meaning the data and sync signals change on the rising edge) and active-high polarity of the HSYNC, VSYNC and DE signals. The user can select the polarity of the HSYNC and VSYNC signals via the SYN_POL register, whether active-high or active-low. The default is active-high. The DE signal is always active-high. Pixel clock inversion and a flexible programmable pixel clock delay are also supported. They are programmed via the clock divide . The DELTA_X and DELTA_Y parameters are programmed via the DISP_SIZE register. The PW_H, BP_H and FP_H parameters are programmed via the HSYN PARA register. The PW_V, BP_V and FP_V parameters are programmed via the VSYN_PARA register.

Table 36. LCD interface timing parameters—horizontal and vertical

Symbol	Characteristic		Unit
t_{PCP}	Display pixel clock period	11.2	ns
t_{PWH}	HSYNC pulse width	PW_H * t_{PCP}	ns
t_{BPH}	HSYNC back porch width	BP_H * t_{PCP}	ns
t_{FPH}	HSYNC front porch width	FP_H * t_{PCP}	ns
t_{SW}	Screen width	DELTA_X * t_{PCP}	ns
t_{HSP}	HSYNC (line) period	(PW_H + BP_H + FP_H + DELTA_X) * t_{PCP}	ns
t_{PWV}	VSYNC pulse width	PWV * t_{HSP}	ns
t_{BPV}	VSYNC back porch width	BP_V * t_{HSP}	ns
t_{FPV}	VSYNC front porch width	FP_V * t_{HSP}	ns
t_{SH}	Screen height	DELTA_Y * t_{HSP}	ns
t_{VSP}	VSYNC (frame) period	(PW_V + BP_V + FP_V + DELTA_Y) * t_{HSP}	ns

9.2.3 LCD driver electrical characteristics

This section provides LCD driver electrical specification at V_{DD33} = 3.3 V ± 10%.

Table 39. LCD driver specifications

Symbol	Parameter	Min	Typical	Max	Unit
VLCD	Voltage on VLCD (LCD supply) pin with respect to VSS	0		VDD33 + 0.3	V
$Z_{BP/FP}$	LCD output impedance (BP[n-1:0],FP[m-1:0]) for output levels VDDE, VSS	_	_	5.0	KΩ
$I_{BP/FP}$	LCD output current (BP[n-1:0],FP[m-1:0]) for outputs charge/discharge voltage levels VDDE2/3, VDDE1/2, VDDE/3)[1]	_	25	_	µA

1. With PWR=10, BSTEN=0, and BSTAO=0

9.3 Ethernet specifications

9.3.1 Ethernet Switching Specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface. All Ethernet signals use pad type pad_fsr. The timing specifications described i the section assume a pad slew rate setting of 11 and a load of 50 pF[2].

9.3.2 Receive and Transmit signal timing specifications

This section provides timing specs that meet the requirements for RMII interfaces for a range of transceiver devices.

Table 40. Receive signal timing for RMII interfaces

	Characteristic	RMII Mode		Unit
		Min	Max	
—	EXTAL frequency (RMII input clock RMII_CLK)	—	50	MHz
E3, E7	RMII_CLK pulse width high	35%	65%	RMII_CLK period

Table continues on the next page...

2. These timing parameters are specified assuming maximum operating frequency and the fastest pad slew rate setting (11). When operating this interface at lower frequencies, increase the slew rate by using the 10, 01, or 00 setting to increase edge rise and fall times, thus reducing EMI.

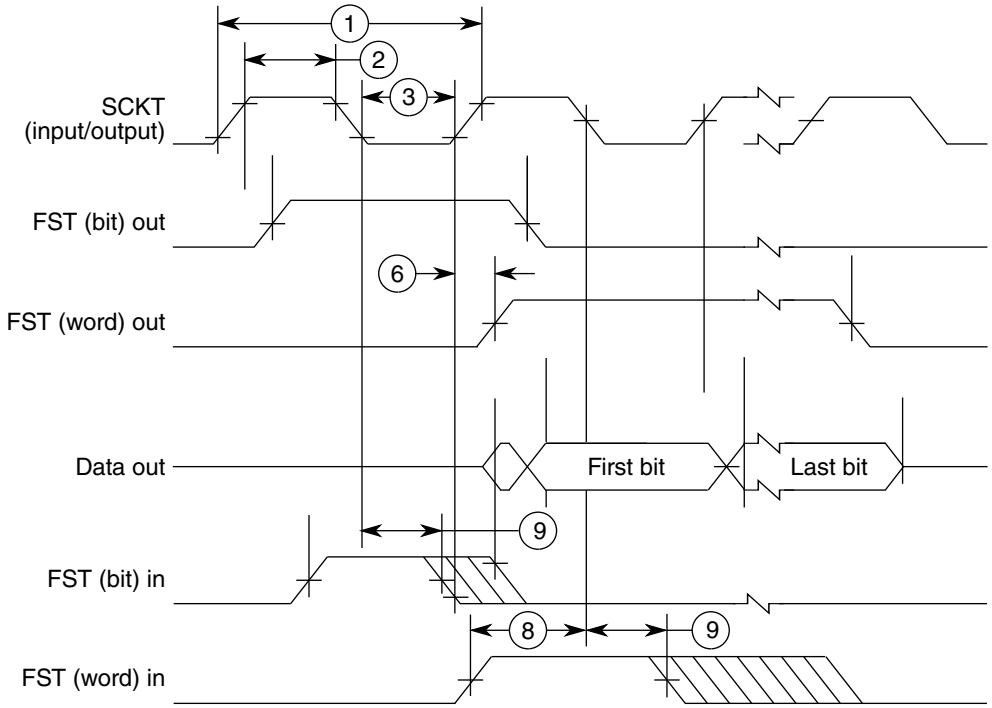


Figure 24. ESAI Transmitter Timing

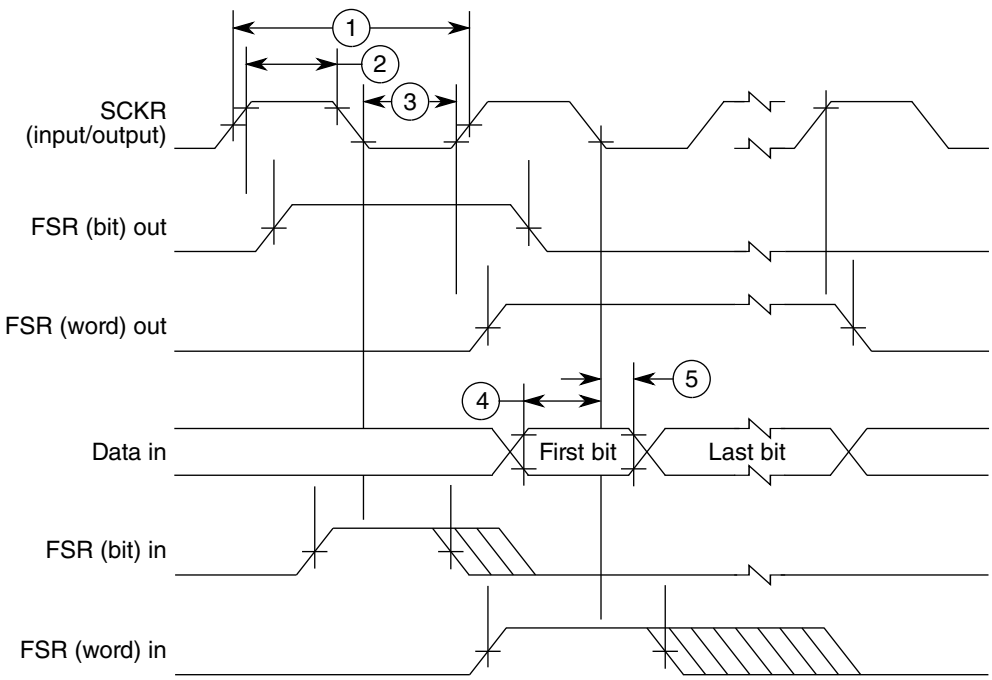


Figure 25. ESAI Receiver Timing

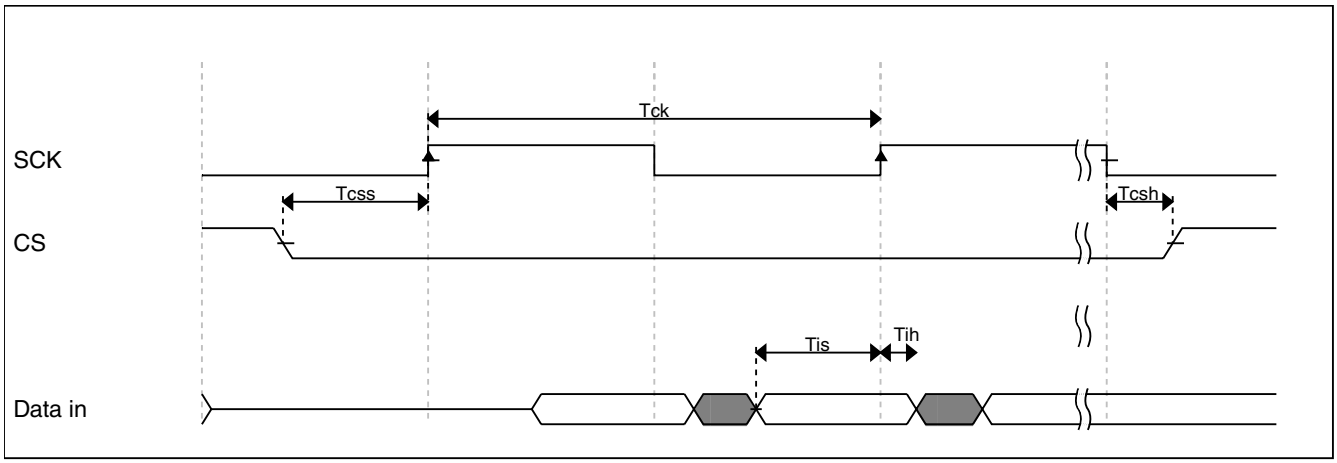


Figure 32. QuadSPI Input/Read timing (DDR mode)

NOTE

- The numbers are for a setting of 0x1 in regiater QuadSPI_SMPR[DDRSMP]
- Read frequency calculations should be: SCK/2 > (flash access time) + Setup (Tis) - (QuadSPI_SMPR[DDRSMP])x SCK/4
- Frequency calculator guideline (Max read frequency): SCK/2 > (Flash access time)max + (Tis)max - (QuadSPI_SMPR[DDRSMP]) xSCK/4
- Hold timing: flash_access (min) + flash_data_valid (min) > SCK/2 + HOLD(Tih) + (QuadSPI_SMPR[DDRSMP])SCK/4
- A negative time indicates the actual capture edge inside the device is earlier than clock appearing at pad.

Table 50. QuadSPI Input/Read timing (DDR mode)

Symbol	Parameter	Value		Unit
		Min	Max	
T_{is}	Setup time for incoming data	6.4	—	ns
T_{ih}	Hold time requirement for incoming data	-3.0	—	ns

NOTE

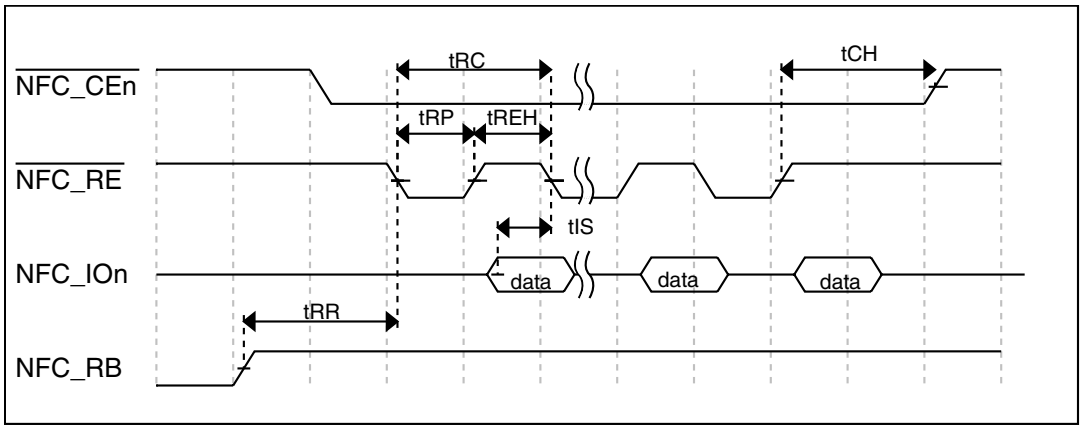


Figure 38. Read data latch cycle timing in fast mode

9.5.3 FlexBus timing specifications

This section provides FlexBus timing parameters. All processor bus timings are synchronous; input setup/hold and output delay are given in respect to the rising edge of a reference clock, FB_CLK. The FB_CLK frequency may be the same as the internal system bus frequency.

The following timing numbers indicate when data is latched or driven onto the external bus, relative to the FlexBus output clock (FB_CLK). All other timing relationships can be derived from these values.

All FlexBus signals use pad type pad_fsr. The following timing specifications assume a pad slew rate setting of 11 and a load of 50 pF[3]

Table 53. FlexBus timing specifications

Num	Characteristic	Min	Max	Unit
	Frequency of operation	—	83[1] (with Wait state)	MHz
			57[2] without Wait state , -1	
FB1	Clock Period	12	—	ns
FB4	Input setup	10.6	—	ns
FB5	Input hold	0	—	ns
FB2	Output valid	—	6.4	ns
FB3	Output hold	0	—	ns

1. Freq = 1000/(11+ access time of external memory+ trace delay for clk and data)
2. Freq = 1000/(17+access time of external memory)

3. These timing parameters are specified assuming maximum operating frequency and the fastest pad slew rate setting (11).

9.5.4 DDR controller specifications

9.5.4.1 DDR3 Timing Parameters

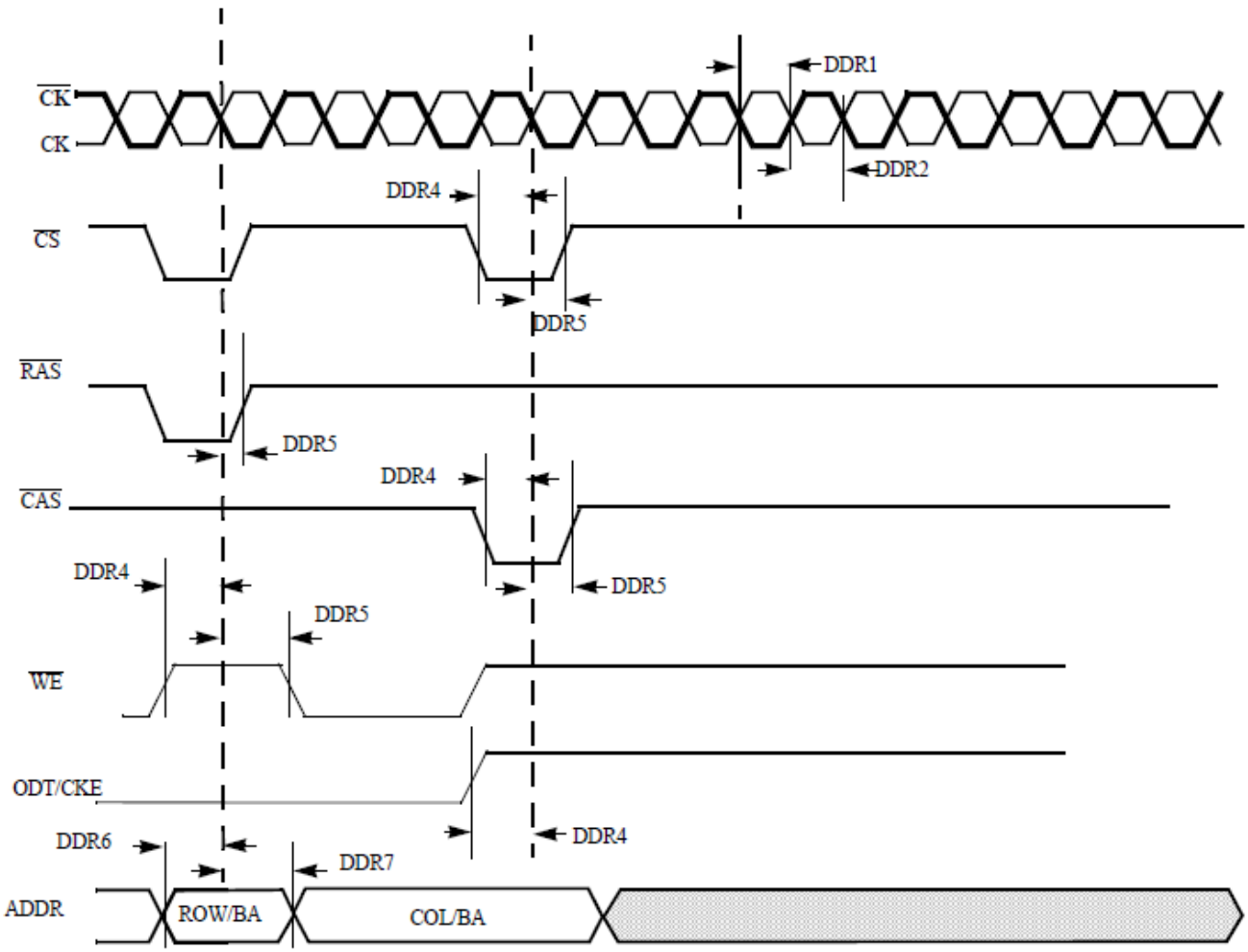


Figure 41. DDR3 Command and Address Timing Parameters

NOTE

RESET pin has a external weak pull DOWN requirement if DDR3 memory is NOT required to support content retention in the device low power modes where core voltage is off but DRAM voltage is on.

9.5.4.2 DDR3 Read Cycle

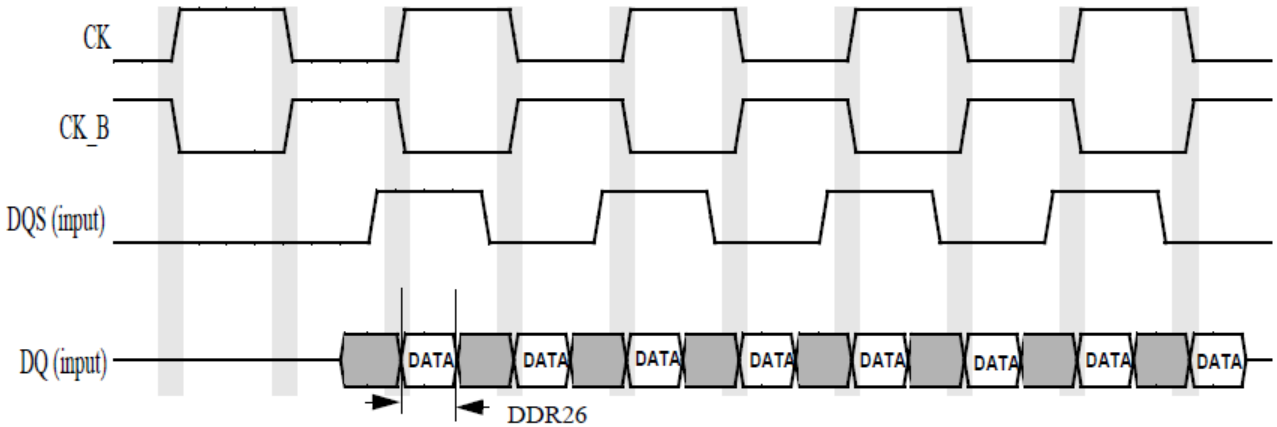


Figure 42. DDR3 Read Cycle

Table 55. DDR3 Read Cycle

ID	Parameter	Symbol	CK = 400 MHz		Unit
			Min	Max	
DDR26	Minimum required DQ valid window width	-	750	-	ps

NOTE

To receive the reported setup and hold values, read calibration should be performed in order to locate the DQS in the middle of DQ window.

NOTE

All measurements are in reference to Vref level.

NOTE

Measurements were done using balanced load and 25 ohms resistor from outputs to VDD_REF

9.7.9 PLL6 (Video PLL) Electrical Parameters

Table 72. PLL6 Electrical Parameters

Parameter	Value
Clock output range	650 MHz ~1.3 GHz
Reference clock	24 MHz
Lock time	<7500 reference cycles
Long term jitter(RMS)[1]	<42ps @ 1128 MHz
Period jitter(p2p)	<130ps @960MHz
Duty Cycle	43%~57%

1. Jitter numbers are measured at divided PLL clock because high frequency cannot be brought-out on IO pad & at use case frequency.

9.8 Debug specifications

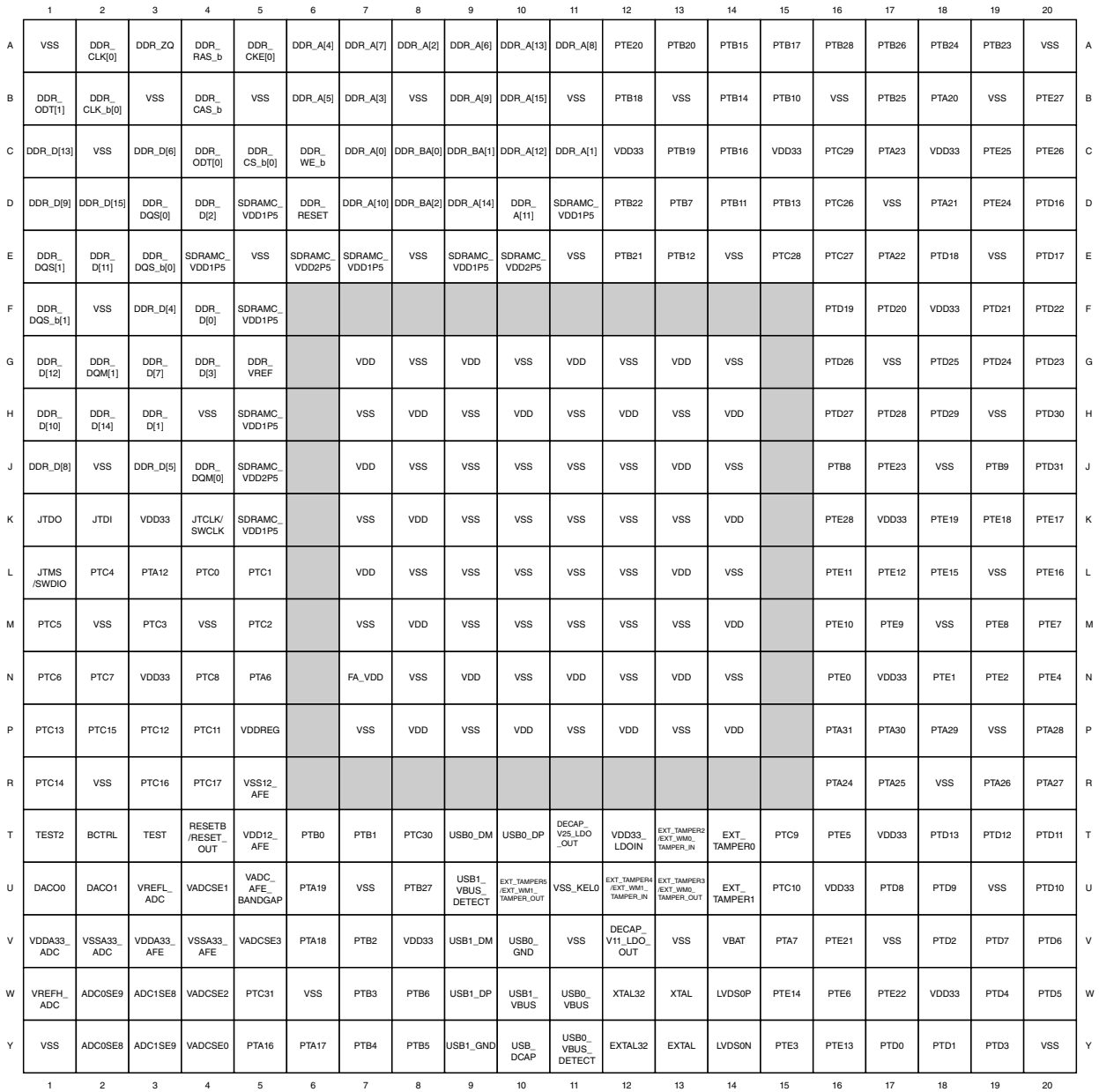
9.8.1 JTAG electricals

Table 73. JTAG limited voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
J1	TCLK frequency of operation			MHz
	• Boundary Scan	-	25	
	• JTAG and CJTAG	-	25	
	• Serial Wire Debug	-	25	
J2	TCLK cycle period	1/J1	—	ns
J3	TCLK clock pulse width			
	• Boundary Scan	20	—	ns
	• JTAG and CJTAG	20	—	ns
	• Serial Wire Debug	20	—	ns
J4	TCLK rise and fall times	Refer Table 21		ns
J5	Boundary scan input data setup time to TCLK rise	8	—	ns
J6	Boundary scan input data hold time after TCLK rise	1.3	—	ns
J7	TCLK low to boundary scan output data valid	—	17	ns
J8	TCLK low to boundary scan output high-Z	—	17	ns
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	TMS, TDI input data hold time after TCLK rise	1.3	—	ns
J11	TCLK low to TDO data valid	—	17	ns
J12	TCLK low to TDO high-Z	—	17	ns

364 MAP BGA	176 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
J4	—	DDR_DQM[0]			DDR_DQM0							
E1	—	DDR_DQS[1]			DDR_DQS1							
D3	—	DDR_DQS[0]			DDR_DQS0							
F1	—	DDR_DQS_b[1]			DDR_DQS_b1							
E3	—	DDR_DQS_b[0]			DDR_DQS_b0							
A4	—	DDR_RAS_b			DDR_RAS_b							
C6	—	DDR_WE_b			DDR_WE_b							
C4	—	DDR_ODT[0]			DDR_ODT0							
B1	—	DDR_ODT[1]			DDR_ODT1							
G5	—	DDR_VREF			DDR_VREF							
A3	—	DDR_ZQ			DDR_ZQ							
D6	—	DDR_RESET			DDR_RESET							
J20	—	PTD31		PTD31	FB_AD31	NF_IO15		FTM3_CH0	SPI2_PCS1			
H20	—	PTD30		PTD30	FB_AD30	NF_IO14		FTM3_CH1	SPI2_PCS0			
H18	—	PTD29		PTD29	FB_AD29	NF_IO13		FTM3_CH2	SPI2_SIN			
H17	—	PTD28		PTD28	FB_AD28	NF_IO12	I2C2_SCL	FTM3_CH3	SPI2_SOUT			
H16	—	PTD27		PTD27	FB_AD27	NF_IO11	I2C2_SDA	FTM3_CH4	SPI2_SCK			
G16	—	PTD26		PTD26	FB_AD26	NF_IO10		FTM3_CH5	SDHC1_WP			
G18	—	PTD25		PTD25	FB_AD25	NF_IO9		FTM3_CH6				
G19	—	PTD24		PTD24	FB_AD24	NF_IO8		FTM3_CH7				
G20	124	PTD23		PTD23/ MII0_ RXDATA[3]	FB_AD23	NF_IO7	FTM2CH0	ENET0_ 1588_TMR0	SDHC0_ DAT4	SCI2_TX	DCU1_R3	
F20	126	PTD22		PTD22/ MII0_ RXDATA[2]	FB_AD22	NF_IO6	FTM2CH1	ENET0_ 1588_TMR1	SDHC0_ DAT5	SCI2_RX	DCU1_R4	
F19	128	PTD21		PTD21/ MII0_CRS	FB_AD21	NF_IO5		ENET0_ 1588_TMR2	SDHC0_ DAT6	SCI2_RTS	DCU1_R5	
F17	129	PTD20		PTD20/ MII0_COL	FB_AD20	NF_IO4		ENET0_ 1588_TMR3	SDHC0_ DAT7	SCI2_CTS	DCU1_R0	
F16	130	PTD19		PTD19	FB_AD19	NF_IO3	ESAI_SCKR	I2C0_SCL	FTM2_QD_ PHA	MII0_ TXDATA[3]	DCU1_R1	
E18	131	PTD18		PTD18	FB_AD18	NF_IO2	ESAI_FSR	I2C0_SDA	FTM2_QD_ PHB	MII0_ TXDATA[2]	DCU1_G0	
E20	132	PTD17		PTD17	FB_AD17	NF_IO1	ESAI_HCKR	I2C1_SCL		MII0_TXERR	DCU1_G1	
D20	133	PTD16		PTD16	FB_AD16	NF_IO0	ESAI_HCKT	I2C1_SDA			DCU1_G2	
Y17	86	PTD0		PTD0	QSPI0_A_ SCK	SCI2_TX		FB_AD15	SPDIF_ EXTCLK			
Y18	87	PTD1		PTD1	QSPI0_A_ CS0	SCI2_RX		FB_AD14	SPDIF_IN1			
V18	88	PTD2		PTD2	QSPI0_A_ DATA3	SCI2_RTS	SPI1_PCS3	FB_AD13	SPDIF_OUT1			

364 MAP BGA	176 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
E4	—	SDRAMC_ VDD1P5			SDRAMC_ VDD1P5							
D5	—	SDRAMC_ VDD1P5			SDRAMC_ VDD1P5							
F5	—	SDRAMC_ VDD1P5			SDRAMC_ VDD1P5							
H5	—	SDRAMC_ VDD1P5			SDRAMC_ VDD1P5							
K5	—	SDRAMC_ VDD1P5			SDRAMC_ VDD1P5							
E7	—	SDRAMC_ VDD1P5			SDRAMC_ VDD1P5							
E9	—	SDRAMC_ VDD1P5			SDRAMC_ VDD1P5							
D11	—	SDRAMC_ VDD1P5			SDRAMC_ VDD1P5							
K3	10	VDD33			VDD33							
N3	25	VDD33			VDD33							
V8	52	VDD33			VDD33							
C12	83	VDD33			VDD33							
C15	—	VDD33			VDD33							
U16	95	VDD33			VDD33							
K17	108	VDD33			VDD33							
N17	127	VDD33			VDD33							
T17	140	VDD33			VDD33							
C18	146	VDD33			VDD33							
F18	158	VDD33			VDD33							
W18	168	VDD33			VDD33							
H7	—	VSS			VSS							
K7	45	VSS			VSS							
M7	82	VSS			VSS							
P7	—	VSS			VSS							
G8	96	VSS			VSS							
J8	107	VSS			VSS							
L8	—	VSS			VSS							
N8	139	VSS			VSS							
H9	144	VSS			VSS							
J9	157	VSS			VSS							
K9	175	VSS			VSS							
L9	176	VSS			VSS							
M9	—	VSS			VSS							
P9	—	VSS			VSS							
G10	—	VSS			VSS							



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A	VSS	DDR_ CLK[0]	DDR_ZQ	DDR_ RAS_b	DDR_ CKE[0]	DDR_A[4]	DDR_A[7]	DDR_A[2]	DDR_A[6]	DDR_A[13]	DDR_A[8]	PTE20	PTB20	PTB15	PTB17	PTB28	PTB26	PTB24	PTB23	VSS	A
B	DDR_ ODT[1]	DDR_ CLK_b[0]	VSS	DDR_ CAS_b	VSS	DDR_A[5]	DDR_A[3]	VSS	DDR_A[9]	DDR_A[15]	VSS	PTB18	VSS	PTB14	PTB10	VSS	PTB25	PTA20	VSS	PTE27	B
C	DDR_D[13]	VSS	DDR_D[6]	DDR_ ODT[0]	DDR_ CS_b[0]	DDR_ WE_b	DDR_A[0]	DDR_BA[0]	DDR_BA[1]	DDR_A[12]	DDR_A[1]	VDD33	PTB19	PTB16	VDD33	PTC29	PTA23	VDD33	PTE25	PTE26	C
D	DDR_D[9]	DDR_D[15]	DDR_ DQS[0]	DDR_ D[2]	SDRAMC_ VDD1P5	DDR_ RESET	DDR_A[10]	DDR_BA[2]	DDR_A[14]	DDR_ A[11]	SDRAMC_ VDD1P5	PTB22	PTB7	PTB11	PTB13	PTC26	VSS	PTA21	PTE24	PTD16	D
E	DDR_ DQS[1]	DDR_ D[11]	DDR_ DQS_b[0]	SDRAMC_ VDD1P5	VSS	SDRAMC_ VDD2P5	SDRAMC_ VDD1P5	VSS	SDRAMC_ VDD1P5	SDRAMC_ VDD2P5	VSS	PTB21	PTB12	VSS	PTC28	PTC27	PTA22	PTD18	VSS	PTD17	E
F	DDR_ DQS_b[1]	VSS	DDR_D[4]	DDR_ D[0]	SDRAMC_ VDD1P5											PTD19	PTD20	VDD33	PTD21	PTD22	F
G	DDR_ D[12]	DDR_ DQM[1]	DDR_ D[7]	DDR_ D[3]	DDR_ VREF		VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS		PTD26	VSS	PTD25	PTD24	PTD23	G
H	DDR_ D[10]	DDR_ D[14]	DDR_ D[1]	VSS	SDRAMC_ VDD1P5		VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD		PTD27	PTD28	PTD29	VSS	PTD30	H
J	DDR_D[8]	VSS	DDR_D[5]	DDR_ DQM[0]	SDRAMC_ VDD2P5		VDD	VSS	VSS	VSS	VSS	VSS	VDD	VSS		PTB8	PTE23	VSS	PTB9	PTD31	J
K	JTDO	JTDI	VDD33	JTCLK/ SWCLK	SDRAMC_ VDD1P5		VSS	VDD	VSS	VSS	VSS	VSS	VSS	VDD		PTE28	VDD33	PTE19	PTE18	PTE17	K
L	JTMS /SWDIO	PTC4	PTA12	PTC0	PTC1		VDD	VSS	VSS	VSS	VSS	VSS	VDD	VSS		PTE11	PTE12	PTE15	VSS	PTE16	L
M	PTC5	VSS	PTC3	VSS	PTC2		VSS	VDD	VSS	VSS	VSS	VSS	VSS	VDD		PTE10	PTE9	VSS	PTE8	PTE7	M
N	PTC6	PTC7	VDD33	PTC8	PTA6		FA_VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS		PTE0	VDD33	PTE1	PTE2	PTE4	N
P	PTC13	PTC15	PTC12	PTC11	VDDREG		VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD		PTA31	PTA30	PTA29	VSS	PTA28	P
R	PTC14	VSS	PTC16	PTC17	VSS12_ AFE											PTA24	PTA25	VSS	PTA26	PTA27	R
T	TEST2	BCTRL	TEST	RESETB /RESET_ OUT	VDD12_ AFE	PTB0	PTB1	PTC30	USB0_DM	USB0_DP	DECAP_ V25_LDO _OUT	VDD33_ LDOIN	EXT_TAMPER2 /EXT_WM0_ TAMPER_IN	EXT_ TAMPER0	PTC9	PTE5	VDD33	PTD13	PTD12	PTD11	T
U	DACO0	DACO1	VREFL_ ADC	VADCSE1	VADC_ AFE_ BANDGAP	PTA19	VSS	PTB27	USB1_ VBUS_ DETECT	EXT_TAMPER5 /EXT_WM1_ TAMPER_OUT	VSS_KEL0	EXT_TAMPER4 /EXT_WM1_ TAMPER_IN	EXT_TAMPER3 /EXT_WM0_ TAMPER_OUT	EXT_ TAMPER1	PTC10	VDD33	PTD8	PTD9	VSS	PTD10	U
V	VDDA33_ ADC	VSSA33_ ADC	VDDA33_ AFE	VSSA33_ AFE	VADCSE3	PTA18	PTB2	VDD33	USB1_DM	USB0_ GND	VSS	DECAP_ V11_LDO_ OUT	VSS	VBAT	PTA7	PTE21	VSS	PTD2	PTD7	PTD6	V
W	VREFH_ ADC	ADC0SE9	ADC1SE8	VADCSE2	PTC31	VSS	PTB3	PTB6	USB1_DP	USB1_ VBUS	USB0_ VBUS	XTAL32	XTAL	LVDS0P	PTE14	PTE6	PTE22	VDD33	PTD4	PTD5	W
Y	VSS	ADC0SE8	ADC1SE9	VADCSE0	PTA16	PTA17	PTB4	PTB5	USB1_GND	USB_ DCAP	USB0_ VBUS_ DETECT	EXTAL32	EXTAL	LVDS0N	PTE3	PTE13	PTD0	PTD1	PTD3	VSS	Y
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	

Figure 59. 364-pin BGA package ballmap

12.2.1 GPIO Mapping

Table 75. RGPIO versus Pins

RGPIO	In GPIO module	Corresponding Pin on the chip	IOMUX register name	IOMUX register address
RGPIO[0]	PORT0[0]	PTA6	IOMUXC_PTA6	40048000

Table continues on the next page...

Table 78. Functional Assignment Pins (continued)

Signal Name	364 MAP BGA	176 LQFP (F-series ONLY)	Power Group	Pad Type	Default Mode (Reset)	Default Function	Input/ Output	Value
DDR_CLK[0]	A2	—	SDRAMC_VDD2P5	DDR	—	DDR_CLK[0]	—	—
DDR_CLK_b[0]	B2	—	SDRAMC_VDD2P5	DDR	—	DDR_CLK_b[0]	—	—
DDR_CS_b[0]	C5	—	SDRAMC_VDD2P5	DDR	—	DDR_CS_b[0]	—	—
DDR_D[0]	F4	—	SDRAMC_VDD2P5	DDR	—	DDR_D[0]	—	—
DDR_D[1]	H3	—	SDRAMC_VDD2P5	DDR	—	DDR_D[1]	—	—
DDR_D[2]	D4	—	SDRAMC_VDD2P5	DDR	—	DDR_D[2]	—	—
DDR_D[3]	G4	—	SDRAMC_VDD2P5	DDR	—	DDR_D[3]	—	—
DDR_D[4]	F3	—	SDRAMC_VDD2P5	DDR	—	DDR_D[4]	—	—
DDR_D[5]	J3	—	SDRAMC_VDD2P5	DDR	—	DDR_D[5]	—	—
DDR_D[6]	C3	—	SDRAMC_VDD2P5	DDR	—	DDR_D[6]	—	—
DDR_D[7]	G3	—	SDRAMC_VDD2P5	DDR	—	DDR_D[7]	—	—
DDR_D[8]	J1	—	SDRAMC_VDD2P5	DDR	—	DDR_D[8]	—	—
DDR_D[9]	D1	—	SDRAMC_VDD2P5	DDR	—	DDR_D[9]	—	—
DDR_D[10]	H1	—	SDRAMC_VDD2P5	DDR	—	DDR_D[10]	—	—
DDR_D[11]	E2	—	SDRAMC_VDD2P5	DDR	—	DDR_D[11]	—	—
DDR_D[12]	G1	—	SDRAMC_VDD2P5	DDR	—	DDR_D[12]	—	—
DDR_D[13]	C1	—	SDRAMC_VDD2P5	DDR	—	DDR_D[13]	—	—
DDR_D[14]	H2	—	SDRAMC_VDD2P5	DDR	—	DDR_D[14]	—	—
DDR_D[15]	D2	—	SDRAMC_VDD2P5	DDR	—	DDR_D[15]	—	—
DDR_DQM[0]	J4	—	SDRAMC_VDD2P5	DDR	—	DDR_DQM[0]	—	—
DDR_DQM[1]	G2	—	SDRAMC_VDD2P5	DDR	—	DDR_DQM[1]	—	—

Table continues on the next page...

Table 78. Functional Assignment Pins (continued)

Signal Name	364 MAP BGA	176 LQFP (F-series ONLY)	Power Group	Pad Type	Default Mode (Reset)	Default Function	Input/ Output	Value
PTA31	P16	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB0	T6	49	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB1	T7	50	VDD33	GPIO	ALT3	RCON30	Input	Disabled
PTB2	V7	51	VDD33	GPIO	ALT3	RCON31	Input	Disabled
PTB3	W7	53	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB4	Y7	54	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB5	Y8	55	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB6	W8	56	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB7	D13	166	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB8	J16	121	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB9	J19	123	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB10	B15	159	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB11	D14	164	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB12	E13	165	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB13	D15	156	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB14	B14	162	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB15	A14	161	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB16	C14	163	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB17	A15	160	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB18	B12	171	VDD33	GPIO	ALT0	GPIO	Input	Disabled
PTB19	C13	167	VDD33	GPIO	ALT0	GPIO	Input	Disabled
PTB20	A13	169	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB21	E12	173	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB22	D12	172	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB23	A19	141	VDD33	GPIO	ALT3	GPIO	Disabled	
PTB24	A18	142	VDD33	GPIO	ALT3	GPIO	Disabled	
PTB25	B17	149	VDD33	GPIO	ALT3	GPIO	Disabled	
PTB26	A17	150	VDD33	GPIO	ALT3	RCON21	Input	Disabled
PTB27	U8	57	VDD33	GPIO	ALT3	RCON22	Input	Disabled
PTB28	A16	151	VDD33	GPIO	ALT3	RCON23	Input	Disabled
PTC0	L4	8	VDD33	GPIO	ALT7	RCON18	Input	Disabled
PTC1	L5	9	VDD33	GPIO	ALT7	RCON19	Input	Disabled
PTC2	M5	11	VDD33	GPIO	ALT7	RCON20	Input	Disabled
PTC3	M3	12	VDD33	GPIO	ALT0	GPIO	Disabled	
PTC4	L2	14	VDD33	GPIO	ALT0	GPIO	Disabled	
PTC5	M1	15	VDD33	GPIO	ALT0	GPIO	Disabled	
PTC6	N1	16	VDD33	GPIO	ALT0	GPIO	Disabled	

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Table 78. Functional Assignment Pins (continued)

Signal Name	364 MAP BGA	176 LQFP (F-series ONLY)	Power Group	Pad Type	Default Mode (Reset)	Default Function	Input/ Output	Value
PTC7	N2	17	VDD33	GPIO	ALT0	GPIO	Disabled	
PTC8	N4	18	VDD33	GPIO	ALT0	GPIO	Disabled	
PTC9	T15	77	VDD33	GPIO	ALT0	GPIO	Disabled	
PTC10	U15	78	VDD33	GPIO	ALT0	GPIO	Disabled	
PTC11	P4	20	VDD33	GPIO	ALT0	GPIO	Disabled	
PTC12	P3	21	VDD33	GPIO	ALT0	GPIO	Disabled	
PTC13	P1	23	VDD33	GPIO	ALT0	GPIO	Disabled	
PTC14	R1	26	VDD33	GPIO	ALT0	GPIO	Disabled	
PTC15	P2	27	VDD33	GPIO	ALT0	GPIO	Disabled	
PTC16	R3	29	VDD33	GPIO	ALT0	GPIO	Disabled	
PTC17	R4	28	VDD33	GPIO	ALT0	GPIO	Disabled	
PTC26	D16	153	VDD33	GPIO	ALT3	RCON24	Input	Disabled
PTC27	E16	154	VDD33	GPIO	ALT3	RCON25	Input	Disabled
PTC28	E15	155	VDD33	GPIO	ALT3	RCON26	Input	Disabled
PTC29	C16	152	VDD33	GPIO	ALT3	RCON27	Input	Disabled
PTC30	T8	58	VDD33	GPIO	ALT3	RCON28	Input	Disabled
PTC31	W5	42	VDD33	GPIO	ALT3	RCON29	Input	Disabled
PTD0	Y17	86	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD1	Y18	87	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD2	V18	88	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD3	Y19	89	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD4	W19	90	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD5	W20	91	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD6	V20	92	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD7	V19	93	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD8	U17	94	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD9	U18	97	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD10	U20	98	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD11	T20	99	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD12	T19	100	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD13	T18	101	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD16	D20	133	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD17	E20	132	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD18	E18	131	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD19	F16	130	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD20	F17	129	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD21	F19	128	VDD33	GPIO	ALT0	GPIO	Disabled	

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Table 79. Revision History (continued)

Rev. No.	Date	Substantial Changes
		Updated Power supply diagram Updated AC electrical specification of following modules: DCU, 12-bit DAC, Ethernet, Enhanced Serial Audio Interface (ESAI), SAI/I2S, Flexbus, MLB, DSPI, 24MHz External Oscillator, JTAG, Debug, ESAI, QSPI Updated Thermal Attributes for 364 MAPBGA Updated Freescale document number for 176-pin LQFP and 364 MAPBGA Updated VREG specifications Added WBREG specifications Updated Recommended operating conditions table Updated DAC INL and DNL charts Updated Pinouts
Rev 4.1	12/2012	Editorial updates: Removed instances of VF7xx and VF4xx.
Rev 5	April 2013	• Removed references to VF1xxR and refernces to F100 and 144 LQFP and 256 MAPBGA • Replaced references to Auto and IMM by R-series and F-series respectively • In the feature list, the ARM Core frequency changed to 500 MHz for F-series • In the feature list, changed the DRAM controller frequency • Updated Part Nummbering format • Clarified the Fields table as per Marketing • Sample numbers updated • From the VREG electrical specifications tables, deleted pre-trimming rows and comments • .In the HPREG electrical characteristics table, add footnote on maximum Output Current Capacity • In the ULPREG electrical characteristics table, clarified max value of Output voltage @ no load and min value of Output voltage @ full load • In the WBREG electrical characteristics table, clarified max value of Output voltage @ no load and min value of Output voltage @ full load

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